Study and Analysis of SRAM memory compiler and characterization

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Certificate

This to certify that *Mr. Makwana Rohan Bharatbhai (12MECV16)*, a student of M.Tech EC (VLSI Design), Institute of Technology, Nirma University was working in this organization since $16^{th} June, 2013$ and carried out his thesis work titled "Study and Analysis of SRAM memory compiler and characterization". He was working in Solution Group (SG) under supervision of *Mr.Nitesh Gautam, R&D Manager*. He has successfully completed the assigned work and is allowed his dissertation report. We wish him all success in future.

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This is to certify that the project entitled "Study and Analysis of SRAM memory compiler and characterization" submitted by Rohan Makwana(12MECV16), towards the partial fulfilment of the requirements for the degree of Master of Technology in VLSI Design of Nirma University, Ahmedabad is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this dissertation, to the best of my knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

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Abstract

As process technologies shrink, the size and number of memories on a chip are constantly increasing and memory designs become a more significant part of the overall system performance, efficiency, and cost. Random-Access Memories can be time consuming and tedious to custom design, and there are not many options for automating this process. Process design kits from foundries and vendors do not include memory compilers and commercial solutions require expensive licenses and are often un-modifiable and process specific. This thesis introduces Memory compiler, and its characterization methodology. The main objective of this project is to by providing a flexible and portable platform for generating and verifying memory designs across different technology node. Currently, the compiler generates Spice netlists for single-port SRAM's using the 28nm foundry, and provides timing/power characterization through Spice simulation. Memory Compiler can be parameterized by number of words, number of bits per word, desired aspect ratio, number of sub banks, degree of column muxing, etc. Area, delay, and energy consumption complex function of design parameters and generation algorithm worth experimenting with design space.

Keywords: Static Random Access Memory (SRAM), memory compiler

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- Rohan Makwana(12MECV16)

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Chapter 1

Introduction

Various devices have been implemented to minimize the power consumption and to maximize the battery life. Constant voltage scaling has significant impact on the overall power dissipation. As the supply voltage reduce, the dynamic power reduces quadratically ($P_{dynamic} = CV_{DD}^2 f$) while leakage current reduces linearly ($P_{leakage} = VI_{leak}$ First order equation). The main difficulty for design engineer is sensitivity of the circuit increase abnormally due to process variation and variability come into the picture.

More specifically, SRAM bitcells having particular small sized transistors very much immune to the process variation, random dopant fluctuation(RDF) and line edge roughness(LER) due to that probability of threshold mismatch occur. Considering the above complexity in SRAM bitcell, there may be increase the chances of failure rate of cell like read failure, hold failure, write failure, and access time failure.

The maximum supply voltage for any technology node derived by the process constraints such as quality and geometrical condition of the gate-oxide. And minimum supply voltage for the SRAM bitcell depends on different process variations at which it hold the data into the cell so, it operates on wide voltage ranges. But as the process technology node increase the mismatch in process increase. Various design such as Read and write assist techniques to control the magnitude and bias of different nodes like word-line, V_{SS} node, bit-lines. This things discussed in Chapter 3.

This chapter is organized as follows.

- History and trend of SRAM memory cell

1.1 History and trend of SRAM memory cell

Different flavours of SRAM bitcells have been introduced having different objective such as bit density, Area, low voltage operation and different timing specification, To improve static noise margin (SNM).

In figure 1.1(a) having loadless 4T bitcell configuration, pMOS acts as access

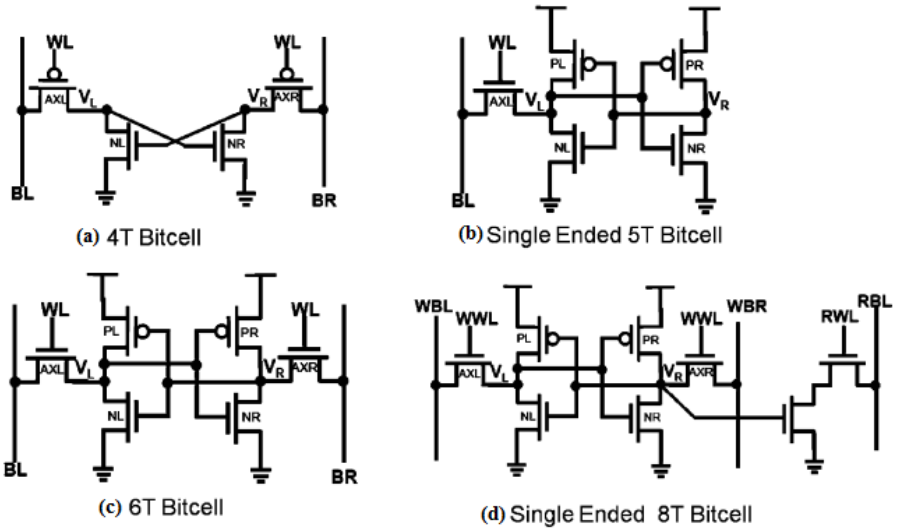

Figure 1.1: Different SRAM bitcell configuration

transistor. The main challenge in this configuration is pMOS OFF current (leakage current) shuould be more than the pull down nMOS OFF current to maintain data "1". Across the process variation (PVT) the subthreshold swing of the MOS heavily increase the design complexity [1]. In figure 1.1(b), it consists of asymmetric cross coupled inverters with single ended bitline [2]. For read and write for this particular cell different precharge voltage requires so that it require different precharge voltages and extra $dc - dc$ converter requires. The two cross coupled two back to back inverter have been accessed by two nMOS transistors which is more widely used in present SRAM memory designs. However, The stability problem in 6T cells in that in the read operation, a pass-gate pulls the "0" storage node up to a non-zero value so new proposed solution which is showed in figure 1.1(d) by adding two nMOS transistor to the 6T structure so that internal node do not disturb. It require different read and write word-lines and can accommodate dual-pot operation with separate read and write bitlines. It has very larger SNM achieved without tradeoff in performance since a read access is still performed by two stacked nMOSs [3].

The remainder of this dissertation is organized as follows. Chapter 2 mainly described about the how to determine the behaviour of memory cell like Static Noise Margin(SNM), Read Margin(RM), write margin(WM) and some discussion on stability of cell. ...

Chapter 2

SRAM 6T Cell Characterization

Memory represents one of the fundamental building blocks of any computation system as it is required to retrieve variables for the computation as well as to store results of the calculation. Memory can be divided into two classes: volatile and non-volatile. Volatile memory loses the stored information when the power supply is removed while non-volatile memory typically retains the data for a few years. Static Random Access Memory (SRAM), which is the main subject of this work, is classified as volatile memory because it relies on a power supply to statically retain data. It is further classified as a random access memory because it allows access to arbitrary locations of data without any restrictions.

This chapter is organized as follows.

- Background, Basic and fundament of SRAM cell at a glance.
- Read Margin, Introduce procedure to find Read Margin and it's metrics.
- Write Margin
- Static Noise Margin

2.1 Background

Figure 2.1 illustrates a schematic representation of a bitcell circuit. The main core of SRAM bitcell (back to back inverter configuration, two access nMOS transistor) is stored one bit per cell. One node in the cell is storing an electrical quantity of "0" which drives the input of an inverting gain element to "1" which then cause the next inverting gain element to drive original node back to a "0". This phenomena is called as positive feedback configuration which increase the robustness(strength) of the system (less immune to noise). The bitcell is accesed using the pair of access nMOS transitor that is use for read and write the content of data. and

those access transistor connect to bitlines(BL and $\overline{BL}$) and it control by the word-line(WL). From design point of view this access transistors are designed in such way to overcome the positive feedback of the cell, write the content and non destructively read the data of cells. So, one of fundamental tradeoff between read and write operation turns into marginal analysis.

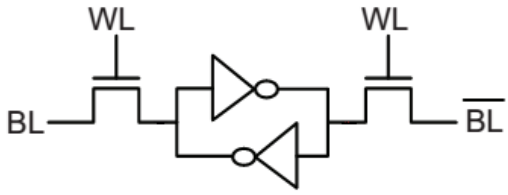

Figure 2.1: Schematic of an SRAM bitcell

2.2 Read Metrics

2.2.1 Static Read Current (I_{read})

It is defined as the current that is being sources from bit-line into SRAM node storing a 0. In read operation, static read current is responsible for discharging of pre-charged bit-line capacitances (C_{BL}) enough to create minimum amount of offset voltage (V_{offset}). so, the correlation of actual read time is defined as below,

$$T_{access} \propto C_{BL} * V_{offset}/I_{read}$$

The above read timing in actual scenario deviates from the above relationship. Reason for deviation is leakage currents from the inactive bitcells which share the distributed RC bitline capacitance C_{BL} (spanning network of selected column for read of the SRAM array). Degradation in I_{read} and read time due to random telegraph signaling (RTS) also contributes to this discrepancy.

Method to find the Read current which is permissible or not which is as follows,
Read Current Measurement:

- Define internal nodes in cells, logic "0" and logic "1".
- Define word-line is at V_{DD}.
- Define BL and $\overline{BL}$ are at V_{DD}.

Measure read current as, the current through the access transistor(which is connect to internal node as logic-"0").
Leakage Current Measurement:

- Define internal nodes in cells, logic "0" and logic "1".
- Define word-line is at 0.
- Define BL and $\overline{BL}$ are at 0.

The leakage current is measured as current through the access transistor

To obtain the condition of failure or pass bitcell, consider the geometrical structure of array calculate the physical row(N_{max}). And build an extra 10x design margin over this value since leakage current can fluctuate. Then the critical constrain for read current is as follows,

$$I_{leak} < I_{read}/N_{max} * 10$$

The Reason for calculating the current through the access transistor, During read condition voltage divider circuit form and resistance of access transistor is higher than the pull down transistor in bitcell so that consider the current through the access transistor. Simulate the bitcell through monte-carlo simulation the higher the monte higher yield.

2.2.2 Read Access Time

To amplify the offset voltage sense amplifier use, but the pulse width of the world-line is also an important part during read operation. In figure 2.2(a) the pulse-width of the T_A is too short to sufficiently discharge the bit-line capacitance to overcome the offset in the sense-amplifier. There exists a pulse-width, $T_{access}(T_A < T_{access} < T_B)$, where the sense-amplifier is on the threshold of a successful read access that is defined as the read access time.This definition of read access time isolates out variability in the read access operation due to variability of the SRAM bitcell and ignores other delays such as word-line driver delay and sense-amplifier delay.

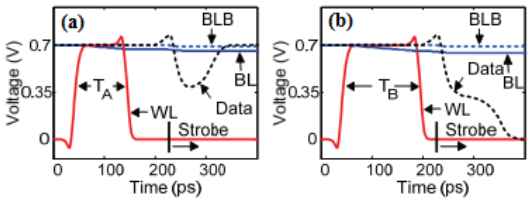

Figure 2.2: Impact of different word-line pulse on read operation

2.3 Writeability Metrics

2.3.1 Static Writeability Margins

In this discussion, bit-line write tripe voltage(BWTV) is characterized instead of other metrics because at what time bitcell core flip is very much depend on the sweeping voltage of bit-line. BWTV write margin corresponds to the voltage applied on word-line which is required to successfully write a new value into the bitcell. This is observed in the bit-line currents as a sharp change in the magnitude and direction of current flowing through the bit-lines.

2.3.2 Critical Writeability

In figure 2.3, write operation to a SRAM bitcell with pulse-width T_A and T_B. Pulse-width T_A is too short and bitcell is not able to write the data because it can not break the positive feedback of the bitcell. While pulse-width T_B sufficient enough for write operation. So, critical pulse-width, T_{write} (T_A<T_{write}<T_B), where the bitcell is on the threshold of a successful write access that is defined as the critical writeability.

By above discussion the writeability (write margin) of the cell defined by below

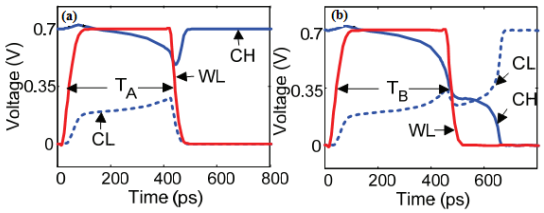

Figure 2.3: Impact of different word-line pulse on write operation

margins,

- Window Margin
- Word-line(WL) driven Margin
- Bit-line(BL) driven Margin

2.3.3 Fliptime Bitcell Setup

Figure 2.4 illustrate the write "1" into the bit-cell core (Initially XT "0" and XB "1") for that discharging the $\overline{BL}$ line and make cell flip. In 2.4(a) show the memory array cell which is very near and little stronger than far top bitcell so, time require to flip the cell 80% of rise and 20% of fall of internal node taking reference signal clock 50% as now days (mostly synchronous circuit use) or WL (word-line)for particular

bitcell analysis 50% . And find the maximum difference between those signals. so for near cell $max(T_{a1}, T_{a2})$<$max(T_{b1}, T_{b2})$. And for monte carlo analysis do all simulation in 5σ.

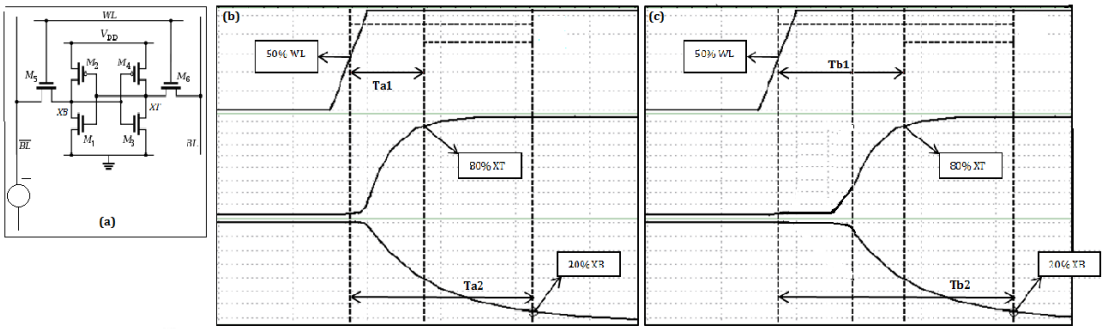

Figure 2.4: Flip-time of bitcell analysis

2.3.4 Measuring Flip-time of core procedure

- Initialize XT node to "0".
- Initialize XB node to V_{DD}.
- Turn on the Word-line (WL).
- Bit-line(BL) at V_{dd}.
- Bit-line complement($\overline{BL}$) is a transient goint from V_{DD} to 0 using piece-wise linear function.
- Write margin defined as the $max(T_{a1}, T_{a2})$ or $max(T_{b1}, T_{b2})$.

2.4 Static Noise Margin(SNM) of Bitcell

Static noise margin essentially characterizes the largest voltage perturbation that can be sustained in the internal node (XT and XB) of bitcell before the bitcell loose the ability to store two states.

2.4.1 Measuring SNM of Bitcell Procedure

- Appending DC noise source inside the SRAM cell.
- Wordline(WL) at V_{DD}.
- BL and $\overline{BL}$ at V_{DD}.
- Initialize internal node XT and XB, "0" and "1".

- Increase V_X from 0 and measure at what time XB node flip and measure E(voltage coupled voltage source) voltage.

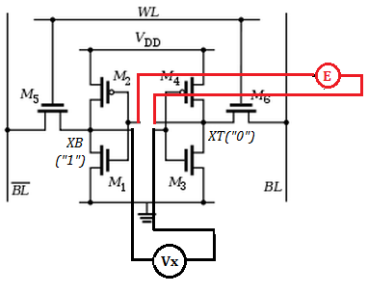

Figure 2.5: SNM measurement Setup

Chapter 3

SRAM Memory Architecture and Overview of Peripheral Designs

One of the most important consideration in designing high performance SRAM memory design is the performance and robustness of memory architecture and it's peripheral designs. For excessive speed, power performance and great environment tolerance of SRAM is obtained by compromise in costs per bit.

In this chapter,

- Architecture of memory is described.
- Designing of Leaf Cell is also described.

3.1 SRAM Memory Architecture

Around 70% of SoC(system on Chip) total area occupy by the memories hence it is most fundament thing to determine the yied and success rate on silicon. To improve the profitability dense and stable memory design is key factor. In this section, illustrate the lower power, High speed and robust architecture described.

3.1.1 Center Decoding Architecture

A conventional memory having single memory array with input-output, decoders and control blocks built around it. In this arrangement one memory array accessed through decoder so, the design in a such way memory array and decoder on different sides. But for dense memory the RC distributed network on wordline and bitline also increase as technology shrinks and it reduce the speed of the memory.

To fast the memory operation, reduce the load of Bitline and wordline through which we can speed up the memory. For that page and bank structure come

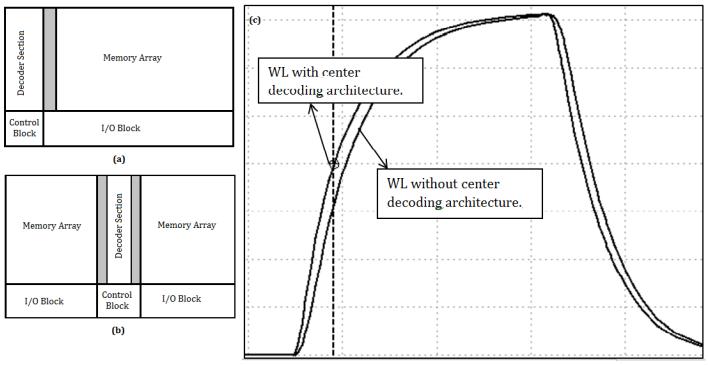

Figure 3.1: Center Decoding Architecture

into the picture. Another most simple and innovative approach is to divide the memory array into the two parts so basically shifting the decoder into the middle of memory core which shows into the figure 3.1(b)[4]. So, without increase in area, speed increase and also power dissipation reduce. Generally this structure also known as "Butterfly Structure".

In case of figure 3.1(a) the time constant of the wordline T=RC and for time constant for wordline is T=$RC/4$ it increase the speed of operation.

3.1.2 Bank Architecture

As memory size increase, the memory architecture become more and more dense. To increase the access time and clock to output interleaving the addresses. The bank architecture is very promising to improve the bandwidth of memory. In figure 3.2(a) group of 4 banks is shown, which having global and local driving circuitry.

The particular one bank architecture included for emulated the timing path involved in memory access operation. BS(Bank Select) signal select the particular bank and which is operates as "Master clock" that is used for decoding particular bank. When BS is logic "0" unselected bank do not interfere with passing control between global control and local control blocks. In figure 3.2(b) shows the global timing circuit for driving the common DBITFB node. The external master clock(CLK) and memory enable(ME) signal are applied to NAND gate that is coupled to an inverter. A one-shot circuit with programmable delay is provided with programmable delay is provided such that the common node is driven high for a predetermine time period. The programmable delay is provided in order to ensure that the common DBITFB node is driven high for a minimum amount of time in a host of applications Wherein variable number of banks and/or different heights of the memory instance are to be accommodated, as may be necessary in compilable architectures.

The output of inverter(which is also provided as an input of programmable delay circuit) drives the gate of pMOS and nMOS transistor. The output of the

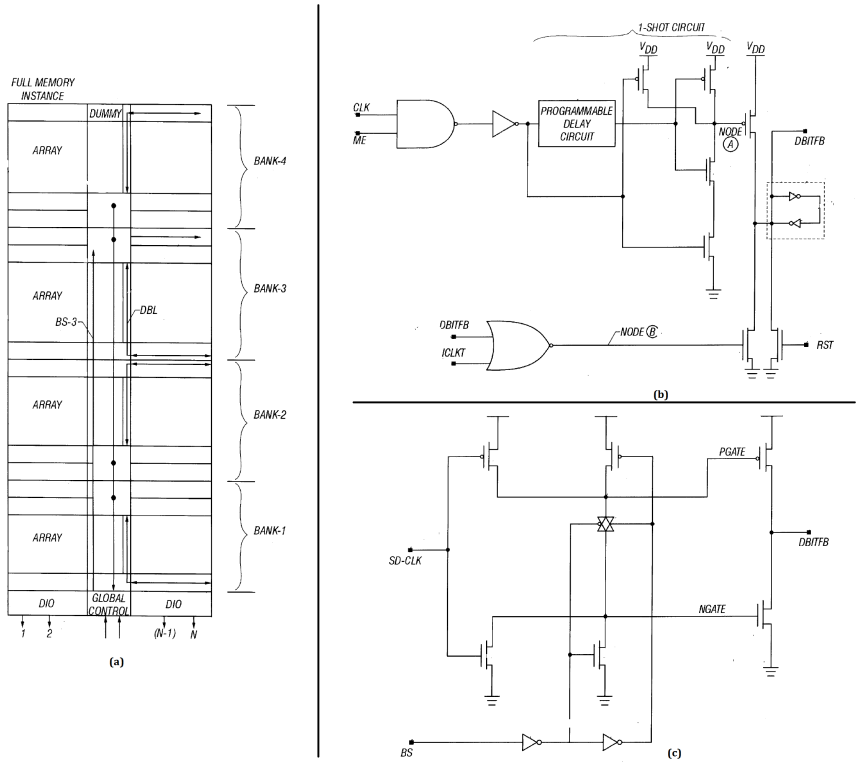

Figure 3.2: Bank Architecture

programmable delay circuit drives the gates of pMOS and nMOS, Which are coupled together at Node A. pMOS devices are operable to pull Node A to a high value (i.e., V_{DD}) When a logic "0" is applied to their gates. Programmable delay and the NAND gate comprised of transistors together form the "one shotâĂİ circuit portion Whereby Node A undergoes a fixed-time negative pulse in response to the rising edge at output. The duration of the programmable delay circuit sets the pulse Width of Node A.

Concentrating further the global timing circuit Accordingly, When both CLK and ME are asserted, Node A is pulsed low, thereby turning on pMOS Which pulls the DBITFB node to a high value (V_{DD}). In the meantime, as external CLK is asserted, an intermediate clock signal (ICLKT) is generated therefrom, Which is applied to a NOR gate. The output node (Node B) of NOR drives nMOS Which is operable to drive the DBITFB node low at the end of the cycle. When ICLKT is asserted (pursuant to the external clock's rising edge),Node B is driven low substantially rapidly, thereby turning off the nMOS pull-down device, prior to activation of the pMOS device. Accordingly, upon encountering the rising edge

of the external clock, the nMOS pull-down device is deactivated and the global timing circuit is operable to drive the DBITFB node to a high value as quickly as possible for a predetermined amount of time (i.e., for the during of the negative pulse of Node A), Without causing contention between transistors. A keeper latch also "cheater latch" which create circularly-coupled inverters and is disposed on DBITFB node so as maintain the voltage level at the node just in case DBITFB is ever "undriven" for particular amount of time.

In figure 3.2(c) illustrate the local driver circuit, forming a portion of the local clock generation for that particular bank. Essentially, the local driver circuit is operable as an inverter pair coupled in series between a reference signal (SDi-CLK) node and DBITFB When the BS signal is high. On the other hand, the local driver circuit tri-states the DBITFB node When BS is low, ensuring that unselected banks do not interfere with the passing of control between the global control circuitry and local control circuitry (Which,in the case of this example, comprises circuitry Where Bank-3 is selected).

3.2 Peripheral Designs

3.2.1 Decoding Architecture

For Random Access Memory, to access the memory the random address information is passed through the row and column decoder circuits. Fundamentally, Decoder create n-bit input to the 2^n output lines. Large storing capacity RAM having large input bits, for example n=8 we require 256 eight input NAND gates. The gate with such higher fan-in lead to higher delays for this case 8 MOS transistors in series and produce larger resistance so, produce larger delay at output side.

There are total 9 address bits which are inputs to control logic out of which 8 bits are used for X predecoders and 1 bit is used for Y predecoder (CM=2) to generate Y predecoded signals YADR[1:0] as shown in figure 3.3(a). The outputs of xpredecoders are the inputs to post decoding input gates. This programming of predecoded lines in the post decoding stage is explained in figure 3.3(b). This is how programming done in a typical memory architecture. All address bits are input to address latches as shown in figure 3.3(a).

3.2.2 Sense Amplifier

Figure 3.4 shows the input decoupled full latch sense amplifier with V_{DD} biasing. This is one of the commonly used sense amplifier in high speed memory applications. Without loss of generality we assume that $\overline{BL}$ goes down and BL remains high, when the memory cell is accessed. The offset voltage of the latch is characterized as the minimum input differential voltage between $\overline{BL}$ and BL that is required for the correct output of the latch. Ideally the two cross coupled nMOS transistors (MN0 and MN1) and the two pMOS pass transistors (R1 and R2) are perfectly matched. For this ideal case, $\overline{BL}$ can be infinitesimally less than

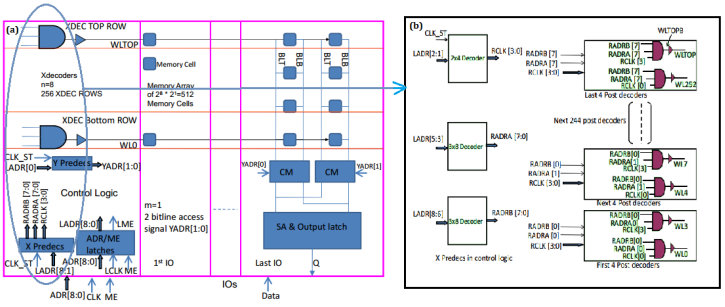

Figure 3.3: A typical Memory post and pre decoding architecture

V_{DD} for $\overline{SAO}$ to go down. But due to process variations, perfect matching is not possible, and hence $\overline{BL}$ needs to be less than V_{DD} by a finite amount for correct reading. This finite value is the offset voltage of the sense amplifier.

For the latch output nodes precharged to V_{DD}, mismatch in pulldown nMOS

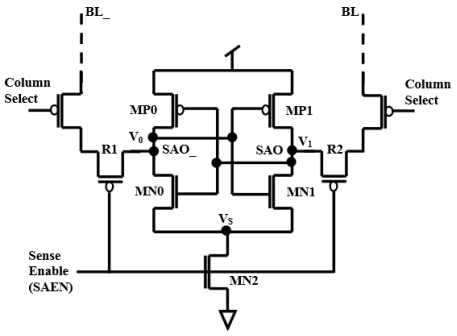

Figure 3.4: Input decoupled latch type sense amplifier

(MN0 and MN1) and input pMOS pass transistors (R1 and R2) contributes to the latch offset. Offset contribution from MN0 and MN1 is named as the intrinsic latch offset and that of R1 and R2 as the extrinsic latch offset. The total latch offset is sum of these two offsets. The variations in column pass transistors do not influence the latch offset because column pass transistors remain ON during sensing operation. The pull up pMOS transistors (MP0 and MP1) do not contribute to the latch offset because they are in subthreshold region during sensing period.

3.3 Dynamic Stability Designs

For V_{min} operation, read and write stability degrades the stability of cell. To enhance the stability of cell different assist techniques used which is described as below. For battery operated device the leakage reduction is more preferable which is also described in section 3.3.3.

3.3.1 Read Assist

By under-driven the wordline(WL) voltage the read margin effectively increase. Figure 3.5 (a) illustrate the Read operation in SRAM memory cell in which during read operation the discharge through the access transistor and pull down nMOS discharge the precharge voltage and create minmal voltage offset and it's drive the sense amplifier. Now, to increase the read stability of cell, has to weaken the pass transistor by underdrive the word line voltage V_{WL} which is less than the supply voltage V_{DD}. In figure 3.5(b) which illustrates the suppression of word line voltage by putting the nMOS transistor which is shown in figure. Since there are two transistor which gate control pins flexible for different voltage range of word-line.

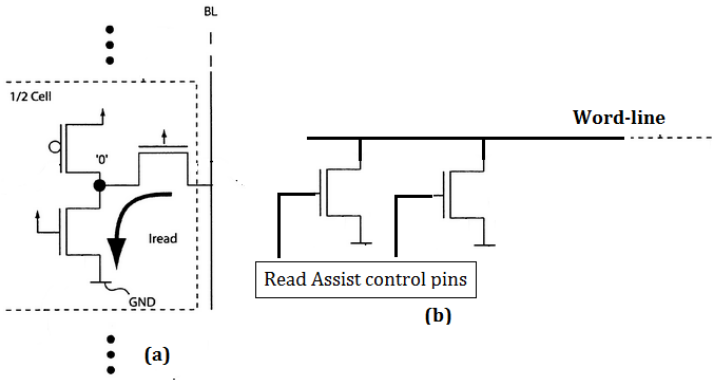

Figure 3.5: Read Assist Technique

3.3.2 Write Assist

To increase the read margin of circuit, weak the access transistor but to increase the write margin access transistor should be stringer. To stronger the access transistor apply negative bias to the source of access transistor so, it increase the write margin

Chapter 4

Validation of Memory Compiler

4.1 Primetime

Primetime check is used for timing analysis. It is a verilog model verification. This command checks the Synopsys library syntax and ensures the timing arcs defined in the Synopsys library exist in the Verilog model. The Synopsys PrimeTime suite, including PrimeTime, PrimeTime SI, PrimeTime PX and PrimeTime VX, provides a single, golden, trusted signoff solution for timing, signal integrity, power and variation-aware analysis

4.2 Libscreen

Libscreen check is to check monotonicity of the liberty file data. This check verifies the slopes of the timing arcs.

4.3 Timever

Timever is a timing verification tool. Timing verification is the process of determining that a given design can be operated at a specific clock frequency without errors caused by a signal arriving too soon or too late . For example, if the data input of a latch arrives after the closing edge of the clock (a setup violation), or if the data input changes before the closing edge of the previous clock (a hold violation), the latch may not store the data correctly. This check adds timing parameters to the Verilog and checks for read/write setup/hold , tcc on the Verilog.

4.4 LibCompare

Libcompare Compare datasheets between compiler versions given in tcl file. It compares timing power and area between two compilers and it reports the percentage deviation in the above mentioned parameters in XLS format.

4.5 Celtic

Celtic is a noise analysis tool provided by cadence. It is used to perform signal integrity sign-off . It identifies nets with low noise immunity to avert potential noise-related problems and lethal silicon failures before tapeout. The CeltIC analyzer accurately calculates the impact of noise on both the delay and functionality of cell-based designs. It performs SoC noise analysis and generates repairs back into place-and-route

4.6 CCSN

Ccsn is composite current source for noise. This model is used for noise analysis. It enables you to generate CCS Noise for accurate noise calculation and validate the noise immunity of the cells in Synopsys compilers.

4.7 CCST

Ccst is composite current source for time. This model is used for time analysis. The CCS timing model is an open source model which is part of the Liberty format specification. Characterization guidelines, development tools, and library validation and correlation tools are available to speed the library characterization and qualification process.
To expedite and simplify CCS library qualification, Synopsys provides a new library QA capability part of Library Compiler that can be used to check the completeness and accuracy of all acquired CCS timing models in a library. In addition, Library Compiler can be used in correlation mode to verify the accuracy of the characterization.

4.8 ECSM

Effective current source modeling. This check is used for Ecsm verification. ECSM is a delay calculation method that uses a current-based cell driver model and a variable pin capacitance receiver model for highly accurate cell-based delay calculation. The model is particularly good at predicting the effect of non-linear waveforms on high impedance interconnects. The model requires additional cell characterization data such as the output current profile for the active transitions of each cell in the library and a variable input pin capacitance table

4.9 Espcv

It is formal equivalence check between Verilog model and a structural model created by tool to verify functionality. ESP-CV is a symbolic simulation-based for-

mality verification tool intended to perform custom equivalence(EQ) checking and provide functional verification coverage for fullcustom IC design.

4.10 ATPG

ATPG is automatic test pattern generation. Two checks are here

- Atpgmen ATPG mentor tool
- Atpgsyn ATPG synopsys tool

It is a Automatic Test Pattern Generation(ATPG) TOOL.

- Used to detect manufacturing defects
- Generates efficient test patterns
- Creates patterns that are re-usable, resulting in lower testing cost
- It is not a functionality checking tool.

It needs a TetraMax model, it should use only primitives (AND,NOT .., gates), not allow to use the behavioral construct, except the memory models. It assume behavioral part as black box.

4.11 Funcver

This is Verilog Functional verification. Synopsys VCS tool is used for this. VCS offers industry-leading performance and capacity, complemented by a complete collection of advanced testbench, bug-finding, coverage and assertion technologies. VCS multicore technology delivers a 2x verification speed-up and cuts down verification time by running the design, testbench, assertions, coverage and debug in parallel on machines with multiple cores.

4.12 Redhawk

Redhwak is a power integraty solution. It is an IR/Power Analysis tool that enables more accurate static and dynamic analysis for on state and ramp up mode. We can easily utilize different utilities for Redhawk to run IR/Power analysis.

4.13 Prescreen

Prescreen is to create LVS and DRC report for corner instances. It helps in generating the Prescreen information (Like Mini QA for BE & Mini QA on Functional & timing checks and much more) by generation , verification and reporting for Synopsys compiler.

4.14 FamilyVerify

This check reports for all the files and corresponding errors. Also check the structure of the compiler. Compiler family validation tests are intended to assure quality of a compiler before it is released. Normally, you run family validation if you want to:

- Validate that an existing compiler conforms to one or more family definitions
- Update an existing compiler to force it to conform to one or more family definitions
- Create a new compiler that is already conforming to one or more family definitions

4.15 IQA

IQA is the integrated QA. It checks full compiler. For corner instances it checks Lib VS db. Pins transition etc. It ensure the quality of instances before the compilers are released. The IQA check also include the capability to ensure that antenna diodes are always present. Transistor recognition is performed so that a given piece of diffusion geometry can be recognized as a source or drain to a gate. If it is not a source/drain, it is a diode and is recorded appropriately.

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