PDK (Process Design Kit) Backend Validation

Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Godhani Dhaval M.

(12MECV10)

Department of Electronics & Communication Engineering

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Nirma University

Ahmedabad-382 481

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Under the Internal Guidance of

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Declaration

This is to certify that

1. The report comprises of my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgement has been made in the text to all other material used.

Godhani Dhaval M.

CERTIFICATE

This is to certify that the Project entitled **“”PDK (Process Design Kit) Back-end Validation”** submitted by **Mr. Godhani Dhaval M. (12MECV10)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology in VLSI Design** of **Nirma University of Science and Technology; Ahmedabad** is the record of work carried out by him under our supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for the examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Place: Ahmedabad

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Abstract

PDK is short for "Process Design Kit". A PDK is a complete set of technology files to enable analog and mixed signal custom IC circuit design in the Design Environment.The "Process" in PDK is the specific foundry process supported by that PDK. A fully integrated PDK includes technologies file (LVS, DRC, Parasitic Extraction, Spice Models) device symbols, CDF, callbacks, Pcells, PV rule files etc.Everything you need to do integrated circuit design. So, these design kits do not have any particular functionality. Rather the users that are the designers of various fields will use these PDK to test their design's functionality. Hence PDK is a central part of the circuit design.

In Physical verification files, it includes runset files for Design Rule Check (DRC) and Layout vs. Schematic (LVS) checks.Design Rule Check(s) (DRC) is the area of Electronic Design Automation that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called Design Rules.LVS performs a comparison process that verifies whether the geometric or layout implementation of a circuit matches the schematic representation.

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Chapter 1

IC Design Flow

There are different set of requirements for the process design flow.All the basic design is tested with the basic design flow.Sometimes we have to change our design when these type of design does not match with the requirements.Sometimes we have to change our need also in case of these type of changes are not allowed to make.Time to market of the design increases when the design goes wrong in its beginning time.So We have to make our design same as the actual one.The best control of process design of top down flow. Combined level of top down flow and bottom up design flow have no one directional flow.Some functions should be removed.

1.1 Design Specifications

Design specs are different for the different transistor level circuits.Limits on silicon area,power dissipation on delay time describe the expected functionality of the design block.By using design specifications it will give designers the freedom for placing the devices.In the starting phase design require particular type of limitations by increasing measures of the transistor.

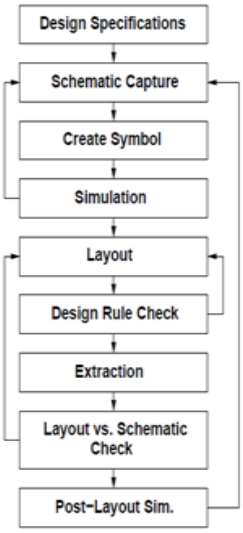

Figure 1.1: IC Design Flow

1.2 Schematic Capture

For the transistor level design By using a schematic editor we can capture the traditional method. To make up a design schematic editors give simple, good to draw, put and connect single components. power pin and ground connections pin are also included in the schematic, as well as all pins for the i/o interface of the circuit.This information is most useful for to generate the netlist which can be used at lastly.We can get a complete circuit schematic by using the different type of transistor level design flow.Some characteristics of the components and interconnects between the devices can be changed as a result of less making steps.

1.3 Symbol Creation

In the starting phase of the design it is very much useful to recognize that there are small components in the design and So by using this step we can make very simple schematic representation of the circuit.Symbol view of the circuit is also helpful for

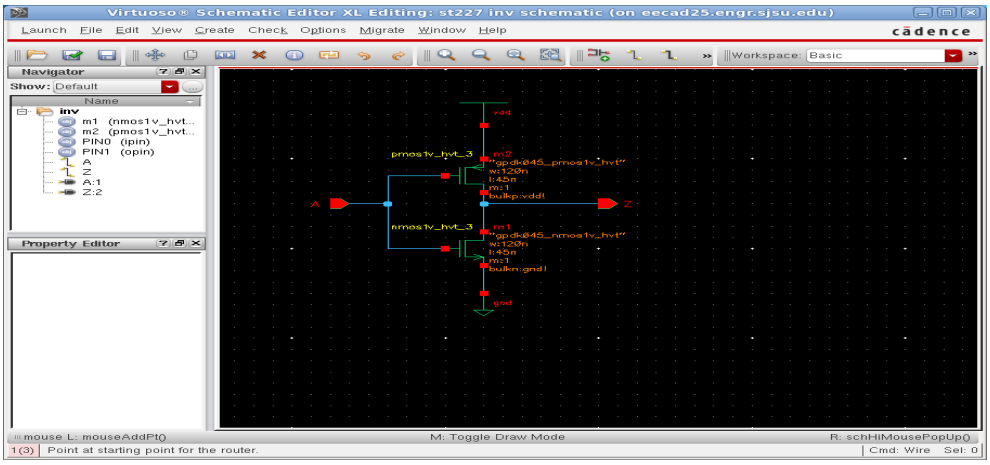

Figure 1.2: schematic

us to make simulation possible for that we have to combine all the components.So first we make the symbol of the circuit then we make the schematic creation of the circuit. Normally some properties of the components and the interconnects between the devices are changed as a result of different steps.

1.4 Simulation

A simulator tool is needed for make simulation of the circuit design.So schematic editor can be used to make the transistor level of design.By using the tool of simulation is called the simulation tool that should also be checked under the great designer and the designer should also check its functionality so we can make greater use of the design and we can make a very useful design for our future purpose.We have to make validation of the design also at the transistor level design.The more important and helpful thing is to complete the editing of this design before we make next step for the future design.Here the main part of the designer is that they can change some of the design properties and make the performance more useful and helpful.So from using the simulation results the designer can give the best results

out of it.And designers can also find the errors out of it.So designer can find errors easily like the added connection.

1.5 Layout

After making the schematic and symbol creation in the design now it is turn to make layout design.Layout design is the most important step in VLSI design.Layout editor is used to make the details of the total geometries and the partitioning of the each mask layer.So the overall circuit performance is depend on the area,speed and the power dissipation.By giving the more effort we can make the detailed mask layout of logic gates.So first we have make the sizing of the transistors.

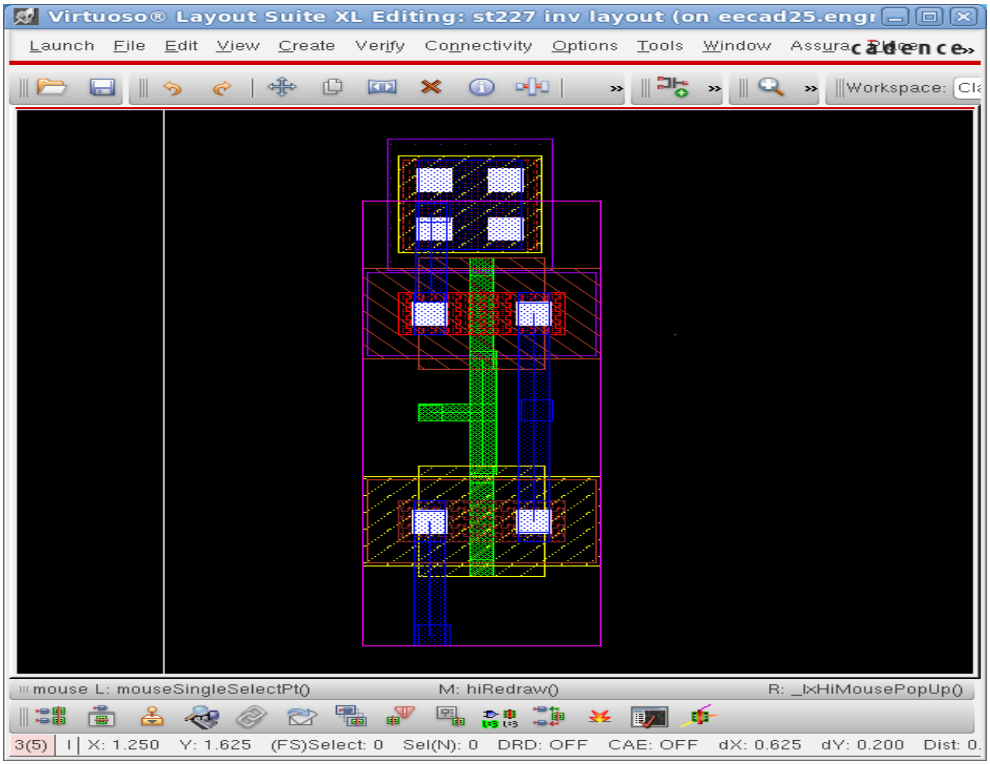

Figure 1.3: layout

1.6 Design Rule Check(DRC)

Design rule manual is provided by the Fabrication lab.By using the design rule manual designer makes the Design rule check deck.So DRC deck is the one kind of code which will check the design rule errors those are coming in the layout. Design rules are set by the designers.There are many different kind of design rules Length rules,width rules,area rules.Semiconductor manufacturer will give the different kind of Design Rules.We have to check that all the parts in the design should work correctly for that all the design rules should be check properly using the design rule manual.

1.7 Circuit Extraction

So after making the circuit layout in the design now it is time to make circuit extraction.Between the layers there are parasitic capacitors and parasitic resistors.The extracted netlist can provide a very accurate estimation of the actual device dimensions and device parasitics which ultimately determine circuit behaviour.So circuit behaviour can be determined by extracted netlist.In Layout Vs. Schematic check extracted netlist are also used.

1.8 Layout versus Schematic(LVS)Check

Layout Vs. Schematic check is the full form for LVS.Actual work of the Layout vs. Schematic check is to check the schematic with the layout design.When there is a mask layout design is ready the design should check with the schematic circuit which is actually made by us earlier.So for this checking first we have to take the mask layout design and we have to compare with the schematic design.We can not say that if the LVS is right then design is successful.It can be happen that design can not be successful still LVS is perfect. There can be different type of errors in

layout vs. schematic check such as missing the port connection.Before we do post layout simulation we have to first improve the errors those are coming in the layout vs. schematic checks.

1.9 Post-layout Simulation

After done the layout vs. schematic checks we have to do post layout simulation.It is called post layout simulation because after the layout is completed we are doing the simulation of that layout.By using the post layout simulation we can check the actual behaviour of the circuit.Post layout simulation will give us the result that if the circuit which we have made is working correctly or not.For post layout simulation designer should have checked the design rule check and layout vs. schematic check perfectly then after we can check the post layout simulation.If the design rule check and layout vs. schematic are getting violations then we can not make the post layout simulation. so first the DRC and LVS check should be pass then we do the post layout simulation.If we are getting success in the post layout simulation then we can not give the clarity that the our design is working fine.

Chapter 2

PDK Basics

PDK is short term for the "Process Design Kit".A Process Design Kit is a complete set of technology files to enable analog and mixed signal (AME) custom IC design in the Environment of the design.PDK is the set of technology files that can provide the designer to great help to make the design successful and make usable for the other design.PDK is the central part of the VLSI design.In Front end and back-end both the sides PDK is useful.In fabrication lab also pdk is used because DRM is made using the PDK technology file.The "Process" term in Process Design Kit is the specific foundry process supported by that particular PDK.In PDK different kind of technology files are present.Rule files,extraction files,setup files.

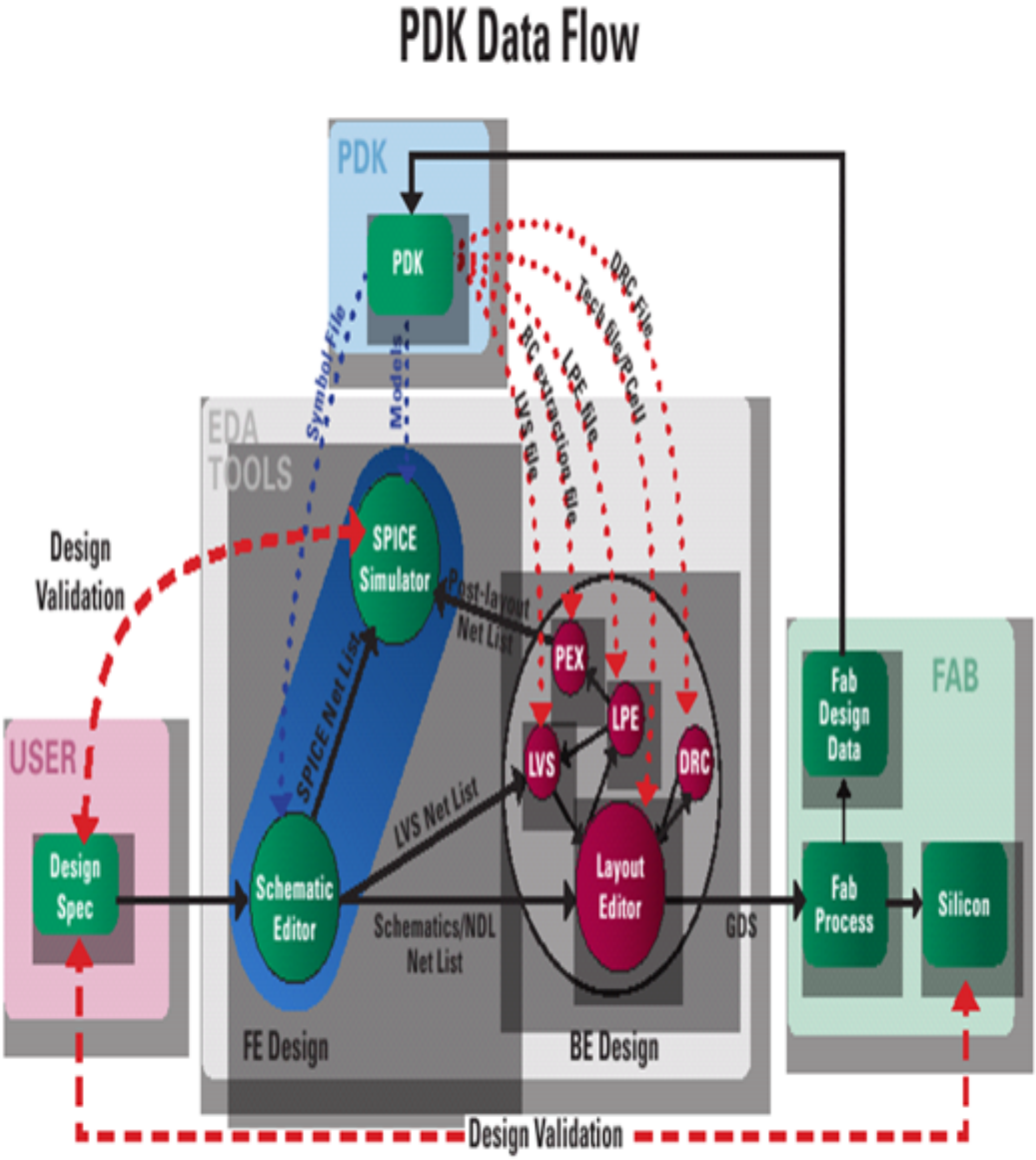

Figure 2.1: PDK Data Flow

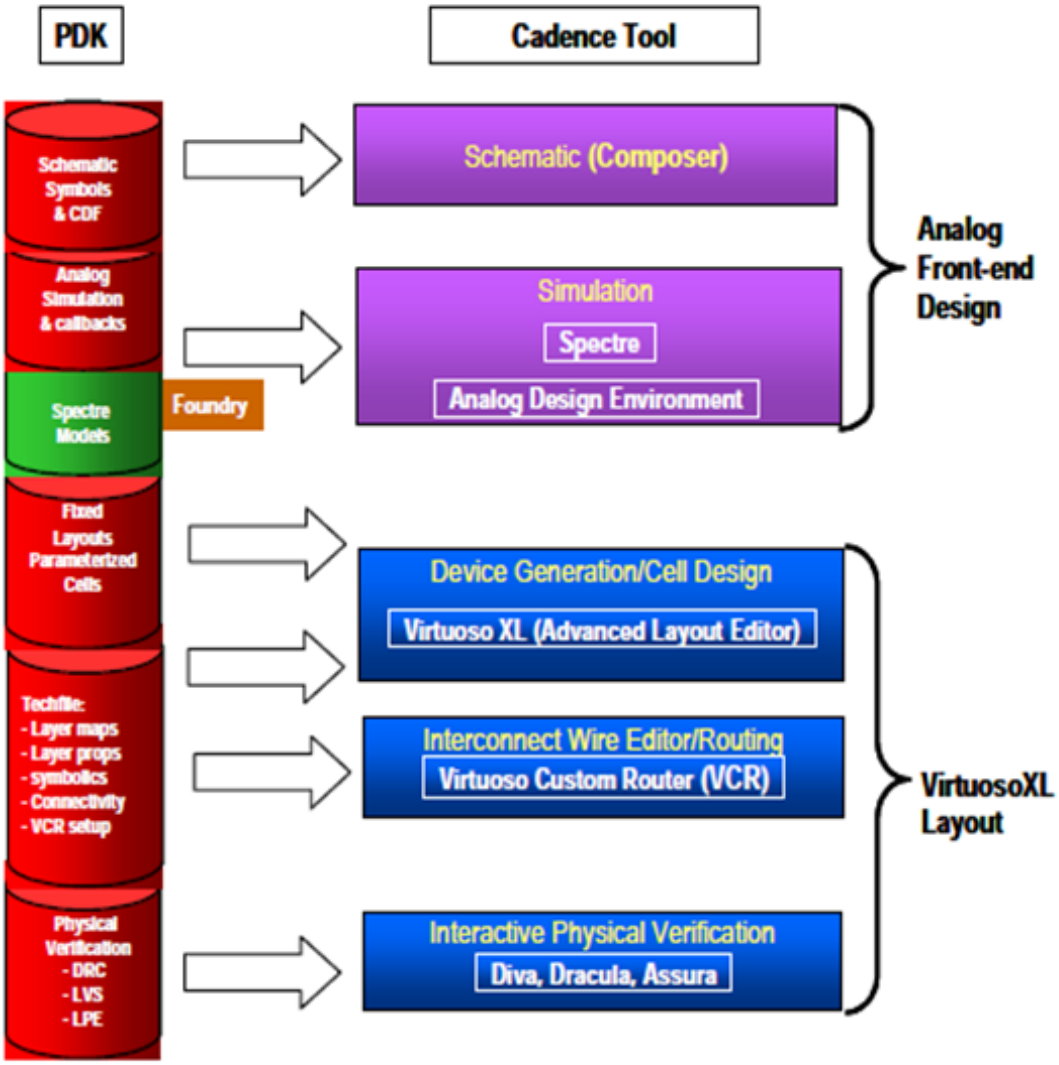

Figure 2.2: PDK Components

Chapter 3

PDK Validation

3.1 Installation of the PDK

Choose a computer where the PDK installation will be done. Go to the directory as follows: cd pdk_install_directory Untar the archive using:
zcat path_to_pdk_tar_file /pdk.tar.Z — tar xf - Set the permissions accordingly.

3.2 PDK Install Directory Structure/Contents

PDK consists of:

- Models
- Technology Database
- Physical verification rule decks and their associated setup files
- Documentation to assist users to run different design flows e.g.
  1. RTL to GDSII - Physical design flow
  2. Schematic to GDSII - Full custom analog & mixed signal design flow
  3. BigA&Smalld SOC design flow and vice versa

The following items setup the standard requirements for a PDK and enables the smooth automated flow for a designer.

Element	Description
	Technology documentation
device specifications	list of supported devices and their specifications
DRM(Design Rule Manual)	defines coding standard, layer design rules, device-specific design rules, and sample layouts
	Design Guidelines
symbols	schematic representation & properties associated with element in device library
sample layouts (or p-cells)	example of how to correctly layout &code devices; automated versions are pcells
placement calculations	calculates indirect parameters (callbacks)

Figure 3.1: PDK structure 1

All the checks are technology dependent.

The checks done are:

- Models and device setup verification
- Functional checks of decks (DRC deck, LVS deck, LPE deck etc)

technology file	defines layers and coding standards
SPICE models	model cards, subcircuits, and behavioral models required to model devices supported by the PDK
	Physical Verification
DRC decks	Checks layout against design rules.
LVS deck	Checks layout against schematic.
LPE deck	Updates pre-layout estimates with physical values.
RCX deck	Adds extracted devices to the circuit representation.

Figure 3.2: PDK structure 2

3.3 PDK setup Checks

This step is mandatory for the PDK validation at beta level. Check the technology options for layouts and schematics. Check the functionality of the scripts. Readability of the documents. Check the callback mode value pop-up. Set up proper help menus.

make sure it is IPDSS version compliant.

Check all the links.

3.4 Backend Checks

Checks to be performed at Validation end:

- Stream In/Stream Out

- display.drf
- Calibre DRC Deck Check
- Calibre LVS Deck Check
- LVS Parameter Mismatch

Verify Results of following Checks (Following mentioned checks need to be performed at Developers end)Make sure that all "FAIL" cases are properly waived.

3.5 OA Counter Check

Following task should be test for OA PDK only OA applies more restrictions to the database consistency two symbol views have to support the same counter to avoid design schematic Check.

Modify script,set proper library Name and rename output file.Run Virtuoso and load tested PDK library.load script in CIW and receive output file.

Perform above steps for libraries from previous PDK version and libraries from current PDK version.

Create difference between old and new pdk files. PASS/FAIL criteria: FAIL if counter mismatches will be found for the same name cells. Extra or Missed cells should not cause the ticket fail.

3.6 DRC Checks

As the technology shrinks, the requirements to check big databases of layout and functional verification become bigger and the time frame required is small. Post design phase if the design fails, it will result in huge losses and large time to market. The physical verificaiton is employed to make sure that the structural design is done and the layout according to the manufacturing and design guidelines.

Design rule check (DRC): defines the yield quality of the design. Layout versus schematic (LVS): This is used to check the functionality of the layout to schematic.

calibre DRC and LVS checks are one of them.

DRC doesnt guarantee that the circuit will perform as desired but it will be manufactured according to the rules without any issues. This formed the base to LVS. DRC checks the satisfactory level of the layout of a design as per the design rules. DRC is an imp step during the Physical verification including LVS, XOR Checks, ERC and Antenna Checks.

Design rules are a set of rules and the parameter values that are provided by the semiconductor foundries and are so given to ensure a smooth process and design at the defined technology.

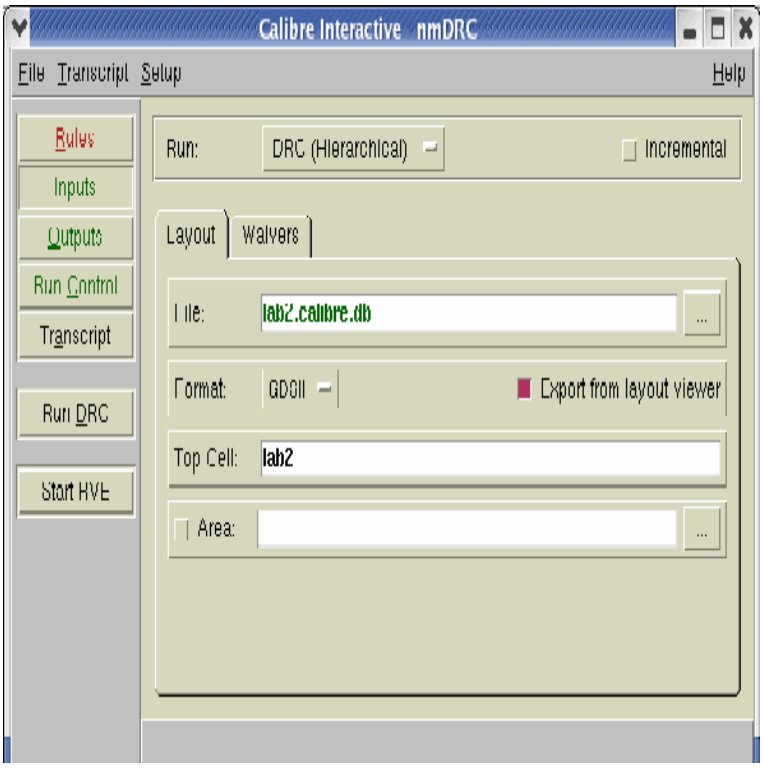

Figure 3.3: Calibre DRC

The first is single layer rules. A width rule specifies the minimum width of any shape in the design. A spacing rule gives the minimum distance between two

nearby objects. These rules will lay for each layer of manufacturing flow, where the lowest metal value is 100nm to 400 nm for highest value.

There should be a relationship between the two layers.An entity of certain type, such as a contact or via, should be coveredby a metal layer.

ADR(Academic design rules) are specified in form of a lambda. This simplifies existing layouts flows. Industrial rules are optimized.DRS (Design rule set) has become difficult with increasing technology.

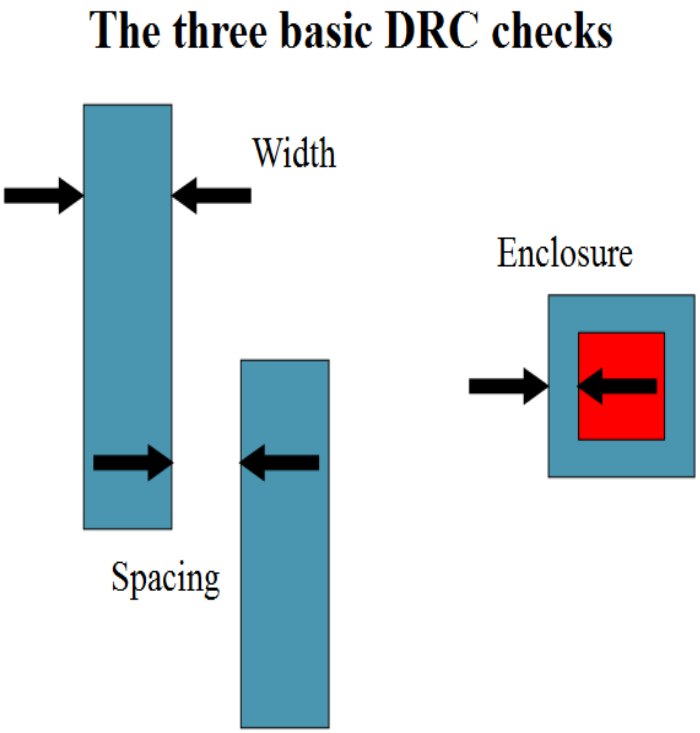

Figure 3.4: Basic DRC Checks

3.7 Design Rule Checking software

The main purpose of the DRC is to ensure sound functionality of the design and smooth manufacturing process with a good yield.

GDSII and process constraints are given to the tool for DRC checking and

to generate report of violations.Manual modifications in the design can be done in order to increase the yield.

Tools from mentor and magma usually understand the standard Verification Rule Format for DRC inputs and computation and the DRC command list is called runset.

- Minimum metal width
- Metal to metal spacing
- Metal fill density (for processes using CMP)
- Well to well spacing
- Minimum channel length of the transistor

3.8 Layout vs. Schematic checks

LVS tools usually employs the LVS rundeck to perform the computation and automation according to the inputs provided and required extractions performed.

LVS tools use the SRVF format to understand the metal constructions in an integrated circuit and the layout rundeck contains the information regarding the metal layers in the IC and the corresponding values and information

1.Extraction: The LVS tool processes db file that represent the circuit and performs area based logical operations to determine the polygon areas and infer the layers,via structures,terminals and wiring of the conductors in the design.

2.Reduction: During reduction the software combines the extracted components into series and parallel combinations if possible and generates a netlist representation of the layout database.

3.Comparison: The extracted netlist and the origninsl netlist is compared to check whether the netlitst is LVS clean using Graph Isomerism check.

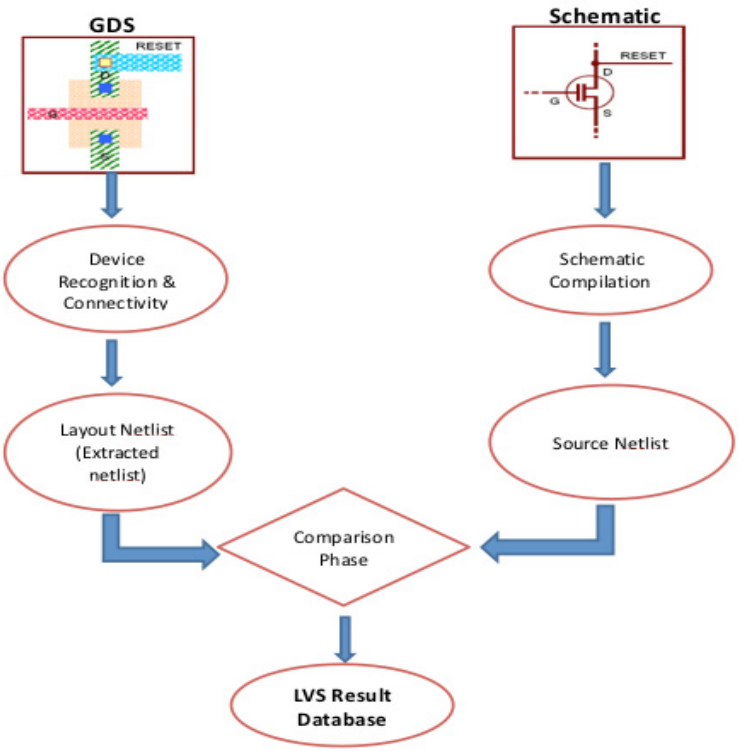

Figure 3.5: LVS Flow

There are a certain kind of errors that come up and the designer has to manually adjust the software parameters. Typical errors encountered during LVS include:

1.Shorts: Two or more wires that should not be connected have been and must be separated.

2.Opens: Wires or components that should be connected are left dangling or only partially connected. These must be connected properly to fix this. Component

3.Mismatches: Components of an incorrect type have been used (e.g. a low Vt MOS device instead of a standard Vt MOS device)

4.Missing Components: An expected component has been left out of the layout.

5.Parameter Mismatch: The netlist posseses some properties and tool can keep some guardband in order to remove the violations. When the parameters go out of that limit, the mismatch happens.

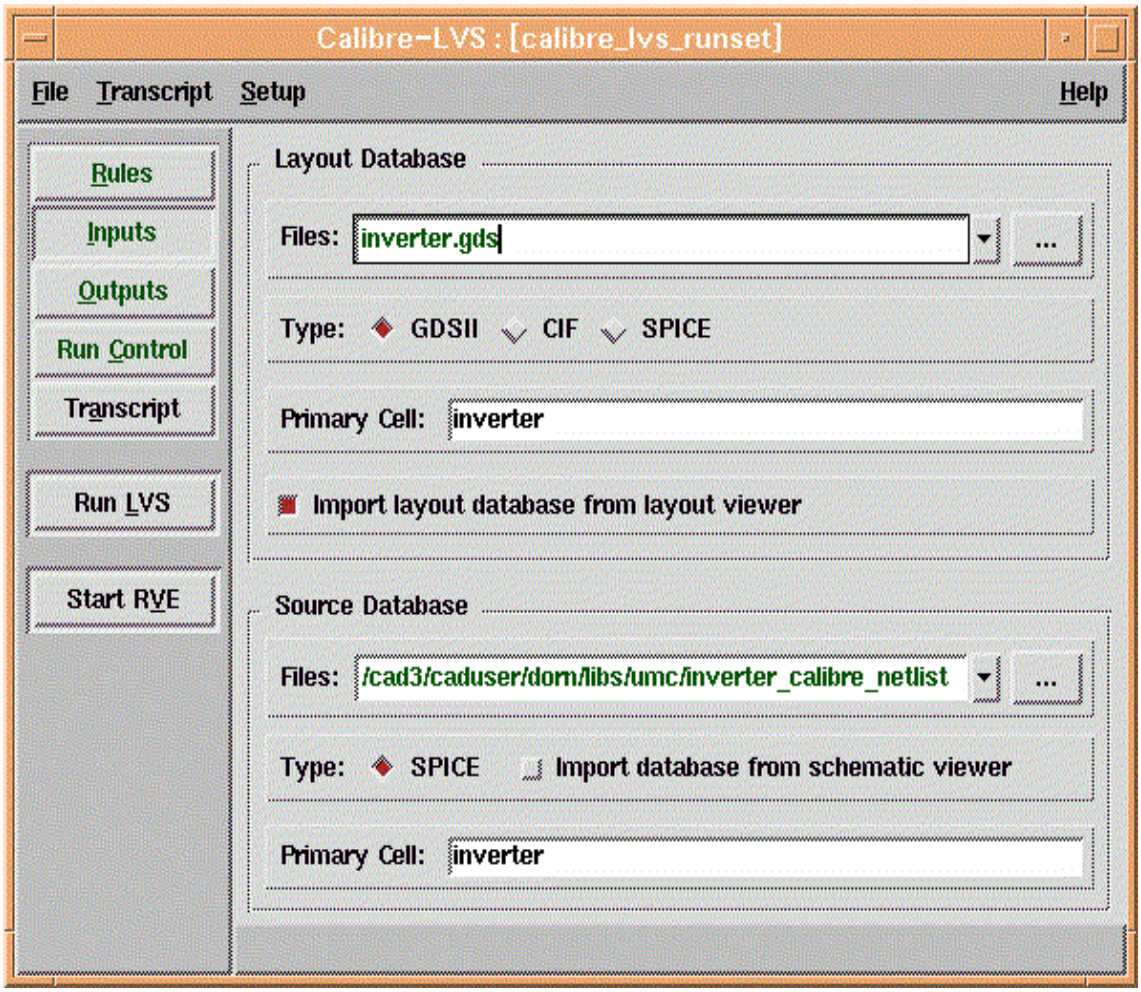

Figure 3.6: Calibre LVS

3.9 IP Regression

IP regression is Base DRC errors should be compared with the run results of previous pdk and the comparison should be captured in an xls spreadsheet. IP Regression is the task in which Run DRC on the IP designs mentioned in the validation plan with the current pdk.then run DRC on the IP designs mentioned in the validation plan with the previous pdk version.use the control file provided by the Design team or else use the default customization.In control file different switches are mentioned. from control file we can give path for GDS9.Run calibre waiver flow instead of simple DRC

run on IPs with current and previous PDK versions.New DRC violations should be validated as per DRM definition of the rule.we should provide remarks whether DRC violations are caused by DRC deck fault or due to layout issues.

Conclusion

- Process Design Kit is the complete set of technology files used to validate the different technologies.
- Design rule check and layout vs. schematic is validated using the process design kit.
- Design Rule Check(s) (DRC) is the area of Electronic Design Automation that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called Design Rules
- LVS performs a comparison process that verifies whether the geometric or layout implementation of a circuit matches the schematic representation.

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