# Interface Circuit Design for MEMS Based Piezoresistive Accelerometer

**Project Report**

Submitted in partial fulfillment of the requirements

for the degree of

**Master of Technology**

**In**

**Electronics & Communication Engineering**

**(VLSI Design)**

By

**Ashish Kumar Parashar**

**(12MECV03)**


**Department of Electrical Engineering**

**Institute of Technology**

**Nirma University**

**Ahmedabad-382 481**

**May 2014**

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Under the Internal Guidance of

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**Ahmedabad-382 481**

# Declaration

I hereby declare that the work presented in this thesis entitled "**Interface circuit design for MEMS Based Piezo-resistive Accelerometer** ", submitted towards completion of partial fulfillment for the award of the Degree of Master of Technology at **Institute of Technology, Nirma University, Ahemdabad (Gujarat)** is an authentic record of my work carried out under the guidance of **Dr. S.C. Bose Scientist F, CEERI, Pilani**, and **Mr. M. Santosh Scientist, CEERI, Pilani**. The project was done in full compliance with the requirements and constraints of the prescribed curriculum.This is to certify that

**Ashish Kumar Parashar**

# CERTIFICATE

This is to certify that the Major Project entitled **"Interface Circuit Design for MEMS Based Piezoresistive Accelerometer"** submitted by **Mr. Ashish Kumar Parashar (12MECV03)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology in VLSI Design** of **Nirma University of Science and Technology; Ahmedabad** is the record of work carried out by him under our supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for the examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

| | |
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**Ashish Kumar Parashar**

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# Abstract

This project presents an interface circuit designed for MEMS based piezoresistive accelerometer in standard 0.35u CMOS technology. Piezoresistive accelerometer is a sensor for g-force which represents acceleration standardized in terms of g = 9.8 m/s2. To read the output an interface circuit is required which consist of various CMOS circuits i.e. ADC, sample and hold, shift register, comparator. In this project 10 bit cyclic ADC components are designed and verified using Verilog-A. The results obtained through schematic confirm to the results obtained through Verilog-A.

# CSIR-Central Electronics Engineering Research Institute At A Glance

If knowledge implies power, then its basic ingredient information is a vital source of power. Scientific and technical information plays an important role in the development of nations. The proliferation of research and development programmers has resulted in an enormous output of the scientific proceedings, etc. that is growing exponentially. Added to this, there is a growing user population, making greater demands for information and increasing cost of materials and services.

**CSIR-CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE (CEERI), PILANI**

Central electronics engineering research institute, popularly known as CEERI, is a constituent establishment of the council of scientific and industrial research (CSIR), New Delhi. The foundation stone of the institute was laid on 21stSeptember 1953 by the then prime minister pt. Jawaharlal Nehru. the actual R & D work started towards the end of 1958. the institute (CEERI) has since blossomed into a center of excellence for the development of technology and for advanced research in electronics. over the years the institute has developed a number of products and processes and has established facilities to meet the emerging needs of electronics industry. CEERI, pilani is a pioneer research institute in the country and a constituent laboratory of CSIR, New Delhi, established in 1957 for advanced Research and Development (R&D) in the field of Electronics. Since its inception it has been working for the growth of electronics in the country and has established the required infrastructure and well experienced man power for undertaking R&D in the

following three major areas:

- SEMICONDUCTOR DEVICES
- MICROWAVE TUBE
- ELECTRONIC SYSTEMS

The activities of Microwave Tubes and Semiconductor Devices areas are done at Pilani, whereas the activities of Electronic Systems area are undertaken Pilani as well as at two centers of the institute at Delhi and Chennai. The institute has excellent computing facilities with many Pentium computers SUN/DEC workstations inter-linking with internet and E-mail facilities via VSAT. The institute has well maintained library with an outstanding collection of books and current periodicals published all over the world. The man power keeps abreast with the latest technologies by working in frontier areas and by interactions with foreign dignitaries through different exchange programs. CEERI with its over700 highly skilled and dedicated staff members, highly equipped laboratories and supporting Infrastructure is all set to take up the challenging tasks of research and development in the above areas.

**SEMICONDUCTOR DEVICES**

**IC Design Group**

The IC Design Group is a team of 12 R&D engineers/scientists. They cover expertise in various aspect of Digital IC Design, CMOS analog and mixed signal design and CAD tools, HDL based and full-custom design methodologies, as well as Semiconductor device modeling and simulation. The IC design Group has all the complete suite of VLSI CAD tools from the leading industry EDA vendors under the University programme.

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

The micro-machined inertial sensors which are composed of accelerometers and gyroscopes have a significant percentage of sensors containing silicon. They can be found mainly in the automotive industry, the biomedical applications, the household electronics, robotics, vibration analysis systems, navigation systems. There are various techniques to transform the action of acceleration on the sensor in to electric signal. These techniques are based on principles capacitive, piezoresistive, piezoelectric, and etc. The concept of accelerometer is not new, but market has motivated continuous researches in this kind of sensors in order to minimize the size and to improve the performance. As we know, the realistic applications create an enormous motivation for research on sensors MEMS, especially accelerometer. In this modern world, the applications require new sensors with a smaller size and high performances. In practice, rare are research which can provide an effective and complete methodology for the design of accelerometers.

## 1.1 Inertial Sensor

Micro-machined inertial sensors, consisting of accelerometers and gyroscopes, are one of the most important types of silicon-based sensors. Micro accelerometers alone have the second largest sales volume after pressure sensors. The large volume

demand for accelerometers is due to their automotive applications, where they are used to activate safety systems, including air bags, to implement vehicle stability systems and electronic suspension. However, the application of accelerometers covers a much broader spectrum where their small size and low cost have even a larger impact. They are used in biomedical applications for activity monitoring; in numerous consumer applications, such as active stabilization of picture in camcorders, head-mounted displays and virtual reality, three-dimensional mouse, and sport equipment; in industrial applications such as robotics and machine and vibration monitoring; in many other applications, such as tracking and monitoring mechanical shock and vibration during transportation and handling of a variety of equipment and goods; and in several military applications, including impact and void detection and saving and arming in missiles and other ordnance. High-sensitivity accelerometers are crucial components in self-contained navigation and guidance systems, seismometry for oil exploration and earthquake prediction, and microgravity measurements and platform stabilization in space. The impact of low-cost, small, high-performance, micro machined accelerometers in these applications are not just limited to reducing overall size, cost, and weight. It opens up new market opportunities such as personal navigators for consumer applications, or it enhances the overall accuracy and performance of the systems by making formation of large arrays of devices feasible. Micro machined gyroscopes for measuring rate or angle of rotation have also attracted a lot of attention during the past few years for several applications. They can be used either as a low-cost miniature companion with micro machined accelerometers to provide heading information for inertial navigation purposes or in other areas including automotive applications for ride stabilization and rollover detection; some consumer electronic applications, such as video-camera stabilization, virtual reality, and inertial mouse for computers; robotics applications; and a wide range of military applications. Conventional rotating wheel as well as precision fiber-optic and ring laser gyroscopes are all too expensive and too large for use in most emerging applications. Micromachining can shrink the sensor size by orders of magnitude,

reduce the fabrication cost significantly, and allow the electronics to be integrated on the same silicon chip.

## 1.2 Accelerometer

An accelerometer is an electromechanical device that measures acceleration forces. These forces may be static, like the constant force of gravity pulling at our feet, or they could be dynamic caused by moving or vibrating the accelerometer. There are two types of accelerometers developed and reported in the literature. The vast majority is based on piezoelectric crystals, but they are too big and to clumsy. They developed MEMS (micro electromechanical systems) accelerometers. The first micro machined accelerometer was designed in 1979 at Stanford University, but it took over 15 years before such devices became accepted mainstream products for large volume applications. In the 1990s MEMS accelerometers revolutionized the automotive-airbags system industry. Since then they have enabled unique features and applications ranging from hard-disk protection on laptops to game controllers. More recently, the same sensor-core technology has become available in fully integrated, full-featured devices suitable for industrial applications. Micro machined accelerometers are a highly enabling technology with a huge commercial potential.

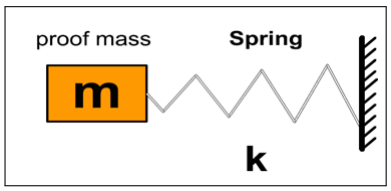


Figure 1.1: Basic Accelerometer operation machanisms

They provide lower power, compact and robust sensing. Multiple sensors are often combined to provide multi-axis sensing and more accurate data .An accelerometer is a sensing element that measures acceleration; acceleration is the rate of change of velocity with respect to time. It is a vector that has magnitude and

direction. Accelerometers measure in units of g  a g is the acceleration measurement for gravity which is equal to 9.81m/s. Accelerometers have developed from a simple water tube with an air bubble that showed the direction of the acceleration to an integrated circuit that can be placed on a circuit board. Accelerometers can measure: vibrations, shocks, tilt, impacts and motion of an object. Accelerometers are part of the most successful MEMS products available since1980s.The basic mechanism of sensing the acceleration is to monitor the displacement of a proof mass attached to a spring as schematically illustrated in Figure.where k is the spring constant and o is the resonant frequency of the system. There are several approaches of sensing the amount of displacement of the proof mass that include as piezoresistive, capacitive, tunneling and optical changes. The capacitive accelerometers play an important role due to their good temperature stability, high sensitivity and low power Consumption.

## 1.3 Types of Accelerometer

There are two types of accelerometers. What differentiate the types is the sensing element and the principles of their operation.

### 1.3.1 Capacitive Accelerometer

In a capacitive accelerometer, the displacement of the proof mass is monitored by changes in capacitance of a parallel plate capacitor where one of the plates is attached to a spring as schematically illustrated in Figure. When the external acceleration is applied to the accelerometer, the moving plate (proof mass) will move from its rest position that changes the capacitance between the moveable and fixed plates. The change in capacitance is usually measured using bridge circuit.

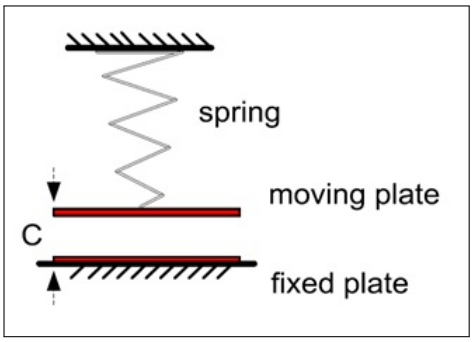


Figure 1.2: Capacitance Accelerometer

### 1.3.2 Piezoresistive Accelerometer

The piezoresistive accelerometer is based on strain gauge technology and is best suited for low frequency applications. It was the first micro machined accelerometer produced and one of the first to be commercialized. The operation principle is based on the change of resistance due to stress generated by deflection of Si beams attached to the proof mass as illustrated in Figure Piezoresistive Accelerometer By positioning the silicon piezoresistors at the highest stress point (usually where the beam attaches the substrate) the resistance change can be maximized. Subsequently, a resistive half-bridge or full bridge can be formed by employing two or four piezoresistors to measure the resistance change.

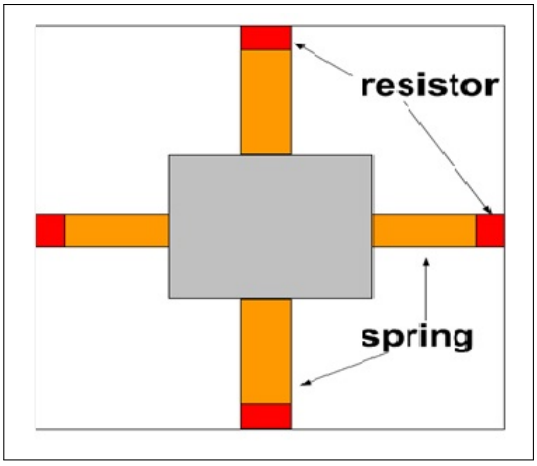


Figure 1.3: Piezoresistive Accelerometer

The main advantages of piezoresistive accelerometers are their simple structure and fabrication processes.

## 1.4 Applications for Accelerometer

From industry to education, accelerometers have numerous applications. These applications range from triggering airbag deployments to the monitoring of nuclear reactors. There are a number of practical applications for accelerometers; accelerometers are used to measure static acceleration (gravity), tilt of an object, dynamic acceleration, shock to an object, velocity, orientation and the vibration of an object. Accelerometers are becoming more and more ubiquitous: cell phones, computers and washing machines now contain accelerometers. Other practical applications include:

- Measuring the performance of an automobile
- Measuring the vibration of a machine
- Measuring the motions of a bridge
- Measuring how a package has been handled

## 1.5 Selecting an Accelerometer

When selecting an accelerometer for an application the first factors to consider are:

**Dynamic Range:** Dynamic range is the +/- maximum amplitude that the accelerometer can measure before distorting or clipping the output signal. Dynamic range is typically specified in g's.

**Sensitivity:** Sensitivity is the scale factor of a sensor or system, measured in terms of change in output signal per change in input measured. Sensitivity refer-

ences the accelerometers ability to detect motion. Accelerometer sensitivity is typically specified in milli volt per (mV/g).

**Frequency response:** Frequency response is the frequency range for which the sensor will detect motion and report a true output. Frequency response is typically specified as a range measured in Hertz (Hz).

**Sensitive axis:** Accelerometers are designed to detect inputs in reference to an axis; single-axis accelerometers can only detect inputs along one plane. Tri-axis accelerometers can detect inputs in any plane and are required for most applications.

**Size and Mass:** Size and mass of an accelerometer can change the characteristics of the object being tested. The mass of the accelerometers should be significantly smaller than the mass of the system to be monitored.

# Chapter 2

# Piezoresistive Accelerometer

Piezoresistors are widely used in micro system sensing due to their low cost, small size, low phase lag, and large dynamic range. They have been used to create MEMs nano manipulators, mischaracterization instruments, pressure sensors, inertial sensors, mass sensors, and elements of high-speed atomic force microscopes (AFMs). Many designers often only consider the performance of the transuding element in the full sensing system, leading to the perception that these sensors are too noisy for precision applications. However, excellent performance may be obtained if the design properly manages the tradeoffs between size, bandwidth, resolution, power, and dynamic range. This requires the ability to accurately predict the effect of all relevant noise sources on the performance of the full sensing system. Here in, we present a systems approach that makes piezoresistive sensor system optimization possible. The emphasis here is on the conceptual layout of a system model, the technical details of modeling the noise sources associated with its components, and the insights and results that come from integrating the individual components to form a view of the systems performance.[1]

## 2.1 Piezoresistive Sensor System Model

In This model is generic in the sense that the sensor may be used to measure a force, F that is applied to the compliant element or a displacement, of the compliant element. The sensor system is composed of a voltage source, VS, which energizes a span temperature compensated (STC) Wheatstone bridge. An instrumentation amplifier boosts the signal from the bridge, which is nulled with a bias voltage and read by an Analog-to-Digital Converter (ADC). This circuit is commonly used and adds little noise to the Strain signal. The model is generalized so that it may be used with a wide range of applications. Through this model, we may gain insight on best design of general and specific sensor systems The model assumes the use of high-performance electrical Components instrumentation amplifier (Analog Devices AD624), voltage source and bias (Texas Instruments REF50xxseries), and ADC (National Instruments 9215 ADC). [2]

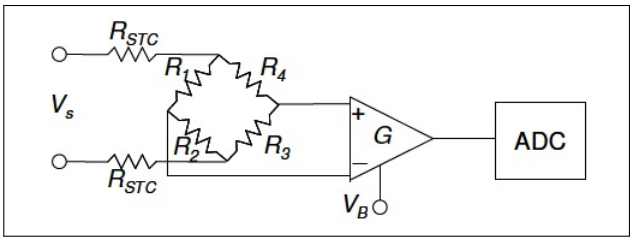


Figure 2.1: Schematic Diagram of DC piezoresistive sensor system [1]

The system model includes the relevant thermal, electrical and mechanical noise sources. These noise sources are included in the model for each subsection, as shown in Figure. The subsections are arranged as shown in Figures above to create the full system model. These figures are a visual representation the characteristic equation of each part of the sensor system. The Laplace transform of all filters, F(s), in the model are assumed to be non-dimensional and have unity, steady-state gain. All n noise sources, n, are considered to be unbiased, uncorrelated, and normally distributed with spectral densities, Sn (f). We apply the following inputs to the compliant element, (i) a force or displacement signal, (ii) mechanical noise, Mv,

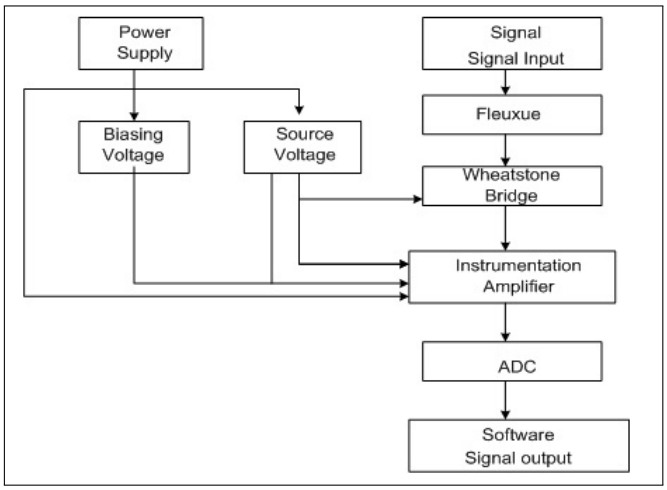


Figure 2.2: Block diagram of piezoresistive accelerometer [1]

e.g. vibrations, and (iii) thermo mechanical noise, Mt, with the spectral density. A mechanical noise scaling factor is used to convert between displacements and forces. This factor has a unity value for displacement Signals or value of k for force signals.[1]

### 2.1.1 Flexure model

The flexure acts as a (a) mechanical filter and (b) transducer that converts a force or displacement into a strain. The flexure behavior is therefore integrated as a gain, F, within the model. The appropriate gain depends upon the intended use of the sensor (force vs. displacement sensing) and the grounding of the flexure (fixed guided or fixed-free boundary)

### 2.1.2 Wheatstone bridge model

The signal is transformed from the mechanical domain to the electrical domain via a Wheatstone bridge. The bridges sensitivity depends upon the bridge type. The type is defined as the number of strain sensitive resistors within the bridge divided by 4. The bridge thermal type determines how the bridge output changes with

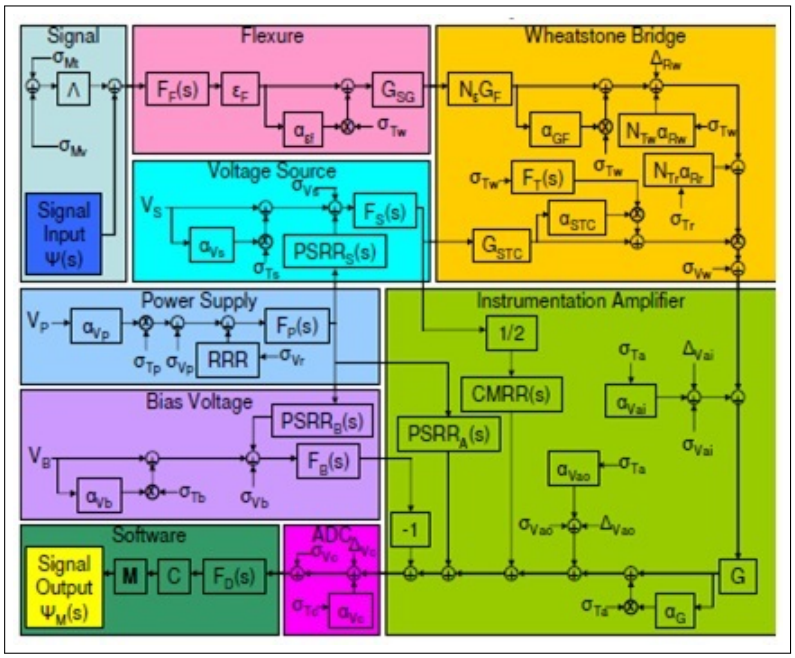


Figure 2.3: Presentation with electrical and thermal noise sources [2]

temperature and is calculated by summing the directional (±) normalized thermal sensitivity for each of the piezoresistors mounted on the device and dividing by 4.

### 2.1.3 Instrumentation amplifier model

The Wheatstone bridge output signal is boosted via the instrumentation amplifier in order to scale it to the full usable range of the ADC. The required amplifier gain is calculated by constraining the maximum input to the ADC to output, which is generally 0.9, or 90% of the ADCs full voltage range. The maximum signal is found by inputting the maximum strain safely achievable in the flexure after the flexure gain.

### 2.1.4 Source voltage model

The source voltage chip provides a steady energizing voltage to the Wheatstone bridge. It is subject to electronic and thermal noise, but a filter is generally used

to attenuate this noise on the DC signal. Any variation in the source voltage will erroneously appear as a force or displacement signal.

### 2.1.5 Bias voltage model

The signal can be adjusted to the center of the operating range through the use of the bias voltage. This voltage simply provides a steady state offset for the output of the instrumentation amplifier. A filter may likewise be used to attenuate electrical or thermal noise.

### 2.1.6 Power supply model

The power supply can produce variations in the force or displacement signal by varying the voltage supply to the main chips in the piezoresistive sensor circuit: the source voltage, the bias voltage and the instrumentation amplifier. These effects are in general highly attenuated through power supply rejection ratios in each of the chips. A low pass filter may be used to further attenuate the electronic and thermal noise in the power supply. The power supply will generate thermal and voltage noise. The voltage noise can be separated into a diode bridge based ripple which is attenuated by passing through the power supply electronics and a broad spectrum noise generated by these electronics.

# Chapter 3

# Analog To Digital Converter

## 3.1 Analog to Digital Converter

Analog to Digital Converter acts as an interface between the analog real world and the digital world. ADCs are used in a number of applications such as multimedia, communication, sensors etc. ADCs execute the operation in different steps i.e. sampling the continuous input, quantizing the sampled data and assigning the digital code to quantized output.[5]

## 3.2 General Characteristics of ADCs

Transfer characteristic of ADCs shows the relation between analog input voltage and digital output code. Here the analog input can have any value between 0 to $V_{ref}$ while the digital code is restricted to fixed or discrete amplitude. The ideal transfer characteristic curve of a 3-bit ADC is shown below each unique digital code corresponds to a small range of analog input voltages. This range is 1 LSB wide (code width") and centered around the code center." All input voltages resolve to the digital code of the nearest code center. The difference between the analog input voltage and the corresponding voltage of the nearest code center (the difference between the solid and dashed lines in Figure below) is the quantization error. Since

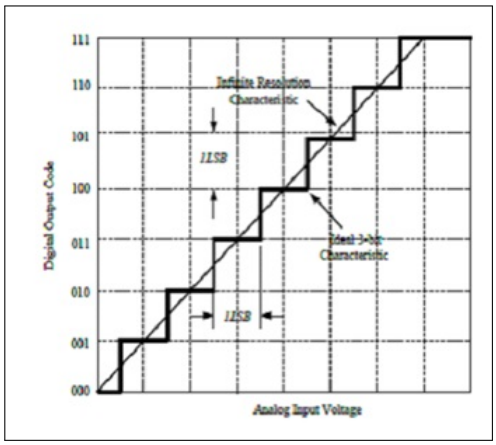


Figure 3.1: Characteristics of ADC[5]

the A/D converter has a finite number of output bits, even an ideal A/D converter produces some quantization error with every sample.

## 3.3 ADC performance characteristics

The various parameters that determines the performance of ADC can be illustrated through

- Static Characteristics
- Dynamic Characteristics

## 3.4 Classification of ADCs

ADCs can be classified based on the resolution, conversion rate, area, input range, power consumption and other constraints. For a particular application, ADC is selected while considering all these factors. Classification of ADC depending upon the resolution and conversion rate is represented in the table below According to specifications of sensor, a 10 bit medium speed ADC is required. There are two architectures for a medium resolution ADC

| Conversion Rate | Types of ADCs | Resolution |
|---|---|---|
| Slow (conversion frequency < 100 Hz) | Integrating | Very high resolution (greater than 14 bits) |
| Medium (conversion frequency = 104- 105Hz) | Successive Approximation Cyclic | Moderate resolution (10 to 14 bits) |
| Fast (conversion frequency = 1 to 600 MHz) | Flash Multiple-bit Pipelined Folding and Interpolating | Low resolution (6 to 8 bits) |

Figure 3.2: Classification of ADC[6]

- Successive approximation ADC
- Cyclic (algorithmic) ADC

## 3.5 Cyclic/Algorithmic ADC

Cyclic ADC is similar to pipeline ADC with single stage and the residual output fed back to the input. They are better compared to the Pipelined structures in terms of area but the conversion rates are low. Cyclic ADCs are well known for their ability to achieve moderate resolution with small silicon area at low or medium frequencies.

### 3.5.1 Operation/Principle of Cyclic ADC

In block diagram of cyclic ADC is shown in figure above. It consists of a sample and hold (S/H) circuit, comparator, multiplier which performs multiply by 2 operations, adder/subtractor circuit. S/H circuit is required to sample the voltage, $V_{in}$.

Switch S1 is used to switch the input of S/H circuit between $V_{in}$ or the output

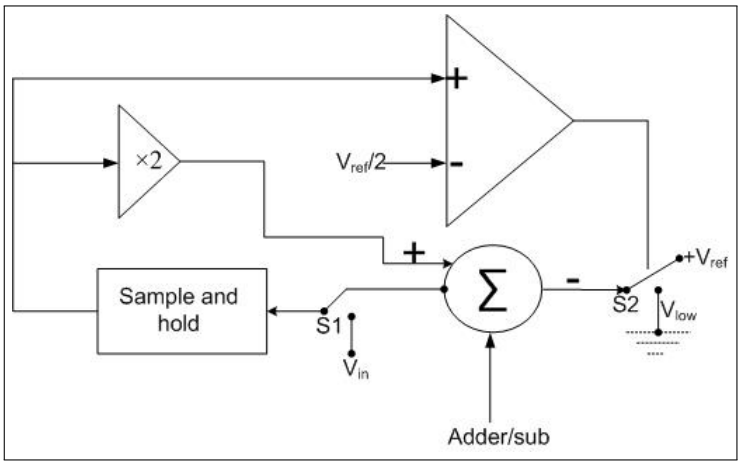


Figure 3.3: Block diagram of Cyclic ADC[6]

of multiplier circuit. Initially, switch will connect to $V_{in}$. The sampled input is compared with the reference voltage, $V_{ref}/2$. According to the comparison, comparator produces a logic 1 or logic 0. The output drives the adder/subtractor circuit. The circuit will subtract either $V_{ref}/2$ or $V_{low}$ to produce the residue voltage. This output is sampled at multiplier which has a gain of 2. The output of multiplier is then sampled at sample and hold circuit through switch S1 for next bit conversions. In this way, the cycle repeats for next clock cycles. It is the digital part of circuit which generates the required clocks for circuit. Clocks help in switching between the different stages i.e. sampling, multiply by two etc.

### 3.5.2 Flowchart of Cyclic ADC

The reference voltage of comparison is fixed at $V_{ref}/2$. Input voltage $V_{in}$ is compared with the reference voltage, $V_{ref}/2$ in first cycle. If $V_{in}$ is greater than $V_{ref}/2$, then the output bit will be 1 and

$$V_{in}(i+1) = 2V_{in}(i) - V_{low}$$

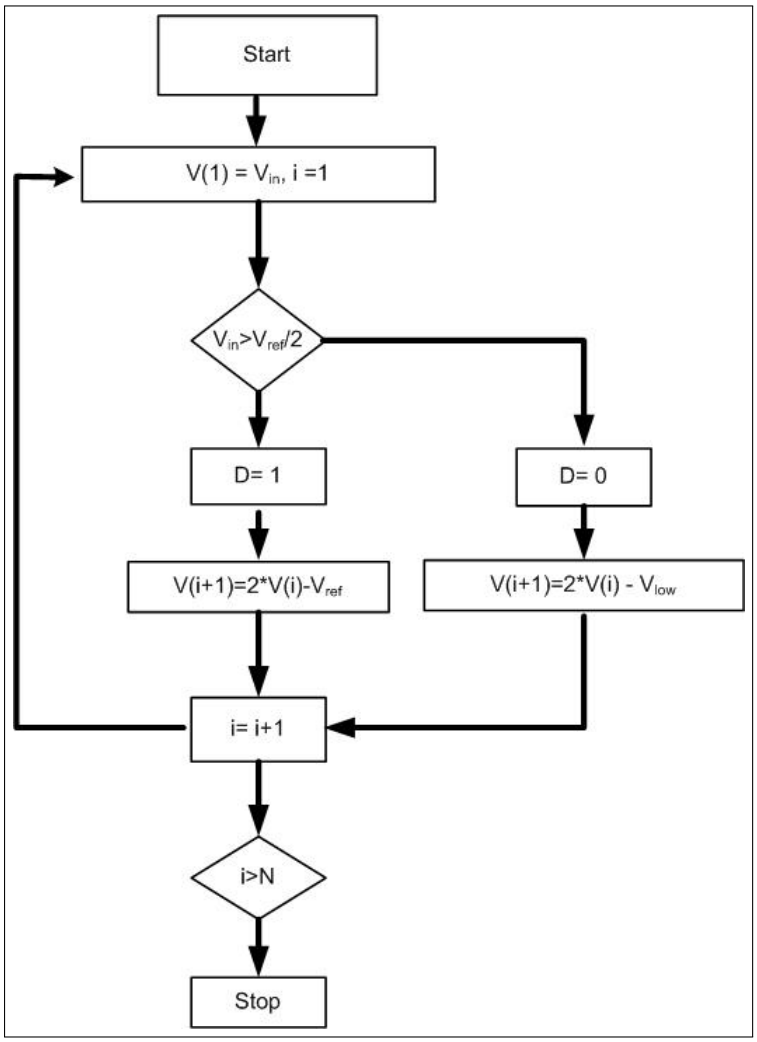


Figure 3.4: Flow graph of cyclic ADC

Here, $V_{in}$ (i) is the previous stage input voltage and $V_{in}$(i+1) is the residue voltage which is used in next cycle for comparison. $V_{low}$ represents the lower range of ADC. If $V_{in}$ is less than $V_{ref}/2$, then the output bit will be 0 and

$$V_{in}(i+1) = 2V_{in}(i) = V_{ref}$$

$V_{ref}$ represents the highest voltage value for which ADC works. In general, the principle can be represented by a simple equation;

$$V_{in}(i+1) = 2V_{in}(i) - bi * V_{ref} - bi\_bar * V\_LOW$$

## 3.6 Successive Approximation ADC

### 3.6.1 Principle

It works on the principle of binary search method. Figure represents the principle for an N-bit ADC working in the range 0 to $V_{ref}$. The weight of MSB i.e. Nth bit can be represented by $V_{ref}/2$. Initially, $V_{in}$ is compared with weight of MSB. This comparison gives the MSB output. If $V_{in}$ is greater than $V_{ref}/2$ then MSB is set to logic 1 otherwise, set to logic 0.If the output is 0 then, next reference voltage ($V_{ref}$*) of comparison is set to $V_{ref}/4$, which represents the weight of next significant bit. For a logic 1 output, next reference voltage ($V_{ref}$*) is set to sum of weights of MSB and the next significant bit i.e. $V_{ref}/2 + V_{ref}/4$. The new value of $V_{ref}$*, is compared with the sampled input voltage to produce the next bit i.e. (MSB-1) output. For N-bit ADC, this conversion repeats for N cycles. When N cycles are completed, then next $V_{in}$ is sampled for its N- bit conversions.

### 3.6.2 Block representation

Figure shows the block level representation of SAR ADC. It consists of a sample and hold (S/H) circuit, comparator, Successive Approximation Register and a D/A converter. Initially, S/H circuit samples the input voltage which is to be converted into digitized form. Output of this circuit goes to the input of comparator. It remains constant during the conversion time which will be N- clock cycles for N bit conversion. The second input of the comparator is VD/A, which comes from the DAC. It changes according to previous bit output of comparator. Initially, VD/A is equal to $V_{ref}/2$. ADC also consists of a SAR logic block which is the digital control circuit. It provides digital input to DAC by manipulating the previous bit of comparator and also stores the digital output for $V_{in}$.

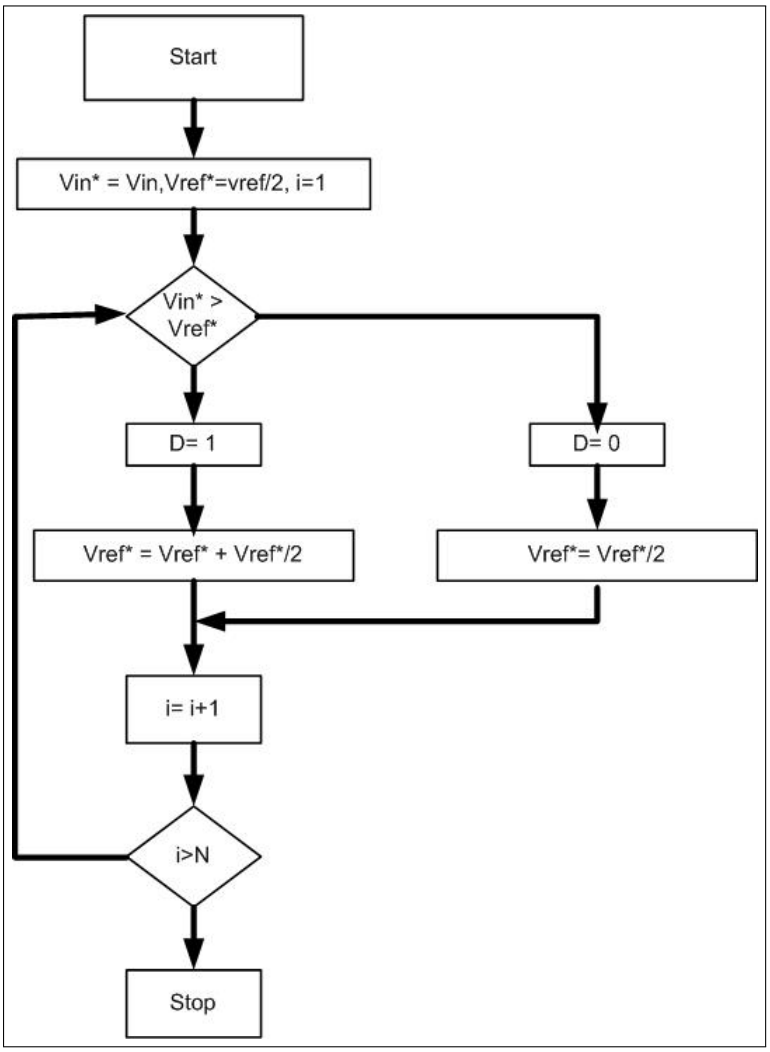


Figure 3.5: Block Diagram of SAR ADC

### 3.6.3 Limitations of SAR ADC

For the implementation of SAR architecture, a DAC is required which is generally based on charge scaling method. The architecture of an N-bit DAC is shown on figure. It requires a number of capacitors with variable capacitances. The capacitance for largest and smallest capacitors is C and C/2N-1. So, the maximum ratio will be 2N-1. The ratio depends upon the resolution of converter. For a high resolution DAC, this ratio will be very large. For example, if a 10-bit DAC is to be implemented then the ratio will be 512. It results in the large element spread. The

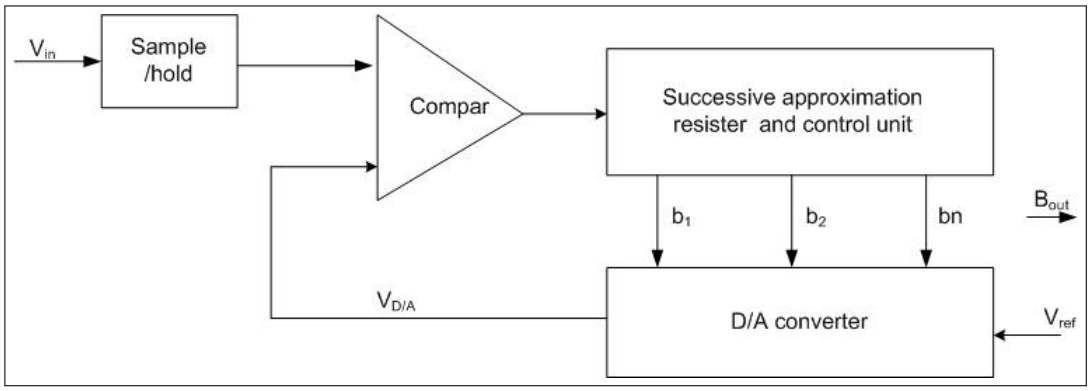


Figure 3.6: Block Diagram of SAR ADC[7]

selection of the size of capacitor becomes difficult with this spread.

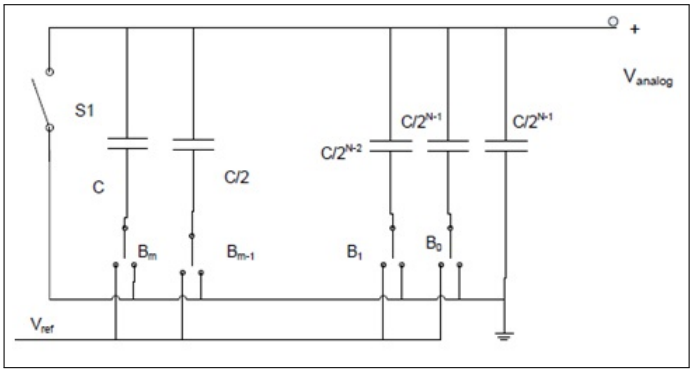


Figure 3.7: N-bit charge scaling DAC[8]

The main problems with the selection of size are:

- If the size of capacitor is very small then, the uniformity and matching accuracy of the capacitors is reduced. It can create error in the output of DAC.
- If capacitor is large it will draw a large amount of current from ground and reference input during the transients. It leads to large settling time of DAC.
- With increase in the capacitance, area increases in the same ratio. So, for 512 times increase in capacitance area of largest capacitor will be approximately 512 times of smallest capacitor.

## 3.7 Comparison of Cyclic and SAR ADC

Both the architectures use a S/H circuit and a comparator. In addition to this, cyclic architecture consists of a multiplier and an adder/subtractor circuit which requires simple circuit implementations but, SAR architecture uses a SAR block and a DAC. The accuracy of SAR is limited by the DAC. Also, the area requirement of SAR ADC increases because of the large number of capacitor in DAC. There are no such issues with the use of cyclic ADC. Therefore, cycle ADC is suitable for the interface circuit of piezoresistive accelerometer

# Chapter 4

# OP-AMP MACROMODELING

## 4.1 Macromodeling

The Macromodel is a model that uses simulation circuit to capture the desired performance of a circuit .the advantage of macromodel is that simulation of large circuits or system become quicker. Macromodeling methodologies for algebraic functions, piecewise linear function, series expansions, and s- and z- transfer function. These methodologies not only are applicable to modeling complex analog circuit and system, but also improve both simulation capability and flexibility of analog simulation without internal modification [6].

## 4.2 Macro modeling Of Op-amp

Op-amp (Operational amplifier) is one of the most important circuits in IC (Integrated Circuit) design. In the ideal situation, Op-amp has characteristics such as infinite differential voltage gain, zero output resistance and infinite input resistance. Yet in the reality, the op-amps are variety in structure, and each has its own characteristics. In circuit level it is reflected in the difference of circuit structure and performance. Op-amp model has many types. According to analyzing accuracy, it can be divided into ideal op-amp model, non-ideal op-amp model and op-amp macro

model, etc. According to the function, the model can be divided into dc model, ac small signal model, large signal model and noise model [6], etc. When we design an Op-amp in system level, macromodel got a very wide range of applications because of it does not involve specific transistors in the circuit and can simplify the simulation process to acquire the basic performance of circuit. A macromodel uses resistors, capacitors, inductors, controlled sources, and some active devices (mostly diodes) to capture the essence of the performance of a complex circuit like an op amp without modeling every internal component of the op-amp.[6] The advantage of the macro model is to permit the tradeoff of model complexity for decreased simulation time. We will start by developing models for the op amp that include various characteristics of the op amp. The complexity of the model depends on what op amp characteristics are being modeled. It is always a good practice to use the simplest possible model in a given application to avoid excessive computational time and memory requirements. The simplest model for the op amp is shown in Fig. 4.1. Note we have used the notation Avd to specify the differential voltage gain of the op amp. This simple op amp model is probably suitable for 90% of the op amp circuit simulations.

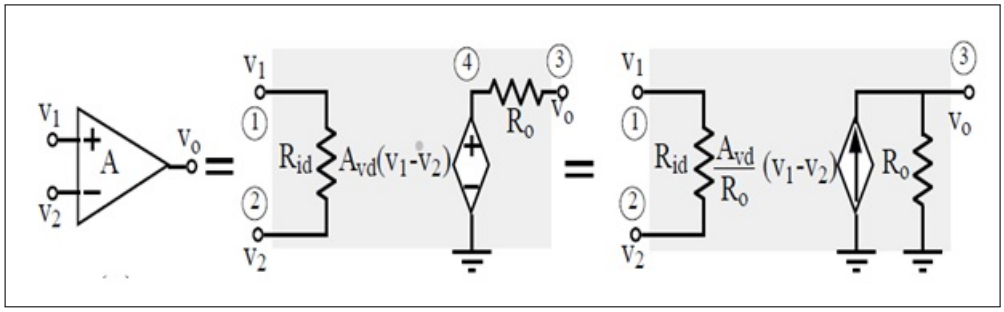


Figure 4.1: (a) Op-amp symbol. (b) Thevenin form of simple model. (c) Norton form of simple model[6]

Fig. illustrates an important point about computer models. The simple models of Fig. part(b) and Fig. part(c) are identical in their electrical performance. However, the Norton form of the model has one less node. Fig. part(b) has 5 nodes while

Fig. part(c) has four nodes Reducing the number of nodes will decrease the order of the solution by a factor of one that generally simplifies the numerical solution and decreases simulation time. With everything else equal, the user should use the model with the minimum number of nodes.

## 4.3 Verilog-A

Verilog-A provides a single language and a single simulator that is shared between block designer and system designer and between analog designer and digital designer [9]. Therefore, it has a big impact on the design of mixed-signal system. Verilog-A can also provide an easy and single design flow, which can naturally support analog, digital and mixed-signal block. And in that circumstance, different designers that are responsible for analog, digital and mixed-signal design can work together more harmonious and communicate with each other more smoothly.
Verilog-A can be applied in four main aspects as below:

1. To model components The basic functions are such as describing the based devices, modeling the function block (A/D, filter, S/H etc.). The ability to add models to a circuit simulator such as Cadence Virtuoso AMS dramatically increases it range, and makes it immensely more powerful.

2. To create a testbench .A testbench is used as a stimulus usually consisted by ideal component and provides a platform for circuit verification. When a designer wants to verify an A/D convert, a D/A convert as the stimulus is essential. Naturally, Verilog-A is used to solve the problem.

3. To accelerate the speed of simulation As the design is getting more and more complex, designers have to spend increasingly time to verify and simulate the design. Verilog-A describes circuit in behavioral level will be simulated faster than that of in transistor level.

4. Can verify the mixed-signal system Verilog-A can combine the simulation of analog, digital and mixed-signal design. It is extremely useful for verifying the mixed-signal system.

## 4.4 Macro modeling of op-amp using Verilog A

When we want to design an op-amp, we should definite the spec of it, such as power consumption, gain, PM and so on. Among those parameters, power consumption of the op-amp is mainly determined by Iq (static current), usually when we count it in a circuit power consumption, it must also add the load current. Gain, namely magnification is one of main indexes in op-amp. Simple model can only consider its gain and ignore other performance parameters. Based on these we can establish a Thevenin form of an op-amp model as shown in figure

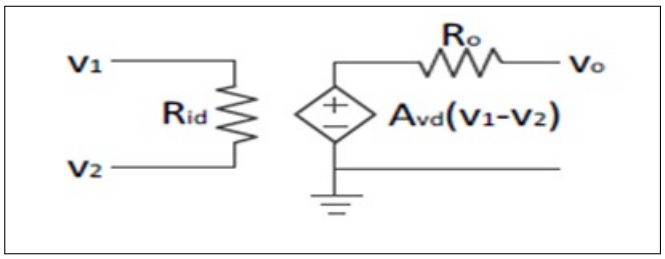


Figure 4.2: Thevenin form of op-amp model

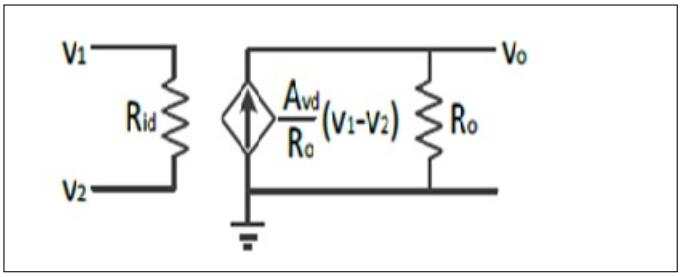


Figure 4.3: Norton form of op-amp model

Above figure has the Norton form of op-amp model: From these two models we can get that the output of the op-amp is:

VO = Avd(V1-V2).

And the description by Verilog-A is as below:

electrical out, inp, inn;

parameter real gain=1e5;

analog begin

V(out) ⟨+ gain*V(inp,inn);

The op-amp provided to me here by at the lab was analyzed by me to get dc_ gain, unity gain bandwidth, phase margin and slew rate. In the figure above, has two input terminal, v- is negative terminal and V+ is positive terminal. Vdd is power supply and Vss is ground. Value of Biasing current is 120 A and compensation capacitance is 499.99f F of transistor level op-amp .

## 4.5 Testing circuit of op-amp

## 4.6 Transistor level Op-amp

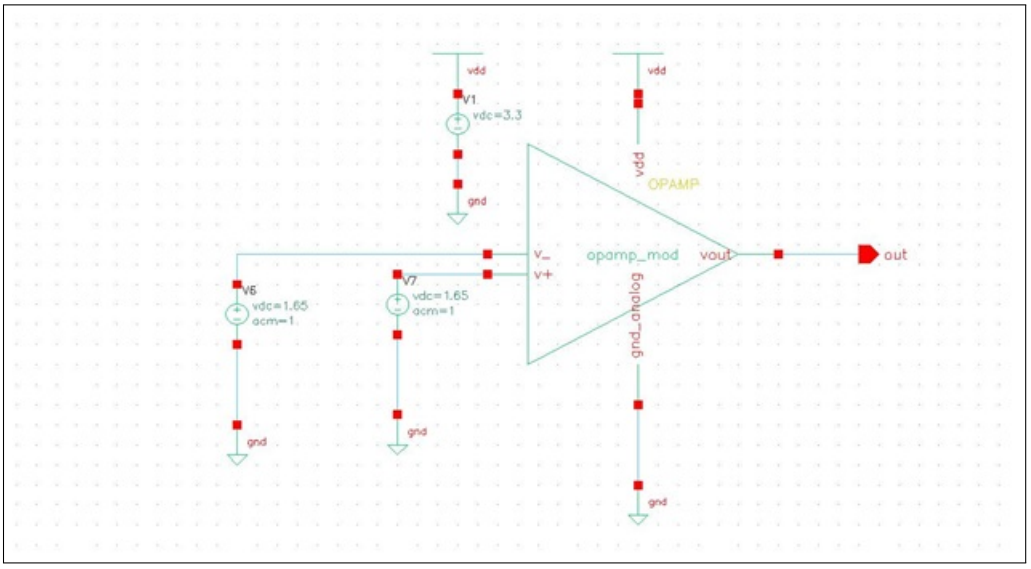


Figure 4.4: Test circuit of transistor level op-amp

## 4.7 Specification of transistor level Op-amp

Table 4.1: specification of transistor level op-amp

| Specification | Result |
|---|---|
| DC_gain | 83.672293 db 15.26214KV |
| GBW | 97.5260 MHz |
| Iin_max | 120 A |
| Slew rate | 240 V/ sec |
| Phase margin | 44.70162 degree |

## 4.8 Simulation result of transistor level op-amp

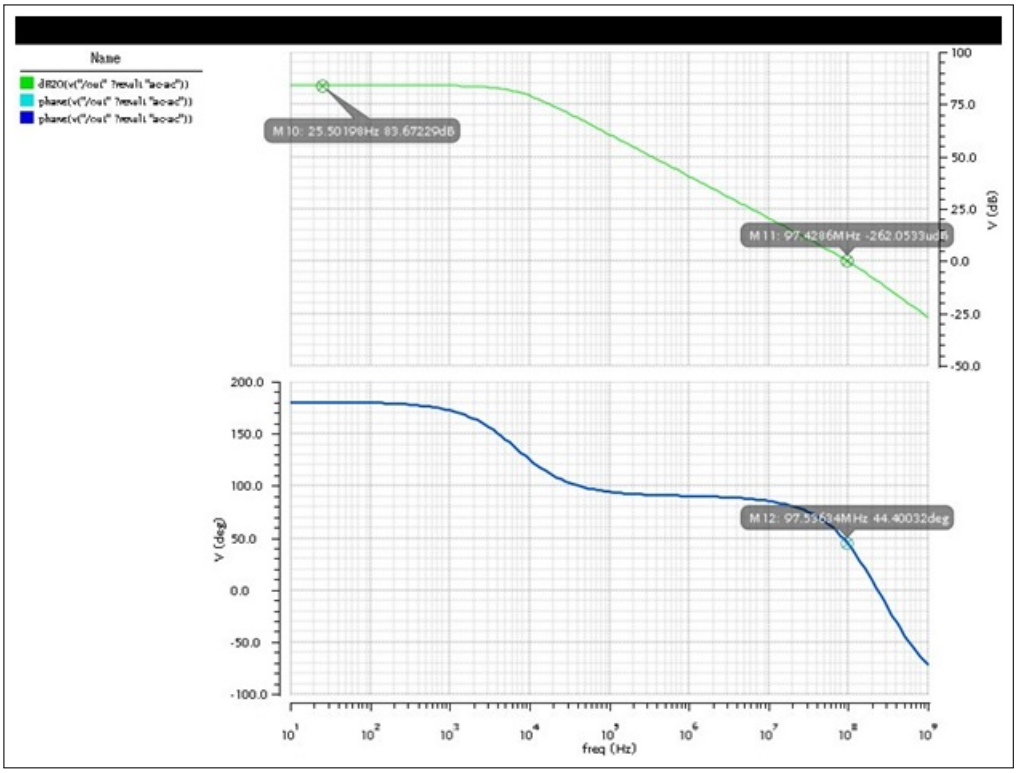


Figure 4.5: simulation result of transistor level op-amp

The result of the simulation of this model shows that the GBW of the op-amp 97.53MHz. And the -3dB bandwidth is about 1MHz. The phase margin of the

op-amp is 44.40.

## 4.9 Macro Model of Op-amp using Verilog-A

The complexity of the op-amp model depends on how to use the characteristics to establish the model [1]. When we design an op-amp with transistors, the power consumption, gain, bandwidth, slew rate are very important parameters that must be concerned. And these parameters will decide whether the op-amp can work properly in the system. Therefore, when we establish a model, these parameters must to be considered carefully. Then we can establish the op-amp frequency characteristic model. Besides the gain, it also contains the op-amp offset voltage and current, bandwidth and slew rate. Unity-gain bandwidth is the frequency when op-amp open-loop gain is equals to 1, shorted by GBW.

$$GBW = \frac{g_m}{2\pi C_1}$$

Which gm is the transconductance of the op-amp and C1 is the capacitance that generated the dominant pole [8]. And slew rate SR stands for the adaptive capacity of op-amp to signal change rate, it unit is V/us

$$SR = |\frac{dV_0}{dt}|max$$

It is common to set the output poles for secondary primary pole. Then the dominant pole will be generated in internal circuit. We can utilize R1 and C1 (Fig.4.6) to establish the dominant pole model in frequency response. If set R1=R0, the model can simulate output resistance like the case that the following figure shows [1]. The output impedance (use R1 to simulate output resistance) is a frequency function in the macro model of Fig.4.6.

If we want the output impedance keep constant, we need to do a further improvement like Fig.4.6. It adds a node and uses an additional controlled source to isolate the

relationship between output impedance and voltage gain frequency response. The additional controlled source will work as a buffer to isolate the op-amp with the following stages. For the reason of the mismatch in the layout and the circuit design the offset effect must be included. So the offset voltage and offset current also be added into the model.

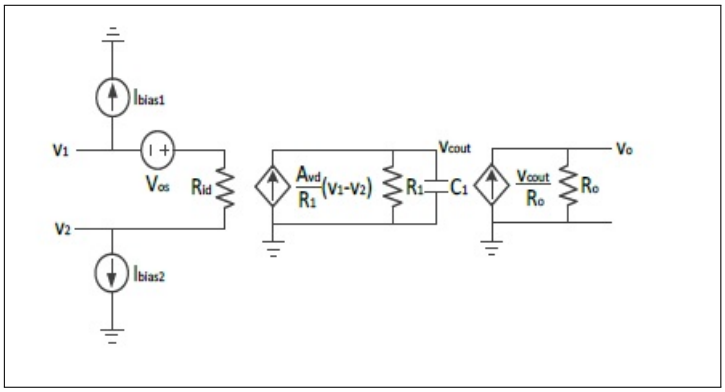


Figure 4.6: Op-amp macromodel with the frequency response

Table 4.2: parameter of macromodeling of op-amp

| **Specification** | **Result** |
|---|---|
| DC_gain | 83.672293 db 15.26214KV |
| GBW | 97.5260 MHz |
| Iin_max | 120 A |
| Slew rate | 240 V/ sec |
| Phase margin | 84.26 degree |
| Input impedence | 1M ohm |
| Output impedence | 100 ohm |

We know that the reasonable value of a CMOS op-amp input resistance is about 1M and the out resistance is 100. The result of the simulation of this model shows that the GBW of the op-amp is nearly 100MHz. And the -3dB bandwidth is about 1MHz. The phase margin of the op-amp is 84.267. This shows that the output pole is the secondary primary pole and the dominant pole is generated in internal circuit.

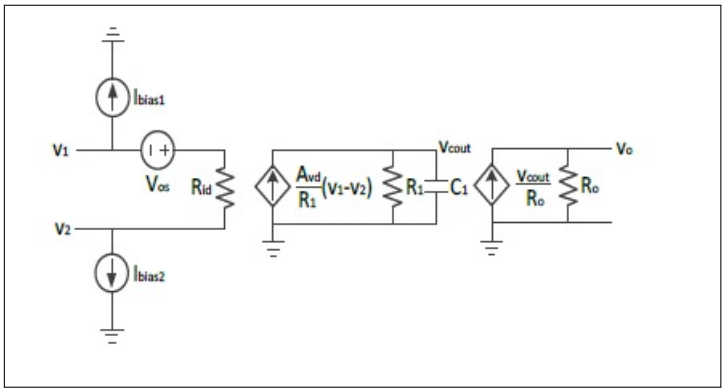


Figure 4.7: Schematic diagram of macromodel Op-amp

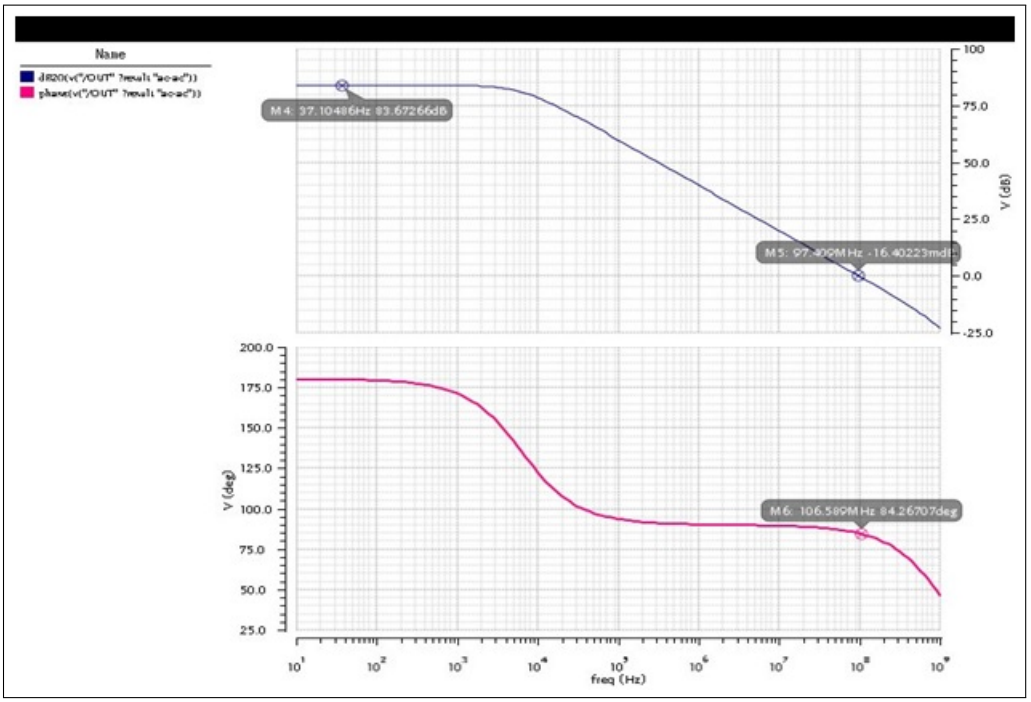


Figure 4.8: op-amp Verilog-A model ac analysis

# Chapter 5

# Implementation of Cyclic ADC

## 5.1 Working of Cyclic ADC

The designed architecture performs one bit conversion in each clock cycle. In one cycle it samples the input, compares the sampled data with reference voltage and produces the residue voltage for next cycle. Residue voltage depends upon the previous bit output. It can be simply described by the equation:

$$Vresidue = 2V_{in}(i) \; - \; bi \; V_{ref} - \; bi \; V_{low}$$

Where, bi is previous bit output. If bi is 1 then Vref is subtracted otherwise Vlow is subtracted. The residue voltage produced acts as the input for the next bit conversion. The complete operation of the design can be described in two stages:

- Sample and hold stage
- Residue generation stage (multiply by 2 and subtraction).

### 5.1.1 Sample and Hold Stage

Figure 5.1 represents the sample and hold circuit used in the design. It consists of capacitor C1, operational amplifier A1 and three switches S0, S1 and S2, where switches control the operation of circuit. The circuit operates in two modes: sample

mode and amplification/hold mode. While switching between the two modes, there should be dead time, in which both modes of operations are OFF, so that the charge leakage does not occur. So, non overlapping clock is used for the operation.

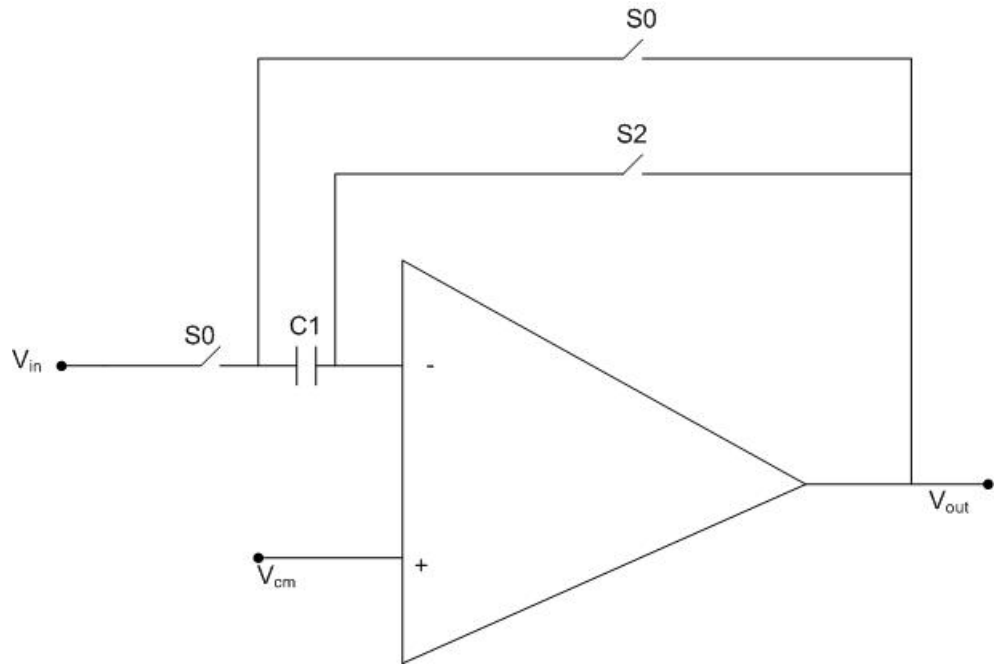


Figure 5.1: sample and hold stage[17]

During first half of clock cycle, the circuit operates in sampling mode. Initially the switch S1 is ON. The amplifier acts as unity gain buffer. This leads to the potential at the inverting node of amplifier equal to VCM. Then, S0 is switched ON which makes the capacitor C1 to track the input voltage. The charge deposited on capacitor C1 during this mode is:

In next half of clock cycle, the circuit is switched into the hold mode by switching S1 to OFF state. During this time, the inverting node of amplifier is in floating condition. Now, S0 is turned OFF. The charge injected by the switch S0 has no effect on the charge hold by capacitor because the left plate of the capacitor is floating. When both the switches are turned off then S2 is turned ON. This makes the circuit to amplifying/hold mode, flipping the capacitor in feedback configuration. The charge on capacitor is given by;

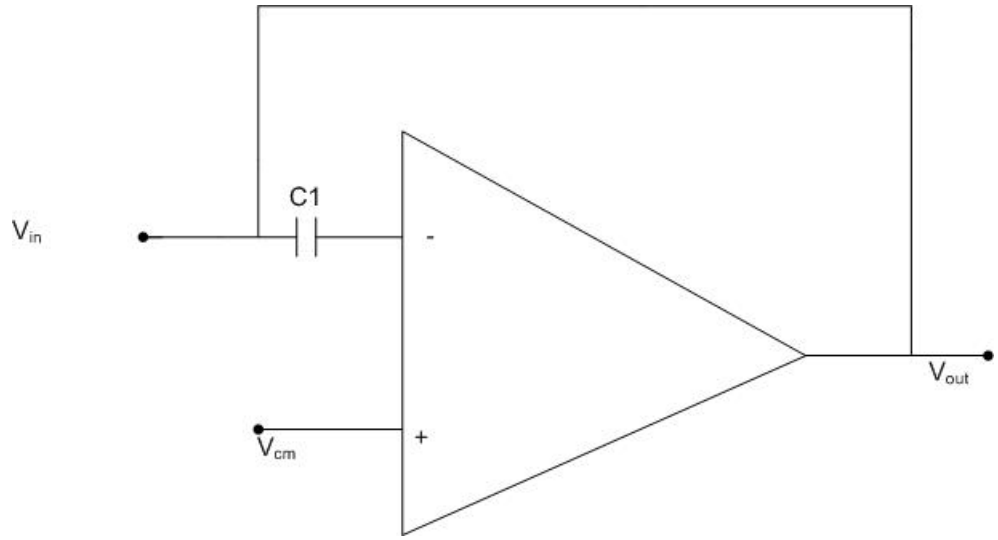


Figure 5.2: sampling mode[17]

$$Q1(hold) = C1\ (V_{out}\ -\ V_{CM})$$

In this mode, the charge remains conserved at the capacitor. By charge conservation,

$$\begin{aligned} \text{Q1 (hold)} &= \text{Q1 (sampled)} \\ C1(V_{out}\ -\ V_{CM}) &= C1\ (V_{in}\ -\ V_{CM}) \\ V_{out}\ &=\ V_{in} \end{aligned}$$

This makes the sampled input voltage to appear at the output.

### 5.1.2 Simulated Output of sample and hold circuit using Verilog-A

In figure below, clock pulse and invertclock_pulse represents the non overlapping clocks with frequency 1 MHz and a duty cycle of 50%. Clock pulse and invertclock_pulse have some delay to avoid overlapping of clocks. Clock pulse is applied to switch S1 and invertclock_pulse is applied to switch S2. Clock pulse with a small delay is applied to switch S0. Output represents the input sampled during first half

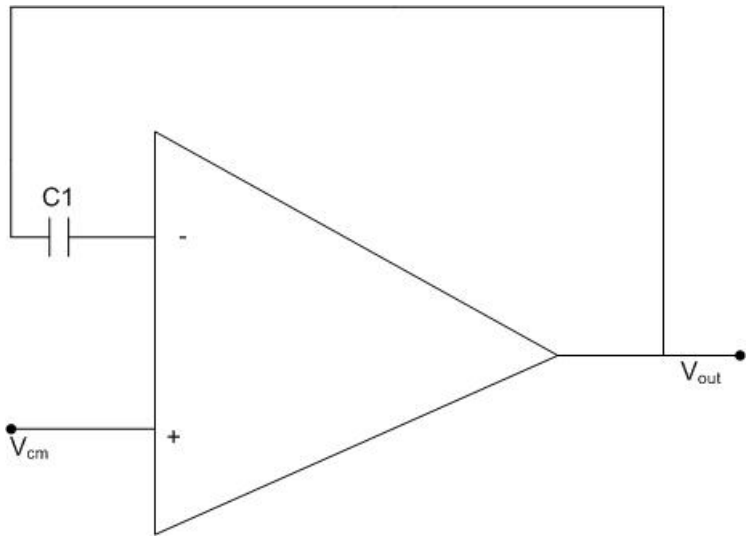


Figure 5.3: amplifying/hold mode[17]

of clock which is 1.64989 V for ideal input of 1 V. In next half of clock, hold output as represented by sample_out is 1.00112V. Similarly, different inputs are sampled in next clock cycles.

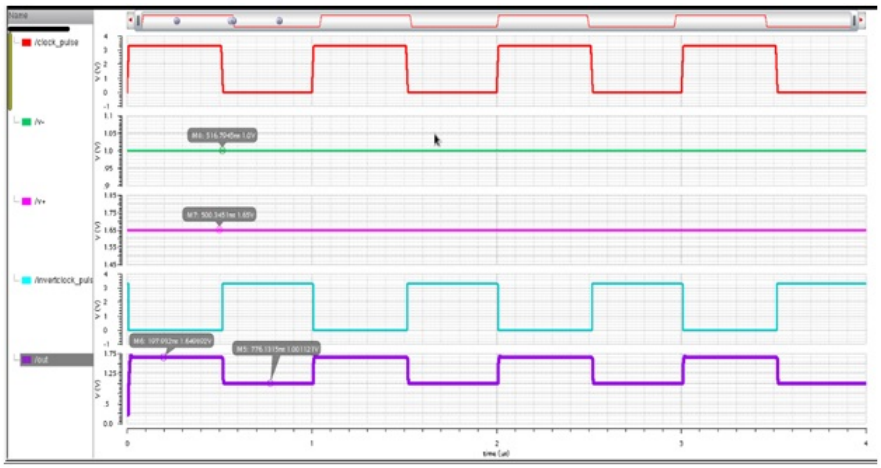

Figure 5.4: simulation result of sample and hold circuit using Verilog-A

In figure below, clock pulse and invertclock_pulse represents the non overlapping clocks with frequency 1 MHz and a duty cycle of 50%. Clock pulse is applied to

switch S1 and invertclock_pulse is applied to switch S2. Clock pulse with a small delay is applied to switch S0. Output represents the input sampled during first half of clock which is 1.6489 V for ideal input of 1 V. In next half of clock, hold output as represented by sample_out is 2.0007V. Similarly, different inputs are sampled in next clock cycles.


Figure 5.5: simulation result of sample and hold circuit using Verilog-A

### 5.1.3 Simulated Output of sample and hold circuit using transistor level op-amp

In figure below, clock pulse and invertclock_pulse represents the non overlapping clocks with frequency 1 MHz and a duty cycle of 50%. Clock pulse and invertclock_pulse have some delay to avoid overlapping of clocks. Clock pulse is applied to switch S1 and invertclock_pulse is applied to switch S2. Clock pulse with a small delay is applied to switch S0. Output represents the input sampled during first half

of clock which is 1.64989 V for ideal input of 2 V. In next half of clock, hold output as represented by sample_out is 2.0008V. Similarly, different inputs are sampled in next clock cycles.

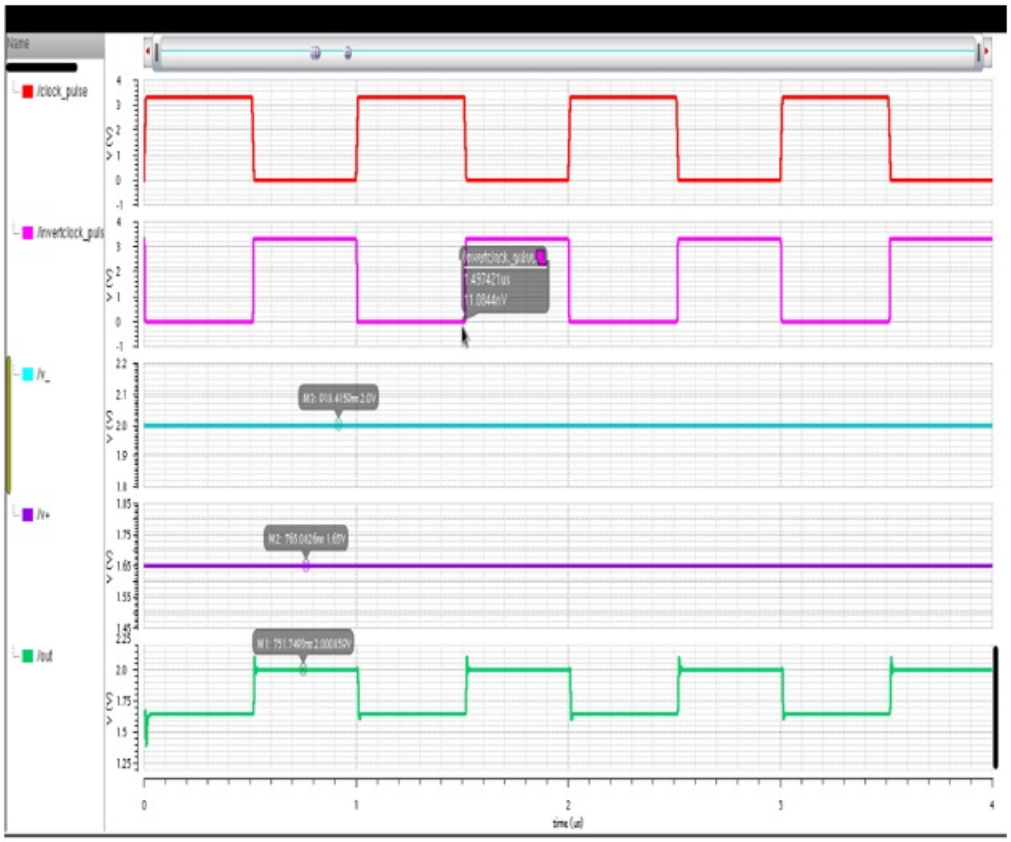


Figure 5.6: simulation result of sample and hold circuit using transistor level Op-amp

In figure below, clock pulse and invertclock_pulse represents the non overlapping clocks with frequency 1 MHz and a duty cycle of 50%. Clock pulse and invertclock_pulse have some delay to avoid overlapping of clocks. Clock pulse is applied to switch S1 and invertclock_pulse is applied to switch S2. Clock pulse with a small delay is applied to switch S0. Output represents the input sampled during first half of clock which is 1.64989 V for ideal input of 1 V. In next half of clock, hold output as represented by sample_out is 1.0010 V. Similarly, different inputs are sampled in next clock cycles

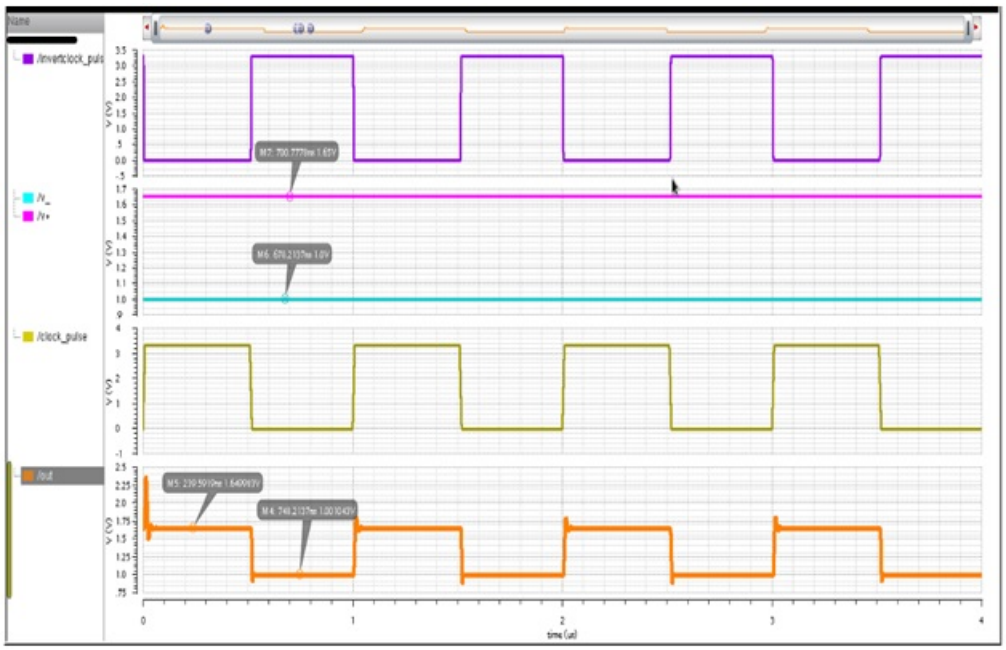

Figure 5.7: result of sample and hold circuit using transistor level Op-amp

Comparison between sample and hold circuit using Verilog-A and transistor level op-amp for the switching capacitance value of 1pF.

Table 5.1: comparison b/w sample hold code and transistor level output when capacitance 1pF

| **Actual input** | **S/H Code output** | **S/H transistor level output** |
|---|---|---|
| 500 mV | 501.163 mV | 501.103 mV |
| 1 V | 1.00106 V | 1.001 V |
| 1.5 V | 1.50087 V | 1.5009 V |
| 1.8 V | 1.8007 V | 1.8009 V |
| 2 V | 2.0006 V | 2.0006 V |
| 2.2 V | 2.2005 V | 2.20015 V |

Now comparing for the switching capacitance value of 800f F.

Finally comparing for the switching capacitance value of 500f F.

Table 5.2: comparison b/w sample hold code and transistor level output when capacitance 800f F

| **Actual input** | **S/H Code output** | **S/H transistor level output** |
|---|---|---|
| 500 mV | 501.429 mV | 501.134 mV |
| 1 V | 1.00126 V | 1.00126 V |
| 1.5 V | 1.50108 V | 1.5012 V |
| 1.8 V | 1.80095 V | 1.8007 V |
| 2 V | 2.0008 V | 2.0010 V |
| 2.2 V | 2.20066 V | 2.2009 V |

Table 5.3: comparison b/w sample hold code and transistor level output when capacitance 500f F

| **Actual input** | **S/H Code output** | **S/H transistor level output** |
|---|---|---|
| 500 mV | 501.172 mV | 501.103 mV |
| 1 V | 1.00193 V | 1.001996 V |
| 1.5 V | 1.501676 V | 1.5019 V |
| 1.8 V | 1.801483 V | 1.8017 V |
| 2 V | 2.00138 V | 2.00171 V |
| 2.2 V | 2.2010 V | 2.2015 V |

### 5.1.4 Residue generation stage

Residue generation circuit consists of multiplier circuit and subtractor circuit. The two operations are performed simultaneously in one clock cycle. The multiplier circuit provides a gain of two. Switches S3, S4, S7, S8 and capacitors C2, C3 makes a multiplier circuit with amplifier. The two capacitors have equal capacitance. This stage also has two modes of operation i.e. sample mode and residue generation mode. During the sample mode (shown in figure 5.6 (a)), amplifier acts as a unity gain buffer. Initially S7 is ON. After a delay, S3 and S4 are switched ON. Input voltage Vin is sampled at C2 and C3. The charge deposited at C2 and C3 is

$$Q2(samplemode) = C2\ (V_{in}\ -\ V_{CM})$$
$$Q3(samplemode) = C3\ (V_{in}\ -\ V_{CM})$$

In the transition to the residue generation mode, S7 turns OFF first. Then, S3 and S4 are turned OFF. The switches S5 and S6 works according to comparator

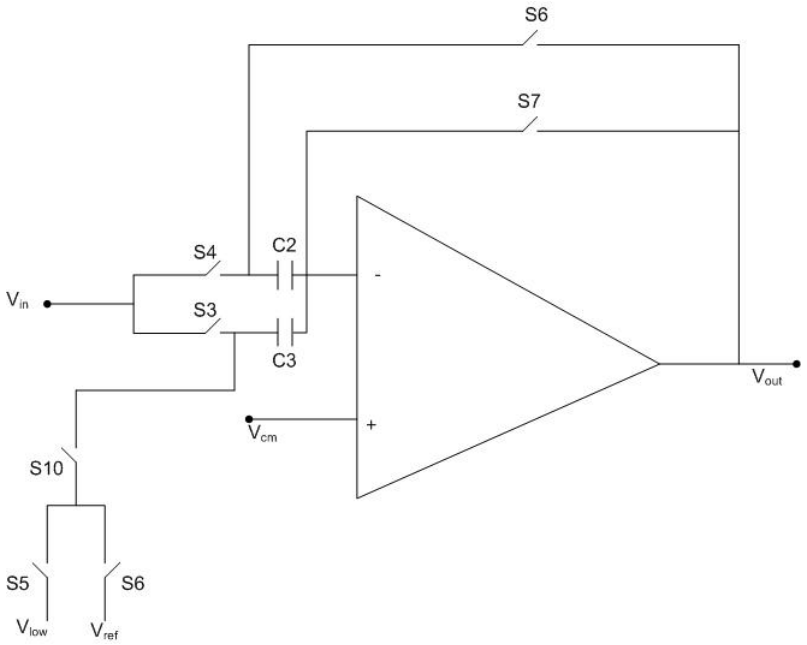


Figure 5.8: residue generation circuit[16]

output. If the output of comparator is 1 then S6 is ON otherwise, S5 is ON. Switch S8 is turned ON which keeps the capacitor C2 in feedback path of the amplifier. When the potential of inverting node of amplifier is stabilized to VCM, then S10 is turned ON. The voltage at left plate of capacitor C3 depends on the switching states of S5 and S6. Lets assume that the output of comparator 1 so switch S5 is ON. During this mode, charge deposited on capacitors can be calculated as;

$$Q2(residuemode) = C2(V_{out} - V_{CM})$$
$$Q3(residuemode) = C3(V_{ref} - V_{CM})$$

By the charge conservation principle, total charge is conserved. So,

$$\text{Q (sample mode)} = \text{Q (residue mode)}$$
$$C2(V_{out} - V_{CM}) + C3(V_{ref} - V_{CM}) = C2(V_{in} - V_{CM}) + C3(V_{in} - V_{CM})$$

In this architecture, capacitors C2 and C3 are equal. So, the above equation for C2 = C3 = C become

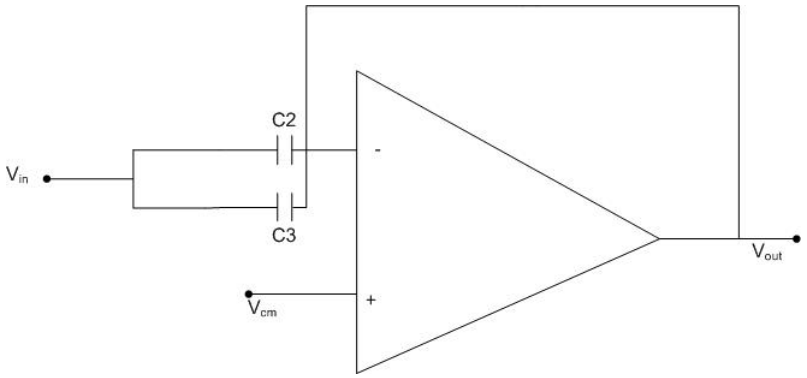


Figure 5.9: Sample mode[16]

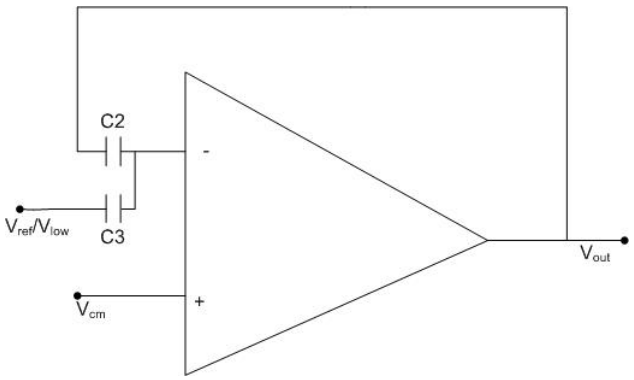


Figure 5.10: multiplication/sub mode[16]

$$V_{out} + V_{ref} \; - \; 2V_{CM} = 2V_{in} \; - \; 2V_{CM}$$
$$V_{out} = 2V_{in} \; - \; V_{ref}$$

Vout represents the residue voltage. The output of sample and hold stage is the input for the residue stage and the output of residue stage is the input for sample and hold stage. During the sample mode of sample and hold circuit, residue circuit operates in residue generation mode. When S/H circuit operates in amplifying mode, residue circuit is in sample mode sampling the output of S/H circuit. In the complete architecture, sample and hold circuit uses two switches to sample the input voltage. One is switch S0, which samples the input Vin . The second switch is S9 which samples the residue voltage at S/H circuit. Initially, S1 is ON for only half clock cycle. Then S9 operates according to requirement for rest of clock cycles

for 10 bit conversions.

### 5.1.5 Simulated Output of circuit using Verilog-A

Figure below represents the input/output waveforms of residue circuit for a voltage Vin = 2 V. A clock of 1MHz is applied to the circuit and period for the waveform is 1sec with pulse width 500nsec . In second half of clock cycle, residue stage is in sample mode. It depends on comparator outputs .if comparator output is 1 then circuit output is 2*Vin  Vref. If comparator output is 0 then circuit output is 2*Vin . In simulation result the comparator output is 1 V. and output of circuit is 1.300907 V.

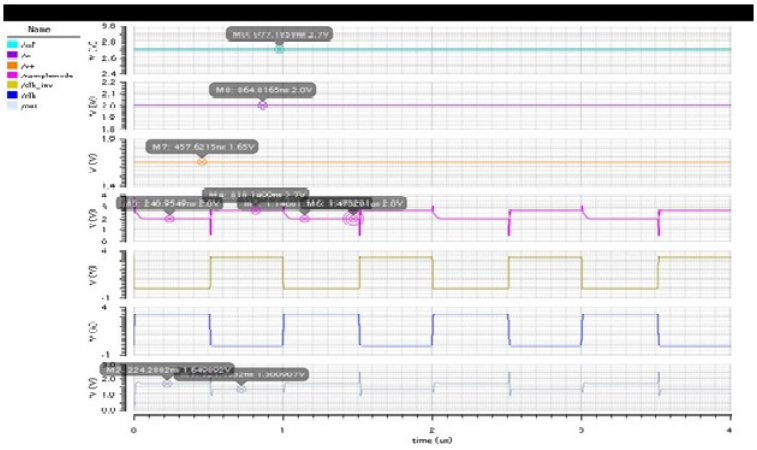

Figure 5.11: simulation result of residue circuit using Verilog-A

Figure below represents the input/output waveforms of residue circuit for a voltage $V_{in} = 1V$ . Here also a clock of 1MHz is applied to the circuit and period for the waveform is 1sec with pulse width 500nsec . In second half of clock cycle, residue stage is in sample mode. In simulation result has comparator output is 0 V. then output of circuit is 2.0009 V.

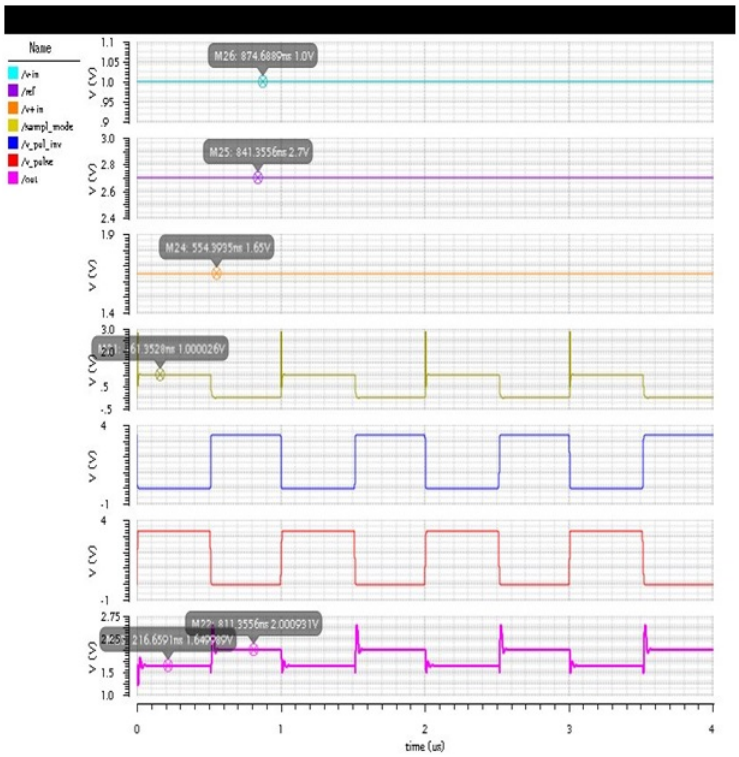


Figure 5.12: simulation result circuit using transistor level op-amp

### 5.1.6 Simulated Output of circuit using transistor level op-amp

Figure below represents the input/output waveforms of residue circuit for a voltage $V_{in} = 2V$. A clock of 1MHz is applied to the circuit and period is 1sec with pulse width 500nsec. In second half of clock cycle, residue stage is in sample mode. It depends on comparator outputs .if comparator output is 1 then circuit output is $2 * V_{in} - V_{ref}$. If comparator output is 0 then circuit output is $2 * V_{in}$. In simulation result has comparator output is 1 V. then output of circuit is 1.300907 V.

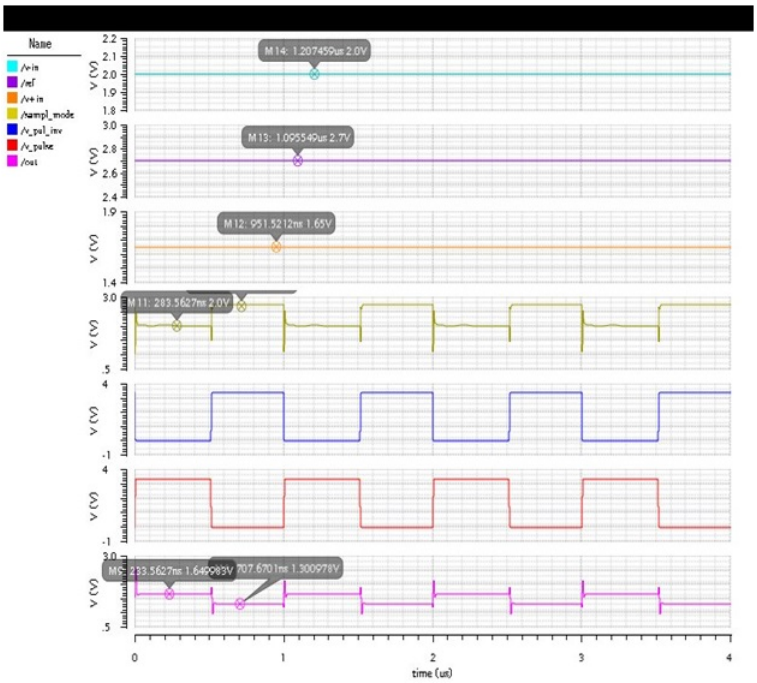


Figure 5.13: simulation result circuit using Verilog-A

Figure below represents the input- output waveforms of residue circuit for a voltage Vin = 1 V. A clock of 1MHz is applied to the circuit and period is 1sec with pulse width 500nsec . In second half of clock cycle, residue stage is in sample mode. In simulation result has comparator output is 0 V. then output of circuit is 2.0009 V.

Case a: when comparator output is 1, the output of residue circuit is $2 * V_{in}$ $-$ $-$ $V_{ref}$. Table below show the comparison of residue code and residue circuit output. Here it is less than 1mV.

Table 5.4: comparison b/w residue code & residue circuit output

| **Comparator O/P** | **Actual I/P** | **residue code O/P** | **residue transistor level O/P** |
|---|---|---|---|
| 1 | 2.2 | 1.700708 V | 1.700855 V |
| 1 | 2.0 | 1.300905 V | 1.300979 V |
| 1 | 1.8 | 901.0466 mV | 901.047 mV |
| 1 | 1.5 | 301.2095 mV | 301.2145 mV |

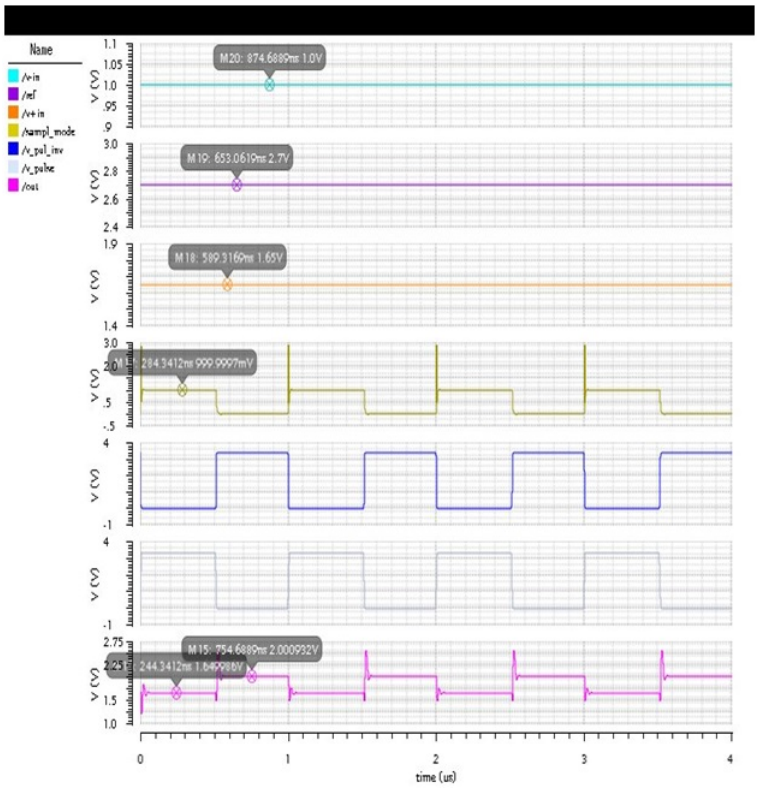


Figure 5.14: simulation result circuit using transistor level op-amp

Case b: when comparator output is 0. The output of residue circuit is$2 * V_{in}$ Table show the comparison of residue code and residue circuit output. Here it is less than 1mV.

Table 5.5: comparison b/w residue code & residue circuit output

| **Comparator O/P** | **Actual I/P** | **residue code O/P** | **residue transistor level O/P** |
|---|---|---|---|
| 0 | 1 V | 2.0007 V | 2.0009 V |
| 0 | 900 mV | 1.800849 V | 1.800982 V |
| 0 | 500 mV | 1.001115 V | 1.001147 V |
| 0 | 400 mV | 801.2178 mV | 801.1846 mV |

### 5.1.7 D Flip flop using Verilog - A

D flip flop is a binary cell capable of storing one bit information. It is triggered by a clock pulse +H triggering and H triggering. D flip flop has two outputs Q and Q_bar .Q is normal o/p and Q_bar is complementary of normal output under normal operating condition. D flip flop has two inputs one input is D_in and another is clock. In a D flip-flop, the data on the d_in input are transferred to the Q output on the positive- or negative-going transition of the clock signal, depending upon the flip-flop, and this logic state is held at the output until we get the next effective clock transition .

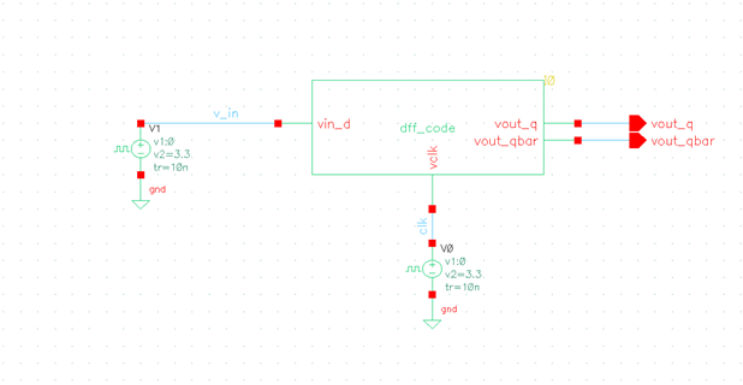


Figure 5.15: D flip flop Schematic Diagram

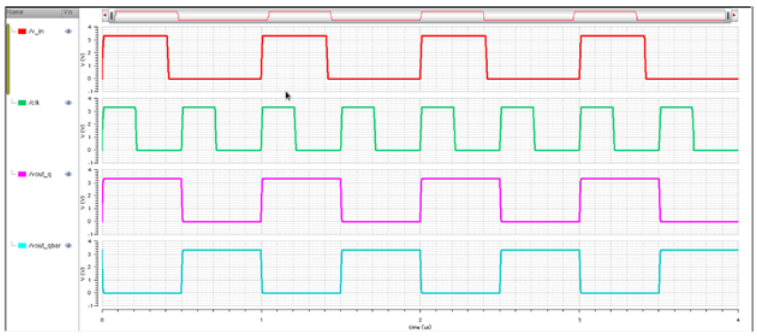

Figure 5.16: D flip flop Results

Figure above represents the input- output waveforms of D flip flop for a input voltage V_in where in the period for the waveform is 1us and pulse width is 400ns.

The period of clk is 1us and pulse width is 500ns. Since Vout_q depends on +H triggering of clk so, the Vout_q is following v_in as per the current condition met at the +H triggering of the clock.

### 5.1.8 Shift resister

Resister is a group of flip flops .A resister containing n flip flops such a resister (n bit resister ) is capable of storing n bits of information. resister are essentially synchronous system where all the flip flop are triggered by a common clock pulse .feeding of new data in a resister is known as loading in resister . Register that is used to store binary information is known as a memory register .A register that is capable of shifting binary information either to the right or to the left is called a shift register. It permits the stored data to move from a particular location to some another location within the register .In shift register ,the flip flops are connected in such a way that the bits of a binary number are entered into the shift register ,shifted from one position to another and finally shifted out. It is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name "shift register". Registers can be designed using discrete filp-flops (S-R, J-K and D type).An n-bit register consists of n flip-flops and the required gates to control the shift operation. There are two methods of shifting the data serial shifting and parallel shifting. The serial shifting method shifts one bit at a time for each clock pulse in a serial fashion, beginning either MSB or the LSB.As a example, a 10-bit register requires ten clock pulses to shift a bit from the input to the output. In a parallel shifting operation, all the data get shifted simultaneously during a single clock pulse. So it is faster than the serial shifting method[18] .It basically consists of several single bits D flip flop , one for each bit connected together in a serial or daisy-chain arrangement so that the output from one Flip Flop becomes the input of the next flip-flop and so on. Generally, shift registers operate in one of four different

modes:

- Serial-in-Parallel-out Register (SIPO)
- Serial-in-Serial-out Register (SISO)
- Parallel-in-Serial-out Register (PISO)
- Parallel-in-Parallel-out Register (PIPO)

**10-bit shift register using Verilog - A**

The shift resister is combination of D- flip flops. 10 bit shift register need 10 D flip flops which are connect together in a cascade. D- flip flop has clk ,Vin ,out_q. The output of 1st D- flip flop is connected to 2nd D- flip flop input. This type of shift resister is called serial in parallel out shift register. As discussed earlier about D- flip flops, 10 separate clocks have given for circuit. Each clock has 1us period and 500ns pulse width. Vin_d is input of first d-flip flop which follow clocks and it gives out1. Out1 is connected to input of $2^{nd}$ D- flip flop. At Every +H triggering the data is shifted by one clock. Inputs and outputs are represented in table of 10 bit shift resister represented below

### 5.1.9 Comparator

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. In the analog to digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. It can be divided into open-loop and regenerative comparators. The open loop is basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers and or flip-flops, to accomplish the comparison of the magnitude between two signals.

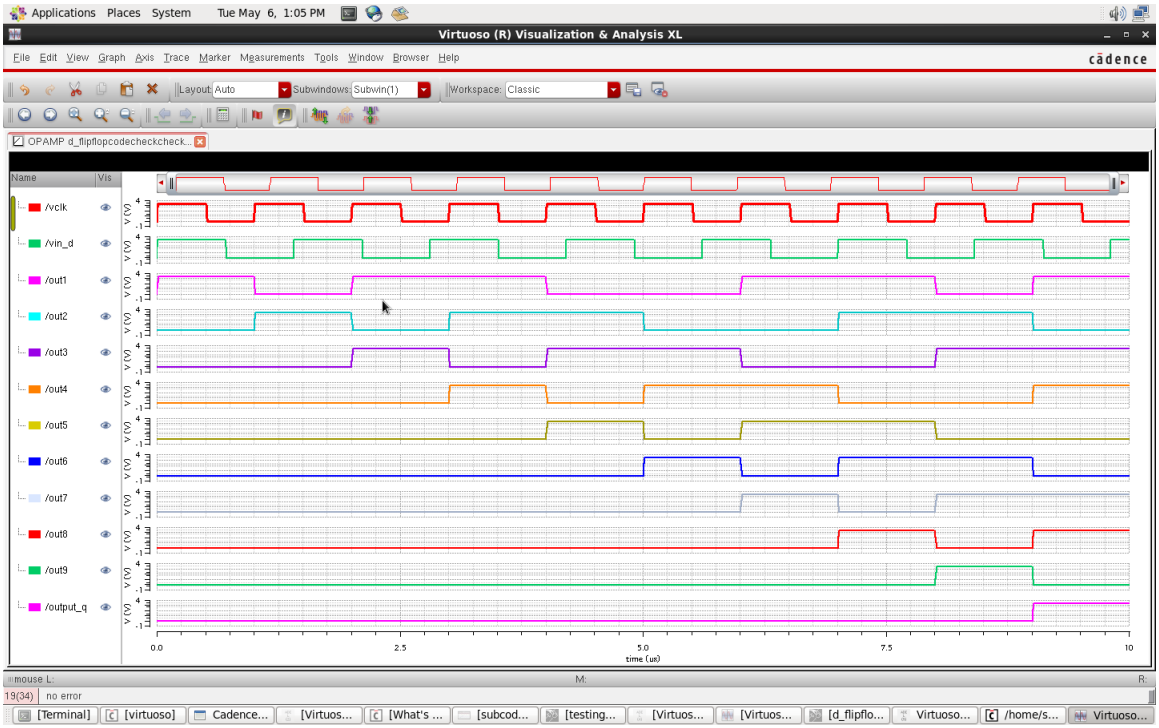


Figure 5.17: 10 bit shift resister using verilog–A

### Characterization of a Comparator

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals VP and VN and one binary digital output Vo. The output of the comparator is high ($V_{OH}$) when the difference between the non-inverting and the inverting inputs is positive [6]. The output is low ($V_{OL}$) when the difference is negative, which is shown in figure below. This symbol is identical to that for an operational amplifier, because a comparator has many of the characteristics as a high gain amplifies. Figure shows reference voltage as $V_{ref}$ equal to 1.65 V. The input voltage is $V_{in}$ having period of 1us and pulse width of 500ns. As per coding if Vin voltage is greater than $V_{ref}$ voltage then output is $V_{OH}$ (here 3.3 V) else output is $V_{OL}$ (here 0V). So, for test signal input voltage is maximum 2 V for the first 500ns and minimum of 0V for the next 500 ns therefore $V_{OH}$ is made available as per the output in the first 500

ns and for next 500ns, output is $V_{OL}$.

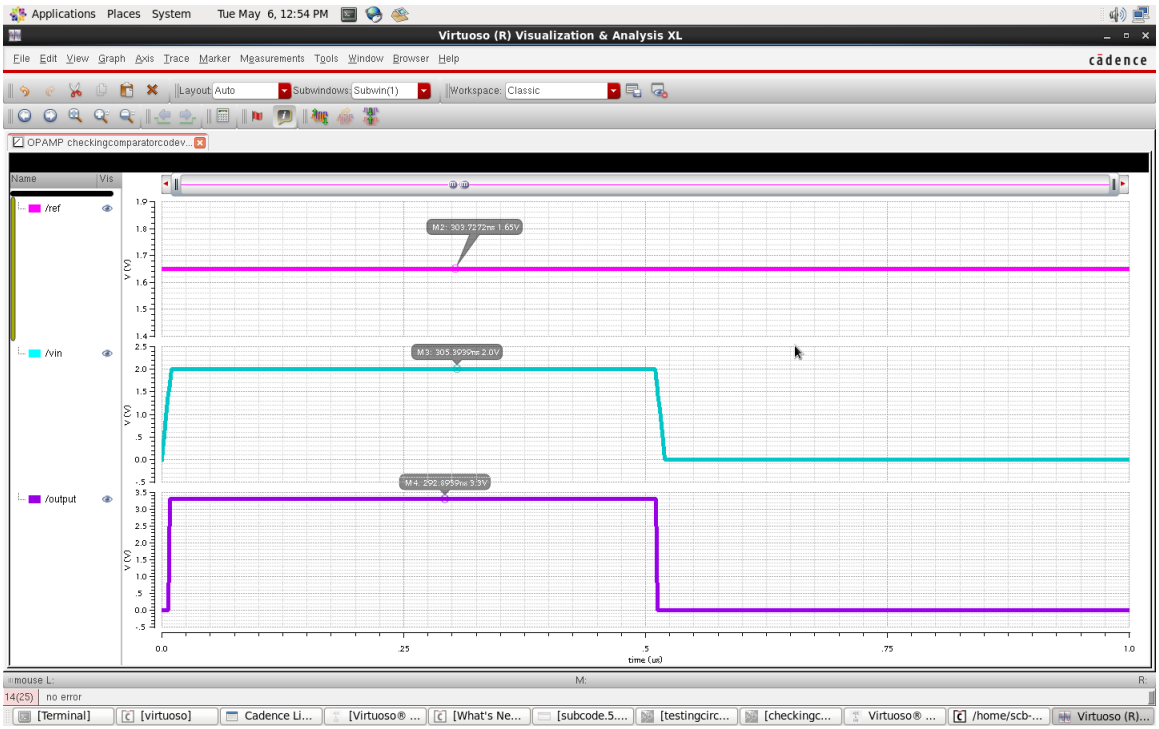


Figure 5.18: result of comparator

In figure $V_{ref}$ shows reference voltage .in this case we have given ref voltage equal to 1.65 V .Vin shows the input voltage . it has dc voltage of 1.65 V, amplitude 1 V , frequency 1M Hz .in our coding if Vin voltage is greater than $V_{ref}$ voltage then output is $V_{OH}$ means 3.3 V and again if Vin voltage is less than $V_{ref}$ voltage the output is $V_{OL}$ .in this case for a period of 500ns our input is greater than 1.65 V so for the first 500ns output is $V_{OH}$ . for another 500ns output is $V_{OL}$ means 0 V.

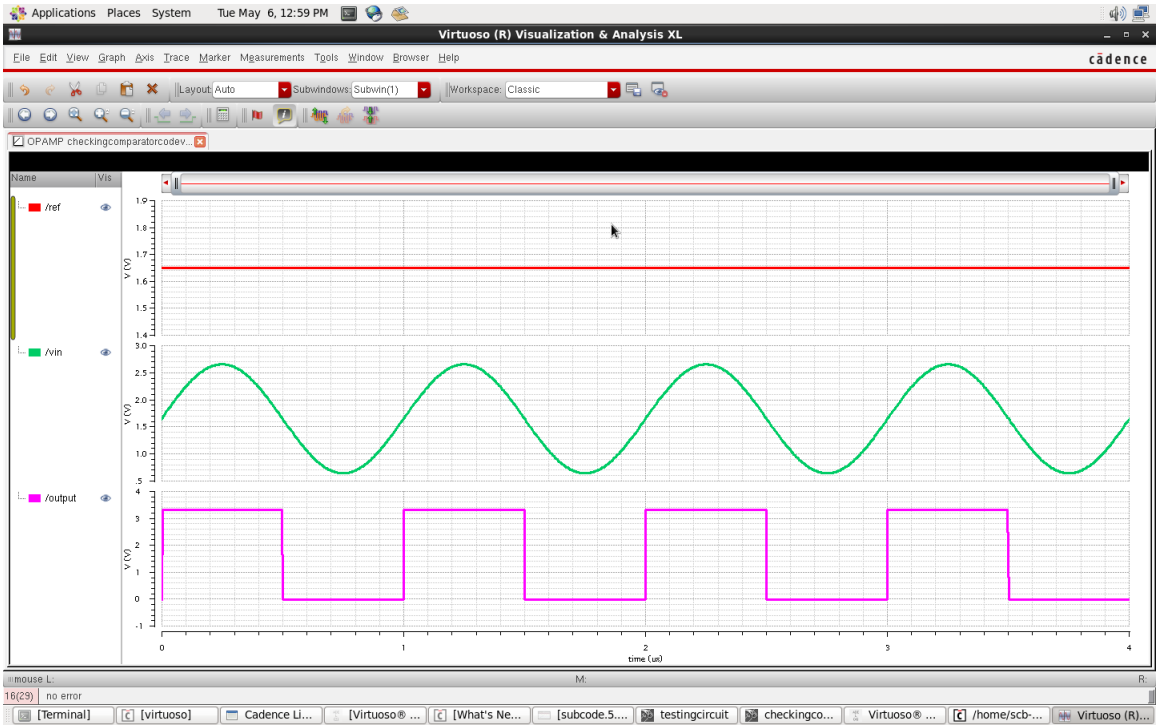


Figure 5.19: result of comparator

# Conclusion

### Conclusion

MEMS based Piezoresistive accelerometer has been studied. Interfacing circuit for the same requires an ADC.Verilog-A description of various components (Sample and hold, subtractar/multiplier, comparator, shift resister) was defined, simulation of which was found to be in accordance with the schematic design of these circuits.10- bit shift register designed has very fast simulation time as compare to the traditional circuit.

### Future Work

Verilog-A description of the 10 bit cyclic adc and comparing its result with the schematic for the same. The work would be to ensure that both the simulation results are matched.

# Bibliography

[1] Robert M. Panas, Michael A. Cullinan, and Martin L. A SYSTEMS APPROACH TO MODELING PIEZORESISTIVE MEMS SENSORS,Culpepper Department of Mechanical Engineering Massachusetts Institute of Technology Cambridge, Massachusetts.

[2] Robert M. Panas, Michael A. Cullinan, Martin L. Design of piezoresistive-based MEMS sensor systems for precision Microsystems,Culpepper Massachusetts Institute of Technology, Department of Mechanical Engineering, Cambridge, MA 02139, United States.

[3] Simone Dalola, Vittorio Ferrari and Daniele Marioli Micromachined piezoresistive inclinometer with oscillator-based integrated interface circuit and temperature readout, Measurement Science and Technology vol. 23 issue 3, 2012.

[4] Tyler Lane Waterfall, Design of Piezoresistive Mems Force and Displacement Sensors thesis, Brigham Young University, 2006.

[5] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 2nd ed. Piscataway, New Jersey: John Wiley & Sons, 2008

[6] Allen, P. E., & Holberg, D. R. (2002), CMOS Analog Circuit Design, New York: Oxford University Press.

[7] D. A. Johns and K. Martin, Analog Integrated Circuit Design, 1st ed. Toronto, Canada: John Wiley and Sons, Inc., 1996

[8] B. Razavi, Principles of Data Conversion System Design, 1st ed. New York, United States: Wiley, 1995

[9] Kenneth S. Kundert, OLAF ZINKE. The Designers Guide to Verilog-AMS. Boston, Kluwer Academic Publishers. 2004

[10] Peng Gang, Behavioral modeling and simulation of analog/mixed-signal systems using Verilog-AMS, Information, Computing and Telecommunication, IEEE Youth Conference, pp. 383-386, 2009

[11] Virtuoso AMS Designer Simulator User Guide,Version 5.7, Cadence Design Systems, Inc.2006

[12] Erik Lauwers, Koen Lampaert*, Paolo Miliozzi*, Georges Gielen, High-level design case of a switched-capacitor low-pass filter using Verilog-A 0-7695-0893-6/0$01 0.00 0 2000 IEEE.

[13] http://www.ovi.org

[14] R.H. McCharles, V.A. Saletore, W.C. Black, D.A. Hodges, An Algorithmic Analog-to-Digital Converter, IEEE ISSCC, Section IX, 1977,pp. 96-97.

[15] P. W. Li , M. J. Chin , P. R. Gray and R. Castello "A ratio-independent algorithmic analog-to-digital conversion technique", IEEE J. Solid-State Circuits, vol. SC-19, pp.828 -836 1984

[16] B. Razavi, Principles of Data Conversion System Design, 1st ed. New York, United States: Wiley, 1995.

[17] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill.

[18] Digital Electronics: Principles, Devices and Applications Anil K. Maini 2007 John Wiley & Sons, Ltd. ISBN: 978-0-470-03214-5.