Design and Simulation of Low Power Low Noise Analog Front End for Digital Hearing Aid

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI DESIGN)

By

Dipesh J Panchal

(11MECV51)

Electronics & Communication Engineering Branch

Department Of Electrical Engineering

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Nirma University, Ahmedabad-382481

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Under the Guidance of

Dr.Amisha Naik

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Certificate

This is to certify that the Major Project entitled "*Design and Simulation of Low Power Low Noise Analog Front End for Digital Hearing Aid*"submitted by *Dipesh J Panchal* (*11MECV51*), towards the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering Branch of Institute of Technology, Nirma University, Ahmedabad is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of my knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

Guide

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- Dipesh J Panchal

11MECV51

Abstract

About 74% of power is consumed by analog front end of digital hearing aid system. Among them 34% power is consume by preamplifier and remaining by Analog to digital converter. Also noise limits the signal level and reduce the dynamic range.So,it is necessary to design low power low noise biomedical systems.To increase battery life,a low power dissipation method is very crucial.

As a preamplifier design, two stage miller compensated operational amplifier is used in sub threshold region for low power dissipation. The graphical method gm/ID Vs ID/W/L is apply for Aspect ratio calculation of MOS transistor. A low noise performance is achieved by selecting PMOS transistor as an input pair in differential amplifier. The gain is changed by selecting different value of input capacitor. The large value of feedback resistor for lower cutoff frequency is designed in weak inversion region.The simulated total power dissipation is 2.15uw, open loop gain is 84dB, phase margin is 71 °, slew rate is 50kv/sec input referred noise is $\frac{3.2uV}{\sqrt{HZ}}$, input common mode range is 0 to 1.7V. the common mode rejection ratio is 98dB and Power supply rejection ratio is 112dB(+) and 87dB(-).The gain is changed from 10dB to 32dB by selecting value of input capacitors. The supply voltage is 1.8V supply with TSMC 0.18um process in mentor graphics.

A first order sigma delta modulator is designed with oversampling ratio of 128, sampling frequency is 256KHz and input signal frequency 1KHz. The power dissipation for first order is 7uw with SNR value 43dB.The total power dissipation is 9uW for preamplifier and sigma delta modulator.

Abbreviation Notation and Nomenclature

TSMC ..... Taiwan Semiconductor Manufacturing Company
MOST ..... Metal Oxide Field Effect Transistor
ADC ..... Analog to Digital Converter
DAC ..... Digital to Analog Converter
CIC ..... Completely in the Canal
ITC ..... In the Canal
BTE ..... Behind The Ear
BAHA ..... Bone Anchored Hearing Aid
OSR ..... Oversampling Ratio
DR ..... Dynamic Range
ENOB ..... Effective number of bits

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Chapter 1

Introduction

From total world population, about 10-12 % of the residents suffering from hearing loss, however only a very small percentage (1-2 %) of this class actually uses a hearing aid. There are following factors affecting for use of hearing aid.[1]

First,
(i) There is the disgrace associated with wearing a hearing Aid.
(ii) A customer disappointment with the devices not meeting their requirements (like low battery life, noise level).
(iii) A high cost of hearing aid.

A main source for hearing aid is listening a music with loud sound, residential near airport, or loud machinery noise in working environment. A hearing aid is a device which is useful for hearing impaired person. The function of a hearing aid is to amplify the sounds to increase hearing range. With advancement in science and technology, people start to use various types of methods to increase the sound to help hearing impaired person. It include analog and digital hearing aid. A most of hearing aids are available in market today are digital hearing aid with use of digital signal processing. So echo and noise cancellation performance is improved.

1.1 Block Diagram

As Shown in Figure.1.1,The Microphone signal is connected with first stage of amplification called preamplifier that enhance the signal strength. The output of preamplifier

is apply to analog to digital converter(ADC) where digital form of signal is obtain with higher value of Signal to Noise Ratio (SNR). [2] A different noise removal algorithms

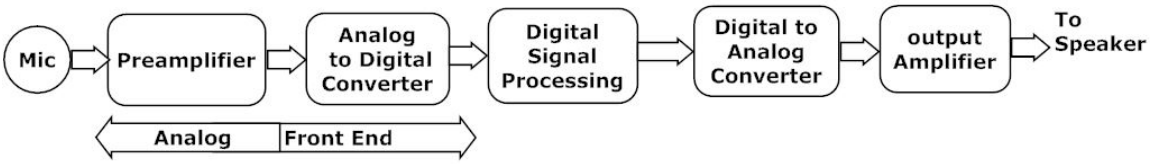

Figure 1.1: Block Diagram of Hearing Aid

are used in Digital Signal Processing and finally output is connected with speaker via Digital to Analog Converter (DAC). The received signal strength is very weak so it is necessary to design high performance analog front end (preamplifier and analog to digital converter) for digital hearing aid.

A Pre amplifier act as an important component of analog front end in hearing aid whose main function is to amplify the sound signal received from microphone, to a certain level so that it can be processed by the digital sound processing. It is a variable gain amplifier which amplifies or attenuates the microphone signal only in the specified frequency range i.e. from 20 Hz to 20 KHz. The primary requirements of the analog front end are:

(i) low input referred noise.
(ii) variable gain for a high dynamic range (more than 100 dB).
(iii) high signal to noise and distortion ratio.
(iv) low power consumption in all part of analog front end to increase battery life.

1.2 Hearing Loss Statistics

A statistics given by Design Service for the Deaf and Hard of Hearing Community that about 278 million people found with moderate to profound hearing loss in united state of America. Among them, 80 % cases found in low-and middle-income countries. Also, about 36 million American (1 out of 10) report some degree of hearing loss.[3]

These include:

(1)18 % of American (45-64 years old)
(2)30 % of adults (65-74 years old)
(3)47 % of adults (75 years old or older).

In India, we have a substantial number of hearing impaired persons especially in rural sector. It is estimated that as many as 50 % of inner city children under the age of seven may have transient hearing loss of up to 10 %.[4]

Figure.1.2 shows a Hearing Loss with increasing an age. It decrease the normal functionality of ear. A Hearing loss may also occur due to birth defects or it may occur due to accident. It shows that hearing loss is more in an age from 25-44. Figure1.3

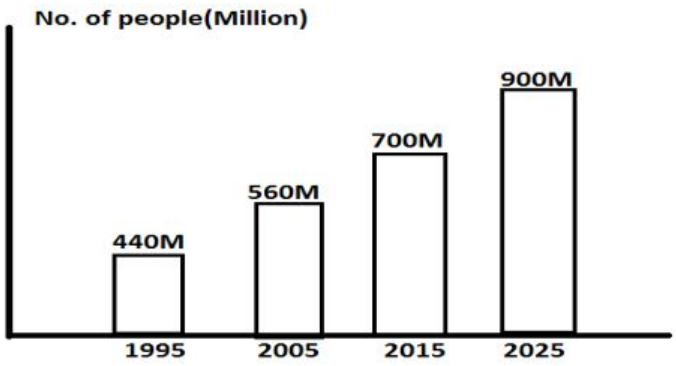

Figure 1.2: Hearing Loss with age

shows increasing rate of hearing loss in number of people with increasing time. It is estimated that up to year 2015 more than 700 million people will suffer by hearing loss. As shown in figure, there is linear increase in hearing loss because of public work place, listening of loud music etc.

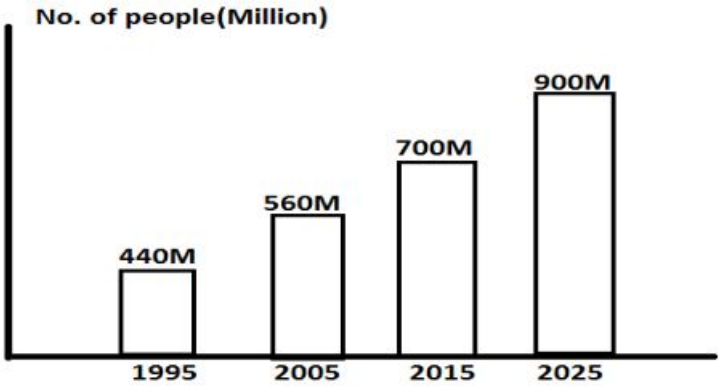

Figure 1.3: Increase In Rate of Hearing Loss

1.3 Motivation

Hearing loss is a third major public health after arthritis and heart disease. At present about 10-12 % of the human population suffers from hearing problems, from which a few percent actually use hearing device. More and more population around the world undergo from hearing losses. Since battery power is used for most of biomedical devices is very less. A battery used in device is zinc air and it has life of at least two weeks at 10Hr use per day. A low voltage is one of the solution but the accuracy and dynamic range of analog front end is reduced. Also battery operated devices are in small in size, less weight and longer life. At same time, external noise reduce the dynamic range of hearing impaired person. So it is necessary to design low power and low noise analog front end for digital hearing aid.

1.4 Objective

The main objective is to design low power low noise variable gain preamplifier and analog to digital converter for hearing aid device to meet different design constraints.

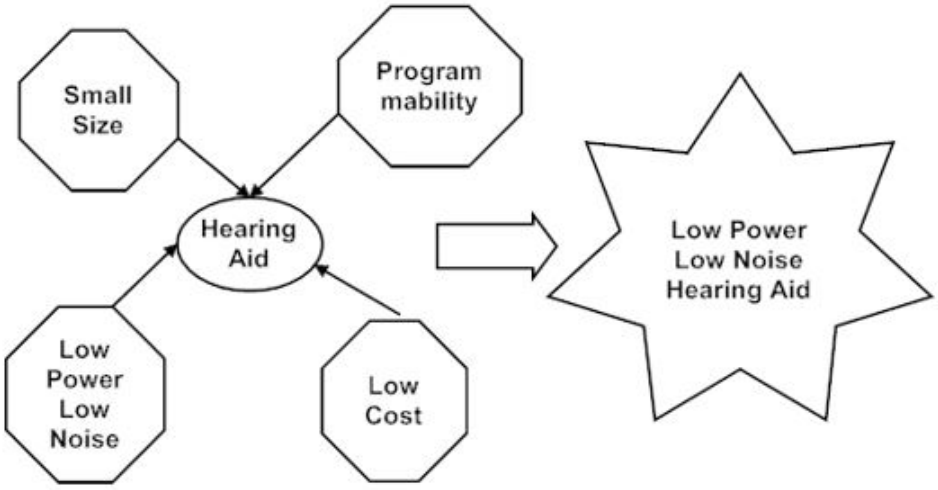

Figure 1.4: Hearing Aid Design Constraint

1.5 Thesis Organization

Chapter 1, *Introduction*, gives the brief idea about what is Hearing aid Technology, flow of system and Block Diagram and Design Constrain, Also includes Hearing Aid Statistics and Components.

Chapter 2, *Literature Survey*, describes about the different types of methods and architecture used for low power and moderate gain conversion, types of hearing aid technology, parameter for preamplifier and analog to digital converter.

Chapter 3, *Design of preamplifier*,Design and simulation of preamplifier, describe the design of operational amplifier for low power low noise.

Chapter 4, *Design and simulation of sigma delta Modulator* describe design and simulation of sigma delta modulator for oversampling and noise feature.

Chapter 5, *Gives concluding remarks and future scope*

Chapter 2

Literature Survey

In this chapter, different types of hearing loss and hearing aid are discussed. Also function of analog front end block as a preamplifier and analog to digital converter are discussed with comparison of available methods.

2.1 Psychology of Ear

The working mechanism of human ear is like the working principle of hearing aid. So it is interesting to know how the human ear works. The human ear is a very complex organ. It has three main part as shown in Figure2.1. [5]

(i) Outer ear
(ii) Middle ear and
(iii) Inner ear.

The function of an outer ear is to receive the sound signal available in an air and directs it towards the middle ear. Normally this function in hearing aid is performed by directional microphones. The middle ear performs three basic functions.

(i) It acts as an impedance matching network
(ii) It acts as an amplifier
(iii) It splits the signal into different frequencies.

A hearing aid device use some kind of impendence matching network, it also con-

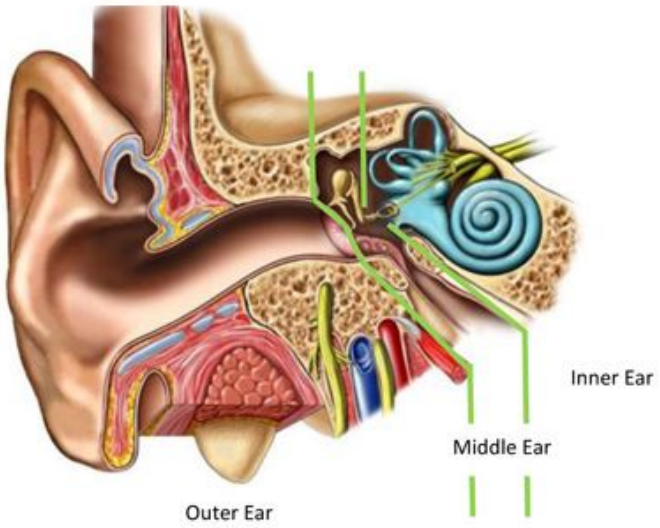

Figure 2.1: Psychology of Ear [6]

tains preamplifier, post amplifier stages, and signal processing techniques, so different frequency bands could be modified according to the hearing impaired person. The third part of ear named inner ear works like a spectrum analyser. It encodes the signal at different frequencies, makes different nerve cells resonate and transmit short pulses to the brain. In hearing aids after analysing different frequencies, it is process by digital signal processor and apply to a digital to analog converter and send to output amplifier and finally to speaker.

2.2 Types of Hearing Losses

Normally the patient can suffer from three types of hearing losses.[7]
(i) Sensory Neural Loss
(ii) Conductive Loss
(iii) Mixed Hearing Loss.

2.2.1 Sensory Neural Loss

A patient having this type of hearing loss have some kind of damage to the auditory nerve system. In this situation, some of the auditory nerves do not properly resonate with their desired frequencies and are not able to send short pulses to the brain. Sensory neural loss could be resolved by using hearing aids, which amplifies sound

signals and stimulate the nerve cells directly. Then Nerve cells convert it into pulses which are then decoded by the brain system.

2.2.2 Conductive Loss

In conductive hearing loss, the middle ear is damaged and one does not possible to get sound signals properly. The conductive loss is resolve by hearing aid if middle ear is not totally damaged. In this case amplification of signal is done by hearing aid device in require band of frequency. Although all types of hearing loss are not corrected by hearing aid.

2.2.3 Mixed Hearing Loss

This type of hearing loss is combination of both conductive and sensory neural loss and is called mixed hearing loss. The conductive loss is because of damage to middle ear while damage in nerve system causes sensory neural loss. A few percentage of population also suffering from mixed hearing loss.

2.3 Types of Hearing Aid

A hearing aid is an electronic device which is operated on external battery source. It amplifies sound signal and improved communication between two persons. The classification of hearing aid is as follow:

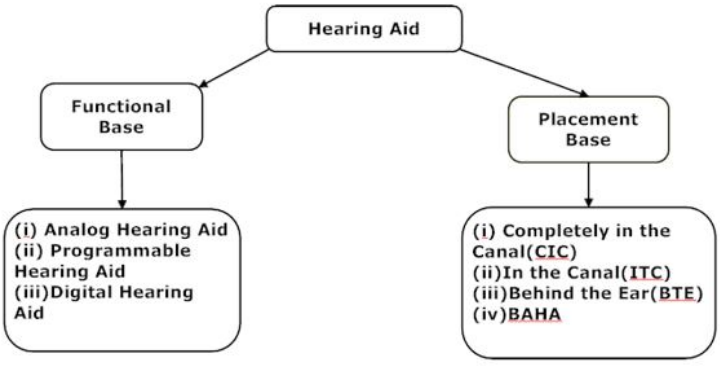

Figure 2.2: Types of Hearing Aid

2.3.1 Analog Hearing Aids

In this type of hearing aid, all components are in analog in nature as shown in Figure 2.3 An input to the system is analog signal from microphone which process by analog system and output is also in analog in nature. The amplifier gain is adjusted by patients need. This type of hearing aid operated on Zinc-Air battery. There are following limitations of analog hearing aid: [8]

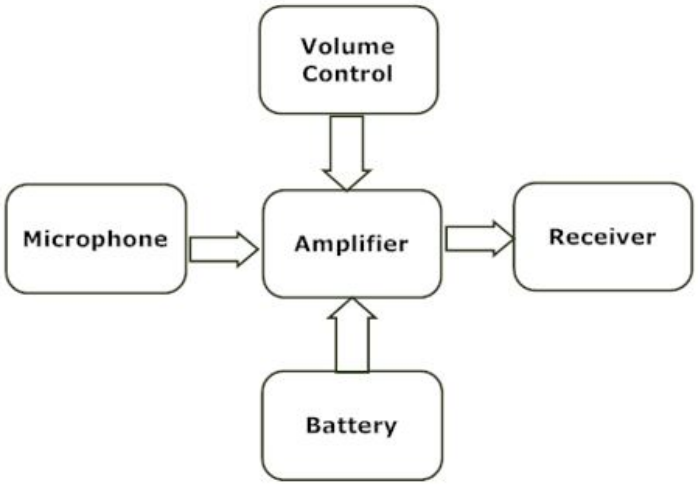

Figure 2.3: Analog Hearing Aid

(i) The analog hearing aid provide the same amplification to all frequencies.
(ii) The programmability of gain is not possible by analog circuits.
(iii) The patients of hearing loss is unable to understand the speech signals in the presence of noise.
(iv)A conventional analog hearing aid is less flexible.
(v)It is difficult to interface with computer system.
(vi)The cost of analog hearing aid is high.

2.3.2 Programmable Analog Hearing Aid

In Programmable Analog Hearing Aids , the audio processing circuits are analog but variable gain amplifier is used with additional programmable control circuit. It is also possible to do frequency adjustment.

2.3.3 Digital Hearing Aid

In this type of hearing aid, all parts are in digital form starting from input to output i.e from audio system to processing unit. The microphone signal is pick up by preamplifier which is a variable gain amplifier or automatic gain control unit. The amplify signal is converted into digital form by Analog to Digital Converter (ADC). The signal quality of digital form is enhance by Digital Signal Processing Unit (DSP). The output signal further converted into analog form for output amplifier and to drive speaker.

2.3.4 Based on placement

There are following types of hearing aid, which are classify based on placement as shown in Figure.2.4.

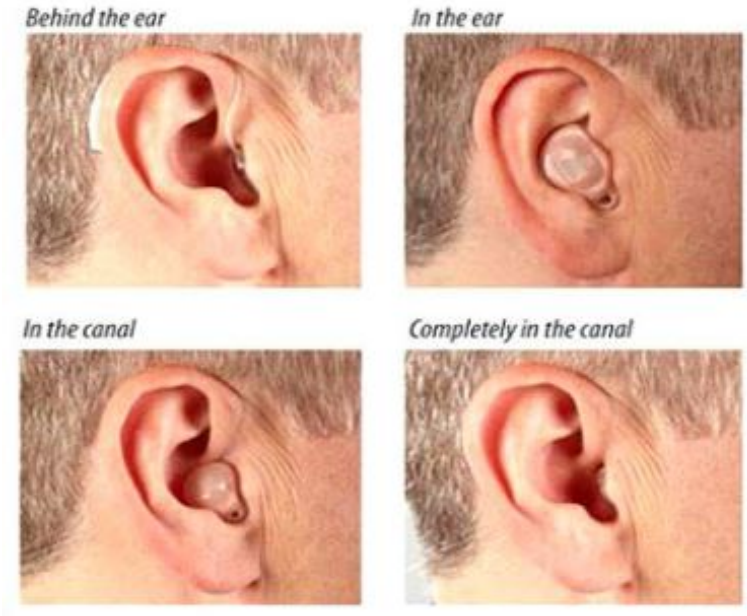

Figure 2.4: Hearing aid Based on placement [2]

(i)Completely in the Canal (CIC): This type of hearing aid is completely placed inside the canal. It is not visible from outside. So hearing impaired patient which do not want to show that he/she has hearing loss. The cost of completely in the canal hearing aid is very high.

(ii)In the Canal (ITC):

This type of hearing aid are useful for conductive hearing loss. It is partially visible from outside and also costly.

(iii)Behind The Ear (BTE):

As name indicate, this type of hearing aid is place behind the ear. The cost is less and visible to other people also.

(iv)Bone Anchored Hearing Aid:

This type of hearing aid is placed inside head through operation. It is useful for patient having conductive loss. The main feature of Bone Anchored Hearing Aid is to transmit sound signal directly to the hearing nerve. [9]

2.4 Audiogram

An audiogram is a graph that give information of the lowest sounds a person can able to hear at comfort level. The audiogram shows the hearing loss across a range of frequencies and is shown in decibels hearing level (dBHL) or decibels hearing threshold level (dBHTL). As shown in Figure.2.5, the test frequencies which are used during hearing testing indicated on vertical lines and the loudness of sounds called Decibel are indicated on horizontal line. These levels are also called hearing threshold. The

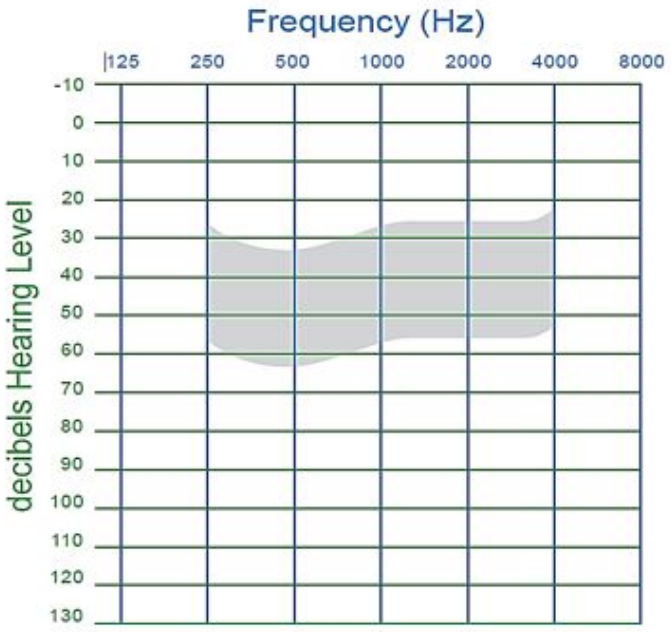

Figure 2.5: Audiogram

indication of threshold is that for any frequency signal, a person can hear test sound very easily. The loudness of the sounds is measured from graph at soft sound to the

loud sound from top to bottom. These numbers are along the left and right sides of the graph. If decibel level is higher, the sound is more louder. For example 40 dB is a murmur (low loud sound) while 100-110 dB(high loud sound) of Jet plane engine. Also Hearing level is measured in decibels (dB or dB HL) not in percentage. Figure.2.6 shows the decibel hearing levels, which match to these degrees of hearing loss. [10]

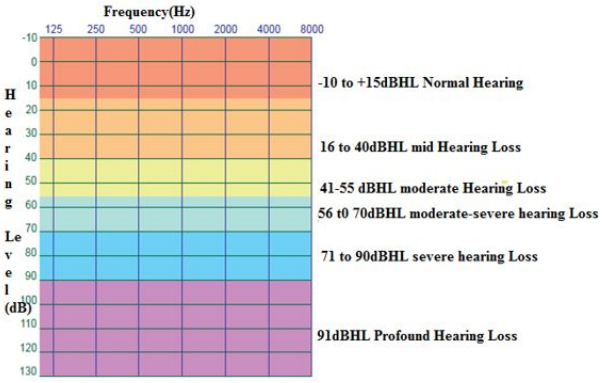

Figure 2.6: Hearing Level

2.4.1 Sound Pressure Level(SPL)

A Sound signal applied to a microphone is expressed as sound pressure level (SPL) with reference to hearing threshold of human ear as:

$$P0 = 20.10^{-6} Pa \tag{2.1}$$

It is expressed in decibels as:

$$SPL = 20.log\frac{Psi}{Pref} \tag{2.2}$$

Where , Psi= sound pressure level incident on the microphones deflecting membrane. The equivalent voltage signal in the dBSPL converted to dBPa which is sound pressure level in decibels normalized to 1 Pascal (Pa) given by:

$$dBPa = dBSPL + 20log[20.10^{-6}]Pascale \tag{2.3}$$

$$dBPa = dBSPL - 94dB \tag{2.4}$$

This sound pressure level incident on the microphone in terms of the absolute Pressure which is converted to voltage in terms of microphone sensitivity(Smic) as:

$$dBV = dBSPL - 94 + Smic(dB) \tag{2.5}$$

Here, Smic=-44dB/V/Pa for conventional microphone. The output voltage Vmo of the microphone is given by:

$$Vmo = 10^{-(dBV/20)} \tag{2.6}$$

The full audio dynamic range is 120 dB, but the useful audible dynamic range is about 60 dB. Figure.2.7 shows the variation in input dBSPL of microphone Vs output voltage of microphone (mV). For normal hearing, range-1 is used where listening is comfortable and output of microphone is 10-15mV. If input range is higher, level of threshold of hearing is reached.

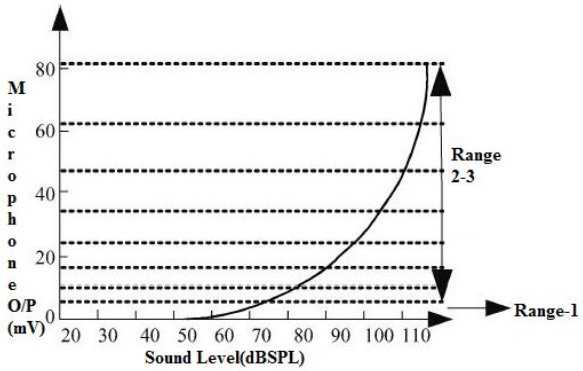

Figure 2.7: Input and output level of microphone [11]

2.5 Analog Front End Component of Hearing Aid

An Analog front end of digital hearing aid contains the following two major units:
(i) Preamplifier
(ii)Analog to Digital Converter

2.5.1 Preamplifier

The function of microphone is to converts incoming sound signal into an analog electrical signal. The output electrical signal is applied to preamplifier before digital conversion. This block provide minimum amplification of 10dB and maximum of 30dB so noise from internal generated signal is reduce and SNR is improve. A compression is also added to control the loud sound. Normally, Automatic Gain Control circuit is used for this purpose and also this function is performed by programmable gain amplifier and variable gain amplifier.A microphone preamp circuit is used to amplify a microphones output signal to match the input level of the devices. [12]

2.5.2 Analog to Digital Converter(ADC)

This is the one of most important and more complex block in digital hearing aid. The available input signal is continuous time signal which is converted into digital 1s and 0s. The conversion is performed by sampling and quantization. The output of ADC is compatible for digital signal processing. The selection of specific ADC is done by design engineer to meet size, power and noise constrain. [13]
There are following types of ADC are as mentioned below.
(a) Flash A/D converter
(b) Pipelined A/D converter
(c) Successive approximation A/D converter
(d) Over-sampling(sigma-delta) A/D converter
(a) Flash A/D converter:
In flash ADC, a ladder voltage divider is designed by 2N resistors. The use of ladder voltage divider to divides the reference voltage into 2N equal intervals. It uses the 2N-1 comparators for finding range of input voltage Vin in 2N voltage intervals. The output of the comparator is apply to combinational logic to translate information. The clock is not used in flash ADC so the conversion time is set by the settling time of the

comparators and the propagation time of the combinational logic. There are following advantages of flash A/D converter:

- Very Fast
- Very simple to design
- Speed is only limited by gate and Comparator
- Propagation delay is very high

It also has following disadvantages:

- More Expensive
- Prone to produce glitches in the output
- Each additional bit of resolution requires twice the comparators
- Pipelined A/D converter

(b)Pipeline ADC:

It is an N-step converter, in which one-bit is converted per stage. After the input signal has sampled, it is compared with Vref /2. The output of each comparator is the bit conversion for that stage. If VIN greater than VREF/2 (comparator output is 1), VREF/2 is subtracted from the held signal and pass the result to the amplifier. If VIN less than VREF/2 (comparator output is 0), then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the residue. It is then multiply the result of the summation by 2 and pass the result to the sample-and-hold of the next stage.

In pipelined ADC, accuracy depends on the most significant stages because small error in the first stage propagates through the converter in subsequent stage which give larger error at the end of the conversion. Each stage require good accuracy.

There are following advantages of pipelined A/D converter:

- Fewer comparators
- Higher resolution possible

The Disadvantages include with pipelined ADC are:

- High accurate OPAMP is require i.e high power
- Errors accumulate if stages have less accuracy

(c)Successive approximation A/D converter:

In successive approximation A/D converter, an n-bit DAC is used to compare DAC output and analog input. In Successive Approximation Register (SAR), digital code supply to DAC of Vin. An output of Comparison changes digital output to bring it closer to the input value Vin.

There are following Advantages of successive approximation:

- It is Capable of high speed and more reliable
- Medium accuracy compared to other ADC types
- Good trade off between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format

There are following Disadvantages:

- Higher resolution successive approximation ADCs will be slower
- Slow speed

(d)Over-sampling (sigma-delta) A/D converter:

In a sigma delta ADC, sampling frequency is very high. An Oversampling converters typically employ switched-capacitor circuits and do not require sample and hold circuits. The output of a modulator is a pulses that represents the average of the input signal. The function of comparator is to give 1-bit data.This modulator is used when high resolution at low frequency is required. Also it not require separate anti aliasing filter.

The following table shows the comparison of different types of ADC in terms of Latency, speed, Accuracy and Area.

Table I: Comparison of ADC type

ARCHITECTURE	**LATENCY**	**SPEED**	**ACCURACY**	**AREA**
Flash Type ADC	Low	High	Low	High
SAR	Low	Low	High	Low
Pipeline	High	High	High	Medium
Sigma Delta	High	Low	High	Medium

2.6 Summary

This chapter described the different types of hearing aid and hearing loss. Also different methods for preamplifier and Analog to Digital converter are discussed. The preamplifier section is require to increase the gain for low power low noise applications. Also sigma Delta ADC is preferred as an analog to digital converter to received amplified signal from preamplifier and convert into digital stream.

Chapter 3

Design and Simulation of Preamplifier

The first block of analog front end for digital hearing aid is a preamplifier, whose main function is to amplify signal received from microphone. If sound intensity is high, gain is compressed to normal hearing level and if sound intensity is low, gain is expand by variable gain amplifier.

In this chapter, different types of low power low noise design methods are discussed with advantages and disadvantages. The MOST is designed to operate in subthreshold region to reduce power dissipation. The graphical method gm/Id Vs Id/(W/L) is used to design operational amplifier. A PMOS input pair used to reduce 1/f noise. A two stage OPAMP with variable gain Amplifier of dynamic range 10dB-32dB is designed and simulated in 0.18um TSMC Technology using Mentor Graphics.

3.1 Design Techniques for Operational Amplifier

A battery operated devices requires low power for its reliable and long duration operation. The new CMOS technologies give more density and reliability of integrated circuits and give less power consumption due to decreased power supply voltage. As technology is scaled down, the threshold voltage of a MOS transistor is not scaling down at the same rate as the power supply voltage is being scaled down. This limit the dynamic range of analog mixed circuit design. The different topology are available for design of operational amplifier as telescopic opamp, folded cascaded opamp and a two

stage opamp. The choice of appropriate design of opamp topology depends upon the opamp specifications. The two stage miller compensated OPAMP topology is more suited for low voltage and high gain applications.

3.2 Low Power Design Methods

For designing an operational amplifier with low power and low noise the following methods are being used:

(i) Floating gate technique
(ii)Bulk driven technique
(iii)Weak inversion.
The Table shows comparison of different methods for low power.[14]

Table I: comparison of different methods for low power

Techniques	**Power Dissipation**	**Noise**	**Leakage Current**	**Silicon Area**	**Cost and Complexity**
Floating Gate	Low	Low	Low Leakage	Large	High
Bulk Driven	Low	Low	Less Noise	small	High
Weak Inversion	Ultra Low	High	Low	Moderate	Low

For MOS design in weak inversion is the most efficient way to achieve low power dissipation in opamp. Also the conventional MOS transistors are used in design so it is not require extra fabrication step and small area and low cost as compared to other techniques. However, Frequency response of devices is poor. The Gain bandwidth product (low) is directly proportional to subthreshold current, which is very low (in nA). For obtaining higher gain, the devices of larger width or low drain current are required that limits the speed of operation.

3.3 Low Noise Design Method

With addition to low power to increase a battery life of portable biomedical devices, low noise operation is also important because if noise effect is high, signal strength become weak and reduce dynamic range. In literature, following methods are proposed for low noise design.[15]

(i) Autozero Technique

(ii) Chopper stabilization

(iii) Weak Inversion Technique

3.3.1 Autozero Technique

In this method, the sampling of OPAMP noise in form of dc offset voltage is done then subtracting the effect of noise from the input signal using a sample-and-hold circuit. So, the autozeroing technique can reduce the low-frequency (1/f) noise of the amplifier. Also, this method increase baseband noise floor, which is caused by the aliasing of the wideband noise that is inherent to the sampling process.

3.3.2 Chopper stabilization

This method is based on modulation technique in which the frequency range of input signal is converted into higher frequency Fc(chopping frequency) where noise level is white noise and then demodulate back to the baseband signal. The higher order low pass filter is require to remove noise level.

3.3.3 Weak Inversion Technique

The noise level in MOS is higher as compared to BJT because of the lower l/f noise of BJTs compared to MOST of same area and higher transconductance at a given device current. However, BJT designed with bulk CMOS process having large base current and collector current limits use in a CMOS design. While MOST operating in the weak inversion region generate the same nature as a BJTs without requirement of large current.[16] For Bipolar Transistor

$$gm = \frac{q.Ic}{K.T} \tag{3.1}$$

For MOS Device in Weak Inversion

$$gm = \frac{q.Id}{n.k.T} \tag{3.2}$$

For MOS Device in Saturation

$$gm = \sqrt{\frac{2KW}{L.Id}} \tag{3.3}$$

From above equations, there is linear relationship between transconductance and drain current like bipolar transistor. So transconductance to drain current ratio can be maximize in subthreshold region and flicker and white noise density is reduced by large transconductance and drain current. The combined white noise and flicker noise for MOS is given by

$$Vn^2 = [\frac{8}{3}K.T.gm.df + \frac{K}{Cox.W.L}.\frac{df}{f}] \tag{3.4}$$

The first term is a white noise which is reduce by selecting large value of gm and second term is 1/f flicker noise which is reduce by selecting large dimension of MOS input pair(W,L). Also mobility of hole is less as compared to electron so movement at si-sio2 interface due to trap charge is less that causes less noise in PMOS device. So here PMOS device pair is selected as an input pair for differential amplifier.
The following table shows comparison of different methods for low noise design, where weak inversion is best choice for low noise OPAMP design.

Table II: comparison of different methods for low Noise

Techniques	**Power Dissipation**	**Noise**	**Leakage Current**	**Silicon Area**	**Cost and Complexity**
Autozero	High	-	Low	Large	High
Chopper Stabilization	High	-	Low	Large	High
Weak Inversion	Ultra Low	High	Low	Moderate	Low

From above comparison of different methods for low Noise, MOS design in weak inversion also give low noise at small range of frequency (1/f noise).

3.4 Design of Low Power Low Noise Preamplifier

The Acoustical Society of America(ASA) provides the Secretariat for Accredited Standards committees. The standards are published by the Acoustical society of America as American National Standards(ANSI) after approval by their respective standard committees and the American National Standards Institute. In this section, low power low noise OPAMP is designed with variable gain amplifier to meet following specification of hearing aid.

Table III: Preamplifier Specifications

Parameters	**Value**
Open Loop Gain	80dB
Gain Bandwidth	300KHz
Phase Margin	60°
Slew Rate	100kv/s
CMRR	80dB
ICMR	0-1.6V
PSRR	80dB
Power Dissipation	$\leq 5uW$
Input Referred Noise	$\leq \frac{5uV}{\sqrt{HZ}}$
Total Harmonic Distortion	$< 1\%$

3.4.1 Design of Two stage Operational Amplifier

In this section, two stage miller compensated opamp is designed as shown in Figure.3.1 The MOS M1 and M2 act as PMOS input differential pair, M3-M4 as a current mirror load, M5 as a current tail in which bias current is flow. M6-M7 act as output transistor pair for second stage. CC is a compensating capacitor, CL as load capacitor and M9 as a nulling resistor.

There are following parameters for Subthreshold design:

The Subthresshold slope factor n of MOST in weak inversion region can be calculated experimentally using ID and VGS curve. It is measured from the slope of linear region ln(ID) and VGS curve as shown in Figure.3.2

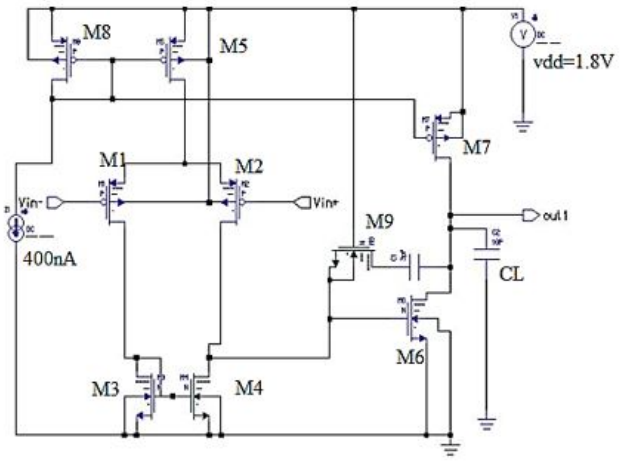

Figure 3.1: Two Stage Miller Compensated OPAMP

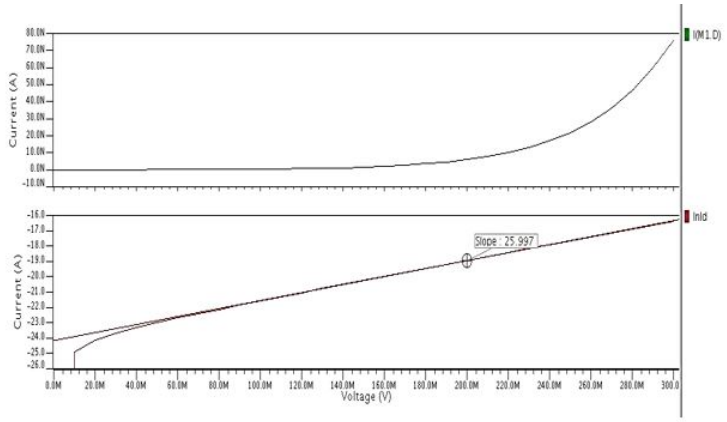

Figure 3.2: Vgs Vs ln(Id) for NMOS

In weak inversion region,

$$slope = \frac{1}{n.VT} \tag{3.5}$$

Slope=25.997, so from equation (3.4) , subthreshold parameter is :

Subthreshold parameter n=1.479

And for PMOS, subthreshold parameter from Figure.3.3 is n=1.602.

Next, the calculation is for channel length modulation factor Lambda. For this IDS vs VDS curve is require for NMOS and PMOS as shown in Figure.3.4 The value of channel length modulation index is calculated from equation (3.3)

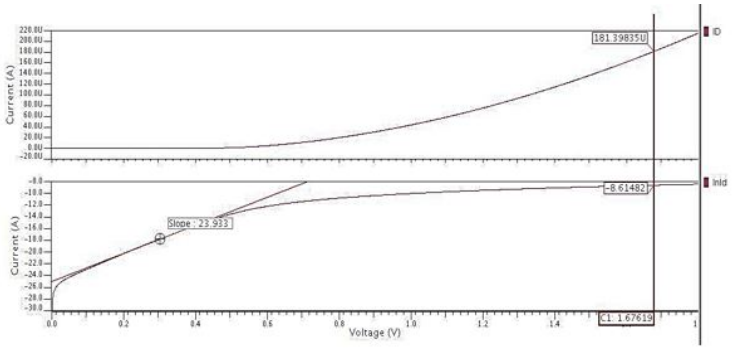

Figure 3.3: Vgs Vs ln(Id) for PMOS

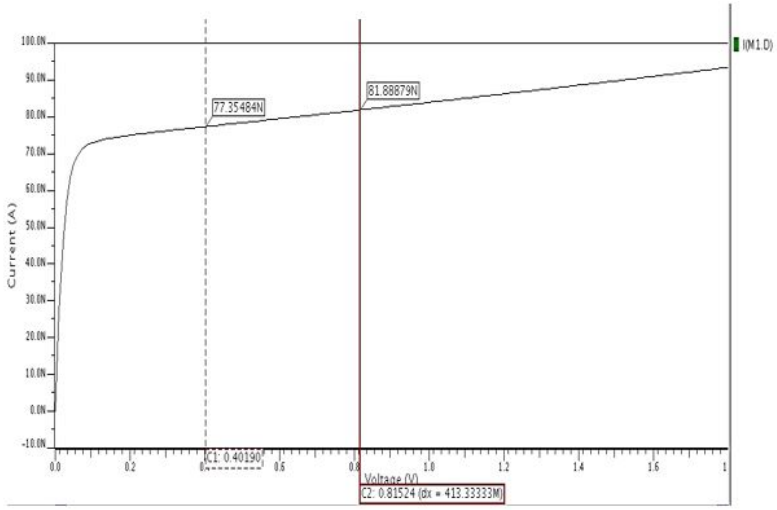

Figure 3.4: Vds Vs ln(Id) for NMOS

$$\frac{Id1}{Id2} = \frac{1 + Ln.Vds1}{1 + Ln.Vds2} \tag{3.6}$$

The Value of Ln for n channel MOS 0.15 and value for PMOS Lp=0.057 from Figure.3.5

3.4.2 Gm/Id Vs Id/W/L Design Method

The conventional methods for analog design, using long channel equations are not producing desired results due to advance in technology. A method known as GM/ID method is developed wherein current is fixed to find out transistor dimensions to fulfil with the specifications such as gain-bandwidth, power consumption, area, etc.

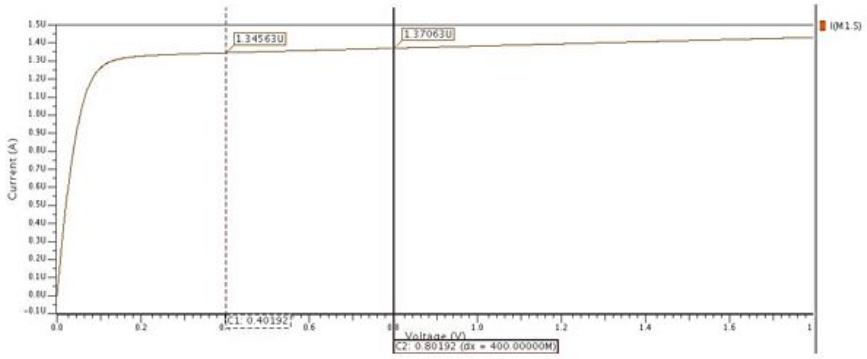

Figure 3.5: Vds Vs ln(Id) for PMOS

This method use different curves to characterize the PMOS and NMOS transistors of a particular technology and it is independent of transistor dimensions. For low power analog circuit design, the weak and moderate inversion regions are used because they provide a good compromise between speed and power consumption. The gm / ID ratio is a universal characteristic of all transistors formed by the same process. MOS transistors are either in strong inversion or in weak inversion. The Conventional method used for strong inversion where the transistor gate voltage overdrive(Vov) as the key parameter, where Vov=Vgs-Vt. [17]

The relation between power and bandwidth is given by:

$$P = \frac{1}{2}\frac{Vdd}{RL}Adc.Vov \tag{3.7}$$

$$W3dB = \frac{3}{2}\frac{RL}{Ri}\frac{1}{Adc}\frac{u}{L^2}Vov \tag{3.8}$$

For fixed value of L, both power and bandwidth of circuit are determined by the selection of Vov If Vov is small to save power, bandwidth is decrease.

$$\frac{W}{L} = \frac{gm}{u.Cox.Vov} \tag{3.9}$$

Also ,with gm and L fixed, smaller Vov result large size device and thus larger Cgs. So Vov is not a good choice as a design parameter. Generally, for MOS transistor, large gm without investing much current and large gm without having large Cgs is require. There are following performance parameter for MOS device.

(i)Transit Frequency: Wt=gm/Cgs

(ii)Transconductor efficiency=gm/Id

(iii)Intrinsic Gaingm.ro

There are following feature of gm/id vs Id/(W/L) method.

(i)It is strongly related to the performance of analog circuits.

(ii)It gives an indication of the device operation region.

(iii)Number of iteration reduced.

The gm/Id is size independent. It gives the designer full provision to choose any region of operation as the curves are continuous and there is no transition between different regions. The level of transistor inversion can be select by this method which allows the designer to make important design trade-offs i.e. between bandwidth, gain and power consumptions, etc. The different curves for a particular technology give complete analog circuit design like two stage OPAMP. There are following steps to design MOS W/L.

Step 1: Plot ID vs Vgs for NMOS and PMOS

Step 2: Plot Differentiation of ID as a gm plot

Step 3: Plot gm/ID vs Vgs

Step 4: Plot ID/(W/L) vs Vgs

Step 5: Selection of gm/ID corresponding to weak inversion and take corresponding value of ID/(W/L).

Figure 3.6 used to find out the dimensions of a transistor. For higher value of gm/Id, device remain in weak inversion region and for low value of gm/Id device enter into strong inversion. The relationship between gm/Id versus Id/(W/L) represents a unique curve for all transistors of same type (i.e. PMOS or NMOS) in a specific technology. This unique characteristic of gm/Id versus Id/(W/L) used determining the transistor sizes.

3.4.3 Design of Two stage Miller Compensated Operational Amplifier

To use gm/ID Vs ID/(W/L) method, plot of ID Vs VGS is found for NMOS and PMOS transistor. The schematic used for this is as shown in Figure.3.7. The source voltage is sweep from 0 to Vdd and plot of Id is generated. The gm/Id and Id/(W/L) plot is shown in Figure.3.8

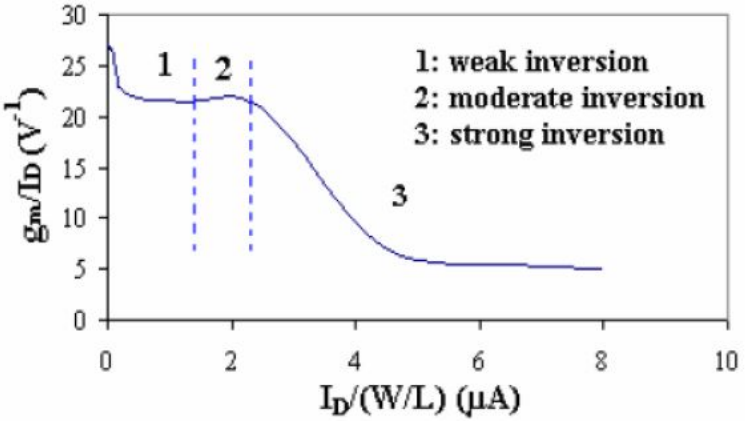

Figure 3.6: Relation between gm/Id and Id/(W/L)

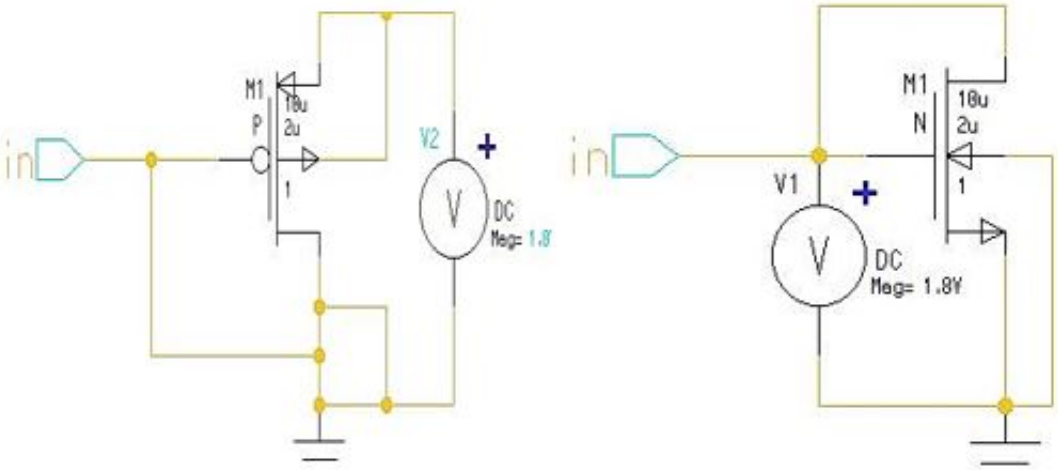

Figure 3.7: PMOS and NMOS circuit

The following steps are apply to calculate aspect ratio for each device.

Step 1: Power Dissipation

Step 2: Compensating Capacitor Cc

Step3: Design of PMOS(M1,M2)

Step4: Design of PMOS(M5)

Step5: Design of PMOS(M7)

Step6: Design of PMOS(M8)

Step7: Design of NMOS(M3,M4)

Step8: Design of NMOS(M6)

Step9: Design of Nulling Resistor

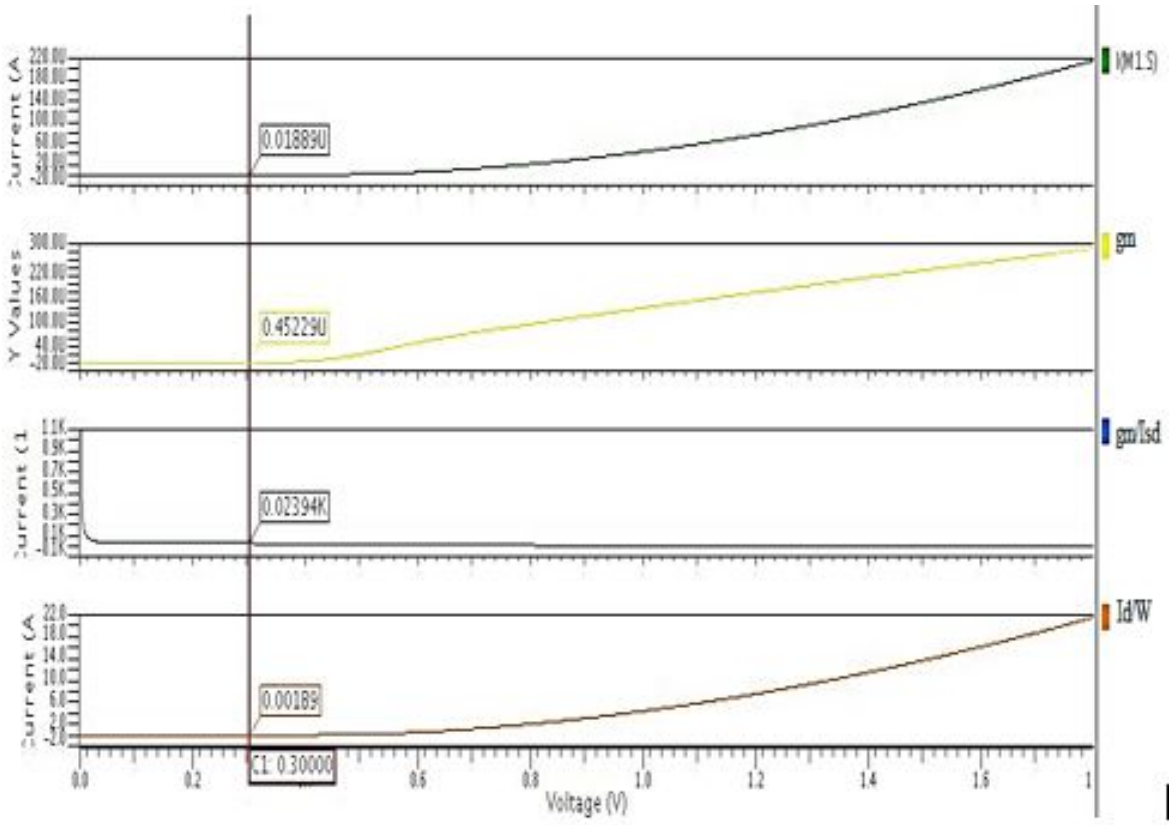

Figure 3.8: GM/ID Vs ID/(W/L) Plot for PMOS

The Table shows operating region and Aspect ratio for each transistor.

Table IV: Aspect Ratio of Transistor

Transistor	**Operating Region**	**Width(um)**	**Length(um)**
M1-M2	Subthreshold	106	2
M3-M4	Subthreshold	26.2	2
M5-M8	Subthreshold	211	2
M7	Subthreshold	422	2
M6	Subthreshold	105	2
M9	Linear	0.109	10

The Load capacitance CL=10uf and Compensation capacitor Cc=3pf.

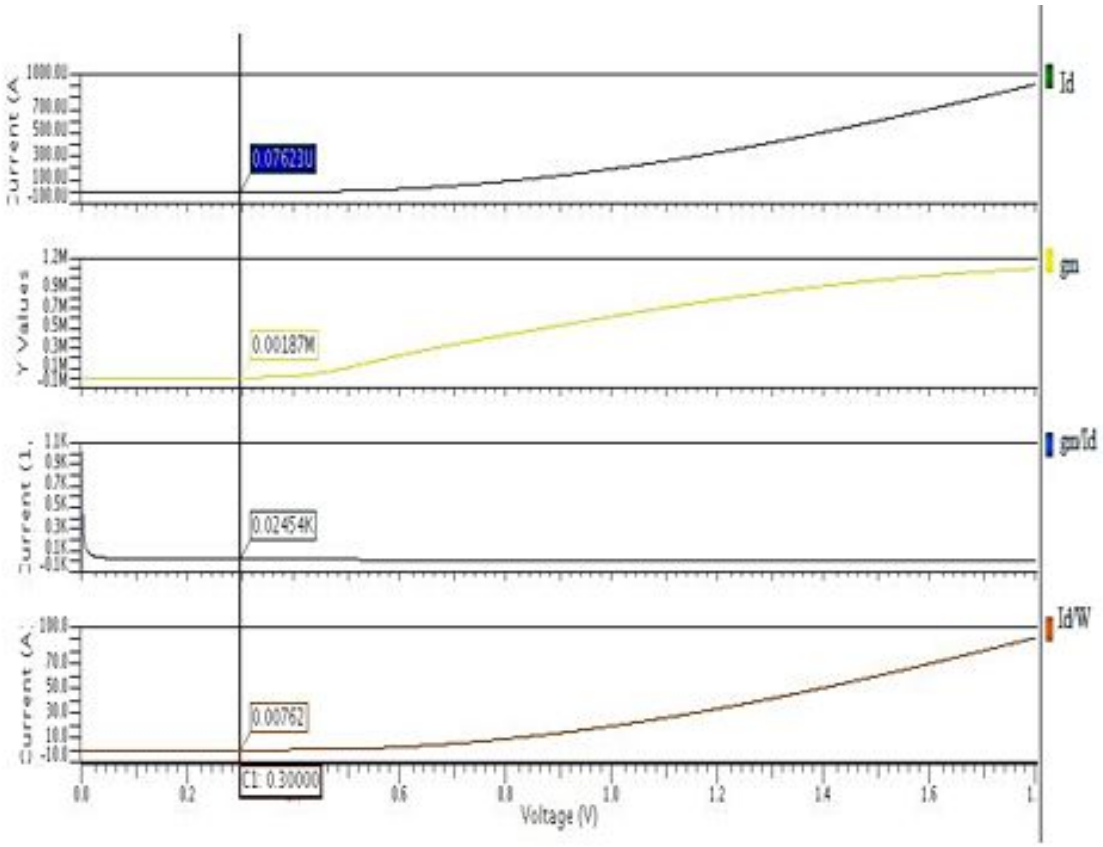

Figure 3.9: GM/ID Vs ID/(W/L) Plot for NMOS

3.4.4 Analytical Method

The drain current Id in subthreshold region is given by

$$Id = \frac{W}{L}.Io.\exp(\frac{Vgs - vth}{n.Vt}).(1 - \exp(\frac{-vds}{vt})) \tag{3.10}$$

For Vds more than 100mV, the second term is negligible

$$Id = \frac{W}{L}.Io.\exp(\frac{Vgs - vth}{n.Vt}) \tag{3.11}$$

Where W/L is the aspect ratio of the transistor, VGS and VDS are the gate-to-source and drain-to-source voltages, respectively, Vth is the transistor threshold voltage, and VT=kBT/q is the thermal voltage (kB is the Boltzmann constant, T the absolute temperature, and q the elementary charge). The subthreshold slope parameter n is a technology-dependent constant (usually 1 to 3), and I0 is a process parameter that also depends on temperature. Similarly to a bipolar transistor, ID changes exponentially

with the control voltage VGS. The transistor behaves like a VGS controlled current source if VDS higher than 3VT.

The transconductance of MOST is calculated by

$$gm = \frac{Id}{n.Vt} \tag{3.12}$$

The value of open loop gain is given by

$$Av = \frac{gm1}{Id1}.\frac{gm6}{id4}.\frac{1}{(Ln + Lp)} \tag{3.13}$$

The value of slew rate is calculated by

$$SR = min\frac{2Id1,2}{Cc}, \frac{Id6,7}{CL + Cc} \tag{3.14}$$

The noise spectral density is given by

$$eq^2 = 2.en^2.[1 + \frac{Kn'BN}{Kp'BP}\frac{L1}{L2}^2]V^2/Hz \tag{3.15}$$

3.5 Simulation of Two stage Amplifier

The pre layout simulation is done in mentor graphics with 0.18um TSMC process. The various analysis results as follows.

3.5.1 AC Analysis

The AC analysis is used to measure Gain and phase margin. The AC Source is connected between inverting and non inverting terminal with common bias voltage 0.9V. The simulation result is shown where gain remain constant for 84dB and unity gain bandwidth of 274KHz. The phase margin when gain becomes zero is 71 °.

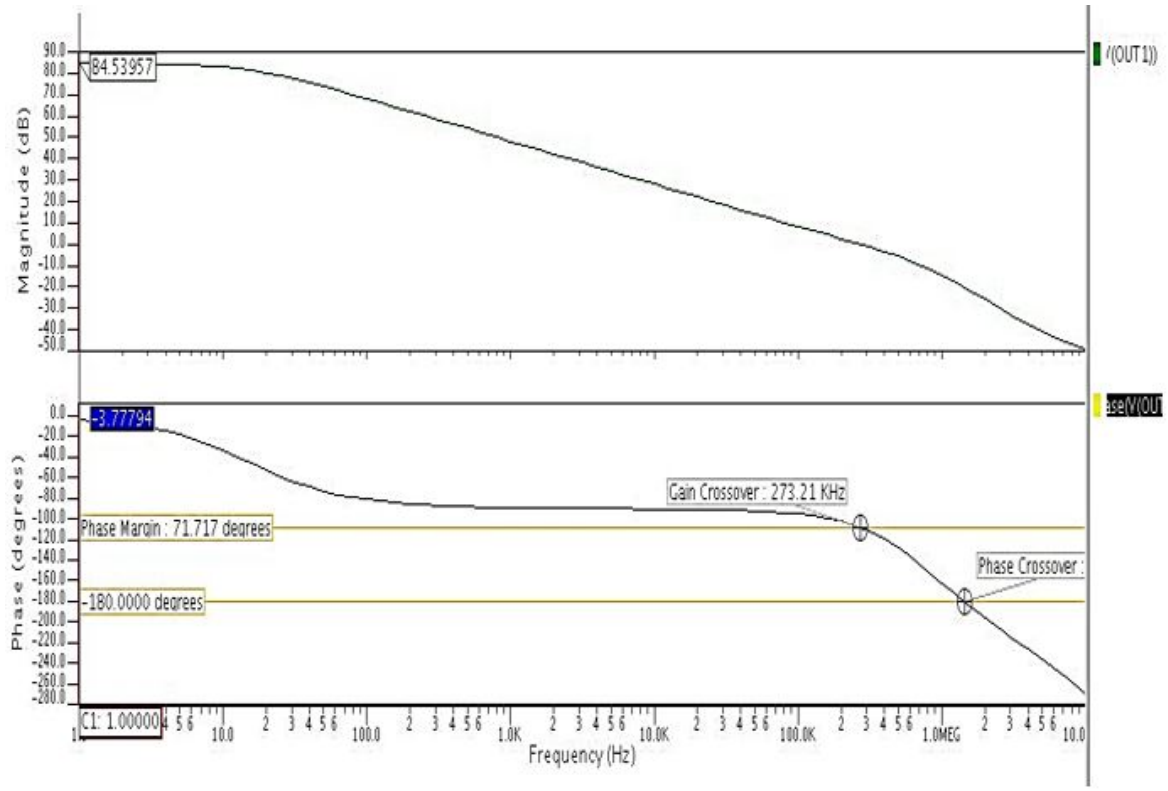

Figure 3.10: Open Loop Gain and Phase Margin

3.5.2 Transient Analysis

In transient analysis measurement where input is connected as sin wave source of 100Hz at inverting terminal and response at output is also sine wave. The ratio of peak to peak output and input is 82.9dB as a differential gain.

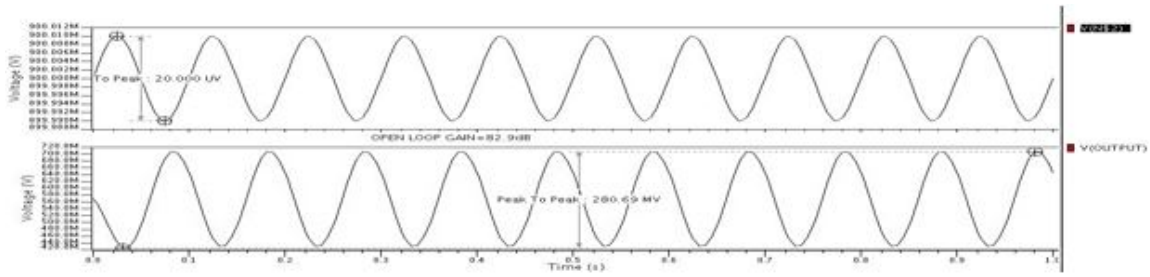

Figure 3.11: Responce for Transient Analysis

3.5.3 Slew Rate

For measurement of slew rate, input is connected with pulse signal of low frequency. The measurement value of slew rate is 50KV/sec and settling time is 75ms.

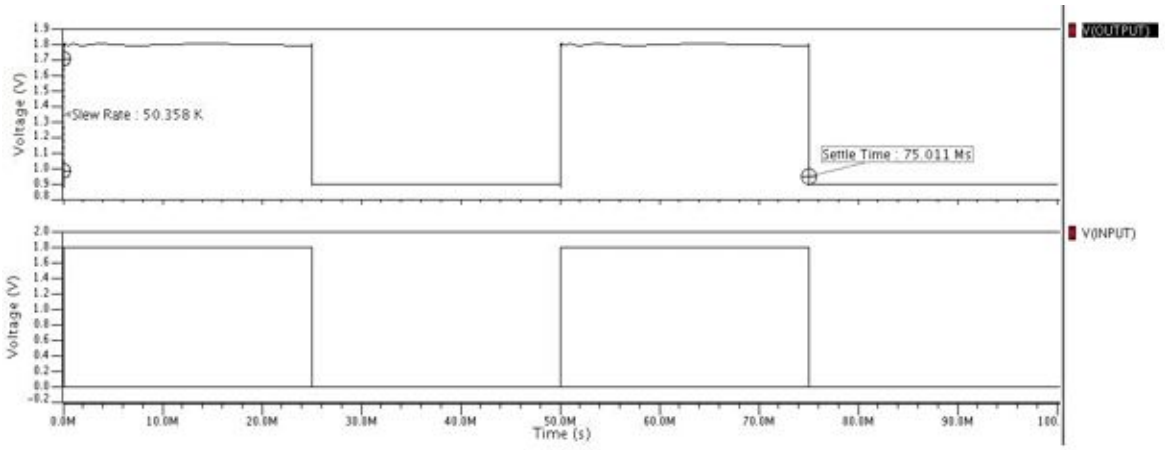

Figure 3.12: Slew Rate Analysis

3.5.4 Common Mode Rejection Ratio

The common mode rejection ratio is found by applying a common ac source between input and by taking ratio of differential gain and common mode gain. The measurement value of CMRR is 97.73dB.

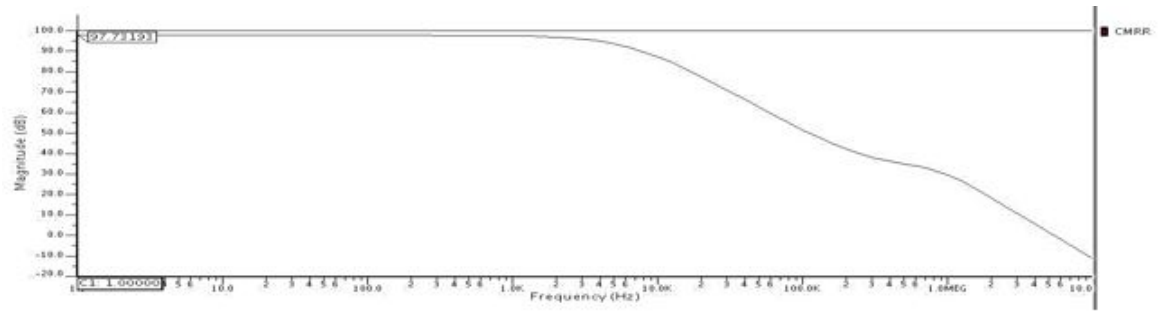

Figure 3.13: CMRR Analysis

3.5.5 Input Common Mode Range

The input common mode range is measure by applying DC input of 0 to 1.8V and output is measure in DC analysis. From graph, ICMR value is 0 to 1.7V.

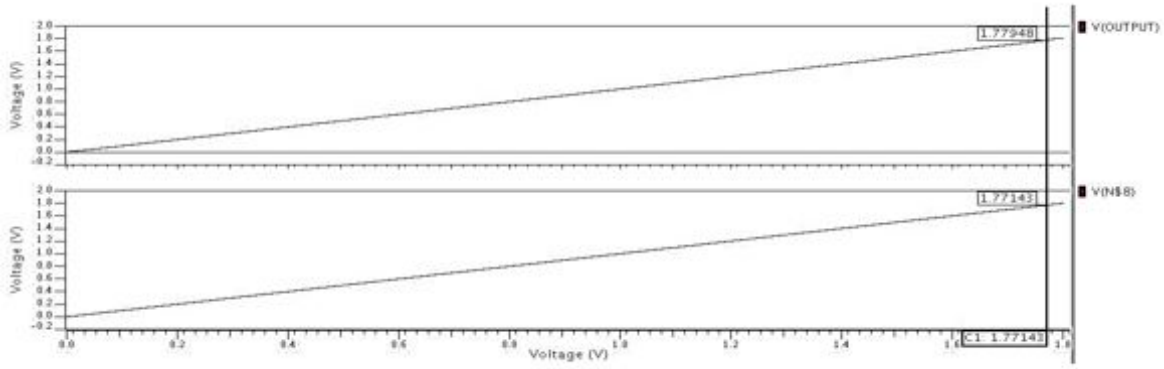

Figure 3.14: ICMR Analysis

3.5.6 Power Supply rejection ratio

The PSRR+ value is measure by applying AC source in series with VDD source and input terminals are connected with only dc source. Then result is subtract from differential gain. Here the measure value of PSRR+ is 112dB. The PSRR- is measure by connecting AC source with VSS and measured value is 87dB.

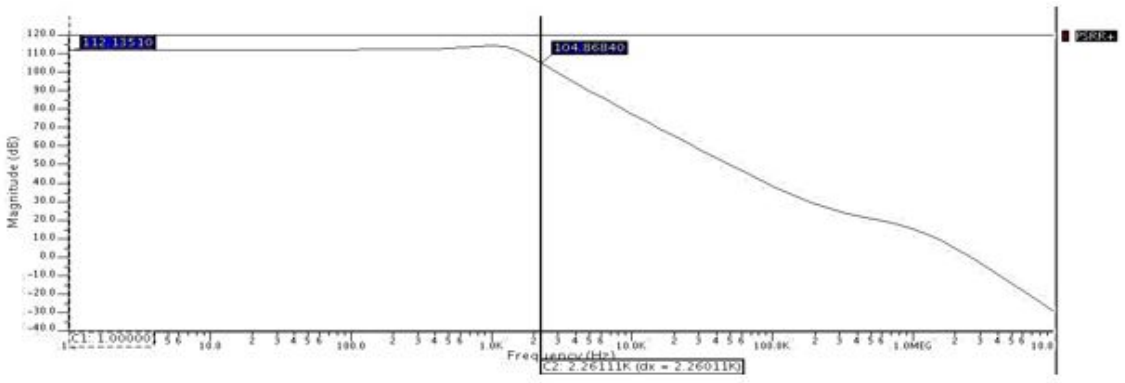

Figure 3.15: PSRR Analysis

3.5.7 Power Dissipation

The simulation of total DC power dissipation is 2.35uW.

3.5.8 Total Harmonic Distortion

The total harmonic distortion is calculated from with respect to fundamental frequency of 100Hz. The measured value of THD is 0.055% at 100Hz. The following table indicate

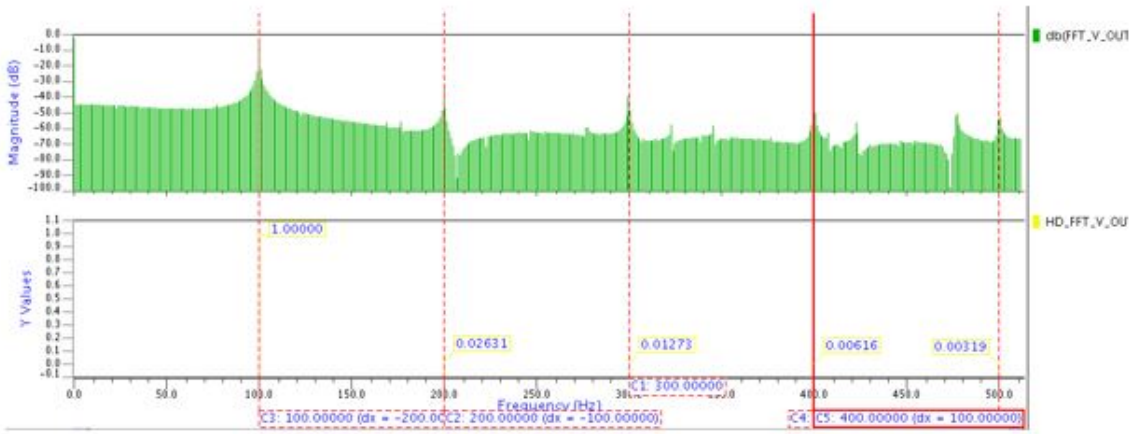

Figure 3.16: THD Analysis

simulated value of OPAMP parameters.

Table V: Simulation Results

Parameters	**Targated Value**	**Simulated Value**
Open Loop Gain	80dB	84dB
Phase Margin	60 °	71 °
Gain Bandwidth	300KHz	274KHz
Slew Rate	100kv/s	50kv/s
CMRR	80dB	97dB
ICMR	0-1.6V	1-1.7V
PSRR	80dB	112dB,87dB
Power Dissipation	$\leq 5uW$	2.35uW
Input Referred Noise	$\leq \frac{5uV}{\sqrt{HZ}}$	$\frac{3.2uV}{\sqrt{HZ}}$
Total Harmonic Distortion	$< 1\%$	0.055%

3.6 Variable Gain Amplifier

To meet the hearing impaired person requirement for comfortable sound, variable gain amplifier is require. Figure.3.17shows the circuit arrangement where the feedback

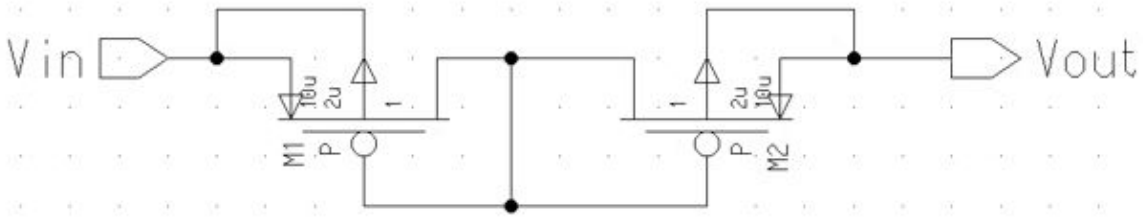

Figure 3.17: High Value Resistor

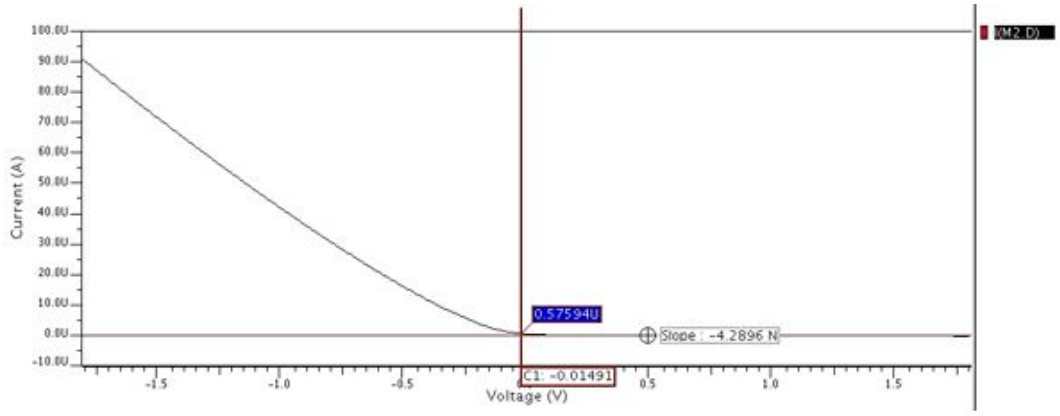

Figure 3.18: Resistance measurement

contains the large value of resistor with feedback capacitor Cf, and input capacitor Cin. The input capacitor value is variable. The closed loop gain is given by

$$Gain = \frac{Vo}{Vin} = -\frac{Cin}{Cf} \tag{3.16}$$

For audio frequency range of 20Hz to 20Khz, at lower cut off frequency of 20Hz.

$$FlowerCutoff = \frac{1}{2..Rf.Cf} \tag{3.17}$$

For Cf=1PF, the require value of Rf= 8G which is very large. To realize large value of resistor, MOST is used in subthreshold region. Figure 3.19 shows the way of achieving

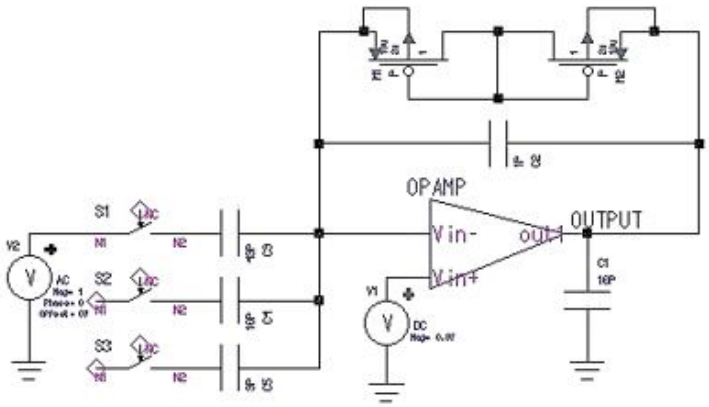

Figure 3.19: Variable Gain Amplifier

high value of resistor using PMOS transistors. The MOS resistor consists of a cascaded of two diode bulk PMOS transistors. The characteristics depends on voltage difference between VIN-VOUT terminals. When Vin greater than Vout, then transistor M1 is in linear region acting as a resistor and M2 behaves as a bipolar transistor with small forward current. When Vout greater than Vin, where M2 acts as a resistor and M1 as bipolar transistor with very small forward current. [19]

The variable gain amplifier is obtain with high value of resistor in feedback path. The gain of amplifier is changed by changing the value of capacitor Cin. The require value of rds for W/L=10u/2u is 2.5Gohms, total is 5Gohms to get lower cut off frequency. With this value, the lower cut off frequency is 32Hz, which is simulated give value of 30.9Hz.

The variablle gain amplifier is obtain through following capacitor values:

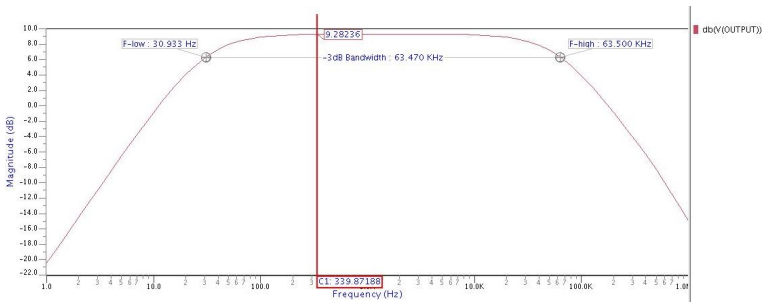

Figure 3.20: Gain Response-1

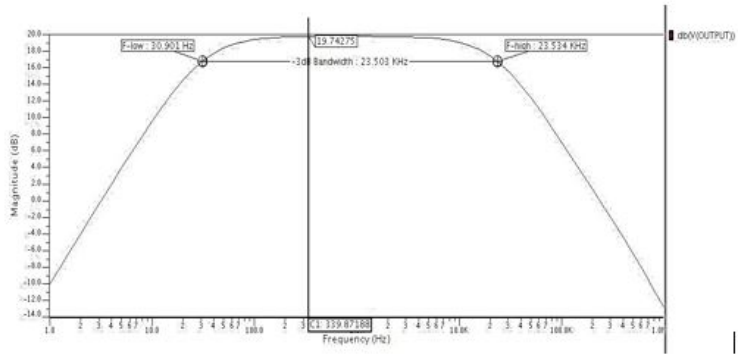

Figure 3.21: Gain Response-2

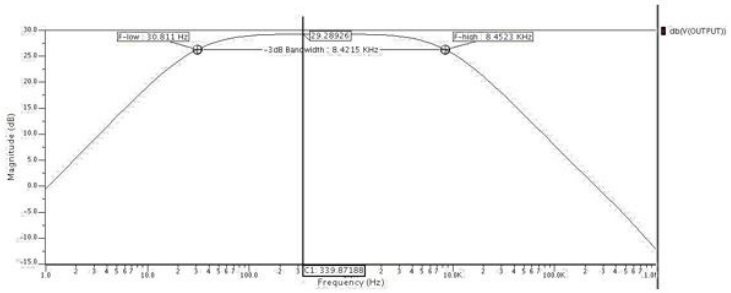

Figure 3.22: Gain Response-3

Table VI: Range of Gain

Capacitors Cin	**Capacitor Cf**	**Gain**
3PF	1PF	10dB
10PF	1PF	20dB
30PF	1PF	30dB

The change in output dBSPL with change in input dBSPL is shown in table.An initially gain is 20dB when input signal is below threshold voltage. When input cross the threshold level, gain is reduced to 10dB by selecting proper input value of capacitors.

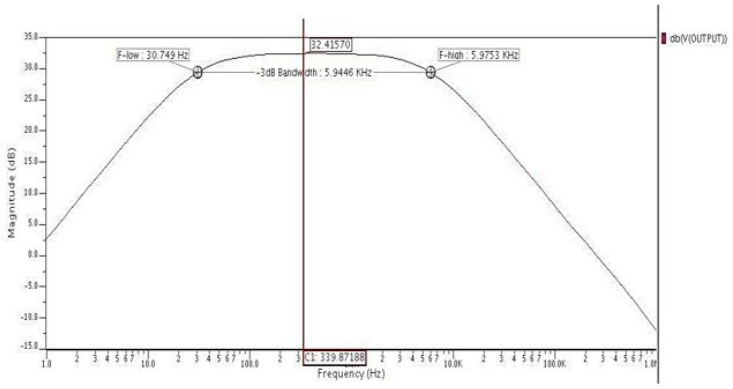

Figure 3.23: Gain Response-4

Table VII: Input and Output dBSPL

Vin(V)	**Vin(dBSPL)**	**Vout(V)**	**Vout(dBSPL)**
15uV	40dBSPL	304uV	60dBSPL
35uV	50dBSPL	357uV	70dBSPL
0.15mV	60dBSPL	1.5mV	80dBSPL
0.5mV	70dBSPL	49mV	90dBSPL
1.58mV	80dBSPL	15mV	100dBSPL
5mV	90dBSPL	15mV	100dBSPL
15mV	100dBSPL	44mV	110dBSPL
50mV	110dBSPL	147mV	120dBSPL

The Figure.3.20 shows the audio frequency range with change in gain value. For maximum sound pressure to microphone(threshold of pain, more than 90dBSPL), the microphone output voltage level is around 10mV. The simulation results shows for Vin=10mVPP Figure.3.24show noise analysis with input and output referred noise.

Table VIII: 1/f Noise

Frequency	**Input referred Noise**
1Hz	$\frac{5.4692uV}{\sqrt{HZ}}$
10Hz	$\frac{0.5576uV}{\sqrt{HZ}}$
100Hz	$\frac{0.1216uV}{\sqrt{HZ}}$

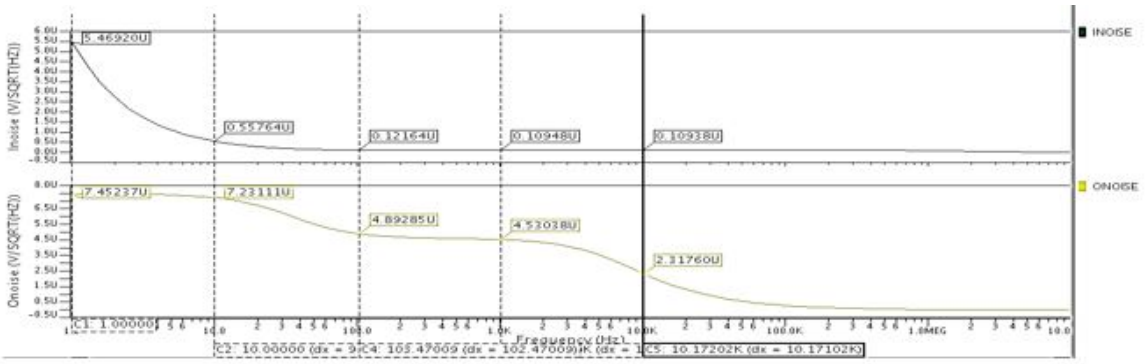

Figure 3.24: Input referred Noise

3.7 Layout of Preamplifier

The layout of preamplifier as shown in figure with DRC and PEX report.

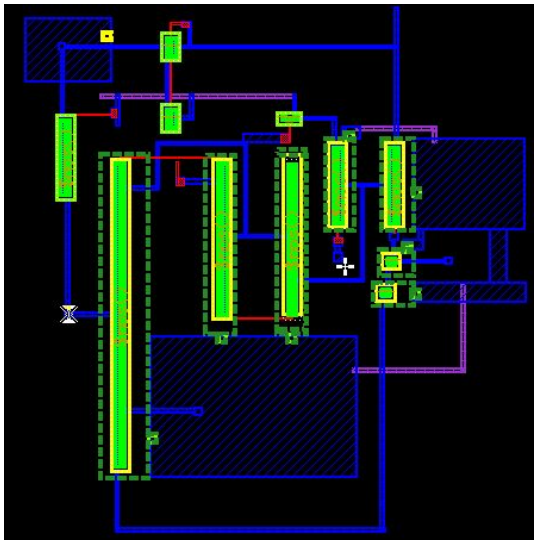

Figure 3.25: Preamplifier Layout

3.8 Comparison of Results

The simulation results are compared with existing design as shown in Table.The supply voltage for different technology are from 0.9V to 1.8V. The comparison indicate that design of MOST in weak inversion give lowest power dissipation. Also input referred noise is noted as $\frac{3.2uV}{\sqrt{HZ}}$.

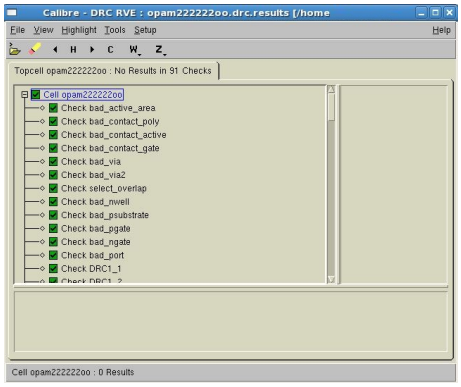

Figure 3.26: DRC report

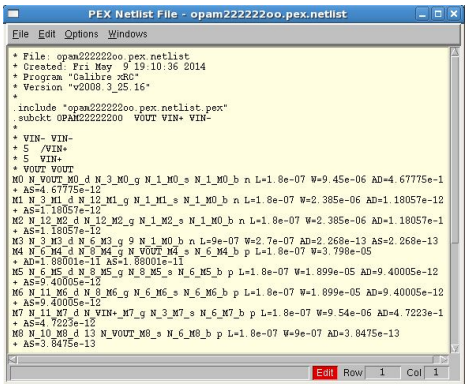

Figure 3.27: PEX report

Table IX: Simulation Comparison

Parameters	**REFE 2013[31]**	**REFE 2006[11]**	**REFE 2002[32]**	**This Work**
Technology	0.13um	0.25um	0.6um	0.18um
Power Dissipation	27uW	38uW	297uW	2.15uW
Power Supply	1.2V	0.9V	3.3V	1.8V
Input referred Noise	2uVrms	3.8uVrms	2.8uVrms	$\frac{3.2uV}{\sqrt{HZ}}$
Bandwidth	10KHz	10KHz	10KHz	30Hz-10KHz
Gain(dB)	-1dB-40dB PGA	continous	-1dB-40dB PGA	10dB-32dB VGA
THD	0.0063 %	–	0.02%	0.055%

3.9 Summary

In this chapter, low power low noise variable gain preamplifier is designed and simulated in 0.18um TSMC mentor graphics tool. The gm/Id Vs Id/W/L design method is used for two stage miller compensated opamp. The varible gain is achieved by using variable input capacitors. Also high feedback resistor is designed in weak inversion region. The total power dissipation is 2.15uW and input referred noise is $\frac{3.2uV}{\sqrt{H}Z}$.

Chapter 4

Design and Simulation of Sigma Delta Modulator

The Analog-to-Digital converters play an essential role in modern portable digital device and communication devices. The function of this block is to convert analog signal into digital signal for further processing. Due to low-amplitude and non-stationary nature of biomedical signals, high resolution and low-power consumption are require for the analog-to-digital (A/D) Converter. In this chapter second block of analog front end as sigma delta modulator is designed and simulated.

The Conventional design of analog to digital converters are called Nyquist converters which require analog components system that are highly related to noise and interference with other signals. On other side, sigma delta or oversampling converters (more than Nyquist rate) that can be implemented using simple and high-tolerance analog discrete and integrated components. Also, Sampling the signal at high frequency avoids the need for sharp cut-offs in the analog antialiasing filters. Additionally, the method of noise shaping is used in sigma delta converters to achieve a high-resolution. The key feature of this ADC is that it is based on oversampling method which uses high frequencies modulation technique and eliminates antialiasing filter at the input to the converter.

The Sigma Delta Modulator is design with following Specifications.

Table I: Specification for Sigma Delta Modulator

Parameters	**Value**
Technology	0.18um TSMC
Supply Voltage	1.8V
Sampling Frequency	256KHz
Input Signal Frequency	1KHz
Oversampling Ratio	128
Dynamic Range	60dB
Power Dissipation	minimum

4.1 Block Diagram of Sigma Delta ADC

The Sigma delta ADC comes under the category of oversampling ADC, which samples the signal at an over sampled frequency of FN=X.2Fs where X is the oversampling ratio and is given by the following equation.

$$X = \frac{FN}{2Fs} \tag{4.1}$$

Figure.4.1 shows the block diagram of sigma delta ADC. The function of modulator is to samples the input signal at a much higher frequency. Also it converts the analog input signal to pulse density modulated signal followed by a decimation filter which contains the original input signal and out of band noise. Both the modulator and the decimator are operated with the same over sampling clock. The modulator is designed with first order, a 1-bit quantize and it generates a 1-bit output. The output of the decimator is N-bit digital data, where N is the output resolution of the ADC and is dependent on the over sampling ratio of the converter.[20]

(i) Modulator:

As shown in Figure.4.2, the modulator is the analog part of sigma delta ADC, the resolution of the converter depends upon the order of the modulator order (N) which is set by the sampling ratio(FN). It consists of an integrator and a comparator (ADC) in the forward path and a DAC in the feedback path. The Delta word is used to

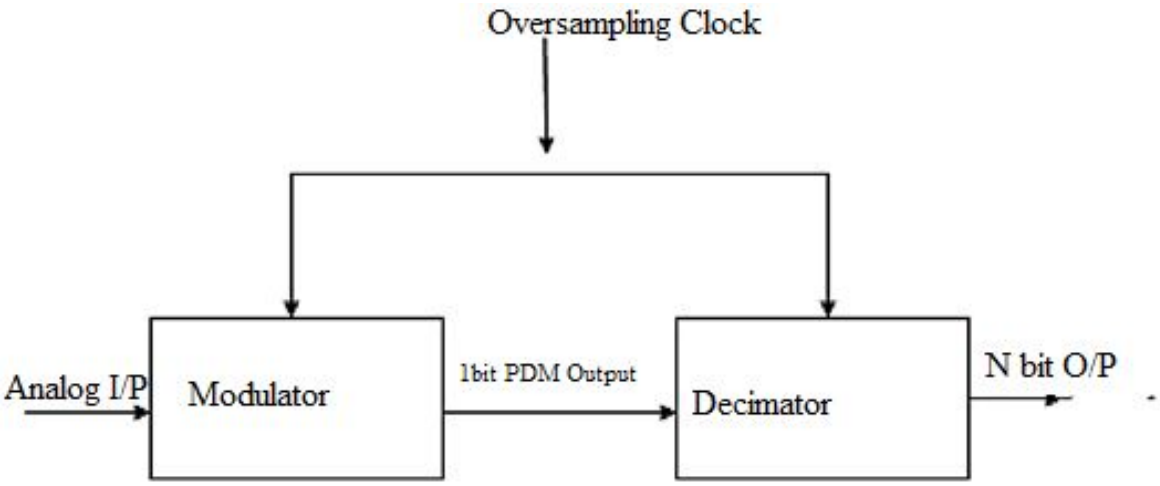

Figure 4.1: Block Diagram of Sigma Delta ADC

show deviation or small incremental change (Delta Modulation) based on quantizing the change in signal by sample to sample. The Sigma is done at the input side of the converter of the output of DAC and the input signal. Hence named sigma delta modulation. Then feedback signal from the DAC is subtracted from the input signal by the summing amplifier, and the error signal is filtered by the integrator (low pass filter). The comparator works as at oversampling clock frequency and act as quantize or ADC which compares the input signal against last sample signal value. If it is larger, output is increased otherwise decreased (Logic 1 and Logic 0). A converter needs a sampling frequency more than twice the signal frequency to reproduce the signal without distortion. The density of the pulses indicates the average value of the input, where most of the pulses are high for the positive peak of analog signal and the density of negative pulses indicate the negative peak of the signal.

(ii) Decimator:

The Decimation is the process of converting the sampling rate FN of an input signal from a given higher rate. It is a digital low pass filter which the samples rate reduction operation. The sigma-delta modulator performs the operation of noise shaping and so the noise is pushed to higher frequencies where is removed. [21]

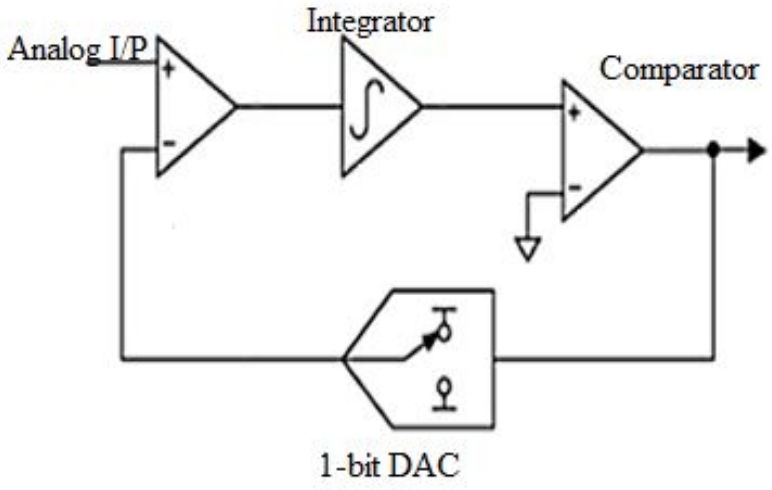

Figure 4.2: Block Diagram of Modulator

4.1.1 Performance parameters

The performance parameters for sigma delta ADCs are Quantizing Signal-to-Noise Ratio (SNR) and Dynamic Range (DR).

SNR is defined as the ratio of the signal power to baseband noise power.

DR is defined as the ratio of the power of a full-scale sinusoidal input to the power of the sinusoidal input for which SNR is one.

The expression for Signal-Noise ratio Kth order is given by

$$SNR(max) = 6.02N + 1.76 + 10log\frac{2K+1}{\pi^4} + (2K+1).10.log(OSR) \tag{4.2}$$

The Effective number of bits given by

$$ENOB = ((L{+}0.5){*}\pi){+}1, where L = order of modulator ORENOB = \frac{(SNDR - 1.76)}{6.02} \tag{4.3}$$

The Dynamic Range is defined as

$$DR(firstorder) = -3.4dB + 30logM \tag{4.4}$$

4.2 Non Overlapping Clock Generator

The circuit used to realized an integrator is a switched capacitor integrator, where four non overlapping clock pulses are required. The circuit is shown in 4.3. The NOT gate and NOR gate are designed using MOST. The switching frequency is 256KHz. The time duration is 3.9uS. The duty cycle is 50%. The simulated output clock as shown in 4.4. The aspect ratio for NMOS NOR gate 2u/1u and for PMOS it is 3u/1u. For NOT gate, aspect ratio of NMOS is 1u/1u and PMOS is 2u/1u.

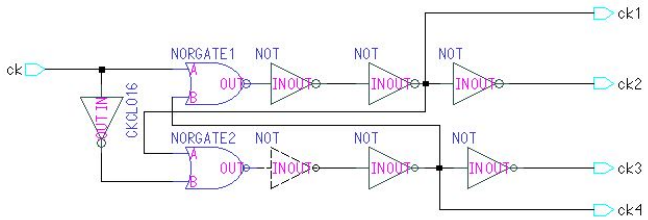

Figure 4.3: Non overlapping Clock Generator

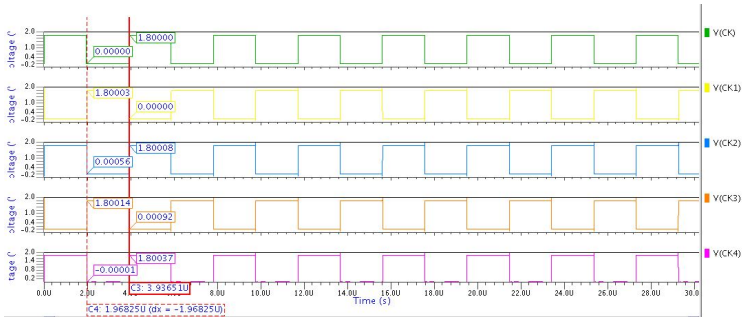

Figure 4.4: Non overlapping waveform

4.3 Switched Capacitor Integrator

The function of switching integrator circuit is to receive input signal from preamplifier and 1-bit DAC as reference signal. The difference or error signal is integrated by switched capacitor integrator.

The selection configuration for switching capacitor integrator is a parasitic insensitive module. The four switches are replaced with transmission gate for low resistance in linear region. The switching capacitor value is calculated from following equations:

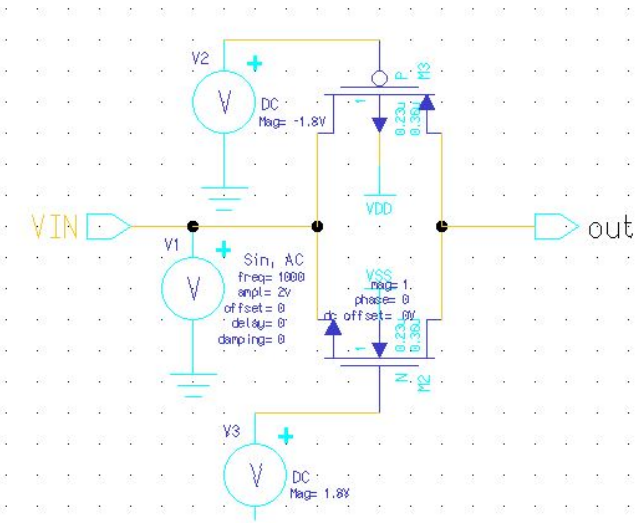

Figure 4.5: Transmission Gate

$$InputThermalNoise = \frac{K.T}{2C} = Vinrms^2 \tag{4.5}$$

$$\frac{1}{LSB} = \frac{Vinmax}{2^N} \tag{4.6}$$

$$\frac{KT}{C}.\frac{2Fb}{Fs}.\frac{1}{Vinmax^2} < \frac{1}{2}LSB \tag{4.7}$$

$$SwitchTurnONtimeV0 = [(1 - \exp(\frac{-t}{RON.C})] \tag{4.8}$$

$$RON = \frac{1}{un.Cox.W/L.(Vgs - Vth)} \tag{4.9}$$

The calculated value of Cin=Cf=1pf for unity gain and Ron=1.52K(NMOS) and 8.19K(PMOS). The Value of aspect ratio for NMOS and PMOS=W/L=0.36um/0.23um. The parasitic insensitive switching integrator is shown in Figure 4.6. The switching frequency is 256KHz and input signal is at 1KHz. The simulation of integrator is

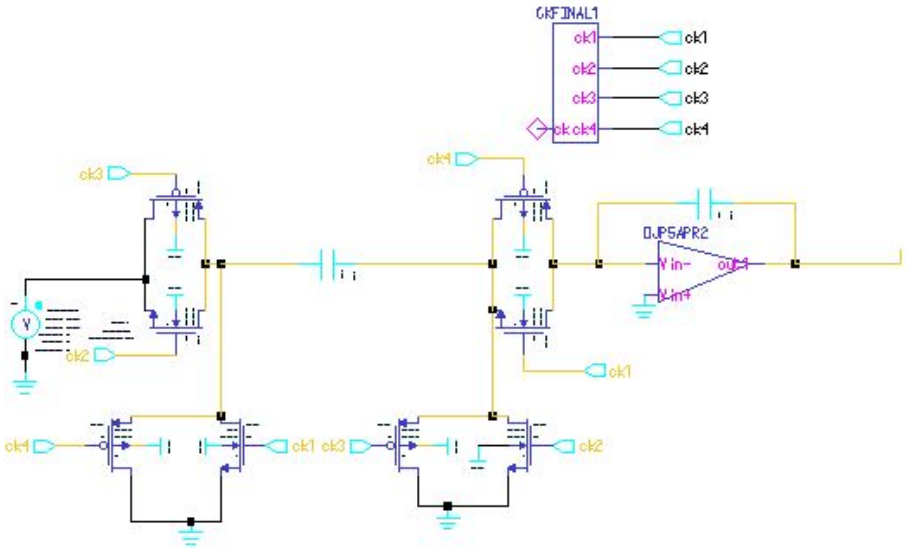

Figure 4.6: Switching Capacitor Integrator

shown in Figure 4.7 for sinwave input of 1KHz. The oversampling ratio is 128.

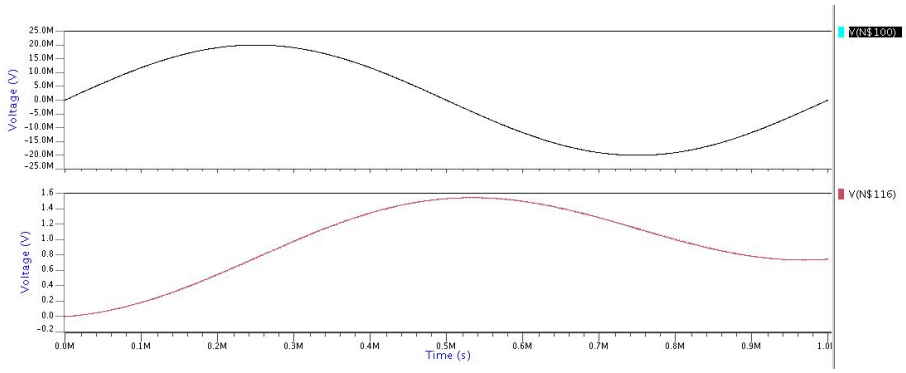

Figure 4.7: Simulation of Integrator

4.4 Comparator

A comparator is a circuit that performs the operation of comparing two analog input signals and decoding the difference in to a single digital output signal. Figure.4.8 shows the circuit diagram of comparator. By applying sine wave input signal, comparator output is switch from rail to rail supply. Figure.4.9 shows the simulation result.

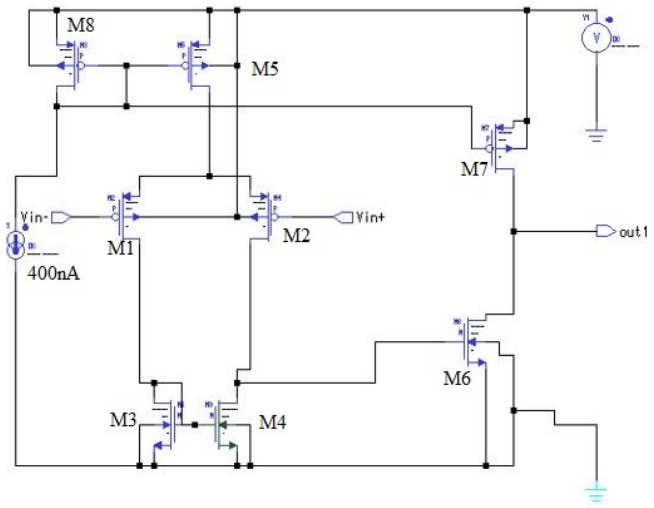

Figure 4.8: Circuit Diagram of Comparator

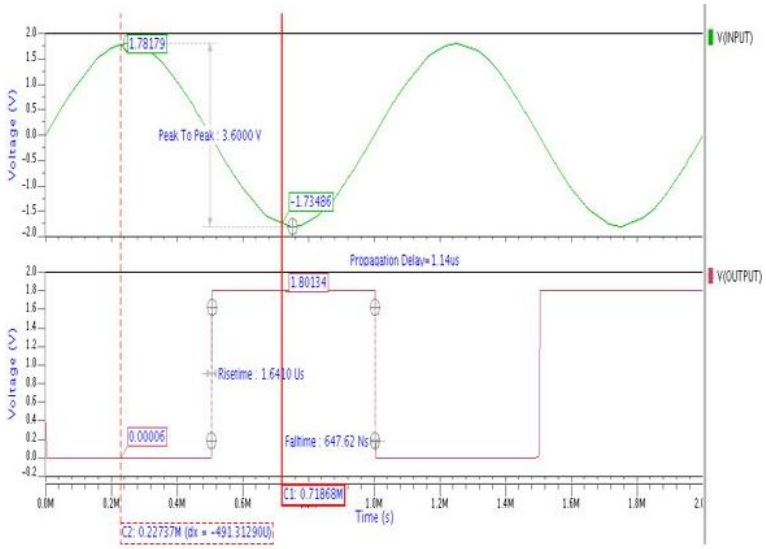

Figure 4.9: Simulation Result

The propagation delay is 1.14uS.

4.5 One -bit Digital to Analog converter

The comparator designed as a two-stage CMOS operational amplifier, will give an output of 1-bit digital input to the DAC. This DAC converts the 1-bit digital to an analog signal and fed back to the SC-integrator again as shown in the block diagram of first order modulator. Figure.4.10 shows the circuit level diagram of 1-bit DAC. The W/L ratio for NMOS is 10um/0.18um and for PMOS is 20um/0.18um. As the

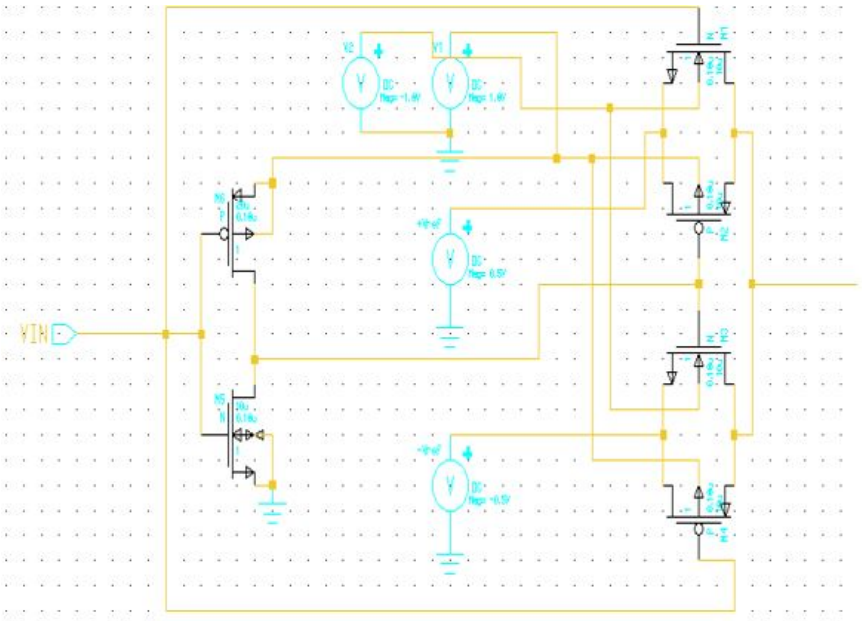

Figure 4.10: One Bit DAC

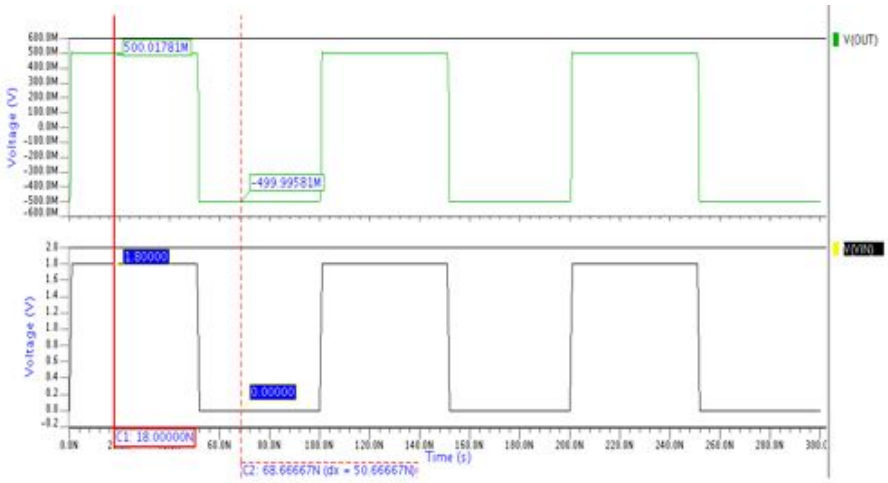

Figure 4.11: Simulation Result

number of bits is only 1-bit, the corresponding analog output will also have two levels and similar to the digital output. The present 1-bit digital-to-analog converter has two reference voltages. A positive reference voltage of +VREF and a negative reference voltage of -VREF.

Case 1: If the digital input = 1 then DAC output = +VREF

Case 2: If the digital input = 0 then DAC output = -VREF

In one bit DAC linearity is determined by the accuracy of switching between the reference signal, for high switching accuracy the system will be very linear.In the basic schematic structure of one bit DAC, the output of one of the inverters is fed as an input of the other inverter, a pulse input is given to the system and get the corresponding analog output, shown in Figure.4.11.

4.6 Simulation of Sigma Delta Modulator

The entire circuit simulation for first order sigma delta modulator is shown in Figure.4.12 for analog input of 0.3V and corresponding 1-bit output in Figure.4.13. The

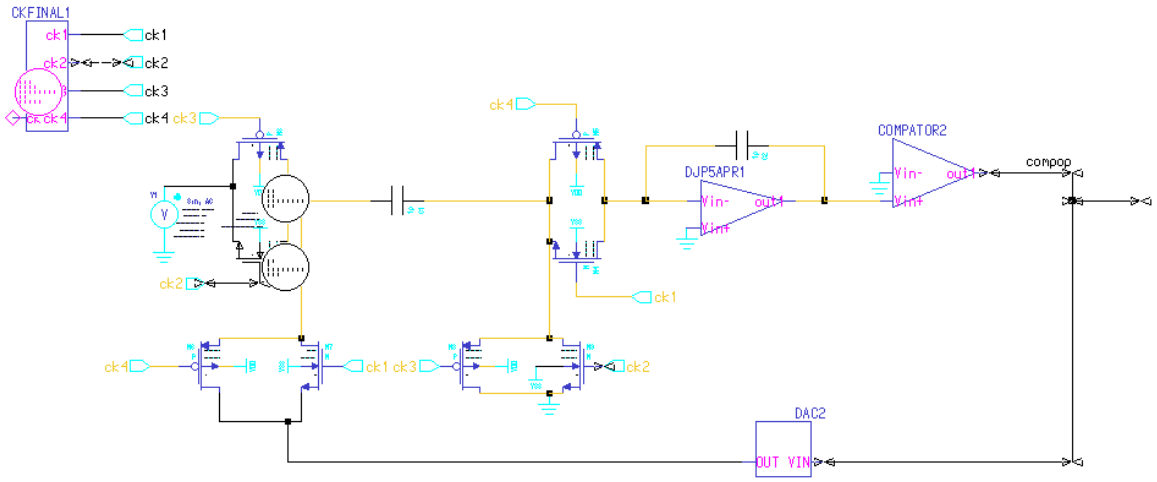

Figure 4.12: First Order Modulator

calculated value of SNR is 63dB and power dissipation is 7.30uW.The measure value of SNR from PSD plot is 43dB and SNDR is 41dB. and Effective Number of bits 6.

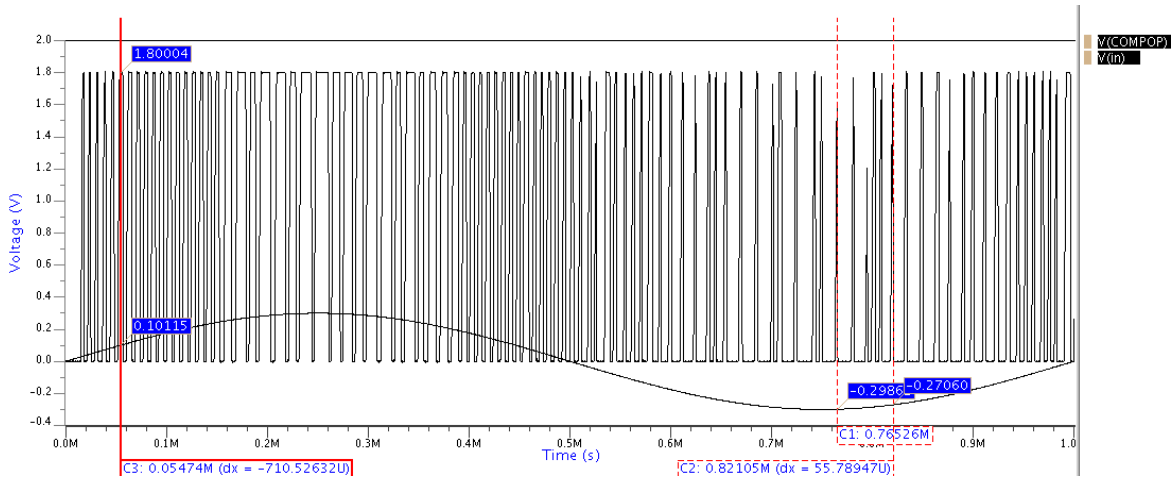

Figure 4.13: Simulation Result for First order Modulator

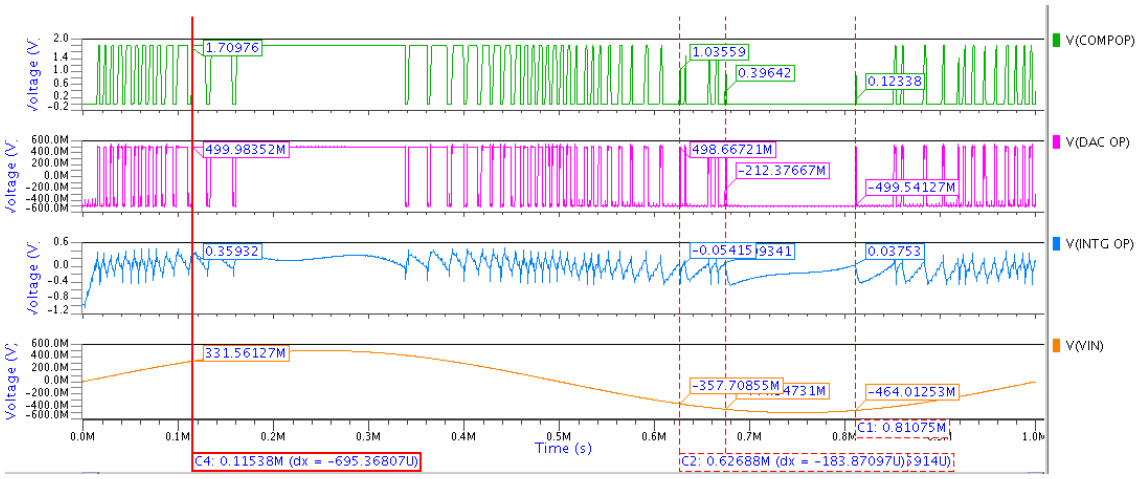

Figure 4.14: Output of Modulator

The simulation results are as shown in Table.

Table II: Simulation Results

Modulator Order	**Power Dissipation**	**SNR**
First Order	7uW	43dB

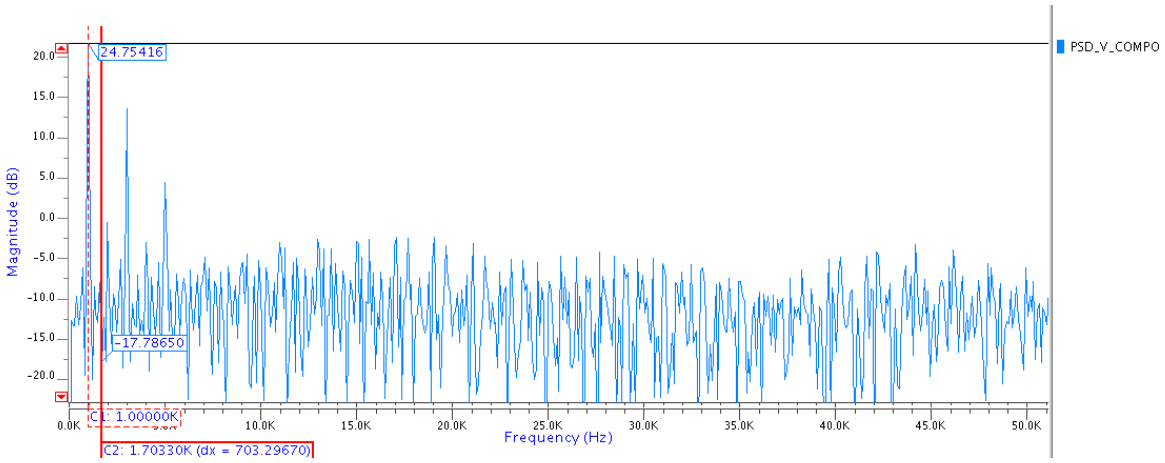

Figure 4.15: PSD plot for First Order Modulator

The comparison for various results is shown in Table.

Table III: Simulation Comparison

Parameters	**REFE 2013[31]**	**REFE 2006[11]**	**REFE 2002[32]**	**This Work**
Technology	0.13um CMOS Process	0.25um TSMC	0.6um TSMC	0.18um TSMC
Power Dissipation	36uW	38uW	297uW	7uW
Power Supply	1.2V	0.9V	3.3V	1.8V
Oversampling Ratio	128	64	64	128
Signal to Noise Ratio	79dB	72dB	75dB	43dB

The combined preamplifier and sigma delta modulator as shown that give 9uW power dissipation. The output as pulsed density waveform is shown in figure for

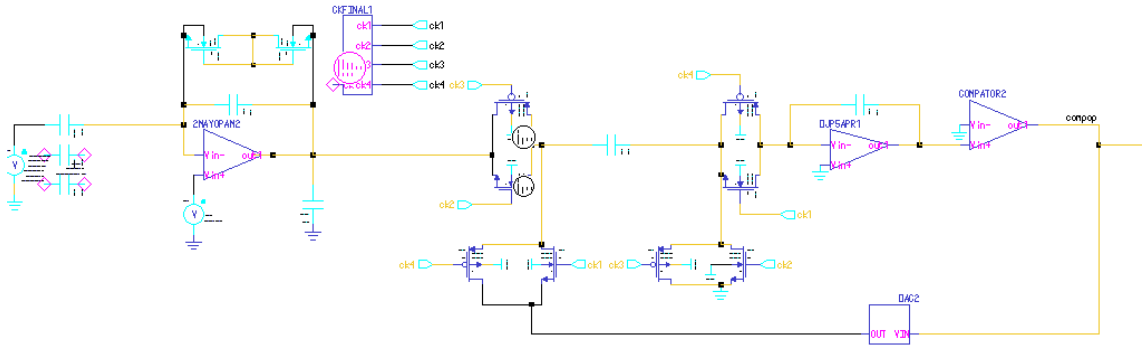

Figure 4.16: Analog Front End

90dBSPL input from microphone.

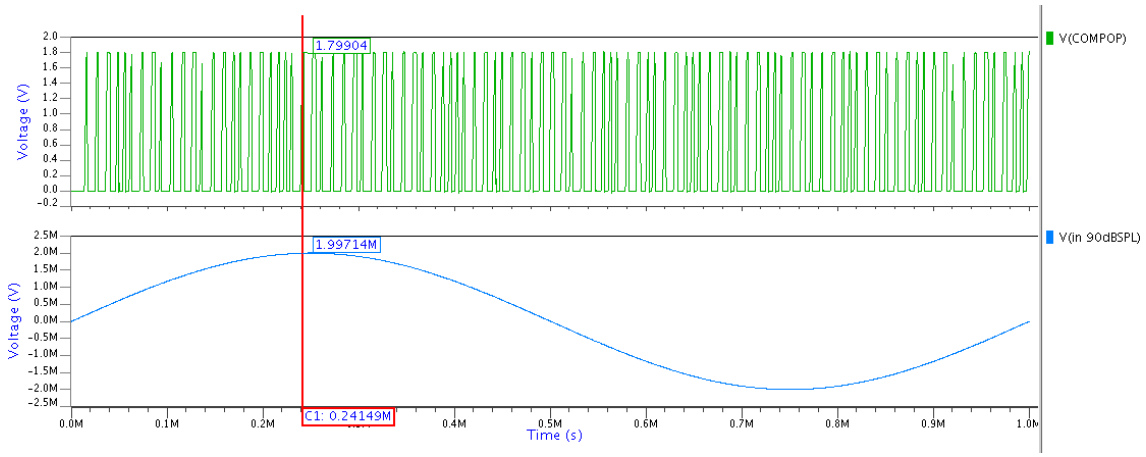

Figure 4.17: Output of analog Front End

4.7 Layout of Sigma Delta Modulator

The layout of entire first order sigma delta modulator is designed in mentor graphics with 0.18um technology.

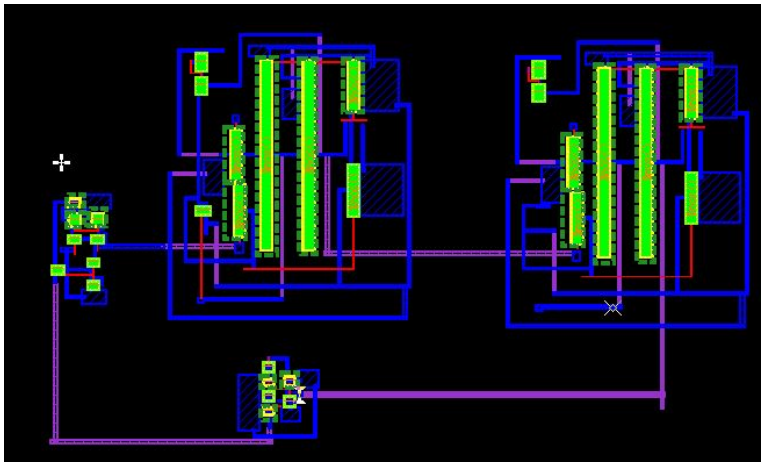

Figure 4.18: Layout of Sigma Delta Modulator

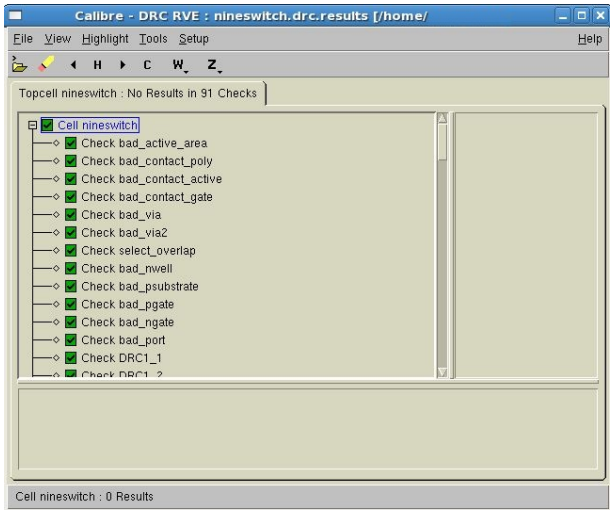

Figure 4.19: DRC Report

4.8 Summary

In this chapter, first order sigma delta modulator is designed with high value of signal to noise ratio and dynamic range. The combined total power dissipation of preamplifier and modulator is 9uW.

Chapter 5

Concluson and Future Work

In present work, literature survey is done for design and simulation of analog front end of digital hearing aid. A gm/id vs Id/W/L method is used for designing two stage miller compensated operational amplifier. Also analog front end is design as a preamplifier with variable gain control and gain is change by input capacitors. The first order sigma delta modulator is designed with low power dissipation and high value of signal to noise ratio.

In future work, optimization is required in terms of power and noise and also design of analog to digital part will be added. An Automatic Gain Control can be added to adjust value of gain according to hearing impaired person.Also multibit sigma delta adc and decimation feature can be added to improve the performance of system.

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List of Publications

[1] Dr N M Devashryee,Dr Amisha Naik,Dipesh Panchal "A Low Power Low Noise Operational Amplifier design for Biomedical Applications", *International Conference on Advances in Engineering,Technology and Science*,26th-27th April,2014,Munnar,Kerala,India.

List of Conference Attended

[1] Seventeenth International Symposium on VLSI Design and Test(VDAT 2013),July-27-30,2013,MNIT-Jaipur,India.

[2] International Conference on Engineering,NUiCONE-2013 in the track Electronics and Communication organized by Institute of Technology,Nirma University,Ahmedabad.

Appendix A

0.18um TSMC Liberary File

.MODEL

.MODEL N NMOS (LEVEL = 53

+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3725327

+K1 = 0.5933684 K2 = 2.050755E-3 K3 = 1E-3

+K3B = 4.5116437 W0 = 1E-7 NLX = 1.870758E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 1.3621338 DVT1 = 0.3845146 DVT2 = 0.0577255

+U0 = 259.5304169 UA = -1.413292E-9 UB = 2.229959E-18

+UC = 4.525942E-11 VSAT = 9.411671E4 A0 = 1.7572867

+AGS = 0.3740333 B0 = -7.087476E-9 B1 = -1E-7

+KETA = -4.331915E-3 A1 = 0 A2 = 1

+RDSW = 111.886044 PRWG = 0.5 PRWB = -0.2

+WR = 1 WINT = 0 LINT = 1.701524E-8

+XL = 0 XW = -1E-8 DWG = -1.365589E-8

+DWB = 1.045599E-8 VOFF = -0.0927546 NFACTOR = 2.4494296

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 3.175457E-3 ETAB = 3.494694E-5

+DSUB = 0.0175288 PCLM = 0.7273497 PDIBLC1 = 0.1886574

+PDIBLC2 = 2.617136E-3 PDIBLCB = -0.1 DROUT = 0.7779462

+PSCBE1 = 3.488238E10 PSCBE2 = 6.841553E-10 PVAG = 0.0162206

+DELTA = 0.01 RSH = 6.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 8.53E-10 CGSO = 8.53E-10 CGBO = 1E-12

+CJ = 9.513993E-4 PB = 0.8 MJ = 0.3773625

+CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233

+CJSWG = 3.3E-10 PBSWG = 0.8157101 MJSWG = 0.1004233

+CF = 0 PVTH0 = -8.863347E-4 PRDSW = -3.6877287

+PK2 = 3.730349E-4 WKETA = 6.284186E-3 LKETA = -0.0106193

+PU0 = 16.6114107 PUA = 6.572846E-11 PUB = 0

+PVSAT = 1.112243E3 PETA0 = 1.002968E-4 PKETA = -2.906037E-3)

.MODEL P PMOS (LEVEL = 53

+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3948389

+K1 = 0.5763529 K2 = 0.0289236 K3 = 0

+K3B = 13.8420955 W0 = 1E-6 NLX = 1.337719E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1

+U0 = 109.9762536 UA = 1.325075E-9 UB = 1.577494E-21

+UC = -1E-10 VSAT = 1.910164E5 A0 = 1.7233027

+AGS = 0.3631032 B0 = 2.336565E-7 B1 = 5.517259E-7

+KETA = 0.0217218 A1 = 0.3935816 A2 = 0.401311

+RDSW = 252.7123939 PRWG = 0.5 PRWB = 0.0158894

+WR = 1 WINT = 0 LINT = 2.718137E-8

+XL = 0 XW = -1E-8 DWG = -4.363993E-8

+DWB = 8.876273E-10 VOFF = -0.0942201 NFACTOR = 2

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.2091053 ETAB = -0.1097233

+DSUB = 1.2513945 PCLM = 2.1999615 PDIBLC1 = 1.238047E-3

+PDIBLC2 = 0.0402861 PDIBLCB = -1E-3 DROUT = 0

+PSCBE1 = 1.034924E10 PSCBE2 = 2.991339E-9 PVAG = 15

+DELTA = 0.01 RSH = 7.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 6.28E-10 CGSO = 6.28E-10 CGBO = 1E-12

+CJ = 1.160855E-3 PB = 0.8484374 MJ = 0.4079216

+CJSW = 2.306564E-10 PBSW = 0.842712 MJSW = 0.3673317

+CJSWG = 4.22E-10 PBSWG = 0.842712 MJSWG = 0.3673317

+CF = 0 PVTH0 = 2.619929E-3 PRDSW = 1.0634509

+PK2 = 1.940657E-3 WKETA = 0.0355444 LKETA = -3.037019E-3

+PU0 = -1.0227548 PUA = -4.36707E-11 PUB = 1E-21

+PVSAT = -50 PETA0 = 1E-4 PKETA = -5.167295E-3)

.END

List of Publications

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