

RS-LDPC Product Code for High SNR Applications

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Abstract: Product code is a promising technique for low as well as high SNR applications due to its superior error correction performance. Indoor video broadcasting is an application where distance between transmitter and receiver is less, hence the received SNR is high. For such an application and similar applications tolerant to high BER, in this paper, we propose a Low Density Parity Check-Reed Solomon (LDPC-RS) product code structure using Bit Flipping algorithm for decoding of LDPC code. For LDPC decoding, bit flipping is preferred over log SPA (Sum Product Algorithm) as it offers lesser hardware and computational complexity. Simulation results for our product code show great error performance in high SNR regions.

Index Terms: bit flipping algorithm, hard decision decoding, LDPC, log-SPA decoding, product codes, RS, soft decision decoding.

I. INTRODUCTION

Channel coding which forms a vital part of the communication systems; use Error Correcting codes for error detection and correction. Error correcting code is an algorithm for expressing information in a pattern such that the errors caused by channel noise, noise added by transmitter or receiver; can be detected as well as corrected. The types of Error correcting codes are convolutional, LDPC, RS, OVFSF, etc. Convolutional codes have numerous applications such as reliable data transfer in digital video, mobile systems, etc., due to their trellis structure which allows the efficient implementation of maximum likelihood decoding algorithms [1]. However, an (n, k, m) conventional trellis module contains n^{2m+k} edge symbols, and this is called the trellis complexity TC of the module (usually it is normalized by k) [2]. It is known that the maximum likelihood decoding complexity is proportional to the trellis complexity of the module that is used for decoding [1]. Low-density parity check (LDPC) codes can provide remarkable performance which is very close to the Shannon limit and are among the best candidates for error control in systems where high reliability and efficiency is needed [3]. This property comes with complex encoders and poor performance for short length [4]. An (n, k) RS code can detect any combination of up to $(n-k)$ erroneous symbols (m -bit wise) and correct up to $(n-k)/2$ of them, where $(n-k)/2$ is

called the RS code's error-correction capability [3]. This property of RS codes makes it robust against burst errors. The only disadvantage of RS codes lies in the lack of an efficient maximum likelihood soft-decision decoding algorithm. The difficulty in finding such an algorithm is in part due to the mismatch between the algebraic structure of a Galois field and the real numbers at the output of the receiver demodulator [5]. Apart from above features, all the applications in the communication industry demand high FEC i.e. excellent error correction performance over noisy channel, less power consumption, higher data rates and throughput with less latency. Merging two codes for improved error correction gives the concept of *product code*. Product code is a promising technique, which covers the strong features of two different codes and tries to eliminate the weaker aspects of individual codes. First introduced in 1954 [3], Product code offers remarkable error correction performance, reliability of transmission and robustness against noise even at higher data rates. Various product code types include RS- convolutional, LDPC-convolutional, RS-LDPC, etc. Rate-compatible protograph-based LDPC codes were considered in [6] and [7]. In [6], they were built by expurgation and lengthening. However, the codes are only available for rates higher than 1/2. Considering the complexity offered by encoding and decoding of convolutional code, we have concatenated RS-LDPC codes as the product code.

The paper focuses on RS-LDPC product code, which offers remarkable error correction performance for both random as well as burst errors. LDPC codes provide clean channel for RS codes [5]. LDPC code has a low computational complexity, which has a linear relationship with the code length and sets a few requests on the hardware; while for RS codes there is an exponential relationship between computational complexity and code length. Also, for RS codes, the maximum error correction capacity is only 30%. LDPC codes have been demonstrated to perform very close to the Shannon limit when decoded iteratively using message-passing algorithms [8].

Using product codes may introduce benefits in the following aspects: (1) The LDPC-RS product code is an interleaved version of serial concatenated code, thus it may have advantages in burst error cases which are quite normal in mobile channels [3]; (2) Other than inflexible decoding order of ‘inner coder-out coder’, we can adopt different strategies of decoding in product code cases based upon the received signal SNR: at high SNRs decoder complexity can be reduced. In our paper, we have analyzed that soft and hard decision decoders perform identically for LDPC codes.

Although having remarkable error correction performance, LDPC-RS product code risks introducing relatively high decoding complexity due to its iterative decoding feature and high system latency since traditional decoding (LDPC+RS decoding) cannot be carried out until one entire code block is successfully received [9]. In our paper we emphasize on reducing the decoding complexity when the received SNR is high. Our analysis is based on the effectiveness of hard decision decoding at high SNR. Some of the applications of the product codes are:

1. Commercially, for the DVB-S2 system, (64800, 32400) LDPC code and the (30, 10) short RS code over $GF(2^8)$ has been tried to construct the LDPC-RS product code. It includes the log-SPA LDPC decoding concatenated by RS hard-decision decoding to test for the decoding gain that the RS component can bring. Experiments show that the decoding gain of the concatenated RS hard-decision decoding is about 0.05dB. The steep waterfall region of the (64800, 32400) DVB-S2 LDPC code can explain the limited contribution of the concatenated RS hard-decision decoding [3].
2. The product code structure is often considered a powerful tool for constructing long code word using relatively short component codes and for combating mixed types of errors (random and burst errors).
3. Product code is a promising technique for the next generation digital terrestrial broadcasting transmission system [3]. Meanwhile, terrestrial broadcasting has its own unique need to exist for services such as news, entertainment, and especially as a national emergency public safety service to provide information to the general public under natural disaster situations (tsunami, earthquake, flood, tornado, forest fire, etc.). Thus we need to keep the terrestrial broadcasting and at the same time improve its spectrum efficiency. For this reason, a new robust transmission system- Cloud Transmission (Cloud Txn) [10] has been proposed for terrestrial broad-casting or point-to-multipoint services [3].
4. Product Codes which inherently integrate interleaving into error control, offers a powerful error-correction method for scenarios where a large interleaver for

correcting mixed types of errors is demanded. For example, Turbo Product Code [11] has already been adopted in OFDM based IEEE 802.16 standard [3].

5. It is also widely used in cooperative network coding scheme, satellite communication standards and digital storage systems.
6. In case of DTV broadcasting system, which does not have strict demand of small latency, by using product code structure more time can be saved as interleaver/deinterleaver modules need not be exploited [3].
7. If negative AWGN SNR decoding threshold is considered it is very robust against co-channel interference, thus offering a promising solution for future broadcasting system [3].

The rest of the paper is organized as follows: Section II briefly reviews the structure of LDPC-RS product codes. Section III details the proposed encoding and decoding scheme. Section IV explains the algorithm for the proposed code and the corresponding Bit Flipping LDPC decoding algorithm. Section V reports the simulation results and analysis. Finally, section VI concludes the whole paper.

II. PRODUCT CODE STRUCTURE

In our implementation of product code, the message is first LDPC encoded followed by RS encoding over Galois field. The codeword is sent over an AWGN channel after BPSK modulation. The codeword is decoded using RS hard decision decoder first, then sent over LDPC Bit Flipping algorithm. The inner LDPC code performs well in combating short random errors. The outer RS code has dual duties: first, it is efficient against burst errors since a sequence of $m+1$ consecutive bit errors can affect at most two RS symbols of size m ; second, the inner LDPC iteration can be terminated as long as the number of residue erroneous symbols is within the outer RS’s capability. Thus the outer code can reduce the inner LDPC iteration number [3]. Moreover, we propose a preliminary decoding scheme which can be applied on high SNR applications. Fig. 1 shows the LDPC-RS product coding scheme.

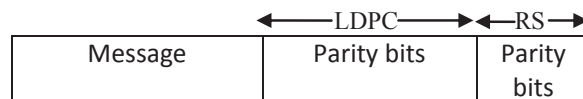


Fig. 1. LDPC-RS product code

Consider the LDPC-RS product code where LDPC follows structure of (N_1, K_1, M_1) and RS code follows $(N_2, K_2, 2t)$ over $GF(2^m)$, where $2t = N_2 - K_2$ and $M_1 = N_1 - K_1$. K_1 is the original message length to which M_1 parity bits are added using LDPC encoding to give N_1 length codeword. (N_1, K_1, M_1) acts as a message for RS encoding, giving $(N_2, K_2, 2t)$; where K_2 is the length of message, $2t$ are the parity bits added

during RS encoding and N_2 is the length of final codeword formed by product code and sent over AWGN channel. Its code rate R is given by $R = N_2 / K_1$.

Encoding

To a message of length K_1 , LDPC encoding is done by adding M_1 parity bits such that N_1 length codeword is formed. M_1 parity bits are generated using parity check matrix H . Matrix H is a sparse matrix which is randomly generated using predefined parity xor equations mutually agreed upon by the transmitter and the receiver. The H matrix used in our scheme has equal row weight, hence is a regular LDPC [12].

The LDPC encoded message is then converted to Galois field of (2^m) . The parity check information for RS code is obtained using the generator polynomial with roots from $GF(2^m)$ [13]. For algorithm see Fig. 2.

Hard Decision Decoding

At the receiver side, first of all RS Hard-decision decoding is used. Although a soft RS decoder will certainly improve the performance, the computational complexity offered is too high [3]. The LDPC hard-decision decoding following RS decoding, helps correct some (if not all) residual errors after RS decoding. LDPC decoding can be done using either of hard-decision or soft decision decoding. Log-SPA owns the best error performance and can also process soft information; whereas Weighted Bit Flipping (WBF) Algorithm is based on the estimation of the erroneous bit locations and process hard information. Hard decision decoding for binary erasure channels (BEC) has very low complexity and its decodability is predictable given the positions of uncertain (erased) bits [14]. For algorithm see Fig. 2.

We have considered WBF algorithm over log-SPA as WBF algorithm and its variants are very effective in terms of the tradeoff between error performance and decoding complexity [14]. Added after RS decoding, this algorithm further improves the error performance and owns a much lower computational complexity compared to log-SPA. The advantages offered by less complex decoder hardware include fast response time, flexibility of changes in hardware when required and rapid development. Hardware requirement of log-SPA in terms of memory is more as compared to WBF. Hence, for applications tolerant to high BER or having high received SNR, WBF is more suitable. Considering indoor application like video transfer where distance of transmission is less and SNR at receiver is high, log-SPA and WBF show similar results (see Fig. 3(a), 3(b)). In such application WBF is preferred, considering the reduced hardware complexity.

III. ALGORITHM

The bit flipping algorithm is a hard decision algorithm which deals with simple messages, where a variable node sends a message to a check node with a value of 1 or 0, then check nodes send a message to its connected variable nodes with a value of 1 or 0 declaring if it is satisfied or not [13].

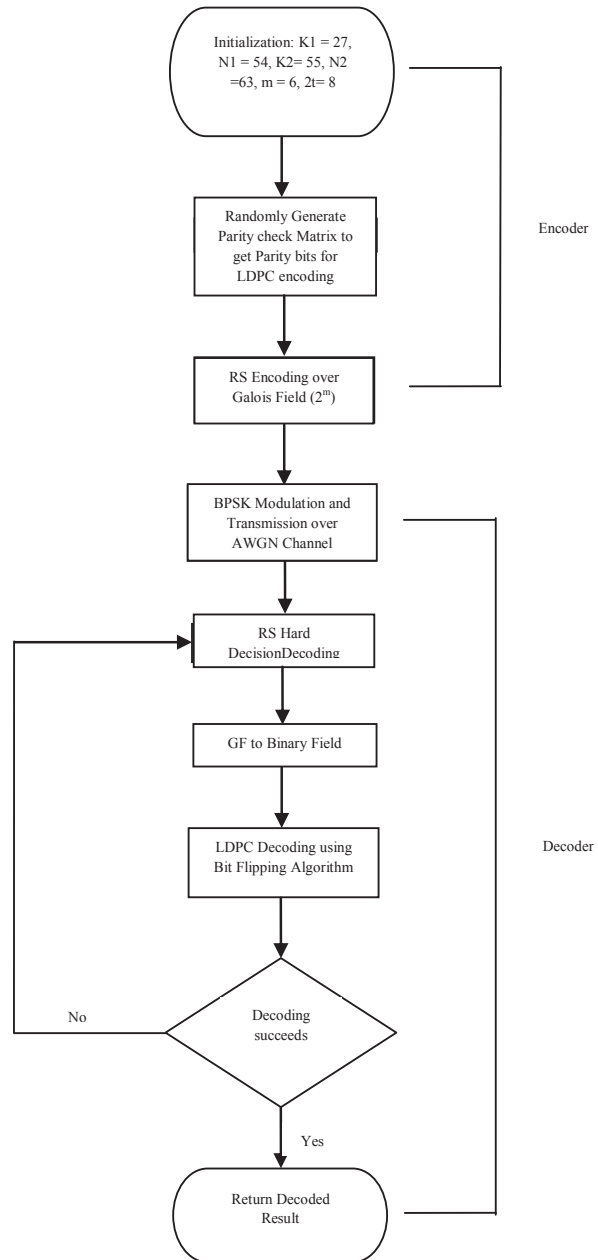


Fig. 2 Flow chart of complete encoding as well as decoding

Steps of Bit Flipping Algorithm are:

1. Initialization: Variable nodes are assigned corresponding bit values from the received vector, and these values are sent as messages to the check nodes connected with each variable node.
2. Check Nodes Update: Each check node calculates response for each variable node connected, assuming other bits are correct and sends a value that result with a sum of 0 to satisfy the parity check equations. If all the equations are satisfied the algorithm terminates.
3. Bit Update: The variable nodes receive values from check nodes and determine if the original received bit is correct, depending on the majority voting of values, received from check nodes. This process is repeated until all parity check equations are satisfied or until number of suggested iterations is reached. If maximum number of iterations is reached, the algorithm terminates and declares failure to converge. It is to be noted that the design of LDPC sparse H matrix ensures existence of one or no transmission error in each parity check equation [12].

IV. SIMULATION RESULTS AND ANALYSIS

We first examine the performance of the proposed code structure for fixed rate LDPC-RS product code. In our simulation, the LDPC component is the (27, 54) code as used in the IEEE 802.11n standard [15] and we use (63, 55) RS code over GF (2⁶). We run simulation for 1000 blocks of such product code. For LDPC the encoding rate is assumed to be 0.5. The code is sent over an AWGN channel after BPSK modulation. The error performance obtained at high SNR, ranges from 10⁻³ to 10⁻⁵.

TABLE I [3]
DECODING COMPLEXITY ANALYSIS

Method	Operation	Number	Average CPU Runtime
SPA	Phi-function ¹	1536 per iteration	0.2sec per iteration
	Real-addition	4320 per iteration	
WBF	Real-addition	1824 per iteration	0.03 sec per iteration
	Comparison	2784 per code	

¹ phi-function is defined as $\phi(x) = \log_2\left(\frac{e^x + 1}{e^x - 1}\right)$.

Seen from the Table I [3], the computational complexity of one WBF iteration is much lower as compared to one SPA iteration. The average CPU runtime (counted over 8.3e5 LDPC columns at each SNR point) varies little with channel conditions and further verifies that the implementation

complexity of WBF is also much lower than log-SPA (assuming DSP implementation). Consequently, by replacing a certain number of log-SPA iterations with a comparable number of WBF iterations, we can reduce the overall complexity. Simulation results for the proposed code structure show that the error performance obtained is comparable to that obtained in [3]. Hence when applications have high received SNR, proposed code structure, which uses Bit flipping for decoding of LDPC codes, can be preferred as it offers less hardware decoding complexity than decoding used in [3].

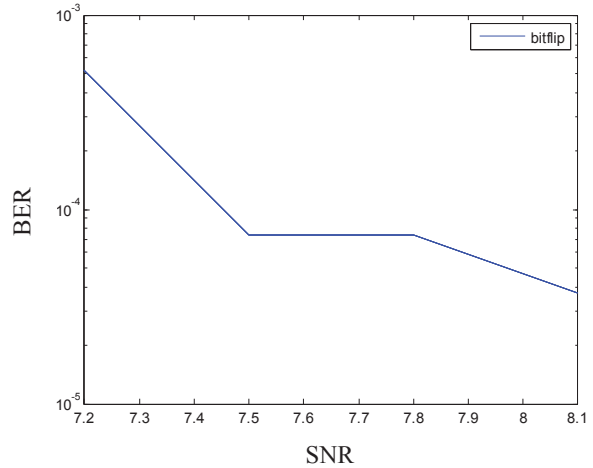


Fig. 3(a) BER vs SNR curve for Bit Flipping Decoding

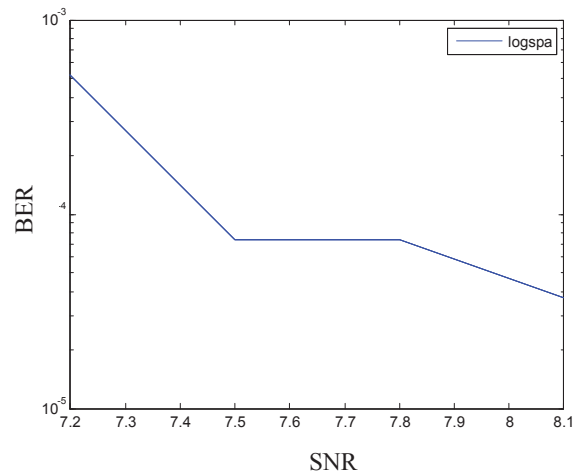


Fig. 3(b) BER vs SNR curve for log SPA Decoding

Discussions of Longer LDPC Code Length

In the above simulations, we mainly consider the short length LDPC codes. The main concern using long LDPC

component code in LDPC-RS product code structure is the problem of long delay due to amazing size of the code block.

Two possible solutions may deal with this problem: to fold the long LDPC code or to use relatively short RS component code. First, we try to apply the folding technique which folds each long LDPC code column to construct the LDPC-RS product code structure in order to reduce the block size. However, we have found mathematically that the folding technique makes the “product property” lost. Given that the “product property” is essential to our decoding scheme, we need to turn to the second solution: to use relatively short RS component code [3].

V. CONCLUSION AND FUTURE WORK

In this paper, we have discussed the LDPC-RS product code which could provide robustness and superior error correction performance for the systems having high SNR or tolerant to high BER. Compared to the simple concatenation of log-SPA and RS hard decision decoding, using WBF scheme reduces hardware complexity and provides sensible tradeoff between error performance and computational complexity. Therefore, we can expect the proposed scheme to be very competitive for the design of LDPC-RS product code decoders. Improving the WBF flipping methods may offer more accurate error estimation with lower complexity and increasing the LDPC encoding rate which is presently 0.5. Implementing low-complexity RS soft decision decoders into the decoding scheme is also of great interest, since we can realize a turbo decoding scheme to further improve the error performance and to get a smoother BER vs SNR curve.

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