WLAN RF and Power Consumption Characterization

Major Project Report

Submitted in partial fulfillment of the requirements
for the degree of

Master of Technology
in
Electronics & Communication Engineering
(Embedded Systems)

By

Eeshan Pujari
(13MECE14)

Electronics & Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
Nirma University
Ahmedabad-382 481

May 2015

WLAN RF and Power Consumption Characterization

Major Project Report

Submitted in partial fulfillment of the requirements
for the degree of

Master of Technology
in
Electronics & Communication Engineering
(Embedded Systems)

By

Eeshan Pujari
(13MECE14)

Under the guidance of

External Project Guide:

Mr. Anilkumar Maligi
Manager,
WLAN Hardware Development Engineering,
Broadcom Communication Technologies Pvt. Ltd.,
Bangalore.

Internal Project Guide:

Dr. Tanish Zaveri
Associate Professor,
EC Branch, EE Department,
Institute of Technology,
Nirma University, Ahmedabad.

Electronics & Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
Nirma University
Ahmedabad-382 481

May 2015

Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in Embedded Systems at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Eeshan Pujari
13MECE14

Disclaimer

"The content of this project report does not represent the technology, opinions, beliefs or positions of Broadcom Communication Technologies Pvt. Ltd., its employees, vendors, customers, or associates."

Certificate

This is to certify that the Major Project entitled **"WLAN RF and Power Consumption Characterization "** submitted by **Eeshan P. Pujari (13MECE14)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in Embedded Systems, Nirma University, Ahmadabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this major project, to the best of our knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

Date: Place: Ahmedabad

Dr. Tanish Zaveri
Internal Guide

Dr. N.P. Gajjar
Program Coordinator

Dr. D.K.Kothari
Section Head, EC

Dr. P.N.Tekwani
Head of EE Dept.

Dr. K. Kotecha
Director, IT

Certificate

This is to certify that the Major Project entitled **"WLAN RF and Power Consumption Characterization"** submitted by **Eeshan P. Pujari (13MECE14)** , towards the partial fulfillment of the requirements for the degree of Master of Technology in Embedded Systems, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

Date: Place: Bangalore

Mr. Anilkumar Maligi
Manager, WLAN Hardware Development Engineering,
Broadcom Communication Technologies Pvt. Ltd.,
Bangalore.

Acknowledgements

I would like to express my gratitude and sincere thanks to **Dr. P.N.Tekwani**, Head of Electrical Engineering Department, and **Dr. N.P.Gajjar**, PG Coordinator of M.Tech Embedded Systems program for allowing me to undertake this thesis work and for his guidelines during the review process.

I take this opportunity to express my profound gratitude and deep regards to **Dr. Tanish Zaveri**, guide of my major project for his exemplary guidance, monitoring and constant encouragement throughout the course of this thesis. The blessing, help and guidance given by him time to time shall carry me a long way in the journey of life on which I am about to embark.

I would take this opportunity to express a deep sense of gratitude to my Project Manager **Mr. Anilkumar Maligi**, Manager and Mentor **Mr. Lakshminarayana Modur**, Principal Engineer of WLAN Hardware Development Engineering, Broadcom Communication Technologies Pvt Ltd. for their cordial support, constant supervision as well as for providing valuable information regarding the project, which helped me in completing this task through various stages.I would also thank to **Mr. Ameen Junaid WH**, **Mr. Harish Reddy**, **Mr. Rajendra Yogaraj**, **Mr. Fagun Pathak** and my intern friends, **Darshan Shah**, **Miral Kotadia**, **Kapil Inchure**; for always giving good suggestions and solving my doubts to complete my project in better way.

Lastly, I thank almighty, my parents and friends for their constant encouragement without which this assignment would not be possible. In particular, I would like to give my sincere thanks to my two classmates, **Jay Shukla** and **Harsh Kotak**, for their help during crucial period of final report making.

- Eeshan Prasad Pujari
13MECE14

Abstract

WLAN chips are used in laptops, mobiles and various other portable market devices. As these WiFi chips are mainly manufactured for portable devices and battery life is prime issue in these devices, testing and analyzing the chip for its power consumption is one of the necessary task during bring-up. The work in this report is mainly related to this power consumption side of the chip. The task of current measurement is performed for various test cases on variety of chip packages and at varied temperatures. Using automated current method of current measurement (CM), various quantitative and qualitative analysis are performed.

Various practical issues faced while doing current measurement, crystal tuning are solved by understanding fundamental reasons behind them. Working principle of transmit power control (TPC) is analysed and explored during debugging process. Some of the practical challenges faced during automation of current measurement setup like interfacing of instruments and measurement accuracy, are explained with proper reasoning and solutions.

Apart from current measurement and debugging, various RF performance related tests are carried out to check various RF parameters of chip like EVM, Rx Sensitivity, Harmonic Distortion etc. Depending upon simulation results generated by these tests, it is verified that customers'specifications are met or not. If not met, respective teams are informed to take corrective actions.

Contents

List of Tables

List of Figures

Abbreviations

WLAN ..... Wireless Local Area Network

EVM ..... Error Vector Magnitude

CM ..... Current Measurement

LDO ..... Low Drop-out

PER ..... Packet Error Rate

AP ..... Access Point

MIMO ..... Multiple Inputs Multiple Outputs

LNA ..... Low Noise Amplifier

PA ..... Power Amplifier

LO ..... Local Oscillator

VCO ..... Voltage-controlled Oscillator

DUT ..... Device Under Test

PAPR ..... Peak-to-Average Power Ratio

NF ..... Noise Figure

SNR ..... Signal-to-Noise Ratio

ATE ..... Automated Test Equipment

ENR ..... Excess Noise Ratio

RF ..... Radio Frequency

Chapter 1

Introduction

1.1 Overview

In today's world of modern radio transceivers, estimated testing cost covers significant portion of manufacturing cost and its portion is escalating with every new generation of RF chips [9]. Any chip after designing does not go to market directly. It is first tested in lab for its performance. Time-to-market of chip mainly depend on time required for testing. If the testing process is sophisticated and giving minute details regarding various parameters in moderate time and efforts, then time of testing process gets reduced and in turn, time-to-market also.

This project is based on testing of WLAN chip for its various RF related performance parameters and power consumption. Results generated from these various tests are analysed to check if customers are being satisfied or not. If results are not in expected range, then various sources of problems are debugged. One of the first sources being suspected is improper measurement setup. There are some issues which are analysed using the current measurement setup to know which part of chip is consuming current more than expected and then that problem is debugged in that direction.

In this project, major portion is dedicated to Current Measurement which, in turn, gives information regarding power consumption of Wi-Fi chip. Current measurement (CM) related information like procedure of CM, practical issues related to it, their solutions, analysis at very fundamental level are included under power consumption characterization. Some of the challenges tackled during automation of this CM setup is also discussed. Apart from this, thermal problem which is straight effect of current consumption of chip is also addressed and analyzed with experiments.

Some RF parameters also affect CM. Their analysis through various RF related test and results is presented along with comparison of their various methods of measurements.

1.2 Motivation

WLAN means Wireless LAN, which itself makes it clear that it consists of one or more than one Access Points (APs) that connect to remote client devices which can be AP through wireless links and/or to any other wired network. Remote devices can be laptops or cell-phones with WLAN cards (WLAN chip + interface to host) installed. APs are generally stationary and most of the time are wall-powered supplied; whereas remote devices are battery operated. The topic of power consumption discussed in this thesis, is mainly focused on investigating the WLAN chip's (which is installed in remote devices) energy efficiency [10].

Battery life is ultimately determined by the power consumed by entire portable device platform like mobile phone. Power consumption by whole platform is nothing but some of power consumed by CPU, memory, display, I/O bus etc.

When WLAN chip is placed inside the remote device, power consumption of interfacing system to the host increases because of following two reasons:

1. WLAN chip itself consumes additional power
2. Interface platform also consumes additional power

As WLAN chip manufacturer, main focus is on first part of above two reasons. So, to know actual power consumed by chip, quantitative analysis is must. This is the basic motivation behind power consumption characterization through method of current measurement. Some RF tests, which affect CM, are also analysed. With power consumption, there comes direct problem of heat dissipation. This leads to thermal related issues, which are also pointed out in this project.

1.3 Problem Statement

Current measurement when WLAN chip is in various states like:

1. **Off state:** WLAN chip is completely switched off.

2. **Sleep state:** Most of parts of circuit remains off, except some critical parts.
3. **Listen State:** Radio section of WLAN chip waiting for packets, but receiving nothing.
4. **Receive State:** Receiving and decoding packets
5. **Transmit State:** Modulating and sending packets

Main aim is measuring currents at various ambient temperatures in above mentioned states and with various optimization settings; analysing the gathered data and checking its correctness; debugging the problems faced during Current measurement. Apart from current measurement, performing RF test like EVM, Sensitivity etc. and various experiments like thermal analysis and effect of air-circulation.

1.4 Thesis Outline

The rest of the thesis is organized is as follows:

Chapter 2, *Literature survey*, describes the various standards of WLAN in brief along with their comparison. General transceiver block diagram is explained in brief. Basics of voltage regulator, simple comparison between switching and linear regulator and various traditional methods of current measurements are discussed.

Chapter 3, *Power Consumption Characterization*, presents basic power topology of any WLAN chip, importance of digital loads in WLAN chip, theoretical and actual way measuring currents, issues related to setup and their solutions. Along with this, thermal problem is also addressed.

Chapter 4, *RF Performance Characterization*, describes various methods of measuring tx and rx parameters of WLAN chip along with their results and inferences.

Chapter 5, *Debug Issues*, describes various issues faced during bring-up of WLAN chip and methods of debugging it along with relevent results and inferences.

Finally, **In Chapter 6**, *Conclusion and Scope* for future scope are presented.

Chapter 2

Literature Survey

2.1 Study of various WLAN standards

In recent years, design of low cost multi-standard mobile devices has gone through shift from technical aspiration to the commercial reality. Usually, the emerging wireless applications are based on new and latest wireless standards. In perspective of radio frequency, these standards differ in operating frequency band, sensitivity, data rate, bandwidth, and modulation type [9].

In 1990, the IEEE 802 executive committee established the 802.11 working group to create a WLAN standard. The standard specified an operating frequency in the 2.4-GHz ISM (industrial, scientific, and medical) band. The standard supports about 1 to 2 Mbps data rates. But after that the need for or requirement of higher data rates increased which, in turn, lead to the invention of more and more WLAN standards. The working group approved two project authorization requests for higher rate physical (PHY) layer extensions to 802.11. The two extensions were IEEE 802.11a5 GHz and the other IEEE 802.11b 2.4 GHz. This first version of the standard operates at the 2.4-GHz ISM band and it supports two modulation schemes direct sequence spread spectrum (DSSS) and a frequency hopping spread spectrum (FHSS) implementations. 802.11b is a PHY extension to the original 802.11 standard. It also operates at the 2.40-GHz band and allows for higher data rates of 5.5 and 11 Mbps. It uses a technique known as complementary code keying (CCK). The 802.11a is another PHY extension to the 802.11 standard. It operates at the 5-GHz unlicensed national infrastructure for information (UNII) band and allows for data rates of 654 Mbps. It uses a technique known as orthogonal frequency division multiplexing. The 802.11g was the next extension to the 802.11 standard. It operates at the 2.4-GHz ISM band and allows for data rates ranging from 1 to 54 Mbps. The 1- and 2-Mbps rates are operated in the DSSS mode whereas the 512

and 11-Mbps rates are operated in CCK mode. Additionally, rates at 6 to 54 Mbps are operated in OFDM mode. The 802.11g standard borrows the OFDM technique and data rates from the 802.11a standard but operates at the 2.4-GHz ISM band. It can therefore operate at very high data rates while being backward compatible with the 802.11b standard.

Comparison of 802.11: b, a, g, n & ac :

Table 2.1: Comparison of IEEE Standards

Standard	**Frequency Band**	**Modulation Scheme**	**Data Rate (Mbps)**
802.11	2.4 GHz	DSSS, FHSS	1,2
802.11b	2.4 GHz	CCK	5.5, 11
802.11a	5 GHz	OFDM	6 to 54
802.11g	2.4 GHz	DSSS+CCK+OFDM	1 to 54
802.11n	2.4 + 5 GHz	OFDM	Up to 600
802.11ac	5 GHz	OFDM	Up to 6.933

Increase in rate over 802.11a/g can be achieved in IEEE standard 802.11n. This can be achieved through wider signal bandwidth of 40 MHz, MIMO implementation and higher coding rates. The signal is modulated using OFDM modulation scheme. It uses 77 Modulation and Coding Schemes (MCSs). Up to 600 Mbps data rate can be achieved.

Standard IEEE 802.11ac incorporates MIMO mode configurations, where we have multiple antennas on transmitter and receiver side (2x2 or higher). The total band of emission is 160 MHz, where each antenna emits in 80 MHz band for 2x2 mode. High data rate (in Gigabits) can be achieved.

2.2 Transceiver Building Block

Transceiver is made up of two words – TRANSmitter and reCEIVER. Figure 2.1 depicts complete transmitter and receiver side chain, amongst which majority of components are inside the WLAN chip and some of them resides either inside or outside of the chip depending upon selected configuration. Blocks shown in light blue colors operates at baseband frequency; whereas, red colored blocks on radio frequency. Brief functionality of each block is explained below–

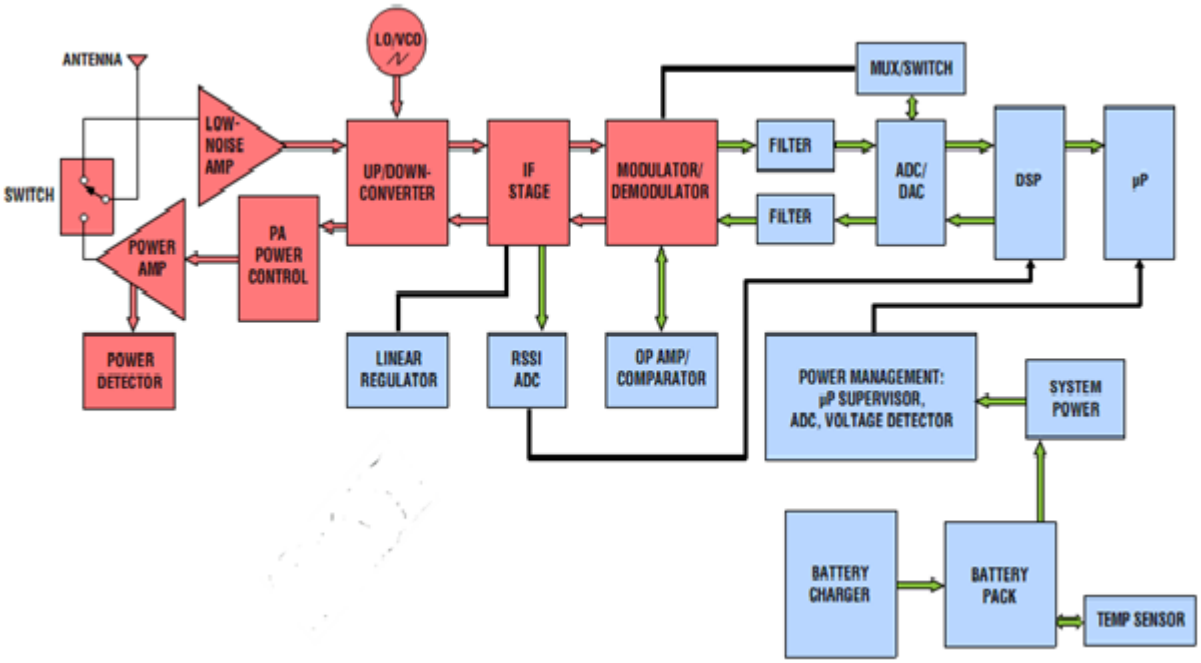

Figure 2.1: Transceiver Building Block [6]

Low-noise Amplifier (LNA):
Function:

- Responsible for amplifying received signal by transceiver

Power Amplifier (PA) :
Function:

- Amplifies transmit signal to the desired power level for proper transmission

Power detector :
Function:

- Used to detect RF power level of PA output transmission
- Converts RF power to DC voltage
- This outputted DC voltage is given as input to ADC

Mixer
Function:

- Nonlinear device that translates RF input signal to lower/ higher output signal

- It's present in both the paths, i.e., transmit and receive path
- High side injection : LO is higher than RF frequency
- Low-side injection : LO is lower than RF frequency

There are two types of mixer :

1) *Downconversion Mixer :*
   - Converts high-RF input frequency to low-IF output frequency
   - Used in receiver
2) *Upconversion Mixer :*
   - Converts low-IF input frequency to high-RF output frequency
   - Used in transmitter

Front - end :

- Combination of LNA and Mixer
- Located at very front of receiver path

I/Q modulator/demodulator :

- Consists of mixer, 90 degrees phase shifter and couple of LPFs

Function:

- Demodulator – Convert IF signal in receive path to I and Q components of baseband which are then processed in DSP
- Modulator – Convert I and Q components of baseband to IF signal

Voltage-controlled Oscillator (VCO) :

- Key to transmitter and receiver frequency generation

Function:

- Heart of PLL which generates clean, precise LO

2.3 Voltage Regulator [5]

Step-down voltage regulators used in electronic devices can be categorized into two separate classes: linear regulators and switching or DC-DC regulators. A linear or an LDO (Low Drop-Out) regulator is in effect a variable resistor that is placed between the input power source (i.e. battery) and the load in order to drop and control the voltage applied to the load. Linear regulators have continuous operation, are typically easier to use, and are definitely a cheaper solution than any DC-DC regulator. Switching regulators provide the highest efficiency and produce the least amount of heat in a system. Therefore, switching regulators are suitable for applications where battery life and heat are important concerns. Efficiency of a regulator is defined as the ratio of output power provided by the regulator to the input power delivered into the regulator and is calculated from :

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}\, I_{OUT}}{V_{IN}\, I_{IN}}$$

Figure 2.2 shows a simplified block diagram of a linear regulator with a resistive load RLoad. Linear regulators provide the most economical solution and are widely available from numerous vendors. Since the input current into a linear regulator is essentially identical to the output current (IIN = IOUT) then, efficiency of any linear regulator can be set by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}\, I_{OUT}}{V_{IN}\, I_{IN}} = \frac{V_{OUT}}{V_{IN}}$$

Simply put, efficiency of a linear regulator is set by ratio of VOUT/VIN. Since the current consumed within the regulator is ignored, efficiency of a linear or LDO regulator is always LESS than VOUT/VIN. So, for a VIN=4V input VOUT=1V, the efficiency is always less than 25% and over 75% of the power provided by a source such as a battery is wasted and converted into HEAT. Efficiency of a linear regulator looks better when the difference between VOUT and VIN is reduced such that $V_{OUT} \approx V_{IN}$ (and $V_{OUT}/V_{IN} \approx 1$).

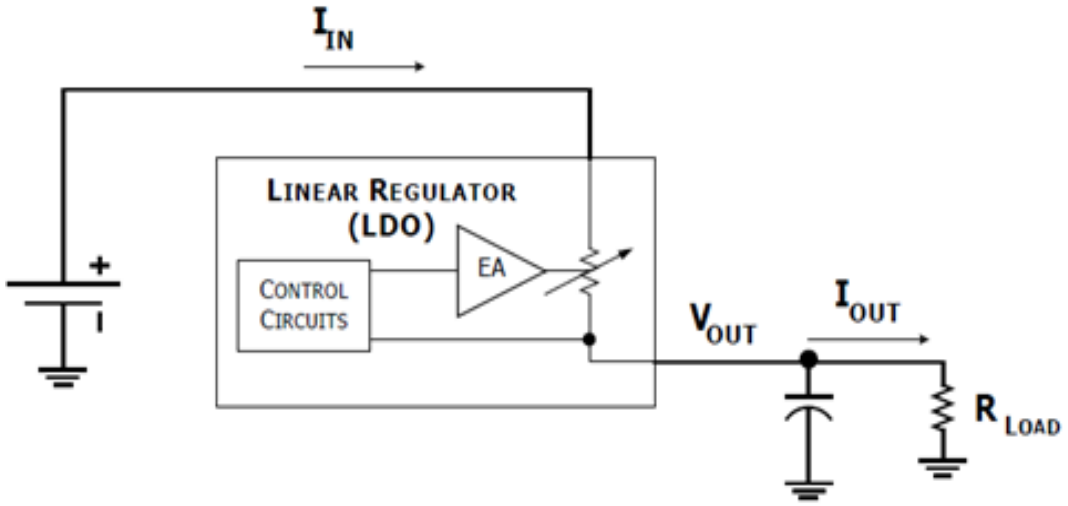

Figure 2.2: Linear Regulator (LDO) [5]

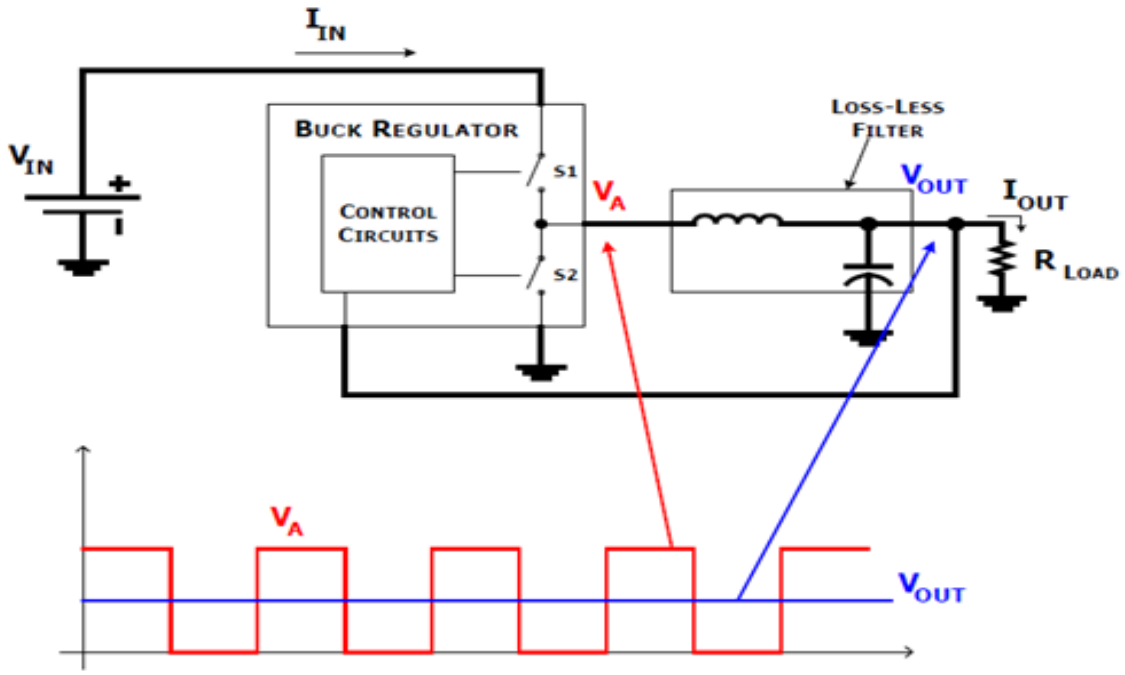

Figure 2.3: Buck Regulator [5]

Unlike linear regulators, switching regulators have non-continuous operation. Figure 2.3 shows a simplified block diagram of a synchronous step-down (Buck) switching regulator. Switches S1 and S2 are operated in a non-overlapping manner to create a digital pulse (VA) that varies from zero to VIN. This generated pulse (VA) is filtered by off-chip passive components such as inductors and capacitors to produce a constant DC voltage at the output. This loss-less filter can be integrated

in the same package along with the die to create a hybrid SiP or module solution.

Switching converters can have efficiencies in the range of 90% independent of input and output voltage ratios and are typically used in applications where efficiency (or battery life) is the most important concern. However, when they are compared to linear or LDO regulators, they cost more and are harder to implement.

Assuming no loss in a switching Buck regulator (100% efficiency), the following relationship would be accurate:

$$V_{IN}\, I_{IN} = V_{OUT}\, I_{OUT} \implies I_{IN} = \frac{V_{OUT}\, I_{OUT}}{V_{IN}}$$

If a battery with 1000mAh (Milliamp Hour) capacity and an average voltage of 3V were used to power a 100mA load at 1V, the battery would last approximately 30 hours with a switching regulator. If a linear regulator were used in the same system, the battery would last less than 10 hours. This would be a 3X improvement in operating time and 3X reduction in generated heat and power loss. Reducing the heat in a portable device would in turn help to prolong the battery life as well since the excess heat will often degrade the performance of the battery.

2.4 Current Measuring Methods

There are basically three methods of monitoring current:

- Optically isolated resistive
- Magnetic
- Resistive

2.4.1 Optically isolated resistive

In the strictest sense as shown in Figure 2.4, this cannot really be considered as a current sensing method in its own right. This is because the opto-isolating device (usually an optically isolated transistor) does not directly measure the current but merely transfers the already sensed current information from the LED to the photodiode as shown in Figure 2.4.

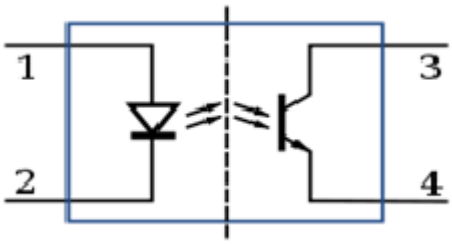

Figure 2.4: Optically isolated method [13]

2.4.2 Magnetic

The magnetic method like optical method, offers isolation but, unlike it, also senses its own current directly without the need for current sensing resistor. The magnetic method as shown in Figure 2.5, commonly uses a current transformer which produces an output voltage that is proportional to the current. This type of magnetic method can only be used with AC measurements unlike resistive and optical methods which can be either. Even so, the use of the magnetic method is only practical at high frequencies rather than low frequencies. This is because the current transformer that would be required at low frequency would be so bulky and expensive as to make it a non-practical solution.

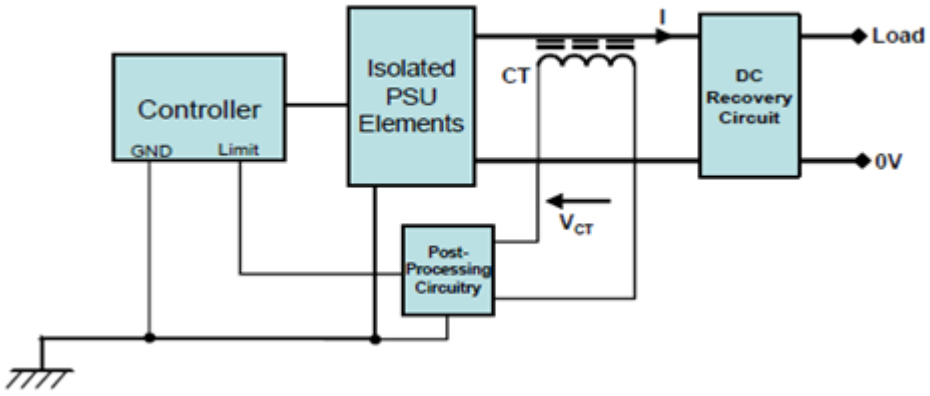

Figure 2.5: Principle of magnetic current monitoring [14]

The main advantage of the magnetic method is that it is a relatively loss-less technique. Hence it is very useful where it is required to monitor very high currents in the hundreds or even thousands of amperes.

2.4.3 Resistive method

This is the simplest, cheapest and the most basic method of current sensing. Inserting a resistance into the current path has the advantage of converting that current into voltage in a linear way that inherently follows Ohm's law of $V = IR$.

Drawback of this method is that the method inherently increases the source output resistance. The effect of this may range from the mildly undesirable (such as slightly reduced terminal voltage) to catastrophic, especially where the introduction of the resistor would interrupt the circuit from the ground plane (e.g. a very noisy design which fails to meet statutory EMC requirements).

Apart from this,it also introduces additional resistance into an electrical circuit. This can result in unacceptable power loss manifested as heat and loss of efficiency.

Since power dissipation is a square function of current ($P = I^2R$), this power loss increases as an exponential function of current. Figure 2.6 illustrates just how very quickly power dissipation builds up in a circuit using resistive current monitoring.

Either of these problems could be alleviated by using a resistance as close to zero as possible. In accordance with this, the lowest value of resistance will produce the lowest power dissipation.

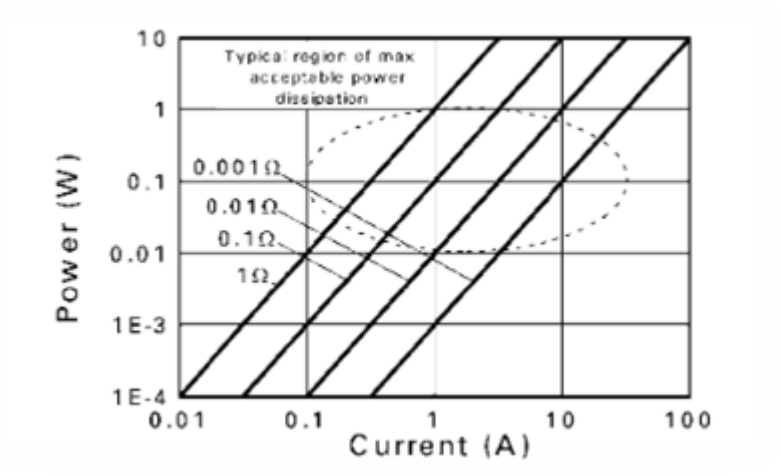

Figure 2.6: Power dissipated vs current measured [14]

In resistor method, current is sensed using current sensing resistors. Current sensing does 2 very important circuit functionality.

1. To know amount of current that is flowing in the circuit

2. To check the faulty condition

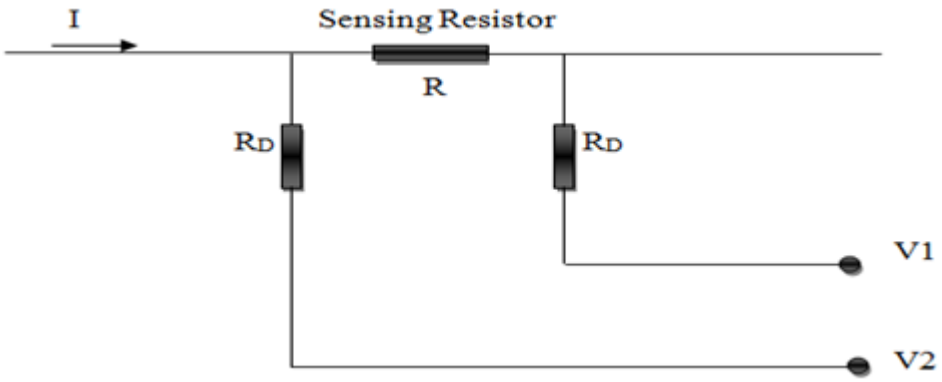

Figure 2.7: Sensing resistor block

where,
R is sensing resistor (56 mOHM to 1 OHM)
R_D is the differential resistor (Zero OHM).

The resistor is a direct method of current measurement that has the benefit of simplicity and linearity. The current sense resistor is placed in line with the current being measured and the resultant current flow causes a small amount of power to be converted into heat. This power conversion is what provides the voltage signal. Other than the favorable characteristics of simplicity and linearity, the current sense resistor is a cost-effective solution with stable Temperature Coefficient of Resistance (TCR) of 100 ppm/degC or 0.01%/degC and does not suffer the potential of avalanche multiplication or thermal runaway. Additionally, the existence of low resistance ($< 1\ m\Omega$ is available) metal alloy current sense products offer superior surge performance for reliable protection during short circuit and over current events.

The Current from the chip flows through the sensing resistor as shown in Figure 2.7 and the voltage drop is measured across the differential resistor as shown.

2.5 Summary

In this chapter, basics of WLAN 802.11 standards and their evolution is discussed. Apart from that, basic building blocks of transceiver are briefly explained. In any portable device, voltage regulator is essential block. Linear and Switching are two main types of regulator. Conventional methods of CM are also discussed.

Chapter 3

Power Consumption Characterization

3.1 General Power Topology

General Power topology of any WLAN chip is shown in Figure 3.1. Major sources of power consumption are Analog section, Digital section, Radio Section. Amongst these power consumed by analog part remains almost same across various chip architecture. What actually keeps changing with new technology and front-end options are digital and radio parts.

Radio section includes currents consumed mainly by Power Amplifier, Mixers, VCO etc. Major contribution comes from PA. It also depends upon position of PA (whether it is inside the chip or outside).

Digital section includes currents mainly consumed by Physical Layer and MAC layer. Apart from these two, there are other logic circuitry which are powered up through this LDO. These currents mainly depend on various features like WiFi standards (11a, 11ac, etc..), SISO or MIMO configuration, size of chip and board etc.

There are mainly two types of regulator inside the chip Switching Regulator (BUCK) and Low Drop-Out (LDO) regulator. Both are DC-DC converter. Battery Supply is directly given to switching regulator and LDO(radio) dividing supply current into two parts I_S1 and I_S2. As buck regulator is not linear one, output current (called as BUCK load current) is related to input supply current (I_S1) through BUCK efficiency. So, BUCK efficiency plays very important role in Power consumption characterization. Other part of supply current I_S2 feeds directly to

the LDO which supplying to the radio section. As LDOs are assumed to be almost linear, output current is almost equal to input supply current I_S2.

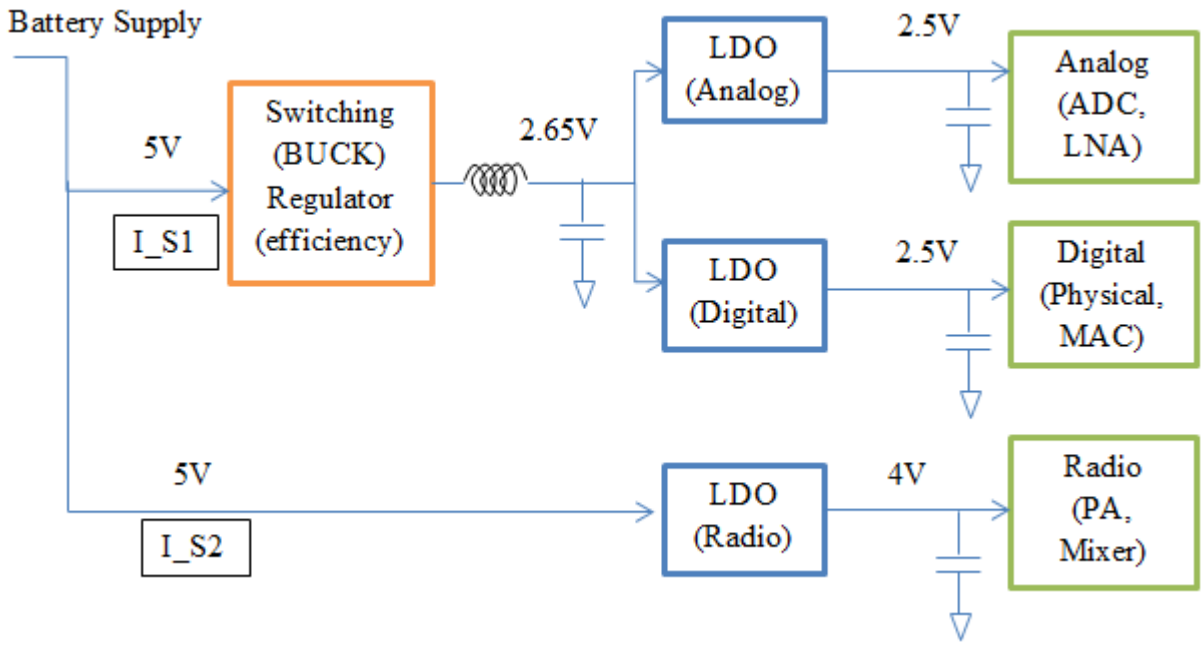

Figure 3.1: Power Topology

3.2 Importance of Digital Loads

Main logic of WLAN chip is implemented in digital. So it is of prime importance to know how much power is being consumed by digital section and analyzing it to reduce it as much as possible.

An ICs total power consumption comprises two types, static and dynamic. Static power typically comes from leakage current and dc current sources. Dynamic current consumption, which is frequency-dependent, often dominates total power. It comes from the charging and discharging of capacitive nodes and the crowbar action of switching transistors connected between the supplies. Figure 3.2 and Figure 3.3 show the capacitive charge characteristics of the common CMOS inverter. The dynamic charging causes power consumption to be directly proportional to the clocking frequency. Power is consumed because of the momentary current flow that occurs when both transistors conduct during a logic transition [4].

Digital logic is implemented with CMOS technology having large no. of CMOS inverters as shown in Figure 3.2 and 3.3. When chip is in any state other than off

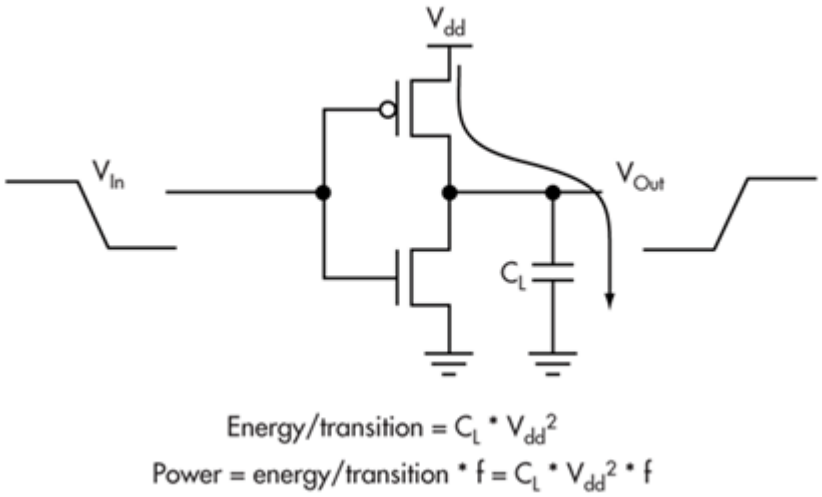

Figure 3.2: Dynamic Charging in CMOS Inverter [4]

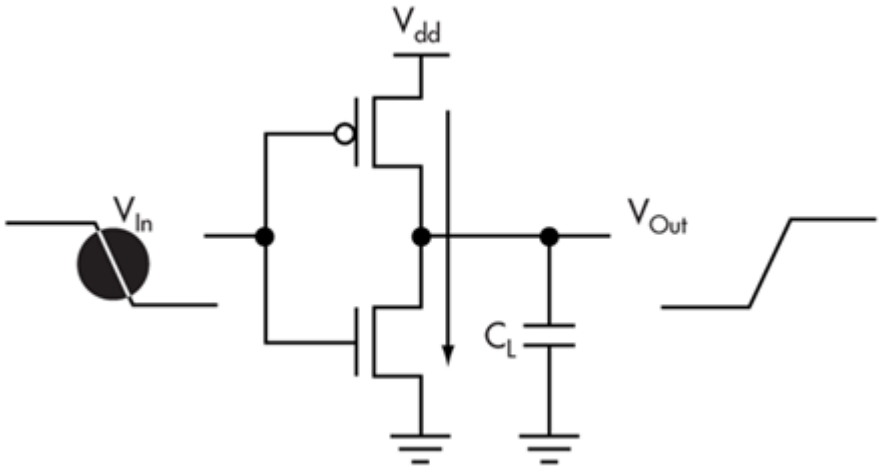

Figure 3.3: Logic Transition in CMOS Inverter [4]

state, at very fundamental level, there is continuous charging and discharging of these output capacitors depending on input frequency and supply voltage. This is very cause of power consumption and dissipation.

$$P_D = V * I = \frac{1}{2} CV^2 f_0 \quad (watt)$$

For such n capacitors,

$$P_D = n\,(V * I) = n\,(\frac{1}{2} CV^2 f_0) \quad (watt)$$

For any given chip, values of C and f_0 are almost same. So, power consumed

by any block mainly depends on voltage supply (V) at its input for frequency of f_0. And if this voltage drops; then, current consumed by circuit will also drop and we will not get actual current consumption. Even worse is that if voltage drops below certain value, then circuits stops working. Hence, one of the main aim of CM setup is that whatever actual voltage is there at any input terminal, it should remain almost same after inclusion of CM setup to get true current consumption.

3.3 Split Currents

Power consumption of overall chip can be found out by measuring supply current (I_S1+I_S2). To know the currents, in particular, we have to measure split currents. Arrangement for the same should theoretically look like as shown in Figure 3.4. LDOs and actual logic are inside the chip. But, for CM, boards are designed in such a way that there signal from LDO to any logic passes through outside the chip where it can be measured by inserting ammeter in between.

But practically, connecting so many ammeters is not possible. Also, inserting ammeter in every path one-by-one is also not possible. Hence, to simplify and accelerate the CM, automated CM setup is used or majority of the times. Sometimes when only one or two currents need to be measured for debug purpose, then manual measurements can be done.

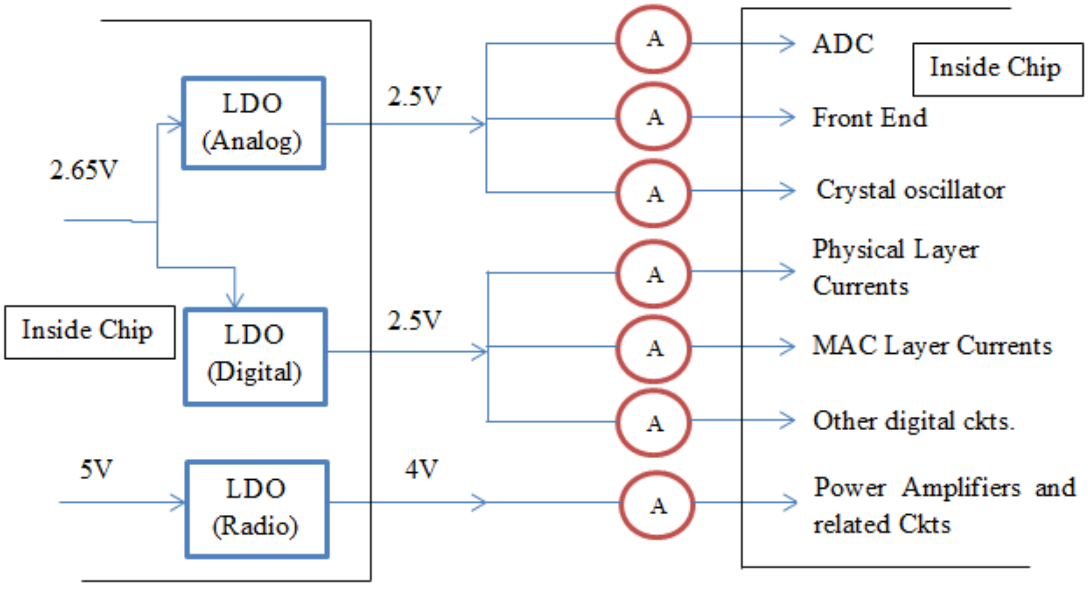

Figure 3.4: Theoretical Split Current scenario

3.4 Types of CM Methods

1) Conventional method using ammeter (Manual Method)

- Like in our conventional way, ammeter is connected in series with particular path through which current is to be measured.

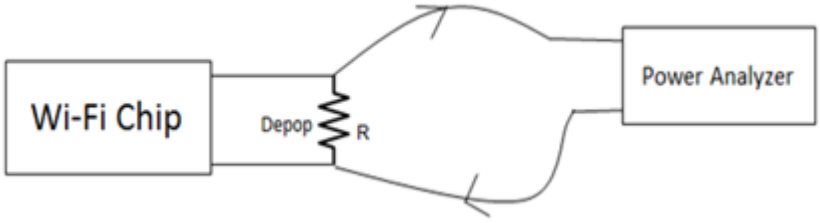

Figure 3.5: Conventional Setup

Adv: Used when few currents need to be measured
Disadv: Time consuming method

2) Using automatic switching (Automated Current method)

- Ammeter is switched between different loads through automated script

Adv: Used for measuring low currents like sleep and listen currents
Disadv: Problem of huge IR drop popped up when measuring high currents

3) Using differential amplifier (Automated Voltage Method)

- Voltage across sense resistance is measured and is converted to corresponding current value.

Adv: Used to measure high currents where the IR drop is high
Disadv: Less accurate in measuring low currents

3.5 Automated Current Method (Detailed)

Automated CM setup is shown in Figure 3.6. For ease of explanation, only digital current split is used as an example. To measure physical layer current, loop starts from LDO(digital), goes through switch structure on CM board and then through ammeter to physical layer circuit inside the chip. $(LDO(digital) \rightarrow A \rightarrow B \rightarrow C \rightarrow$

Ammeter $\rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow$ *Physicallayer*) In this, LDO and physical layer logic are inside the chip; point A and G are on board with chip and B,C,D,E,F on CM board with switches. These switches close and open one-by-one, thus inserting ammeter to every path to measure respective split current. CM loop is quite large, which poses multiple issues in process of measuring currents which are discussed in next section.

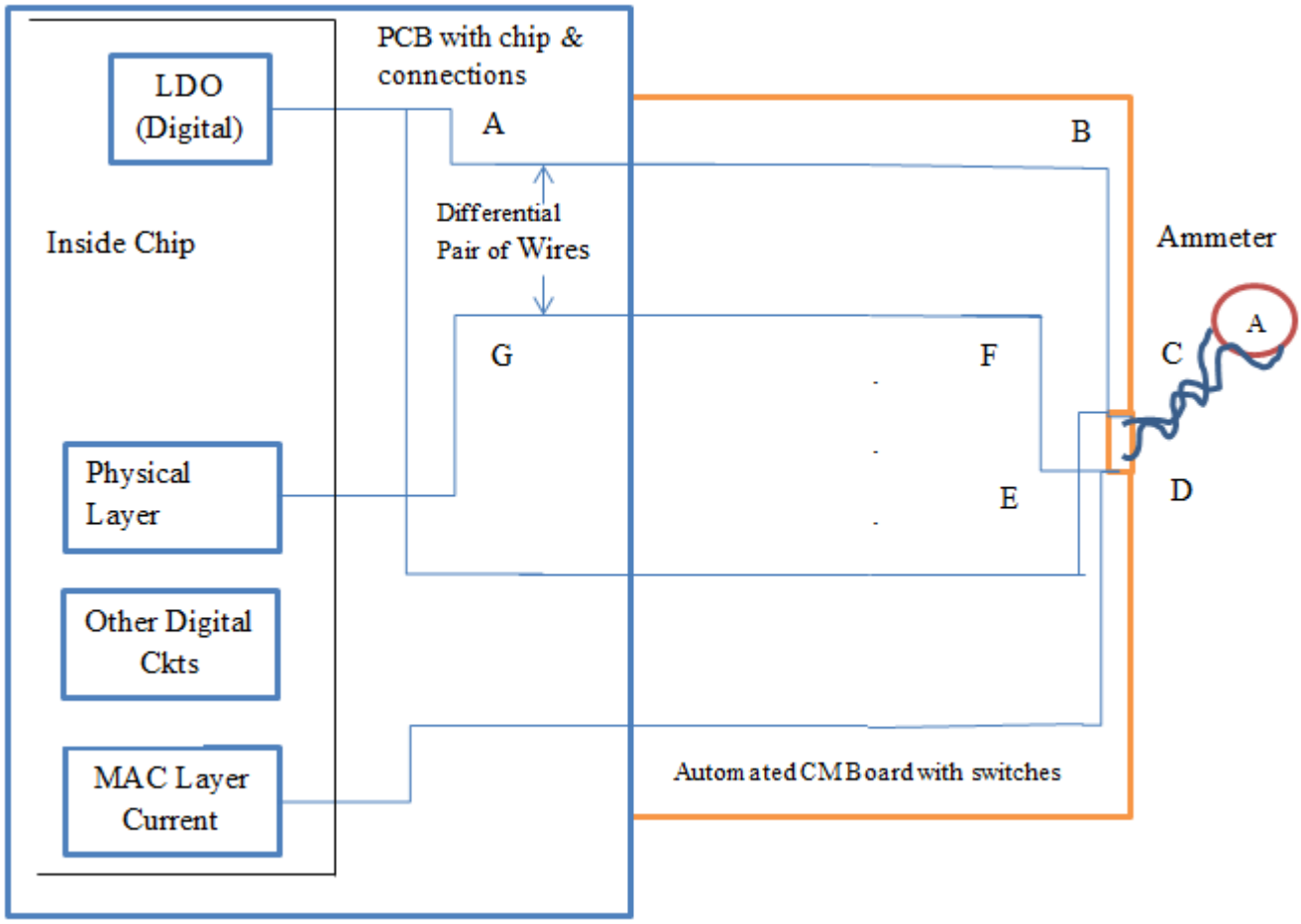

Figure 3.6: Automated CM setup

3.6 CM setup related issues and their solution

Very common and dominant issue is "Resistance of Entire Path". As CM path is made up of conducting material like copper in trace and connecting wire, heat dissipation in form of electrons vibration increases; thus, reducing actual current value. One more additional source of resistance is switch resistances. There are 2

series switches in CM path which connects and disconnects ammeter to/from the path whose current is being measured at that time. Only solution to this problem is reduce length of the wires and reduce switch resistance. We implemented former solution and found good improvement in the currents measured. Later part comes in future scope.

Other issue is of "Loop Inductance". Due to high frequency of switching of digital logic, the issue is more dominant in digital currents. For CM, two wires are carrying currents of high frequency into opposite direction, that is, from LDO to ammeter and from ammeter to physical or MAC layer or any other digital ckts inside the chip. Self and mutual inductance induced in wires causes voltage drop along the CM loop. So, if voltage at LDO output (Point A) is 2.5V; then voltage at input of any digital ckt (Point G) is lesser than 2.5V depending upon loop inductance. (its around 2.4 to 2.47V) As explained earlier, if logic receives lower input voltage than expected, then it will consume lesser current than expected; thus giving wrong value of current. So, these two problems together cause voltage to drop from point A to G, which in turn reduces current consumed. ($V_{AG} \approx 20 to 120 mV$)

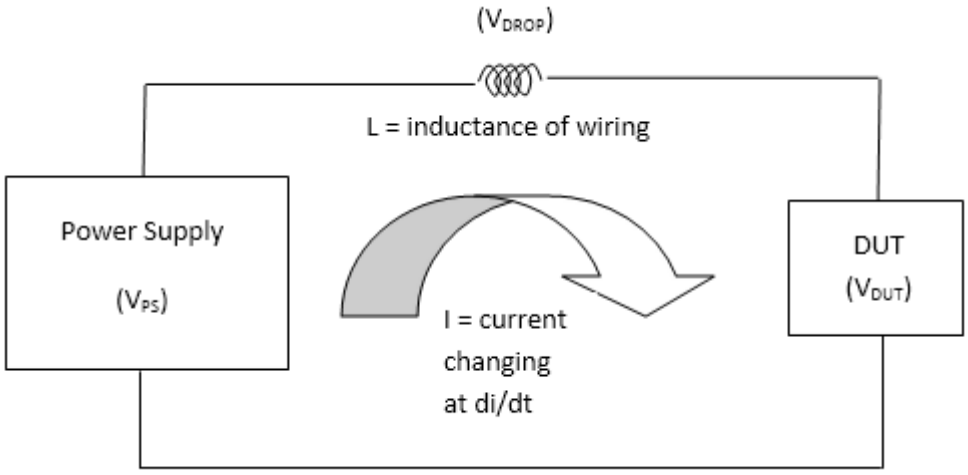

Figure 3.7: Voltage drop due to L [3]

Solution to problem of Resistance of Entire Path is to reduce length of the wires and reduce switch resistance. Reducing length of the wires include both, i.e., reducing length of the trace on the board and also using minimal wire to connect ammeter to the CM board. We implemented this solution and found good improvement in the currents measured. Later part comes in future scope.

Twisting of connecting cables from CM board to ammeter, as shown in Figure 3.6, is the prime solution for reducing the loop inductance. This achieved by cancelling inductance produced in adjacent loops of twisted cable as shown in Figure 3.8, 3.9. The twisted pair cable helps to reduce loop area (S) and decrease effect of induced voltage in function of magnetic field, balancing the effects (average of the effects according to the distances):

$$V_b = \frac{d}{dt} \oint \overrightarrow{B} \, . \, \overrightarrow{dS}$$

Twisting the cables also prevent the cables from separating (if they were loosely connected), which further gives mechanical stability to the setup. The crosstalk between the pair of wires and the level of electromagnetic interference can be reduced by the cancellation effect. (as shown in Figure 3.10)

Such a twisting of traces is not possible of the boards. So there, separation between differential pairs of traces is kept minimal, i.e., path ABC and DEFG are routed very near to each in board design. Also, length and area occupied by these traces are also kept as low as possible to reduce resistance and to reduce loop area, which in turn, lowers loop inductance.

After implementing these solutions, we found fair amount of increase in correctness and reliability of measurements.

We mainly take care of these things while doing measurements of digital or analog split currents and not for total supply currents or PA currents. Reason being, if due to longer length of wire and parallel connecting cables, voltage at input of switching regulator drops from 5V to 4.8V; then also output of regulator will be 2.65V only. Whereas if output of LDO(digital) or LDO(analog) drops by 40mV also, then there is no further regulator to come. That voltage directly appears at input of logic ckt, thus leading to the erroneous situation.

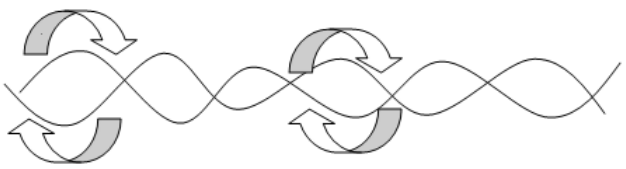

Figure 3.8: Magnetic field effect in adjacent loop of twisted cable [2]

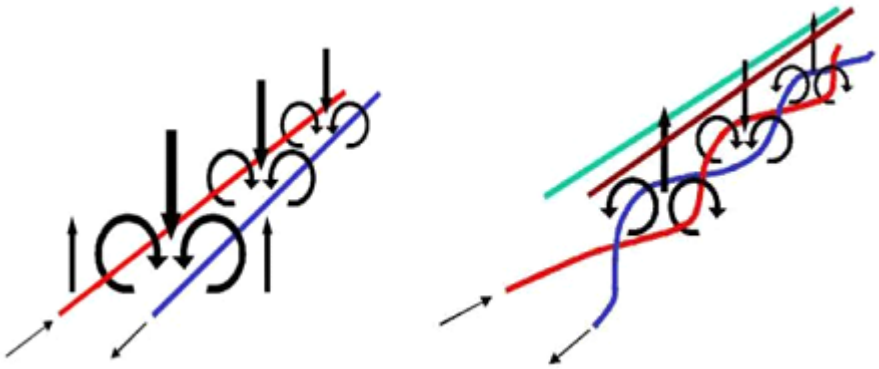

Figure 3.9: Additive and Cancellation effect of Magnetic field [1]

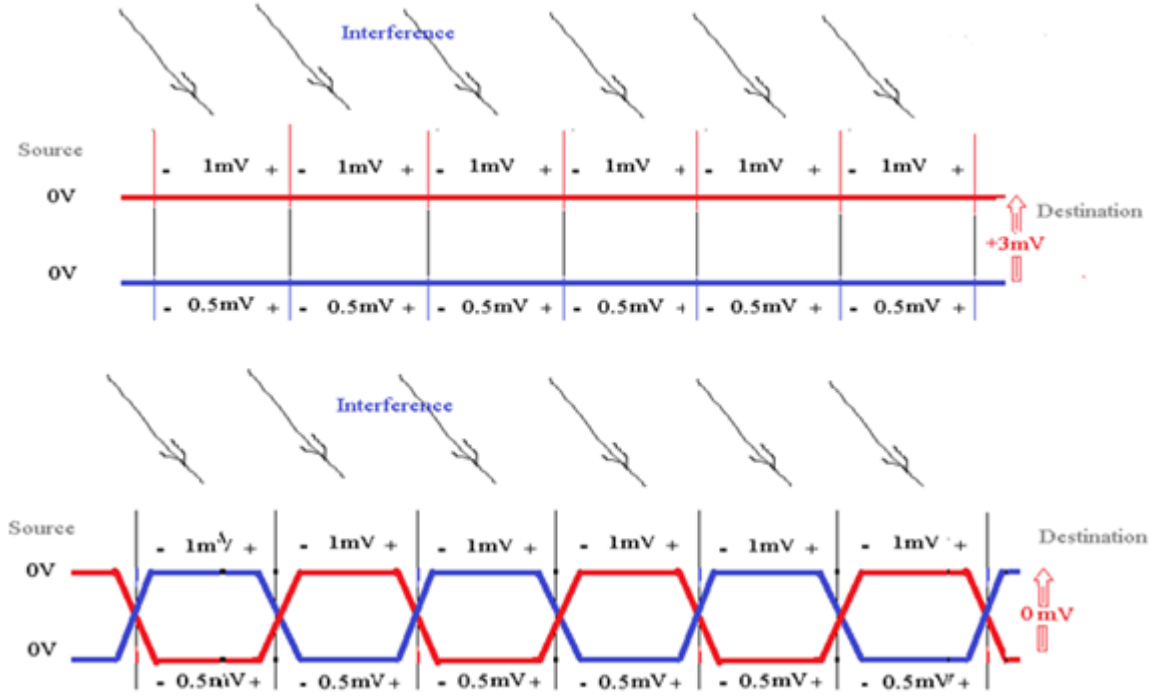

Figure 3.10: (a) Parallel Pair, the interference causes higher pickup voltages in red than blue wire (b) Twisted Pair, the interference alternately produces high and low pick-up voltage in both wires [1]

3.7 Self-check Method of result verification

Now, to know whatever currents we measure are correct or not, sanity check is performed on setup every time, before starting any split CM. Efficiency of switching regulator is used for this purpose.

$$BUCK\ load\ current = (Digital + Analog + Interconnect\ current)_{measured}$$

Figure 3.11 shows relationship between input and output current of BUCK regulator through efficiency. Efficiency is ratio of output to input power. For buck regulator, input current and voltage are I_S1 and 5V; and output current and voltage are BUCK load current and 2.65V. So, we calculate BUCK load current from above formula. We first measure I_S1 through CM setup.

$$Efficiency = \frac{2.65 * BUCK\ load\ current}{5 * I\_S1}$$

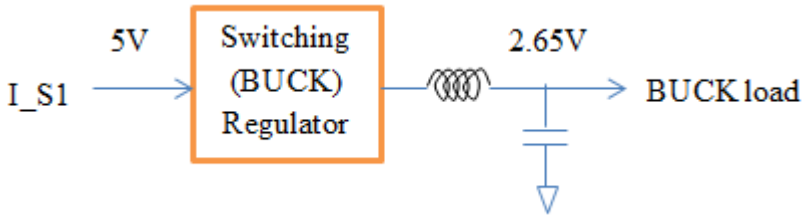

Figure 3.11: BUCK Regulator Efficiency

And, then using BUCK efficiency and BUCK load current, we calculate I_S1. So, if following condition is satisfied,

$$| I\_S1_{cal} - I\_S2_{meas} | < (\ 10\ to\ 20\ mA)$$

then, setup is considered to be ready for CM.

3.8 Accurate BUCK Efficiency Measurement

In above topic, we have assumed some value of buck efficiency for self-check. But, this value need to be first accurately calculated first. This topic discusses the

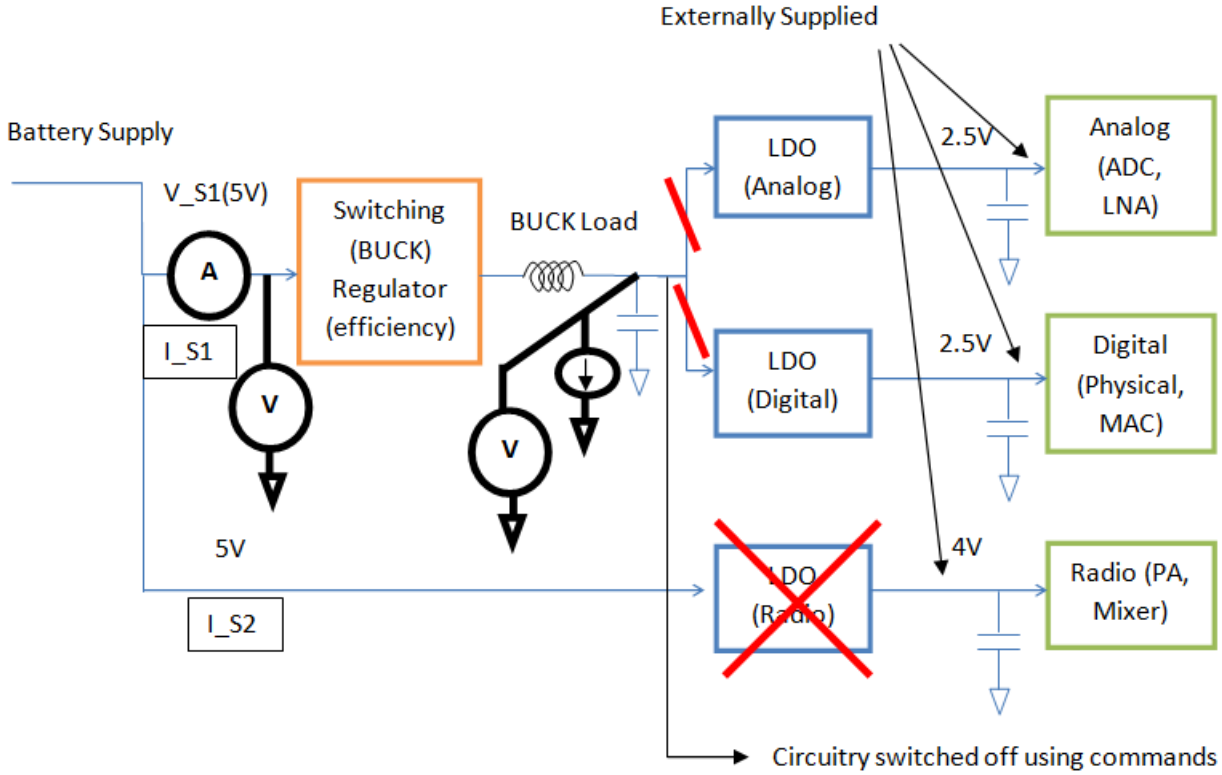

Figure 3.12: Circuit modification for accurate buck efficiency measurement

methodology used for such measurements. Figure 3.12 shows circuit modification for this experiment.

To measure efficiency of buck, we need 4 values , input current (I_S1) for which ammeter is connected at the input of buck; input voltage (V_S1) which is actually battery supplied 5V, but practically its not never equal to it and that is why voltmeter is connected between input and ground; output voltage (BUCK out) which is also theoretically fix, but same as input, this one is also measured using voltmeter. Lastly, buck load current, on which actually buck efficiency depends, is varied using CC load.

Actual buck output to chip is cut off by either breaking the path or by switching off those blocks through commands so that they will not draw any current. But, chip need to be initialised so that buck regulator and other chip parts come to their predefined reset state. For this purpose, minimal parts which need to be initialised are powered up externally.

Buck load current is varied from 35 to 395 mA, and other three parameters are measured. Using efficiency formula from previous topic, buck efficiency is calculated for each buck load current and graph is plotted.

	ip vtg	ip curr	op vtg	op curr	CBUCK Eff
	SR_VBAT	SR_VBAT	BUCK out	BUCK load	
	V	mA	V	mA	%
Initally	5.0986	4	2.6628	--	
	5.0986	24.29	2.6628	35	75.254
	5.0986	45.24	2.6628	75	86.582
	5.0986	66.74	2.6628	115	89.991
	5.0986	88.98	2.6628	155	90.976
	5.0986	112.1	2.6628	195	90.848
	5.0986	135.91	2.6628	235	90.303
	5.0986	160.57	2.6628	275	89.445
	5.0986	186.06	2.6628	315	88.419
	5.0986	212.48	2.6628	355	87.257
	5.0986	239.81	2.6628	395	86.024

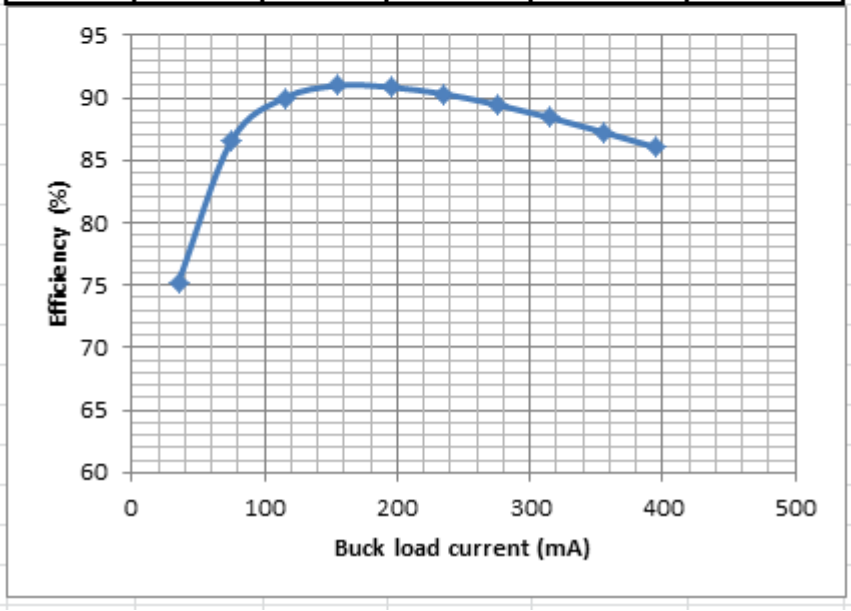

Figure 3.13: BUCK load current vs BUCK efficiency

From the results it is concluded that, buck efficiency is highest when load current is between 150 to 250 mA. So, we should try to operate buck in this region to get maximum out of it.

3.9 Thermal Problem and its analysis

Another major issue related to power consumption is thermal problems. Because as chip consumes power, it dissipates heat, which in turn increases junction temperature of chip and current consumed by it. That means, its a cyclic process.

As we know Thermal resistance (θ_{ja}) can be defined as "the difference between junction temperature (T_j) and the ambient Temperature (T_a), under the condition that the WLAN chip dissipates electric power of 1W."

$$\theta_{ja} = \frac{T_j - T_a}{P_D} \quad (degC/W)$$

$$\implies T_j = \theta_j * P_D + T_a \quad (degC)$$

where, P_D : Power dissipation in Watt

From the formula, it is clear that as power consumption increases, junction temperature of the chip increases for a particular ambient temperature. From above discussion, we have seen that major sources of power consumption in WLAN chip are digital and radio sections. But, if we analyze the power topology, digital section is a part of I_S1 current and radio section is a part of I_S2 current at battery supply level. So, we tried to find out relationship between change in T_j to change in I_S1 and I_S2 currents. We plotted two graphs–

1) $\triangle T_j$ vs $\triangle$I_S1 keeping I_S2 almost constant.

2) $\triangle T_j$ vs $\triangle$I_S2 keeping I_S1 almost constant.

These graphs indicate increase in current (I_S1 or I_S2) per degree rise in junction temperature or by how much amount current (I_S1 or I_S2) should increase to make one degree rise in junction temperature. From such graph, we try to find out which section of chip is contributing more in thermal problem and report it to chip design team, which will try to reduce it by various ways.

There is one more factor in thermal problem air circulation. If we test chip in with and without air circulation condition, then there is drastic change in behavior of junction temperature. As with air circulation, heat generated by chip is moved away from it; thus keeping temperature lower. But, in actual portable devices, there is no provision for air circulation. So, we have to analyze and create environment like devices and test the chip. This tells how much it will heat up when placed inside the device. (see Figure 3.14)

As we have seen that, when chip is in active mode, it consumes current and heats up. But, there is some upper threshold value of temperature (T_{th}) above which WLAN chip may not do its intended job properly. So, thermal problem creates reliability issues if threshold is crossed and thus imposes upper limit on working ambient temperature of the chip. This gives thermal analysis, very much importance in power consumption characterization.

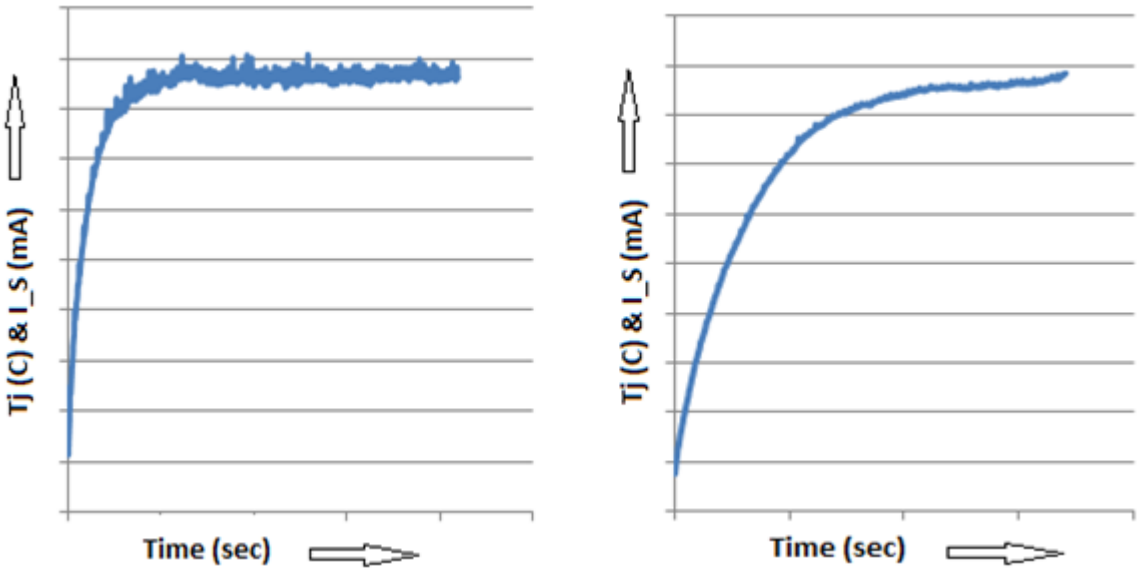

Figure 3.14: Effect of air-circulation on Tj and Supply current

There is chip-to-chip variation also in CM as well as in thermal analysis. No two chips will consume exact same currents and heat up to same junction temperature.

This thermal problem causes mainly due to following reason, fundamental reason being less availability of surface area to dissipate heat.

1) High density of logic implemented inside the chip

2) Compact size of chip and board

3) Thin trace size

As we are in era of nanotechnology, size of chip is becoming smaller and smaller and logic is becoming more and more complex. This makes complex logic implementation in smaller area with very high speed of switching frequency. And, size of portable devices is reducing, forcing size of boards to be smaller and more compact. So, there is no space for routing thicker trace which helps in heat dissipation.

Tj delta [C]	I_S2 delta [mA]
9	37
10	52
14	62
16	72
26	121
35	160
45	183

Tj delta [C]	I_S1 delta [mA]
0	14
2	30
2	35
3	46
4	55
6	90
7	110
8	113
8	120
9	131
10	140
11	150
12	166
13	180
13	192

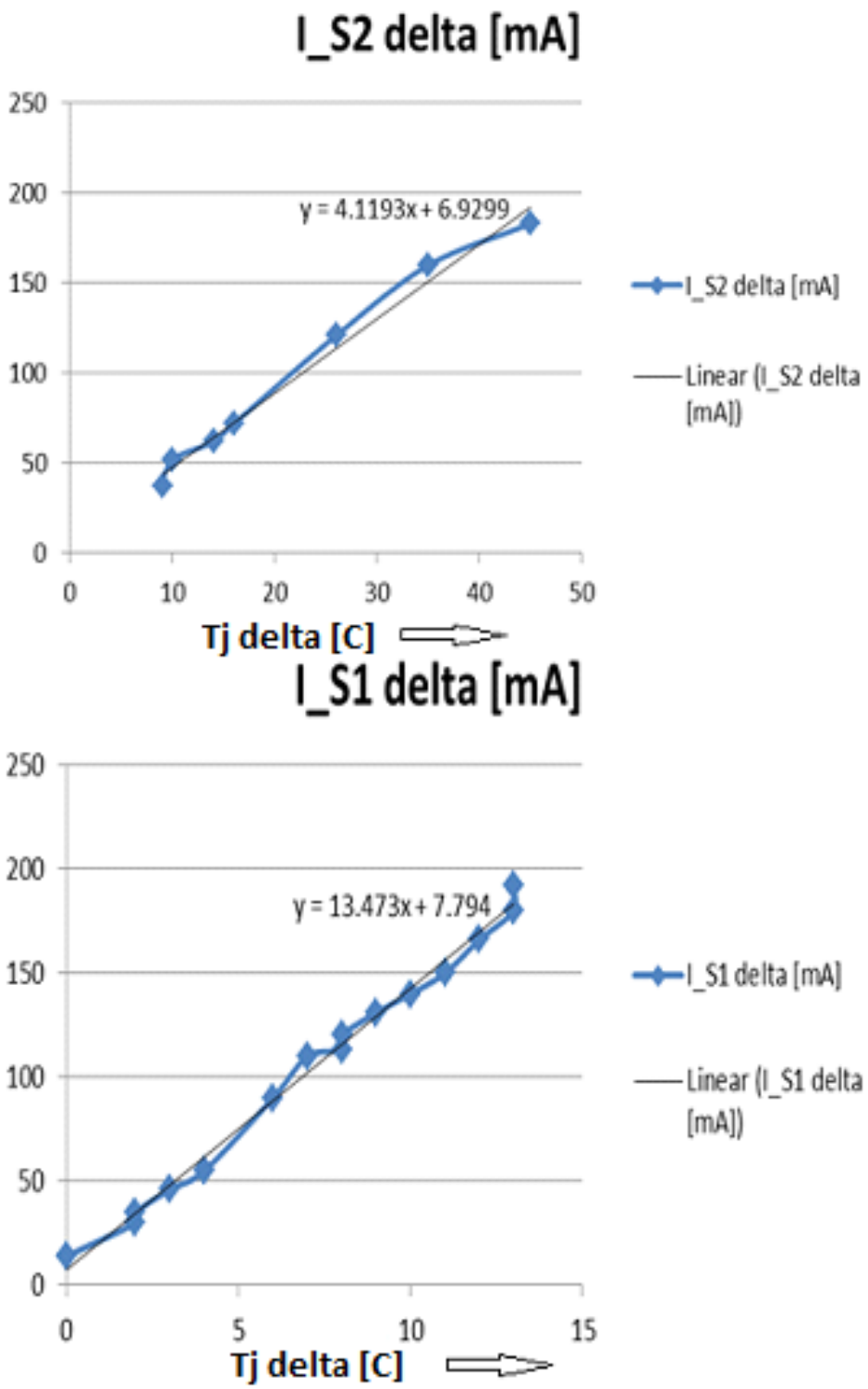

Figure 3.15: Thermal analysis Plots

To improve thermal behavior, careful designs of board will be helpful. We have make use of multi-layered PCBs and more no. of vias at appropriate location. Using thicker traces for particular signal lines (like supply current) providing more area of heat dissipation.

3.10 Consideration of some RF characteristics in CM

Now, currents are measured when chip is in various modes of operation. Mainly there are two modes Tx and Rx mode. In Rx, there are listen and active mode; whereas in Tx, currents are measured when chip is in fully active mode. (In both tx and rx active mode, wlan chip transmits and receive large no. of packets)

Setup for tx and rx CM is shown in Figure 3.16. When DUT is in rx mode, its sensitivity need to be adjusted so that it receives max no. of packets. This is achieved through adjustment of attenuation between signal generator and DUT. When DUT is in tx mode, it can not transmit at any power. It is decided by the EVM performance. So, power is adjusted max power such that EVM performance is acceptable. All these things need to be checked before starting CM.

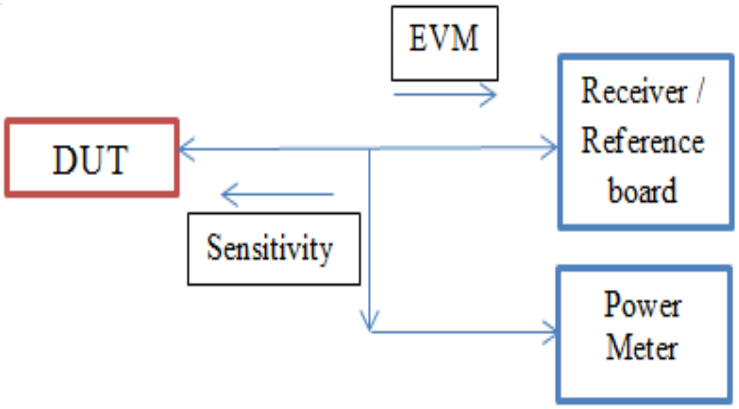

Figure 3.16: CM bench setup

3.11 Challenges in CM Setup Automation

3.11.1 Measurement Accuracy:

In automation of CM setup, its not like bench setup where we can use short connecting wires and get measurement accuracy. In test bed of CM setup, though test equipment are kept in vicinity, still connecting wires required are of longer length. This creates issue of measurement accuracy.

Power supplies are of prime importance in testing, particularly, related to power consumption. Longer wires having resistance cause voltage to be dropped from supply end to DUT end. This inaccuracy gets carry forward into further testing process.

To eliminate this, at very starting level only, power supplies come with SENSE inputs. These inputs are connected to same output leads at DUT side such as, SENSE+ to Vout+ and SENSE- to Vout-.

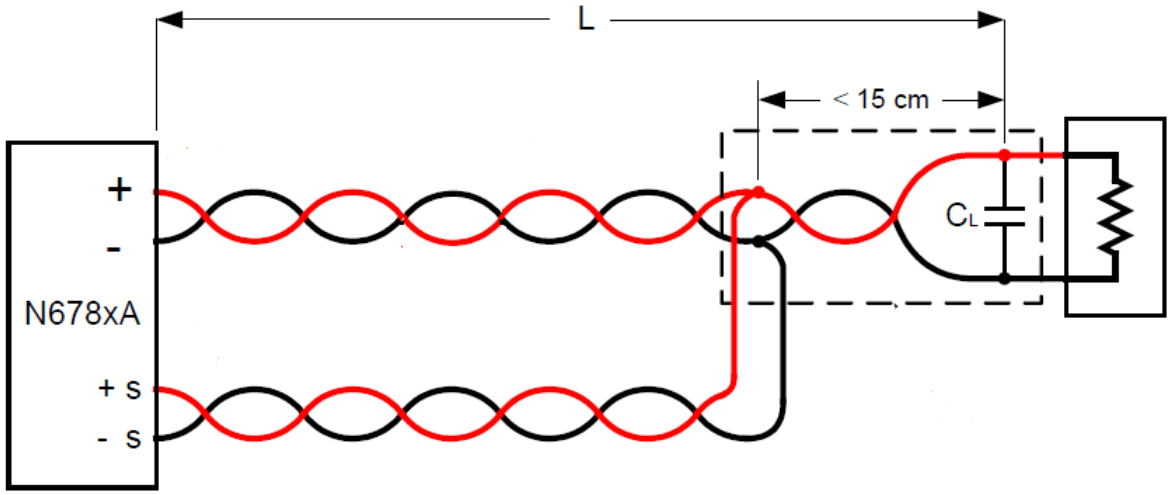

Figure 3.17: Remote Sensing Connection [16]

Most of the AC-DC power supplies include "Remote Sense"terminals (+ and - Sense) which are used to regulate output voltage of supply at the load side. Since the wires that connect supply output to its load have some internal resistance. When flow of current increases through these wires, according to Ohm's low, voltage drop across these wires also increases (I x R = Voltage Drop). This leads to delta between output voltage supplied by the source and input voltage at the load side. This can be solved using with use of the two Remote Sense wires connected from the supply to the load that will compensate for unwanted voltage drops along the wire and

reduce delta between voltages at two end of connecting wires [15].

Figure 3.18 depicts schematic of power supply's remote sense circuitry. Polarities of sense wires should be correct, i.e., the +Sense wire must be connected to load closer to +Vload and Sense wire must be connected to load closer to -Vload. In case of reverse connection, current will flow through Sense wires and burn out internal Rsense resistors, causing a malfunction of the supply [15].

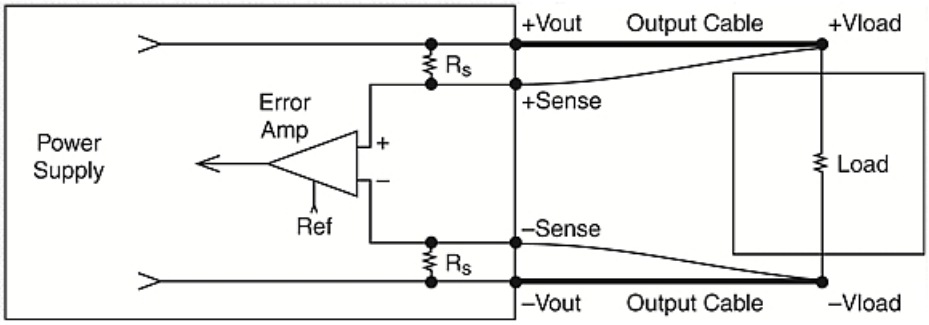

Figure 3.18: Remote Sense Schematic [15]

There are some limits till which remote sensing can help to regulate supply. After that, to reduce wire resistance, thick gauge wires are used. As these wires have more cross-sectional area, resistance per unit length automatically decreases, thus decreasing loss in wires.

3.11.2 Interfacing of Test Equipment:

The bench test instruments, on large scale, require interfaces like GPIB or LXI to communicate. And, these interfaces use language known as SCPI, Standard Commands for Programmable Instrumentation to send the commands to the instruments.

SCPI:

SCPI stands for "*Standard Commands for Programmable Instruments*". To control programmable test and measurement equipments, SCPI has provided a certain standard format of syntax and commands to be used. Syntax, data formats and command structure defined by this standard, is applicable to almost all the instruments. It has specified general commands (such as OUTPut and MEASure), which could be used with any test instrument. These commands are categorised under subsystems. SCPI works on higher abstract layer and not on physical communications layer. Physical communication link is established by interface protocol being

used. SCPI was created for IEEE-488 (GPIB); but due to its many advantages, it is now used with RS-232, Ethernet, USB, VXIbus, etc. also.

Commands are written and sent in ASCII textual strings through physical layer (e.g., IEEE-488) to connected instrument. Instruments response to the query commands normally using ASCII strings. However, if data is in bulk, then binary formats can be used.

Let's take one example of SCPI command. "MEAS:VOLT:DC? 10.0,0.001"– This command, as name suggest, is used to make DMM measure value of a DC voltage regardless its measurement range and its vendor or model. The instrument to which command is sent, could be anything other than DMM, as long as it can make the measurement. As can be seen from command structure, SCPI commands are very similar to a natural language [18].

3.12 Summary

This chapter explains about need of CM, it's types in brief as well as in detail and problem faced during CM along with their solutions. Thermal problem is also analysed with help of various experiments. Finally, self-check method of result checking and issues related to test setups are discussed.

Chapter 4

RF Performance Characterization

4.1 Test Setup

There are 2 different ways in which the same tests are carried out in the lab. One is using bench setup and other using the testbeds.

BENCH SETUP

In this testing method the setup is something like this, DUT is placed on the adapter board, DUT is then connected through Bench using either of the three interfaces (SDIO, JTAG or PCI). The commands are sent in to the DUT through bench. For running any command or test on the DUT we need to rush in to the particular BENCH machine.

The device will process in this commands and produce output, this output is measured by connecting output of antenna with the power meter and spectrum analyzer. This method is preferred when only single parameter is to be measured and interference free environment is not required. Tcl commands are used for communicating with DUT.

TESTBED SETUP

This method of testing is preferred when interference free environment is required. This uses python scripts for communication with lab equipments. It is a fully automized test station which is used to carry out all kind of test as per the requirement. It is capable of measuring a large number of parameters specific to the test which is carried out. There are two different types of test stations one is transmitter testbeds and another is receiver testbed.

All the transmitter related tests like evm measurement , transmitter gain are performed on tx station and the tests like receiver sensitivity etc are performed on receiver station. The readings of spectrum analyzer and power meter are automatically measured during the test and their log file is created. With particular command, result from log file are plotted for all the parameters that it has measured during the test.

For Tx and Rx test, both bench and testbed setups generalized diagram can be shown in Figure 4.1.

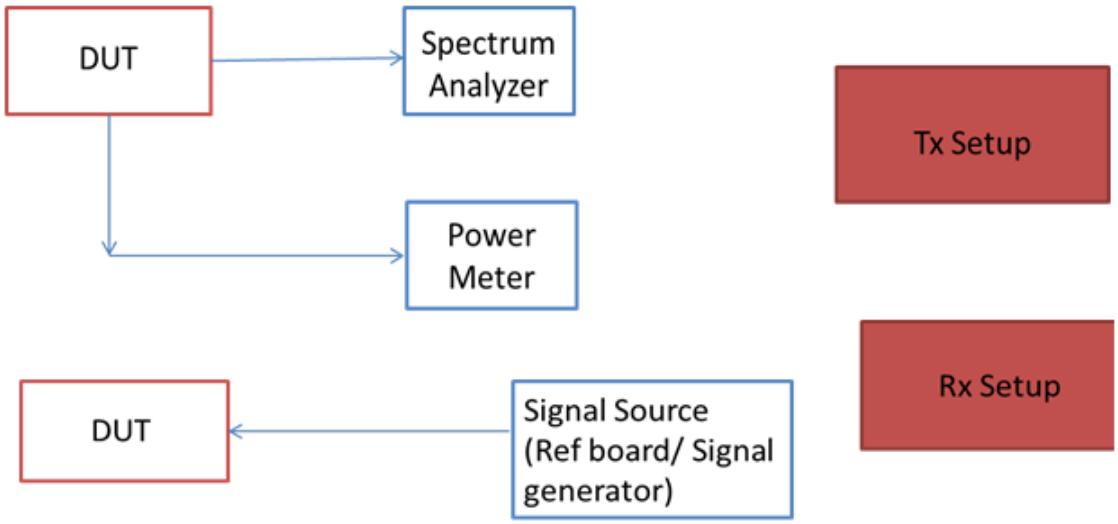

Figure 4.1: Test Setup for RF Test

4.2 Tone and Packet Transmission

We have performed various tests on DUT to measure its different parameters. The most primary test we did was sending in tone and packets. Sending a tone means to just transmit a single frequency continuous wave from an antenna of DUT. Some tickle commands are send in order to send a particular frequency tone. The experiment of sending a tone is useful in phase noise measurements and noise figure measurements.

The next experiment done was to transmit a large number of packets at a particular frequency. In order to transmit the packets, various parameters are needed to be specified using tickle commands. This experiment to transmit packets is used to determine different parameters like EVM (Error vector magnitude), Receiver sensitivity, Spectrum masks, ACPR (Adjacent channel power rejection) etc.

4.3 Transmitter Test

4.3.1 Error Vector Magnitude (EVM):

EVM is a single scalar number, primarily related to transmitter side, indicates quality of modulation scheme applied on the signal. In measurement of EVM, comparison of actual symbols with their ideal impairment-free symbols on the constellation diagram is done and error vectors are computed as shown in Figure 4.2. Offset gets created between real constellation points and the ideal ones due to deterministic and systematic errors. However, non-systematic impairments such as noise causes an "error ball"or "error cloud"of uncertainty in constellation diagram around ideal constellation points. According to IEEE specifications for the 802.11a and g standards, at 54 Mbps, EVM should be atleast 25 dB [8]. Mathematically, EVM can be defined as,

$$EVM = \sqrt{\frac{\sum_{i=1}^{M} |Z(i) - R(i)|^2}{\sum_{i=1}^{M} |R(i)|^2}}$$

where,
Z - measured signal
R - reference (ideal) signal
M - number of measurements
i - measurement index

Definition of EVM clearly indicates that EVM is an estimation of the error signal magnitude when compared with its corresponding ideal part. Maximum value of EVM can 1, or 100%, and minimum 0. If EVM is smaller in percent, then quality of the modulated signal will be superior. EVM can also be expressed in decibels as 20 log (EVM).

EVM is computed based on in-phase (amplitude) and quadrature phase data (phase). Number of bits required to encode specific data symbol in I versus Q plane, depends on the complexity of modulation scheme being used. The error vector mostly defined as the rms value over time.

Various impairments in the system affect the EVM. Impairments can be phase noise, non-linearity, quadrature imbalances, filter cut-offs and bandwidth. The reason that the EVM is considered to be one of the best measure of the quality of the transmitter is that it is mainly impacted by many of such impairments [8]. The EVM can be used as direct measure of modulation-demodulation accuracy and signal quality.

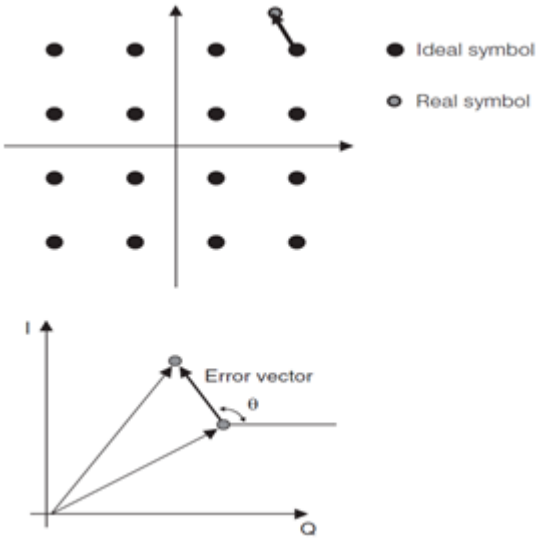

Figure 4.2: Pictorial description of Fundamentals of EVM [8]

EVM Plot and Inferences:
This test is performed on transmitter testbed. Single run of EVM test gives information about parameters like EVM vs Transmit power (dBm), Local oscillator feed through (LOFT) Vs. Transmit power, IQ imbalance, PAPR (peak to average power ratio), frequency offset (ppm), etc.

In EVM Vs. Transmit Power plot, EVM noise floor and spread i.e. difference of transmit power at a particular EVM level for low, mid and high channels are observed. Lower EVM noise floor and lesser spread is desired. Increment of EVM with increase in output power is due to nonlinearity of PA. As we start increasing power above certain level, PA will start moving into nonlinear (Saturation) region. LOFT is amount of local oscillator frequency power radiated at the output of the mixer. The results are better if we get lesser LOFT value. I-Q imbalance gives idea about fluctuation of the constellation points around reference (ideal) constellation points.

Frequency offset is measured in parts per million (ppm). 1 ppm corresponds to 1Hz frequency change per 1 MHz center frequency. It indicates how much actual center frequency is shifted (offset) with respect to desired one.

4.3.2 Second Harmonic Distortion (HD2):

On whatever frequency the signal is transmitted, it'll have its harmonics in multiple of the original frequency. HD2 is the second multiple of original frequency. Our

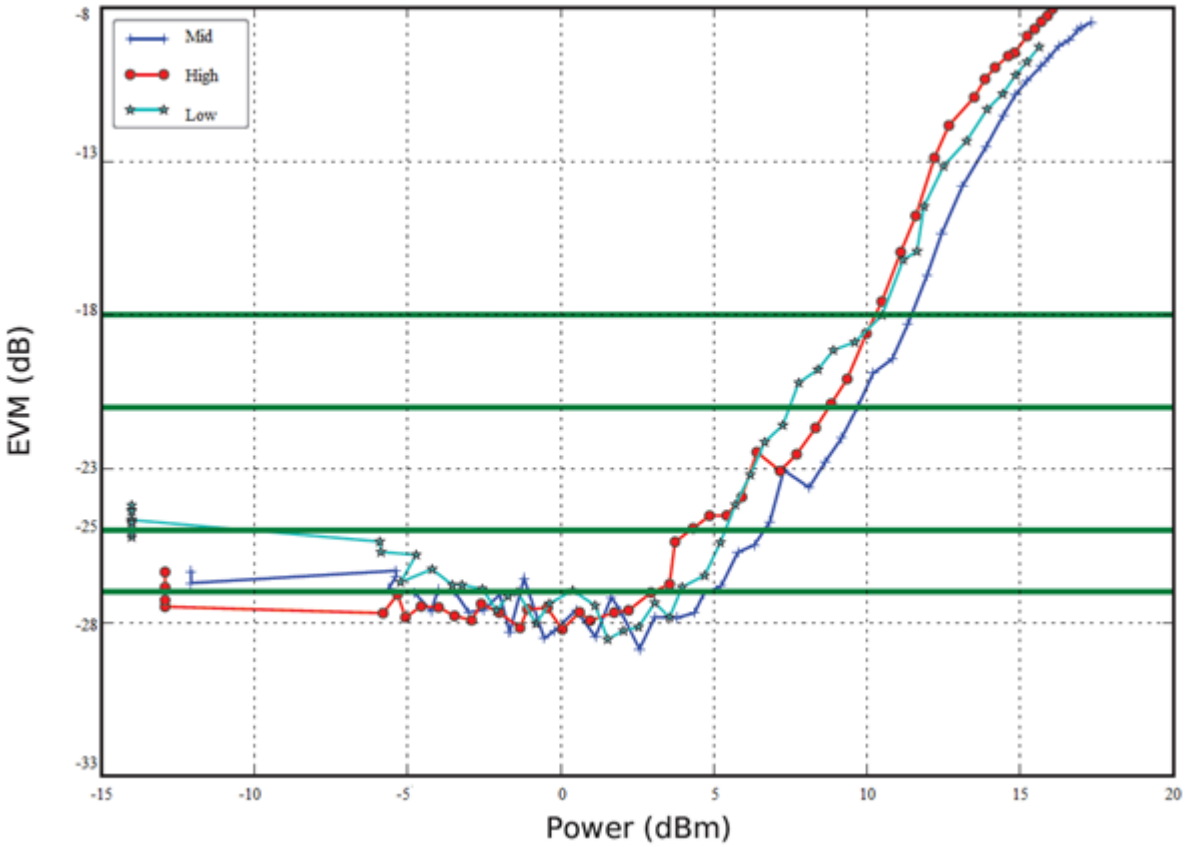

Figure 4.3: EVM Vs Output Power

signal should confine within the defined band, but due to signal's harmonics we get undesired signal out of the defined band. The power level of this undesired harmonic signal should be below some standard level. The test is run on the transmitter testbed to check whether undesired harmonic signal power level is below the standard level or not.

4.3.3 Transmitter Power Control (TPC):

Concept:

As power consumption is primary goal in any chip design, during transmission it is always better to transmit with highest efficiency. For that depending on run-time condition, power need to be adjusted to particular value. But, this task cant be done manually. So there is provision to set desired power level according to conditions, and dedicated hardware with help of firmware ensures that power at antenna out is remains in around desired power level.

Working:

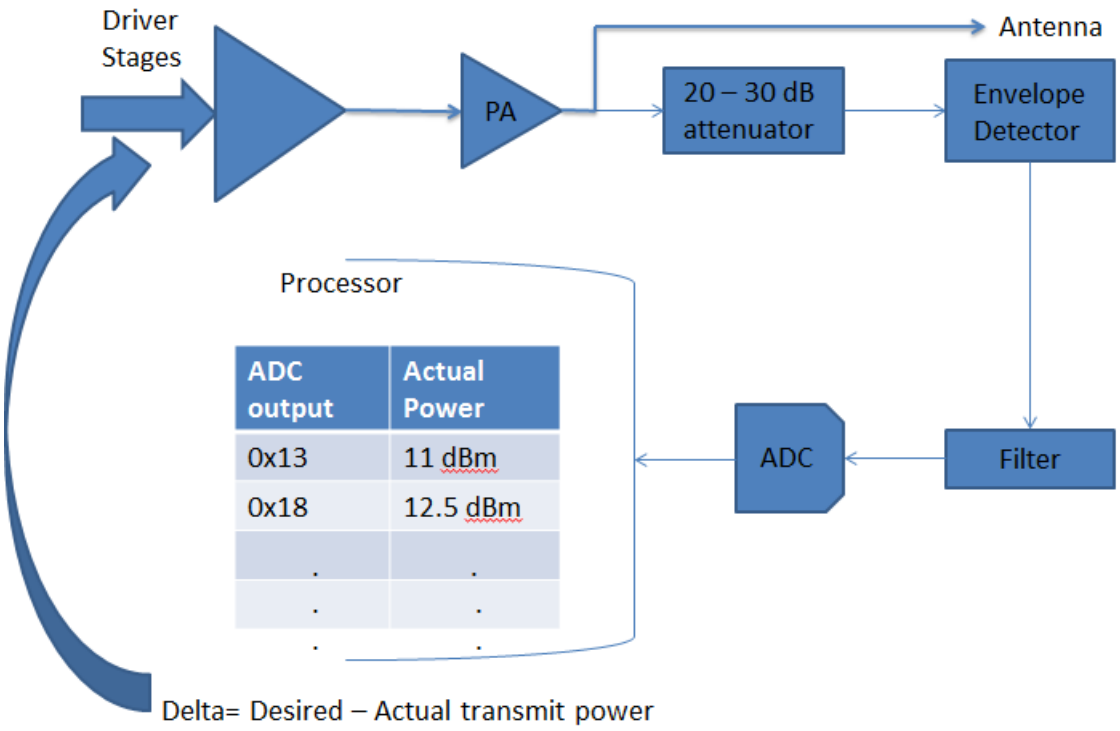

Figure 4.4: Block diagram of TPC hardware

There are driver stages prior to PA to control various PA settings. In general, PA output goes to antenna. So, it is being tapped at PA output and fed to envelop detector after attenuating signal by 20-30 dB. Output of detector, is then passed through filter to get smooth DC analog voltage which basically corresponds to power at antenna out. This is also known as TSSI.

Its corresponding digital value is sourced to processor through ADC, which is then used by processor to determine power actual power from LUT which is already built while intializing the chip.

Then, depending on delta between desired and actual power, driver stages adjust settings of PA to converge power at antenna out to the desired value.

Results:

The Figure shows the TSSI results across various powers. The gray dashed line indicates he estimated power from calculations of normalized tssi val using a polynomial equation and the dotted points indicate the measured power from a power meter for different channels 1, 7, and 13. It can be seen that measured power falls exactly on the estimated power. This tells that the chip is estimating the power

exactly across channels.

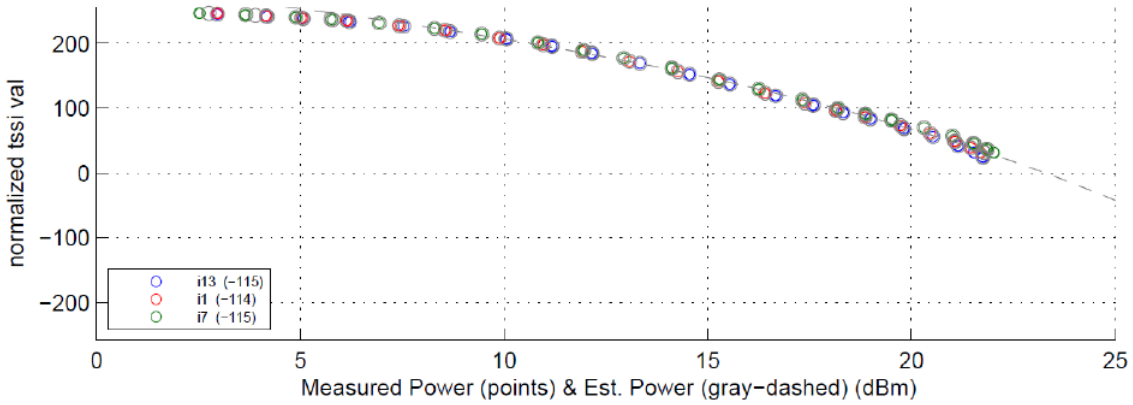

Figure 4.5: TSSI Result Graph

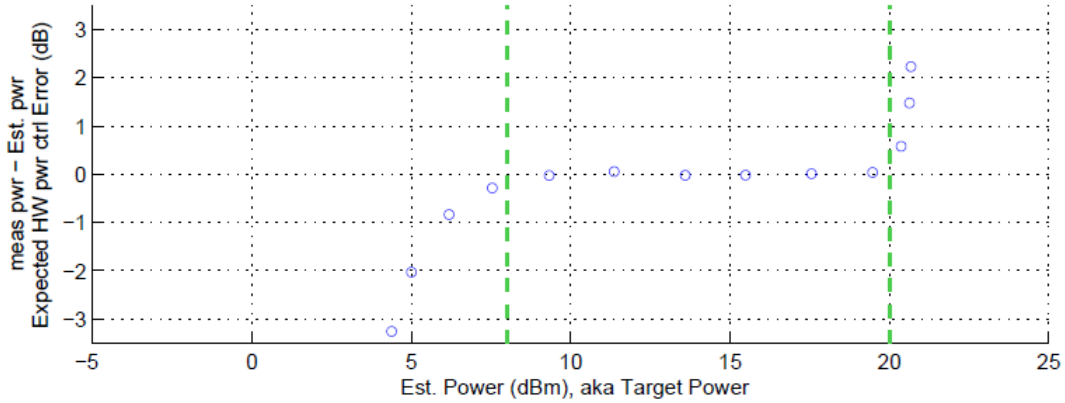

Figure 4.6: TPC Result Graph

Figure. 4.6 shows that for particular band of power levels, TPC works with zero error; otherwise error increases drastically on both sides of that band.

4.4 Receiver Test

Main performance measured at receiver side is sensitivity . In this section, sensitivity of the receiver is measured and calculated.

4.4.1 Receiver Sensitivity:

Receiver systems are normally required to process very small signals. The weak signals cannot be processed if the noise magnitude added by the receiver system is larger than that of the received signal. Increasing the desired signals amplitude is one method of raising the signal above the noise of the receiver system. Signal amplitude can be increased by raising the transmitters output power. Alternately, increasing the antenna aperture of the receiver, the transmitter, or both allows a stronger signal at the receiver input terminals. Increasing the physical size of an antenna is one method to increase its aperture[11].

Higher heat dissipation is typically required to increase transmitter output power. Cost, government regulations, and interference with other channels also limit the transmitter power available for a given application.

Increasing receiver antenna size obviously increases the housing size for portable product enclosing the antenna structure, such as a cellular telephone or pager. Because raising the desired signal amplitude above the noise added by the receiver may not always be practical, a weak signal might be processed by lowering the added noise. In this case, the noise must be decreased such that the noise amplitude is somewhat below the weak signal amplitude. Depending on the RxPER the sensitivity of the receiver keeps on varying[12].

Test procedure:

First the access point (AP) is initialized and made ready to transmit packet and then DUT is initialized to receive the packet from reference DUT. The number of packet transmitted and the number of packets received are measured. Depending on no. of packets received and decoded, the PER is calculated. During this period, power transmitted by access point is continuously monitored using power meter.

If PER at DUT side exceeds 10% at perticular power level of AP, then that power level is considered as “Sensitivity of DUT”.

Result Plots and Inferences :

Receiver sensitivity is defined as minimum signal power required to detect the

signal with Packet Error Rate (PER) less than 10%. This test is performed on receiver station.

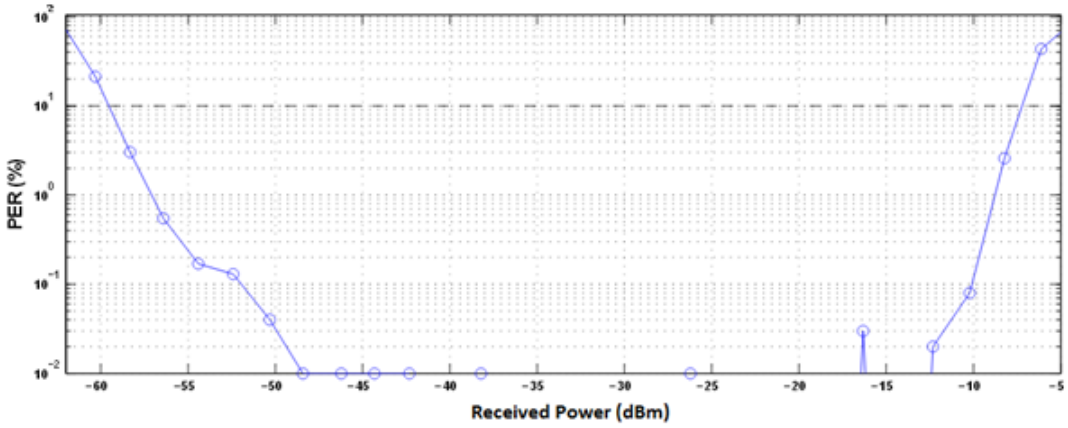

Figure 4.7: Packet Error Rate (PER) for Different Received Power Levels

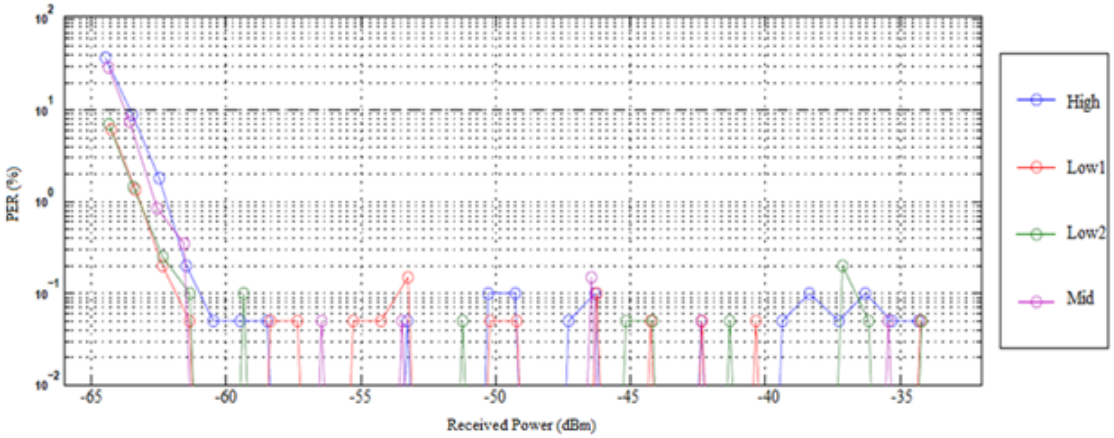

Figure 4.8: PER Vs Received Power for different WLAN channels

Reference transmits packets within a particular power range in discrete manner and at DUT side, for each power level PER will be calculated. Result of the test is a plot of PER Vs Received Power.

Receiver sensitivity is defined from the Plot of PER Vs Received Power. As we can see from Figure 4.7 that power corresponding to cross over point of actual curve and 10% PER threshold is sensitivity of the receiver.

Due to fading, high frequency signal undergoes more attenuation with distance. As a result of that high frequency channel will be having less sensitivity as compared to Mid and Lower frequency channels. This can be observed from the Figure 4.8.

4.4.2 Jammer Experiment:

Purpose :

To check at how much minimum distance jammer device can reside without affecting faithful reception of DUT.

Methodology and Analysis :

Figure 4.9 shows setup made to do this jammer experiment. DUT and AP are initialised in channel X; whereas, remote device means jammer is initialised in channel Y.

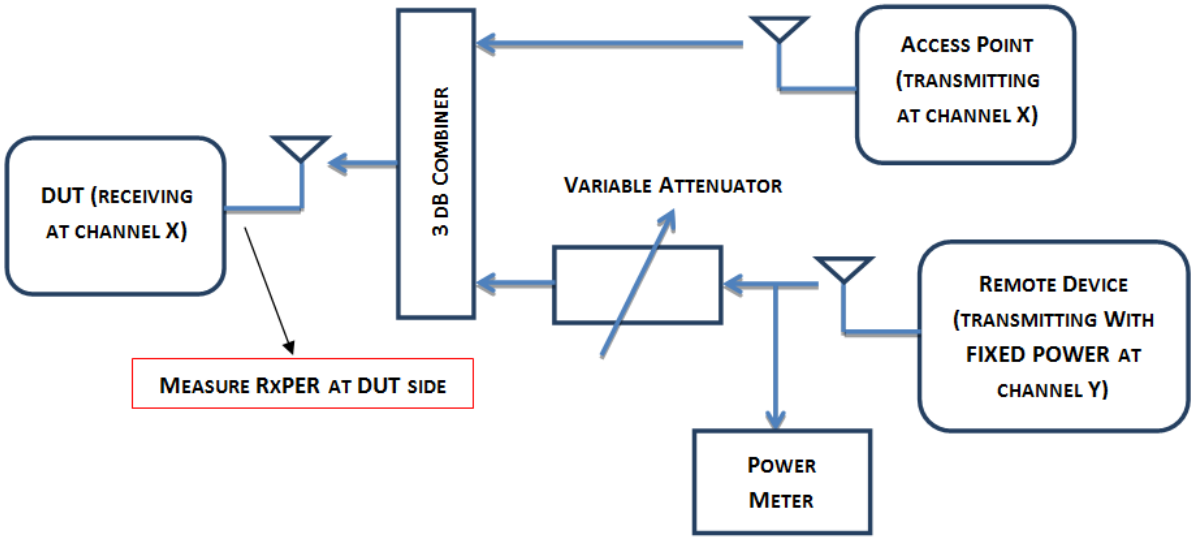

Figure 4.9: Jammer experiment setup

In this experiment, initially, jammer tx is kept off and dut in rx active mode and it receives packets from the AP. At this time, RxPER is measured which is called baseline RxPER. After that, jammer is made to transmit at fixed particular power which is continuously monitored by power meter. Attenuation between dut and jammer is varied which gives feel of distance between dut and jammer being varied. At every attenuation value, RxPER at dut side is measured.

The atteunation value at which, RxPER value at dut will cross some threshold predefined mark, test will be stopped. One thing is that, more attenuation indicates more distance between dut and jammer; whereas less attenuation means less distance.

We started with lower attenuation and then went n increasing it. At one particular attenuation value, RxPER went below required threshold, indicating faithful

reception on dut side from AP. This indicates that minimum attenuation required between DUT and any other remote device which transmitting at fixed power level.

4.5 Summary

This chapter explains about transmitter and receiver tests along with results and analysis. Basic test setup is also explained with its various types.

Chapter 5

Debug Issues

5.1 Chip Start-up Sequence

There is particular predefined steps which are hard-coded in chip are followed when chip is powered on.

Figure. 5.1 shows expected current waveform during chip power-up. Supply current starts ramping up from the instance chip is powered on. In waveform, as we can see, there are certain peaks whose magnitudes are predefined according to customers specifications. Because, these peaks affect overall average current consumption by chip during power on.

During start-up, initially switching regulators and crystal are turned on. Then, second large spike corresponds to power on of LDO supplying to radio section, particularly PA. After that, MAC layer and other digital circuitry gets power.

So, this is start-up sequence consumes some predefined average current which if exceeded creates a serious issue to be debugged.

Issue:

When actual current graph of start-up sequence was captured, it was observed that average current is more than expected. This difference was observed at battery supply current level, but actually which part of chip is consuming more current during power on, was actual debug issue.

Debug process:

To debug this issue, we used process of elimination. As from general power

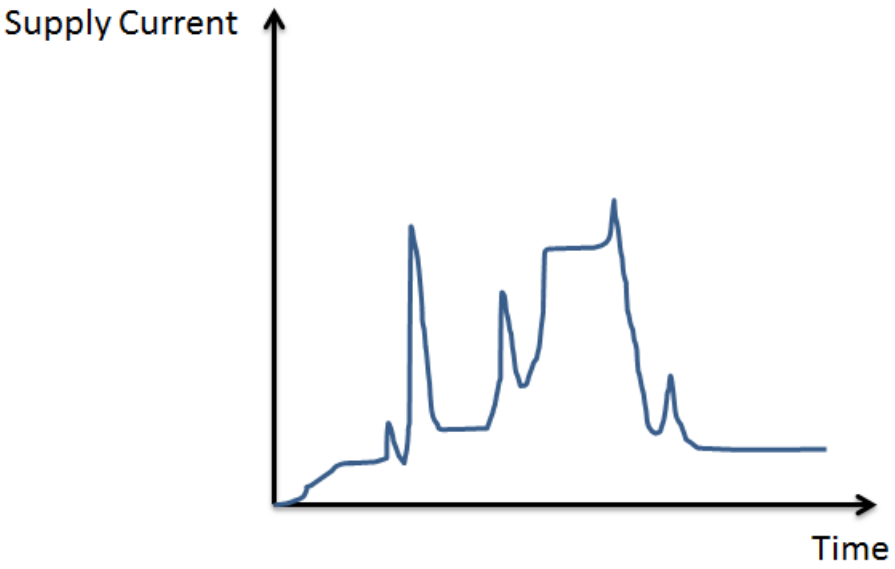

Figure 5.1: Expected current waveform

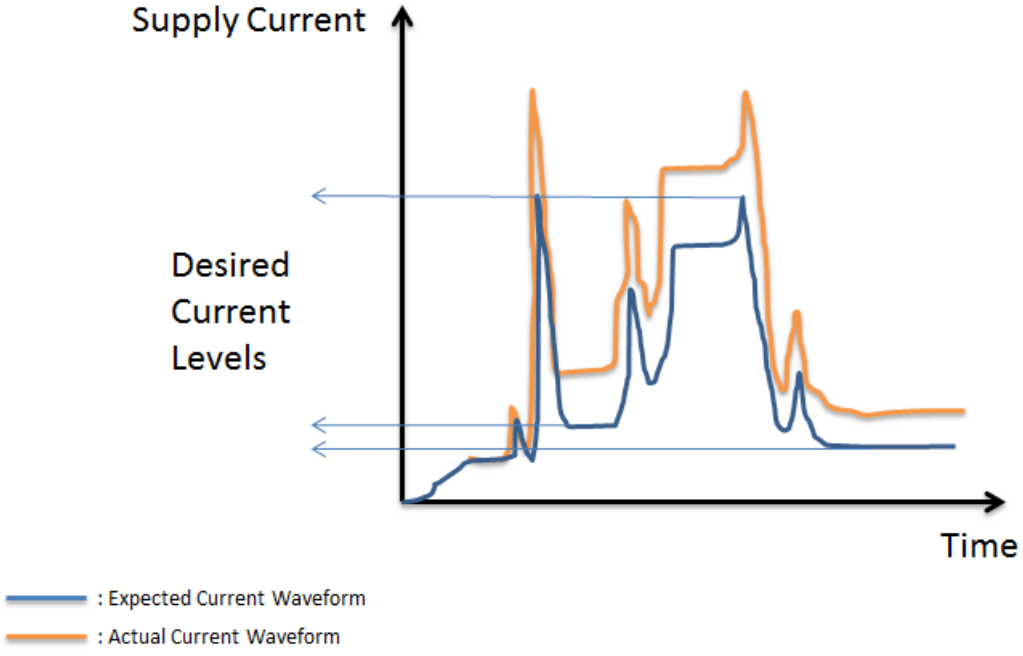

Figure 5.2: Actual current waveform

topology, we knew that through which path supply current reaches to individual block in chip.

As battery supply directly goes to switching regulator and LDO of RF section,

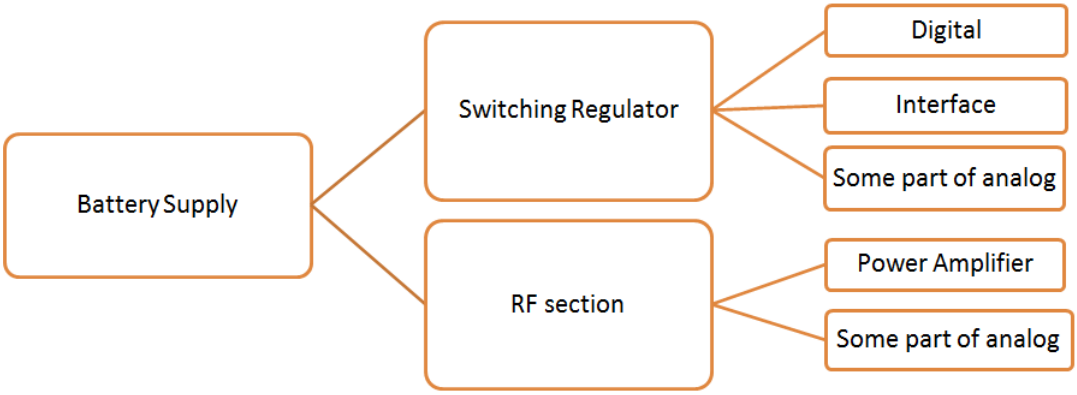

Figure 5.3: Simplified power topology

we checked current graph at output of switching regulator and RF section. But, we found SR output to be clean and rf section output to be suspicious. So, moved further down the line of RF section and found culprit to be LDO of PA which was not get turned off properly to zero once it is made on during power on.

To debug this issue, we used automated current method of CM. In this, instead of switching from one rail to another, we locked the ammeter into only one desired current rail and observed the current graphs. This way, we debugged the issue, and informed the concerned team to look into it.

5.2 Crystal Tuning:

During chip design phase, crystal oscillator circuit design is of prime importance. There are many cases, where due to lack of attention towards oscillator circuitry, whole project gets delayed. After giving proper attention also, theoretical design is not always work as expected when it is actually manufactured and got integrated with the other system circuitry. Hence, whenever chips come for testing, one of the initial tasks is to verify crystal oscillator circuit performance.

Issue:

While transmitting single tone, crystal frequency offset was crossing its predefined threshold value (ppm) with time which was not acceptable.

Debug process:

A crystal oscillator circuit which is practically implemented, is shown in Figure. 5.4. It comprises of Quartz Crystal, inverter (inside chip IC), 2 resistors and 2 capacitors.

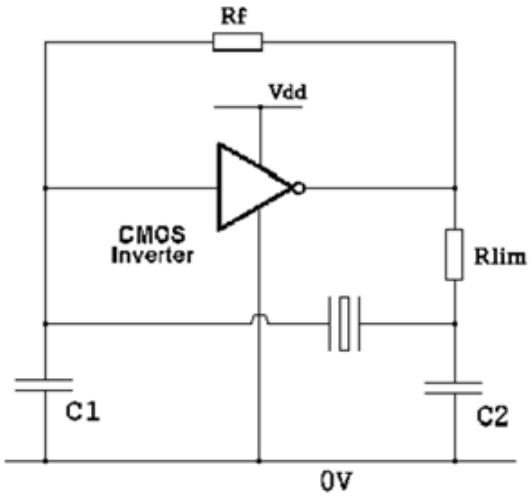

Figure 5.4: Crystal Oscillator Circuit [20]

In this type of setup the crystal is said to be in parallel resonant mode. The inverter which is internal to the WLAN chip acts as amplifier and provides approximately phase shift of 180deg. with respect to output from input and the PI type network formed by the quartz crystal, RLIM, C1 and C2 provides additional phase shift of 180deg. So the round the loop phase shift is of 360deg. One of the conditions required to sustain oscillation gets satisfied with this. The other condition required for proper start-up and sustained oscillation is that circuit should provide loop gain, around the closed loop, equal to or greater than 1.

The resistor Rf around the inverter acts as negative feedback resistor and settles the bias point of the inverter near middle of the supply, operating the inverter in the high gain linear region. The resistor value is high, usually in the range of a 500KW 2MW.

As frequency was getting set properly at the beginning, tank circuit should not have any problem. So, we did experiment to check dependency of Rlim on this frequency offset.

RLIM:

Working oscillator circuit can be made using only capacitors without Rlim; but, drive power of crystal will cross recommended value set for this design. Addition of

Rlim will certainly decrease crystal drive power; but, it will also reduce loop gain to the extent from where the oscillator may not start. As, there is no straight-forward relation of Rlim to actual crystal power dissipation and loop gain, we use a rule of thumb, which says that, start design with Rlim = the reactance of C2 (at the required oscillator frequency) [20].

In our case, initially Rlim was 3Kohm. As it reduces the loop gain, with this value, loop gain was very near to 1. After some time of operation, this loop gain due to time and heating, going down. As it was not having much margin over 1, it was coming below 1 and basic requirement for oscillation getting violated.

Then, we set it to 0 ohm, because of which gain increased too much and moved away from unity gain. It was equivalent to not having Rlim in the circuit. As seen from the graphs, it is clear that, because of no Rlim, time as well as frequency domain response was not so good.

That means we cant completely neglect Rlim. So, we chose value to be 240 ohms, which decreased loop gain; but still having good margin from 1. It also improved time and frequency domain response as shown in Figure. 5.4

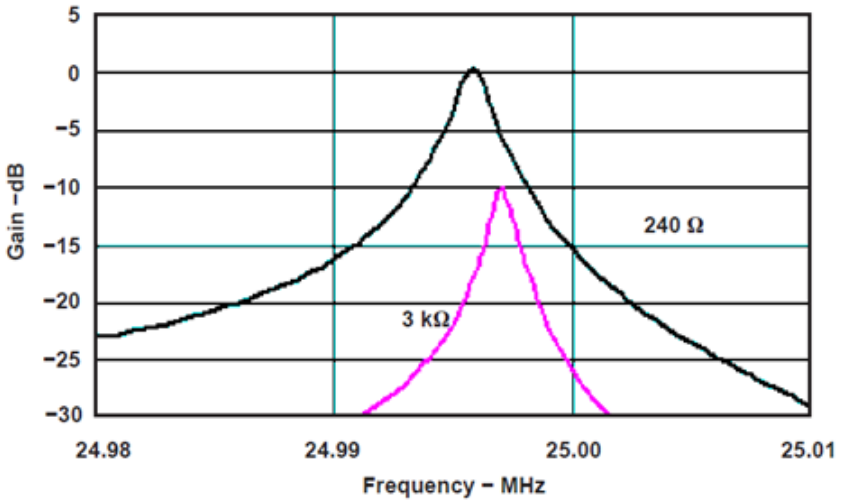

Figure 5.5: Effect of Rlim on Frequency Response of Feedback Network [19]

Ideally the inverter provides phase shift of 180deg., but the inherent delay of the inverter gives additional phase shift which is proportional to the delay. In order to ensure round the loop phase shift is n*360deg, the pi network should provide phase shift less than 180deg. due to the inverter delay. RLIM can be varied to accomplish this. The closed loop gain and phase can be altered by varying RLIM, by keeping fixed C1 and C2.

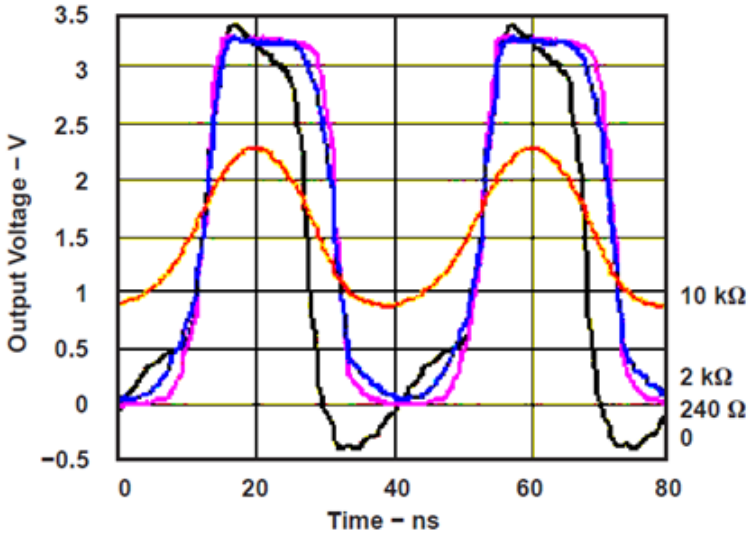

Figure 5.6: Effect of Rlim on Oscillator Waveform (25 MHz) [19]

5.3 Third Order Intermodulation Products:

Nothing (neither chip nor test boards) is perfect or works as expected, when it comes from foundry. Any chip, at very initial stage of bring up, need to be calibrated for their performance to be on expected lines.

Issue:

In wlcsp package, third order inter-modulation product (IM3) value for higher power tones was exceeding predefined threshold value and thus, degrading transmission performance parameters like EVM. Effect of Digital Pre-distortion (DPD) on IM3 was very negligible.

Debug process:

There are many non-linear devices in transmitter chain like Mixer, gain amplifier and major one is power amplifier (PA). When any frequency passes through devices apart from desired frequency, its harmonics also get generated. When more than one tones of various frequencies pass through these devices, along with baseband tones, various inter-modulation products also get generated.

As the issue was related to higher IM3 value, first we reproduced that problem. For that following experimental setup was used. (Refer Figure 5.7)

Non linearity of the PA gives rise to the harmonics and inter-modulation products, which significantly reduces the original signal integrity. Hence, in any WLAN

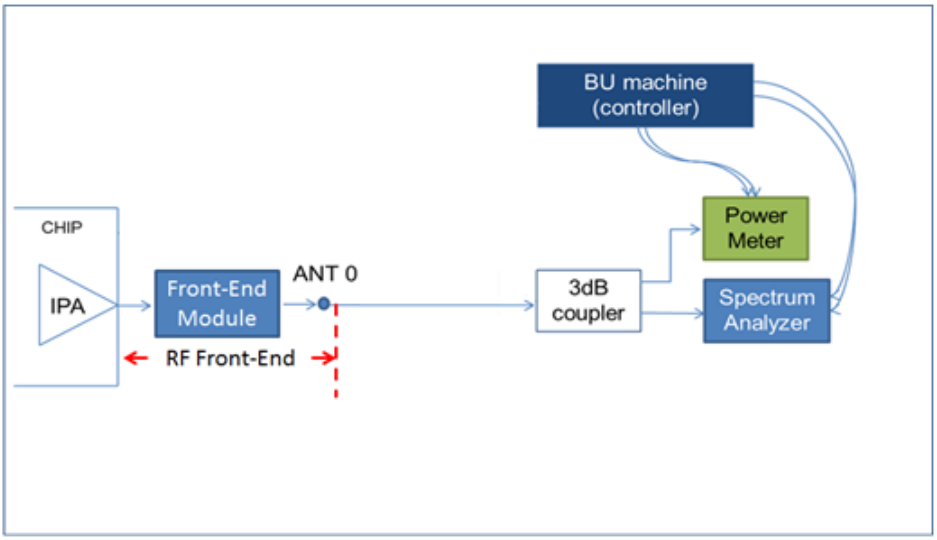

Figure 5.7: Experimental Setup for analyzing the inter-modulation products

system, where 52 subcarriers per bandwidth are used for signal transmission, linearity of the power amplifier is very much important factor for the signal integrity.

Figure 5.7, is an experimental setup used for analyzing the inter-modulation products. Spectrum analyzer is used to capture the frequency response of the tones of interest and their corresponding harmonics. Power meter is used to keep the track of the total output power of the packet being transmitted from the chip.

Chip by itself can be made to generate 2 tones using same Local Oscillator which is combined and given out by the chip. The signal coming out of the chip-out can be passed through the FEM and it reaches the antenna port after passing through different matching networks, diplexer, and different switches present in the RF path.

Signal hence available at the output is captured and analyzed by feeding it to power-meter and spectrum analyzers.

In the above experiment, keeping the center frequency as 5180MHz, 2 tones were transmitted with the frequency offset of +3MHz and +5MHz respectively. It can be seen that the inter-modulation products coming up at $2f2 - f1$ and $2f1f2$ respectively at +7Mhz and +1MHz.

IM3 values for complete power sweep are obtained with channel 5530Mhz with desired tones at the offset of 2Mhz and 3Mhz. So, there IM3 products will appear at frequencies 5531Mhz and 5534Mhz.

Digital pre-distortion is used to increase the linearity of PA and decrease IM3

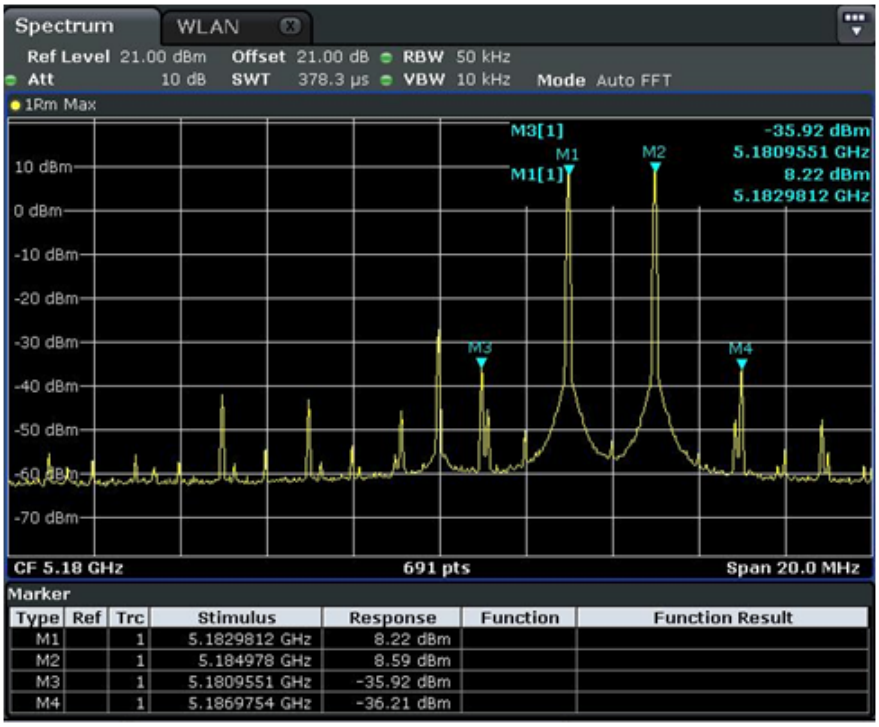

Figure 5.8: Tones and their IM products at power level of approx. 8dBm

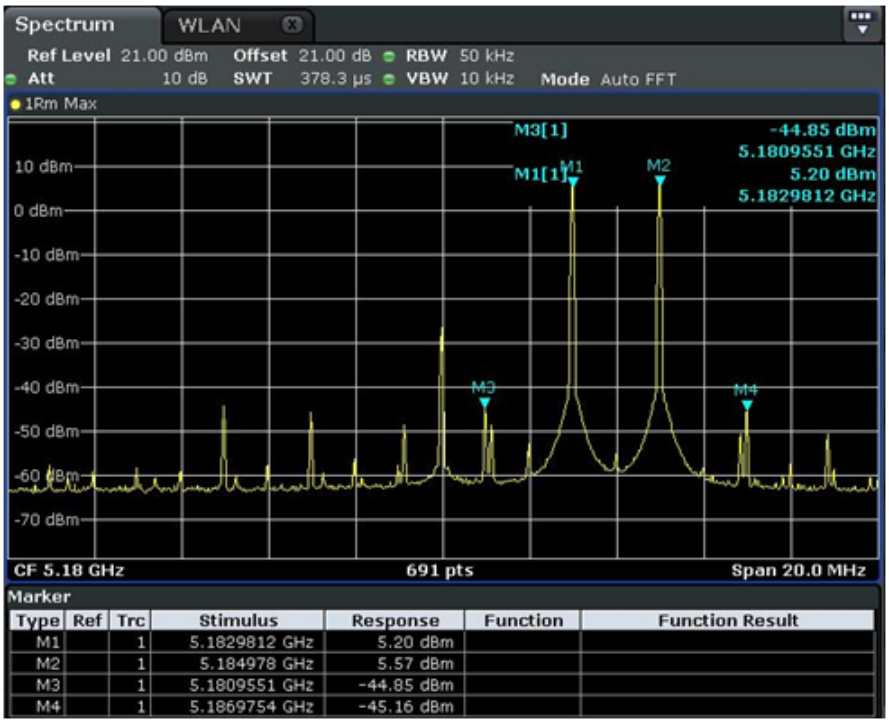

Figure 5.9: Tones and their IM products at power level of approx. 5dBm

Channel	f1_pow (dBm)	f1_freq (Mhz)	f2_pow	f2_freq	IM3_pow1	IM3_freq1	IM3_pow2	IM3_freq2
5530	18.343	5532.041	18.177	5533.039	2.761	5531.042	2.985	5534.038
5530	-37.501	5532.518	17.833	5533.039	0.541	5531.042	0.881	5534.038
5530	-41.121	5532.344	17.441	5533.039	-2.643	5531.042	-2.131	5534.038
5530	-40.503	5531.823	16.941	5533.039	-8.731	5531.042	-7.704	5534.038
5530	16.412	5532.041	16.302	5533.039	-24.058	5531.042	-20.256	5534.038
5530	-45.124	5532.344	15.543	5533.039	-9.380	5531.042	-10.306	5534.038
5530	14.526	5532.041	14.477	5533.039	-7.452	5531.042	-7.965	5534.038
5530	-43.402	5532.475	12.922	5533.039	-13.193	5531.042	-13.585	5534.038
5530	11.759	5532.041	11.704	5533.039	-19.404	5531.042	-20.209	5534.038
5530	10.671	5532.041	10.657	5533.039	-24.549	5531.042	-25.616	5534.038
5530	-51.580	5532.475	9.277	5533.039	-27.880	5531.042	-29.242	5534.038
5530	8.187	5532.041	8.171	5533.039	-33.910	5531.042	-36.685	5534.038
5530	-55.485	5532.301	5.688	5533.039	-41.417	5531.042	-44.409	5534.038
5530	4.270	5532.041	4.270	5533.039	-45.328	5531.042	-48.124	5534.038
5530	2.984	5532.041	2.957	5533.039	-48.624	5531.042	-48.548	5534.038
5530	-61.257	5532.518	1.785	5533.039	-60.597	5531.520	-67.034	5533.821

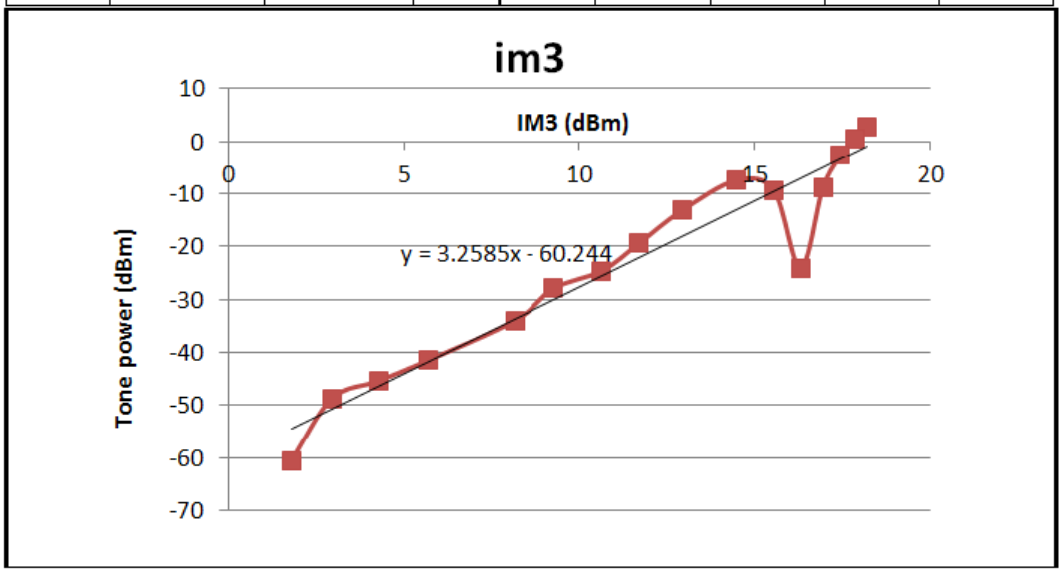

Figure 5.10: IM3 vs Transmitted Power

values. But, as here, we have observed that with and without DPD, value of IM3 was remaining same. That indicates that either DPD not happening properly or there is some issue with board design. Hence, respective teams are informed to look into this matter.

5.4 Summary

This chapter discusses about the various issues faced, reasons behind them and methodology adapted to debug these issues.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The wireless communications systems are influenced by various factors like cost, frequency bands, power consumption, functionality, size, volume of production, and standards. Due to increase in IoT market, recently, Wi-Fi functionality is getting more importance. It has been integrated with many applications making smoother pass-way to WLAN into mass-consumer markets. There is also high demand for increased data rates for communication. Due to all these, IEEE 802.11 standards have significantly gone under scanner and have continuously upgraded to higher specifications without making compromise with acceptable RF performance.

One of the ways of doing quantitative analysis of power consumption is measuring currents drawn by various modules of chip. Using automated current method explained in section 3.5, various current values are measured during various states of WLAN chip like off, listen, active and reset. Based on measurements done, power optimisation techniques can be properly designed to reduce current consumption of specific block inside the chip. Issues faced during CM, discussed in chapter 3, are overcome by using fundamentals of electronic circuit theory and VLSI design. As per simulation results, we have experimentally analysed thermal problem related to WLAN chip along with air-circulation effect.

While performing CM, there were issues which are not related to measurement setups. Then, to debug those issues, RF performance parameters of WLAN chip were tested and analysed. Based on simulation results shown in chapter 4, corrective measures were taken to improve RF parameters.

Automated current method is efficiently utilized to debug major power con-

sumption related issues, as described in chapter 5. There are many issues which came during automation process which are solved with trial and error method.

6.2 Future Scope

Whatever modifications are done in CM setup to improve its accuracy, can be incorporated in board design itself, in future. Later, CM setup can be made fully automated so that anybody can perform CM on its own without help of any particular person.

Bibliography

[1] Discussion on ResearchGate - What is the basic idea behind the twisted pair? Why are the two wires twisted? How does this arrangement compensate undesirable distubances? [Online]. Available: *http* : *//www.researchgate.net/post/What_is_the_basic_idea_behind_the_twisted_pair_Why_are_the_two_wires_twisted_How_does_this_arrangement_compensate_undesirable_disturbances*

[2] Inductive Coupling and how to Minimize their Effects in Industrial Installations [Online]. Available: *http* : *//www.smar.com/en/technical − article/inductive − coupling − and − how − to − minimize − their − effects − in − industrial − installations*

[3] Conquer The Challenges Of High-Current Pulses [Online]. Available: *http* : *//electronicdesign.com/test − amp − measurement/conquer − challenges − high − current − pulses*

[4] Understanding Low-Power IC Design Techniques [Online]. Available: *http* : *//electronicdesign.com/power/understanding − low − power − ic − design − techniques*

[5] Linear or LDO Regulators Step-Down Switching Regulators [Online]. Available: *http* : *//www.aivaka.com/LDOvsSPC.pdf*

[6] Maxim Integrated Wireless Technology Tutorial [Online]. Available: *http* : *//www.maximintegrated.com/en/images/appnotes/*4651*/index.cfm*

[7] Shairi, N.A.; Rahman, T.A.; Aziz, M.Z.A.. *RF Receiver System Design for Wireless Local Area Network Bridge at 5725 to 5825 MHz*, Asia-Pacific Conference on Applied Electromagnetics Proceedings

[8] Arya Behzad; *Wireless LAN Radios, System definition to Transistor design.* IEEE Press, 445 Hoes Lane, Piscataway, NJ 088854

[9] Rashad.M.Ramzan,*Flexible Wireless Receivers: On-Chip Testing Techniques and Design for Testability*, Dissertation No. 1261, Linkping Studies in Science

and Technology, Department of Electrical Engineering Linkping University, SE-581 83 Linkping, Sweden Linkping

[10] Atheros communication. *Power Consumption and Energy Efficiency Comparisons of WLAN Products*, White paper [Online]. Available: *http* : *//www.qca.qualcomm.com/wp* − *content/uploads/*2013/09/$Power_Consumption_whitepaper.pdf$

[11] Choong-yul Cha and Sang-Gug Lee. *A 5.2GHz LNA in 0.35um CMOS Utilizing Inter -Stage Series Resonance and Optimizing the Substrate Resistance*, IEEE Journal of Solid State Circuit, Vol.38, No.4

[12] P. Leroux and M. Steyaert. *High-performance 5.2GHz LNA with on-chip inductor to provide ESD protection*, Electronics Letters, Vol.37, No.7

[13] Opto-isolator [Online]. Available : *http* : *//en.wikipedia.org/wiki/Opto* − *isolator*

[14] Peter Abiodun Bode, *Current measurement applications handbook*

[15] Power supply Remote Sense mistakes remedies [Online]. Available : *http* : *//www.edn.com/electronics*−*blogs/power*−*supply*−*notes/*4418253/*Power*−*supply* − −*Remote* − *Sense* − −*mistakes* − − − *remedies*

[16] Agilent Technologies Low-Profile Modular Power System Series N6700 - Users Guide

[17] Integrating traditional and modular test instruments [Online]. Available: *http* : *//www.edn.com/design/test* − *and* − *measurement/*4389598/*Integrating* − *traditional* − *and* − *modular* − *test* − *instruments* − 4389598

[18] SCPI Programming: Strenghts and Weaknesses [Online]. Available: *http* : *//www.edn.com/electronics* − *blogs/test* − $cafe$/4424791/$SCPI$ − *programming* − −*Strengths* − *and* − *weaknesses*

[19] Use of the CMOS Unbuffered Inverter in Oscillator Circuits [Online]. Available: *http* : *//www.ti.com/lit/an/szza*043/*szza*043.*pdf*

[20] Rakon Limited, *IC CRYSTAL OSCILLATOR CIRCUITS*.