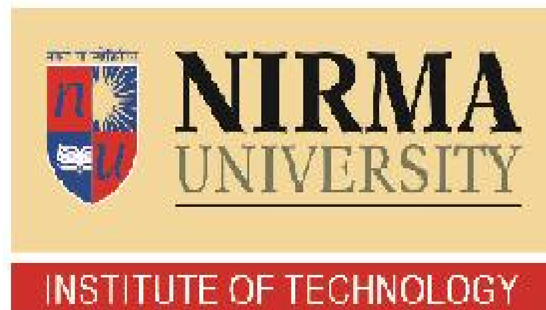
Validation of mixed signal IP building blocks

Major Project Report

Submitted in partial fulfillment of the requirements
For the degree of

Master of Technology
In
Electronics and Communication Engineering
VLSI Design

By
Dushyantsinh V. Dabhi
13MECV02



Electronics &Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
Nirma University
Ahmedabad-382481
May 2015

Validation of mixed signal IP building blocks

Major Project Report

Submitted in partial fulfillment of the requirements
For the degree of

Master of Technology
In
Electronics and Communication Engineering
(VLSI Design)

By
Dushyantsinh V. Dabhi
13MECV02

Under the guidance of

Mrs. Priya J. Adavi	Dr. Amisha P. Naik
Engineering Manager	Associate Professor

Electronics &Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
Nirma University
Ahmedabad-382481

May 2015

DECLARATION

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in Communication Engineering at Nirma University and has not been submitted elsewhere for a degree.
b. Due acknowledgement has been made in the text to all other material used.

-Dushyantsinh Dabhi
13MECV02

DISCLAIMER

“The content of this paper does not represent the technology, opinions, beliefs, or positions of Intel Technology India Pvt. Ltd. its employees, vendors, customers, or associates.”

CERTIFICATE

This is to certify that the Major Project entitled “Validation of mixed signal IP building blocks" submitted by Dushyantsinh V. Dabhi (13MECV02), towards the partial fulfillment of the requirements for the degree of Master of Technology in VLSI Design, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

Dr. A. P. Naik
Internal Project Guide

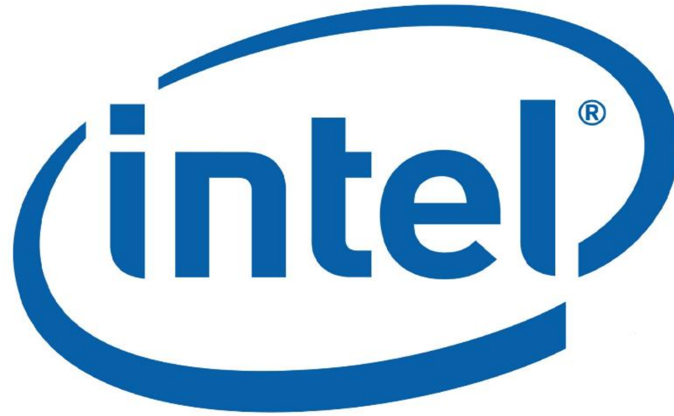
Dr. N. M. Devashrayee
Program Coordinator

Dr. P. N. Tekwani
Head of EE Dept.

Dr. Ketan Kotecha
Director, IT-NU

Date:

Place: Ahmedabad



Intel Technology India Pvt. Ltd.

Certificate

This is to certify that the project entitled **"Validation of mixed signal IP building blocks"** submitted by **Dushyantsinh Vikramsinh Dabhi (13MECV02)**, towards the submission of Project for requirements for the degree of Master of Technology in VLSI Design, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

Mr. Ananda N. Sitaraman
Engineering Manager,
IPG-MIG India,
Intel Technology India Pvt. Ltd.,
Bangalore.

ACKNOWLEDGEMENTS

First and foremost, sincere gratitude to my managers Mrs. Priya J. Adavi, Mr. Ananda Sitaraman and Mr. Iqbal Mohamed. Also I want to thank Intel Technology India Private Limited, Bangalore for assigning me such project and guide me through.

I would like to express my gratitude and sincere thanks to my mentor Mr. Amith Cm at Intel Technology India Private Limited, Bangalore for his valuable guidance throughout the internship, he has given me valuable advices and support for my project work which I am very lucky to benefit from.

I would also thank to my Program Coordinator, Dr. N. M. Devashrayee, Professor, VLSI Design, Institute of Technology, Nirma University, Ahmedabad for giving valuable the advice and support throughout the academic period.

I would also thank to my Project Coordinator, Dr. A. P. Naik, Professor, VLSI Design, Institute of Technology, Nirma University, Ahmedabad for giving valuable support for the project work.

I would also like to express my gratitude to all faculty members of Nirma University for providing encouragement, exchanging knowledge during my post-graduate program.

I also owe my colleagues in the Intel, special thanks for helping me on this path and for making project at Intel more enjoyable.

-With Sincere regards,
Dushyantsinh Dabhi
13MECV02

ABSTRACT

The amount of circuits on the chip is increasing day by day. These different circuits have to function under the all difficult operating conditions which include wide variation of the temperature, supply voltage and the process. Also the circuits must function properly during entire lifetime of the product. So, it is imperative to verify the reliability of the circuits at the extreme difficult condition in terms of fluctuation of supply voltage and the varying temperatures since these parameter will vary according to ambience. Each circuits in IP has its own specifications so to simulate its behavior different kind of analysis like transient analysis, DC analysis and AC analysis has to be carried out. In the reliability analysis we need to evaluate the impact of different phenomena like electro-migration, aging, burn in, Electrical over stress for the reliable operation of devices and interconnects of the circuits. The power dissipation is also a major concern in today's era of submicron regime as the feature size decrease the amount of leakage will be very high in the circuits. It is necessary to find the value of currents in active and standby mode when we are operating the circuits in the extreme corner where the supply voltage and temperature are having its peak values.

Table of Contents

Declaration iii

Disclaimer iv

Certificate v

Acknowledgements vii

Abstract viii

Chapter: 1 12

Introduction 12

1.1 Different building blocks in the SOC. 12

1.2 Introduction to DisplayPort Standard 13

1.3 Objectives of Display port 13

1.4 Circuit Validation challenges 14

1.5 Process Corners 15

Chapter: 2 17

Literature Review 17

2.1 Clocking Terminology 17

2.1.1 Synchronous 17

2.1.2 Mesochronous 17

2.1.3 Plesiochronous 18

2.1.4 Asynchronous 18

2.2 Electro-migration (EM) 19

2.2.1 Failure mechanism in electromigration 19

2.2.2 Electromigration Dependency on Physical Effects 20

2.3 Second-order effects considered in the QRE simulations 21

2.3.1 Hot Carrier Injection Effect (HCI) 21

2.3.2 Negative Bias Temperature Instability (NBTI) 23

2.4 Process Variation 24

2.4.1 Geometry variations of transistor: 25

2.4.2 Device material parameter variations: 25

2.4.3 Device electrical parameters variations: 25
2.4.4 Classification of process variation 26
2.4.5 Process variations in interconnects 27
2.5 Power dissipation in CMOS 27
2.5.1 Current components causing leakage 27
Chapter: 3 29
Validation of Clock Distribution Block 29
3.1 Introduction of clock distribution block 29
3.2 Difficulties in validating the CD block 30
3.3 Simulation results for the CD block 31
3.3.1 Output waveforms 32
Chapter: 4 33
Reliability Validation for Devices and interconnects 33
4.1 Why reliability validation of interconnects is imperative? 33
4.2 How to do the reliability validation of interconnects 33
4.3 Quality and Reliability of the Devices 34
4.4 Aging, Burn in and EOS simulations 34
4.5 How to do the Quality and Reliability simulations 36
Chapter: 5 38
Power simulation 38
5.1 Importance of power measurements 38
5.2 Low power techniques 39
5.2.1 Power gating 39
5.2.2 Power Sequencing 43
Conclusion 48
BIBLIOGRAPHY 49

List of Figures

Figure 1 Generic arrangement of IP blocks on the SOC 12
Figure 2 Process Variation 16
Figure 3 Synchronous clocking system 17
Figure 4 Mesochronous clocking system 18
Figure 5 Plesiochronous clocking system 18
Figure 6 Asynchronous clocking system 19
Figure 7 Void (open circuit) and hillock (short circuit) 20
Figure 8 Recursive effect of temperature 20
Figure 9 DAHC Injection 22
Figure 10 CHE Injection 22
Figure 11 SHE Injection 23
Figure 12 Generic arrangement of the clock distribution block 29
Figure 13 Effect of Duty cycle distortion on ON-OFF period 30
Figure 14 Waveforms of operating clocks 32
Figure 15 power supply ramp 35
Figure 16 power simulation measurement 38
Figure 17 Power gating 39
Figure 18 o/p waveforms for m=5 40
Figure 19 o/p waveforms for m=10 41
Figure 20 o/p waveforms for m=15 42
Figure 21 power sequencing example 43
Figure 22 power sequencing with firewall mechanism 44
Figure 23 schematic of full adder for power dissipation analysis 45
Figure 24 waveforms for full adder (inputs, outputs & control signal) 46

List of Tables

Table 1 Process Corners 15
Table 2 Constraints for the CD for functional simulations 31
Table 3 Constraints for aging, burn in and EOS validation 36
Table 4 Simulation result for m=5 41
Table 5 Simulation result for m=10 42
Table 6 Simulation result for m=15 43
Table 7 value of currents for “v1” supply 47
Table 8 value of currents for “v2” supply 47

Chapter: 1

Introduction

1.1 Different building blocks in the SOC.

There are different types of analog and digital blocks are present in the SOC. The blocks like transmitter, receiver, SerDes, Amplifier, Phase locked loop (PLL), Delay locked loop (DLL), Analog to Digital converter (ADC) and the Digital to Analog converter (DAC) are implemented on the SoC.

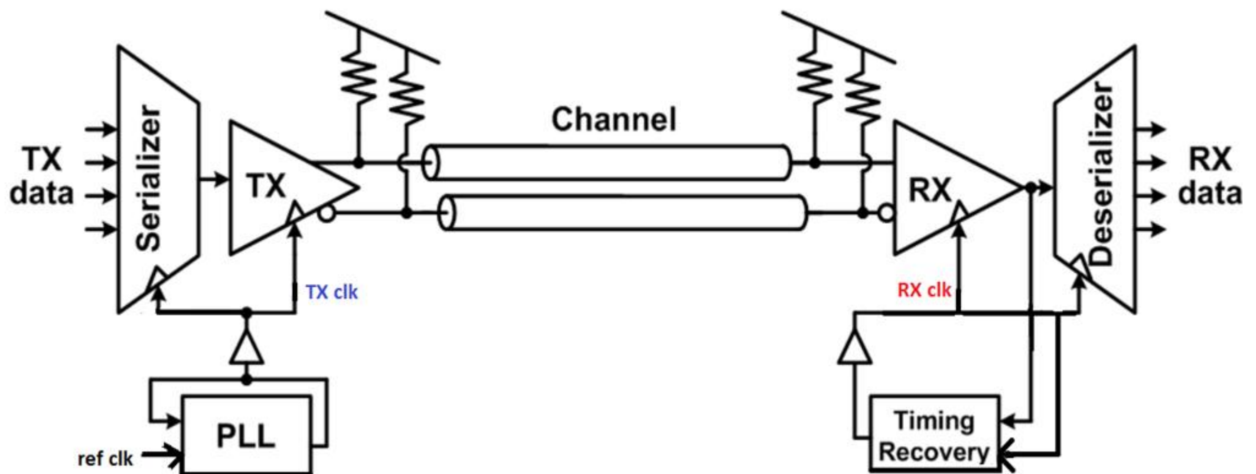


Figure 1 Generic arrangement of IP blocks on the SOC

The transmitter is used to send the data from one chip to the other chip or to the external world like from processor to graphic processor. The receiver will take the data and pass it to the core of the chip for the further processing. So, the transmitter and receiver will constitute the IO pads of the SOC.

PLL is basically used to convert the low frequency signal to the high frequency signal. As shown in figure Ref clock is say of 20MHz which is coming from the crystal oscillator. This signal is to be converted to 2GHz for the high data rate application. Phase detector, Low pass filter, divider and Voltage Controlled oscillator are incorporated to implement the PLL. At the receiving end in the timing recovery circuit PLL is used for Clocked Data recovery (CDR). At the receiver side from the incoming data and the reference clock the output clock frequency is generated.

Seriallizer-Deseriallizer are popularly known as SerDes. Seriallizer will convert the incoming parallel data to serial data and Deseriallizer do the opposite function. SerDes is implemented by using the buffer queue.

In the SOC we have multiple domain signals so to convert those signals into specific domain ADC and DAC are used.

1.2 Introduction to DisplayPort Standard

The DisplayPort standard used in digital interface used in both internal connections, such as interfaces within a laptop, mobile, tablet or monitor and any other external display connections which includes interfaces between a PC and monitor (projector), between laptop and television or external between a device such as DVD player and television.

It is an industry standard to accommodate the digital display technology within the PC and CE industries. It integrates internal and external connection methods to reduce complexity of devices, supports essential features for cross domain applications, and provides scalability in the performance to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

1.3 Objectives of Display port

This DisplayPort defines a scalable digital display interface. It is having the provision of audio and content protection capability for broad application within personnel machine and other hand held devices of consumer applications. The display port interface is designed such that it can support both internal chip-to-chip and external box-to-box digital display connections. Internal chip-to-chip applications include usage within a laptop or other hand held devices for driving its monitor panel from a graphics processor, and usage within a monitor or television for driving the display panel from a display controller.

1.4 Circuit Validation challenges

As the complexity of the Integrated Circuit (IC) increases and their size gets reduces. Nowadays ICs which have the amalgamation of digital and analog circuits. Each of these circuits have their own set of parameters so all of those parameters need to meet for the proper operation of the circuit. So, the task of validating these mixed signal circuit blocks will be daunting.

As the length of the device decreases the second order effects like short channel effects, narrow channel effects and other sub-micron effects will be dominant. These effects will degrade the performance parameter such as rise time, fall time, propagation delay etc. So, the painstaking effort is essential for validating the all the IPs (Intellectual Property) in the whole SOC (System on Chip).

To validate the functionality of these circuits we need to incorporate various kind of analysis like transient analysis, DC analysis and AC analysis. In addition to this we have to make sure that the circuits operates correctly in the hazardous conditions like at high temperature as well as fluctuations in supply voltage. It means that we must check the functionality at elevated temperatures, at the various supply voltages and the different skews. In the validation process these variations are consolidated as PVT corners. According to the requirements we will make the use of different PVT corners.

As we know the transistor count will be double on a die after eighteen months, our process of validation has to be completed during the specified time frame. The EDA tools are intelligent enough that the validation process can be expeditiously carried out with minimum percentage of bugs.

1.5 Process Corners

To understand the behavior of the circuit under all possible types of condition the corner case analysis is necessary. During the fabrication process engineer will consider many parameters they can be classified as geometrical parameters and device model parameters. The geometrical parameters includes the channel length and width of the MOS transistor whereas device model parameters includes threshold voltage, gate oxide thickness and carrier mobility.

Also the operating condition is an important measure for process engineers which includes the power supply and temperature other parameter also like pressure, humidity etc. Mainly, three types of process corners are used named as slow, typical and fast as shown in the table. But depending on the consumer requirement different cross skew analysis is also incorporated. In the cross skew analysis one device will be faster and its counterpart will be slower.

Table 1 Process Corners

Skew	**Temperature (C)**	**Supply Voltage (V)**
Slow	LOW	LOW
Typical	MEDIUM	MEDIUM
Fast	HIGH	HIGH

There are two types of process variation

1) Inter die variations
2) Intra die variations

In the Intra die variations on the same die during the fabrication process dose of dopant may increase or decrease so device fabricated on die will have slight variations in their threshold voltages. The thickness of oxide layer sometimes may vary which also affects the device property.

In the Inter die variation there is wafer level process variation. Each die has its own mechanical criteria so wafer prepared on different die might have different device properties.

The following diagram illustrates the skew variation of the device.

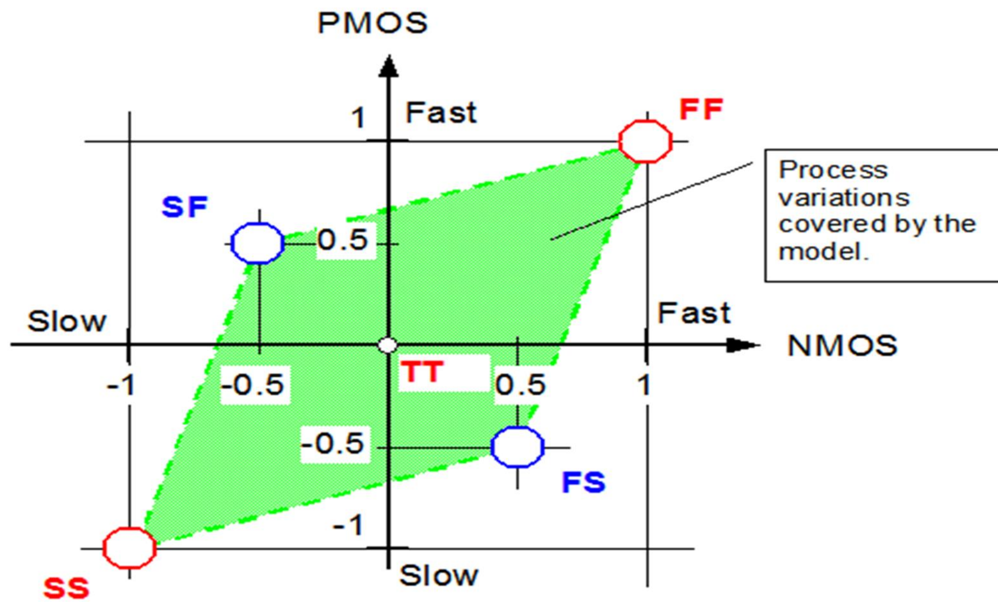


Figure 2 Process Variation

SS: NMOS-slow, PMOS-slow
FF: NMOS-fast, PMOS-fast
SF: NMOS-slow, PMOS-fast
FS: NMOS-fast, PMOS-slow
TT: NMOS-typical, PMOS-typical

Here, the X- axis represents NMOS and Y-axis represents PMOS. The SS and FF are extreme conditions. We will validate our circuits at these two corners, if the circuits work according to specs we qualify the circuit for other corners also. We have to validate the functionality of circuits at cross skew corner also i.e. one type of device is faster and other is slower than we have to run the circuits on these corners also. These cross skew analysis is especially carried out for analog building blocks in the SoC.

Chapter: 2

Literature Review

2.1 Clocking Terminology

There are four types of clocking mechanism are used depending on the operating frequency.

2.1.1 Synchronous

As shown in the figure in this mechanism the two circuit on the chip will get the clock signal with same frequency and the phase. Generally, this kind of technique is used in low speed buses where the frequency can rise up to 200 to 30MHz.

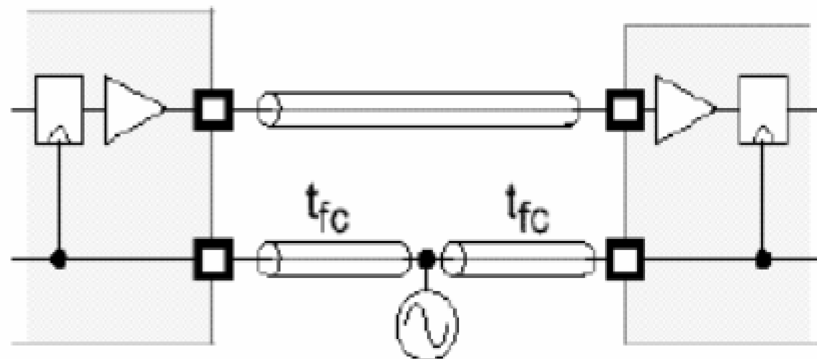


Figure 3 Synchronous clocking system

2.1.2 Mesochronous

As shown in the figure in this mechanism the two blocks on the chip will get the clock signal with same frequency but different phase. So, in this mechanism phase recovery circuit is imperative at the receiver end. It is used in fast memories, internal system interface and MAC packet interface. For CDR (Clocked Data Recovery) the DLL (Delay Locked loop) is used at the receiver end. It is used in medium frequency application up to 2GHz

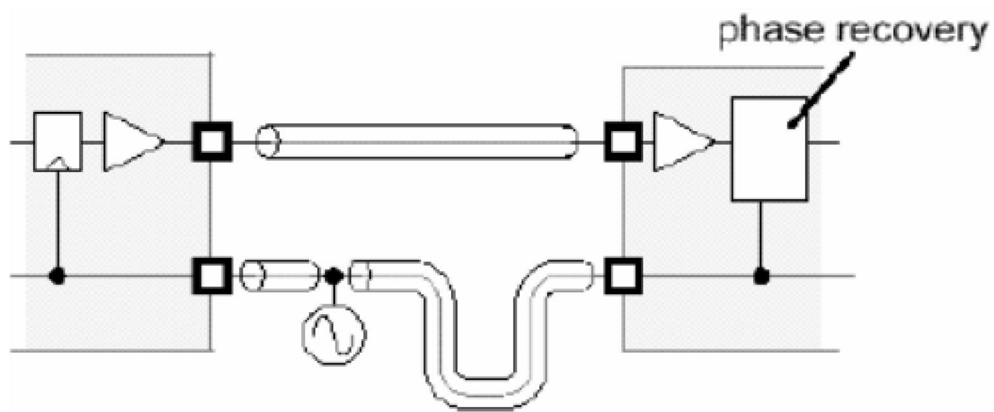


Figure 4 Mesochronous clocking system

2.1.3 Plesiochronous

In this clocking mechanism both the circuit on the chip will get almost the same frequency with slightly drift in the phase. Phase Locked Loop (PLL) is used at the receiving end for data recovery. It is widely used in high speed links.

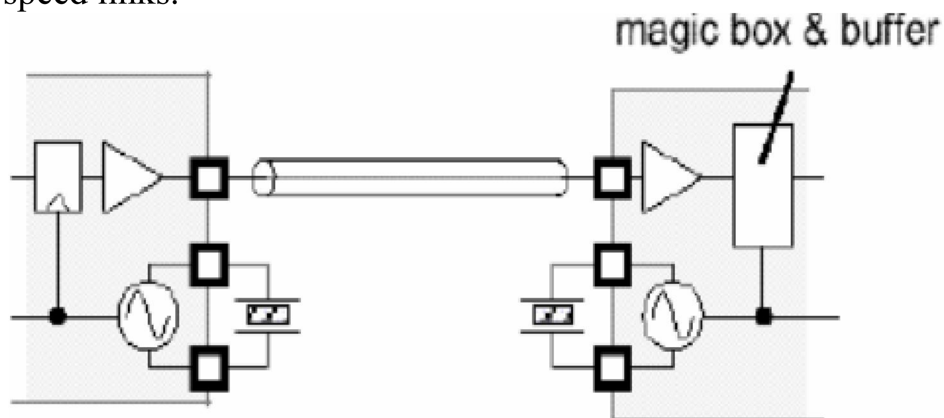


Figure 5 Plesiochronous clocking system

2.1.4 Asynchronous

In this technique as name suggests there is no clock involved. It operates on request and acknowledge handshake procedure. It is generally used in embedded system, UNIX, Linux.

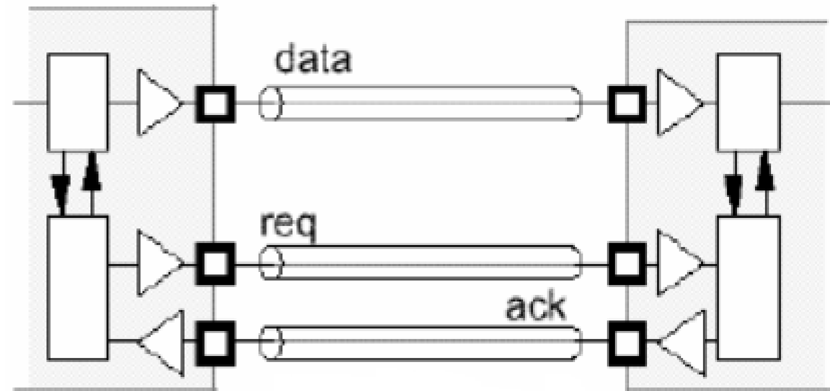


Figure 6 Asynchronous clocking system

2.2 Electro-migration (EM)

Below the 28nm process node electromigration severely affects the interconnects. These are the metal layers in the integrated circuits. So the performance and reliability of circuits are imperative since the EM may deteriorated the metal lines.

When there is gradual displacement in the metal atoms the phenomena of electromigration come into existence. If the current density is quite large in the metal lines the ions of the metal drift in the direction of the electron flow. This current density depends on the different factors like which material used for metal lines, crystal structure of metal, and the magnitude of forces that attempt to remove them from their location, including the temperature and mechanical stresses.

2.2.1 Failure mechanism in electromigration

There are two different failure mechanisms. The first example in Figure 7 shows a “void” where flux of carriers going outside from the cross section area of the conductor is higher than incoming flux of carriers. If it is other way around then the defect in the conductor is referred as “hillocks”. Both type of defects are shown in the following figure. Mostly we are seeing the effect of “void” during the validation of IP block.

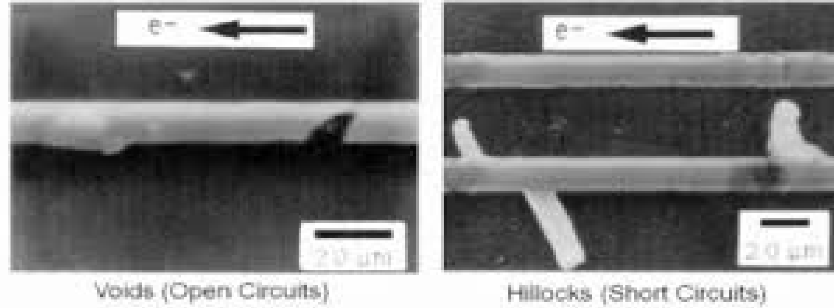


Figure 7 Void (open circuit) and hillock (short circuit)

2.2.2 Electromigration Dependency on Physical Effects

Temperature

Temperature is a most critical parameter on which the EM is depend upon. The following figure shows a cycle which eventually finishes into failure due to temperature.

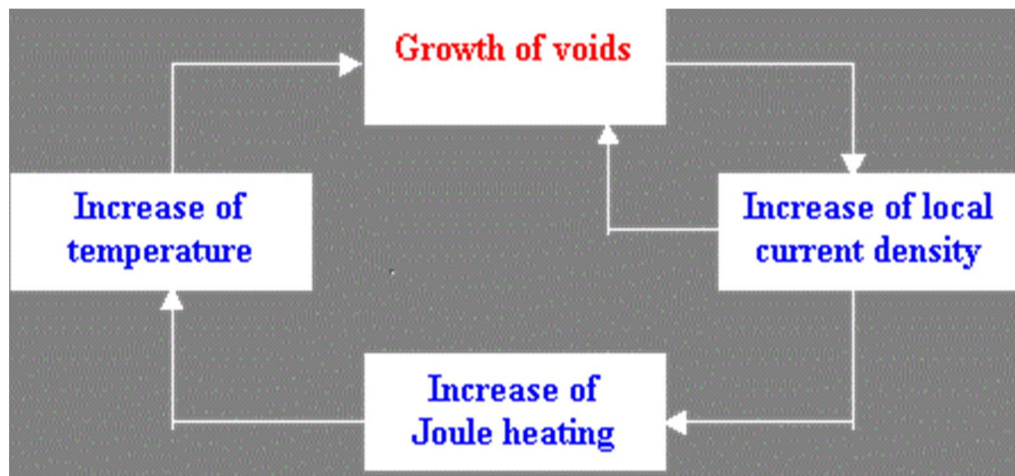


Figure 8 Recursive effect of temperature

As high current flows through the narrow interconnect void begins to develop so the metal wire becomes narrow at that point. Due to the narrowing of the width of the wire there is an increase in the current density at that point this will lead to raise in the temperature. So th metal wire will be heated up. This heating of the wire follows the joule heating principle. Joule heating is result of RMS current.

Now increase in temperature lead to forming, more and more voids in the interconnect. Eventually it results in open circuited. Sometimes

also it may happen that metal line can be short circuited with the neighboring line which is very close to that.

2.3 Second-order effects considered in the QRE simulations

2.3.1 Hot Carrier Injection Effect (HCI)

Hot carrier injection (HCI) is a degradation phenomenon in transistor. It can occur when an electron or a hole gains kinetic energy to surpass a potential barrier of interface state in the transistor and break the bond. The term "hot" associated in HCI means the temperature to model the carrier density. It is not representing the temperature of the whole transistor or circuit. It might be the case while operating the chip at elevated temperature electron can be trapped in the SiO2 layer below the poly or metal gate of a transistor, so the switching characteristics of the device can be changed forever. The HCI directly degrades the drain current (Id) in saturation region. So, HCI has to carefully model during the reliability analysis.

As feature size decreases, Electric field in channel region increases which leads to gain high kinetic energy by holes & electron (Hot carrier). These carriers are generated due to very high electric field in the drain of the MOS, hence they may degrade the operation of the device by producing the defects in the SiO2 layer. The interface of oxide and Si-SiO2 layer will be degraded. Hot carriers also generate parasitic currents in the transistor.

Different types of Hot Carrier Injection

1) Drain avalanche hot carrier injection

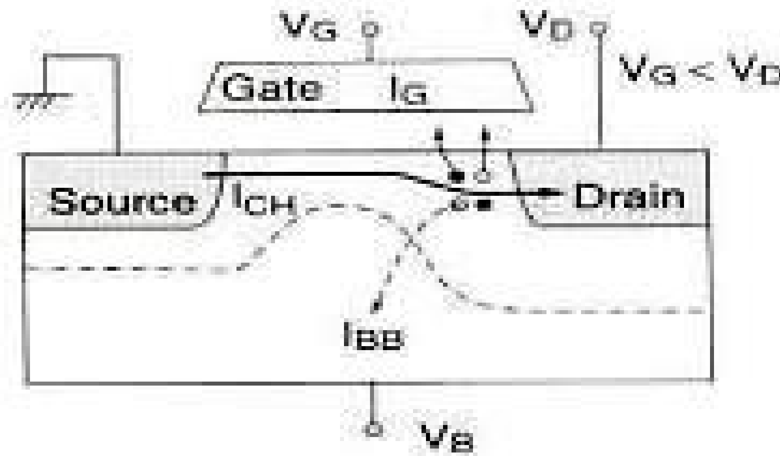


Figure 9 DAHC Injection

When $V_D > V_G$, the acceleration of channel carrier causes Impact Ionization. The generated electron–holes pair gain the energy to break the barrier in Si-SiO_2 interface. These carriers are injected towards the gate through tunneling and creates the interface states which causes the threshold voltage shift in the device.

2) Channel Hot Electron

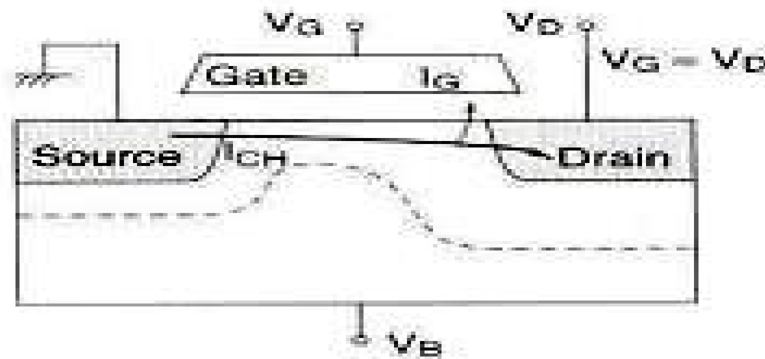


Figure 10 CHE Injection

When both V_G and V_D are higher than source voltage, some electrons driven towards gate oxide. These will create the interface state which results in shift in the threshold voltage of the device.

3) Substrate Hot electron injection

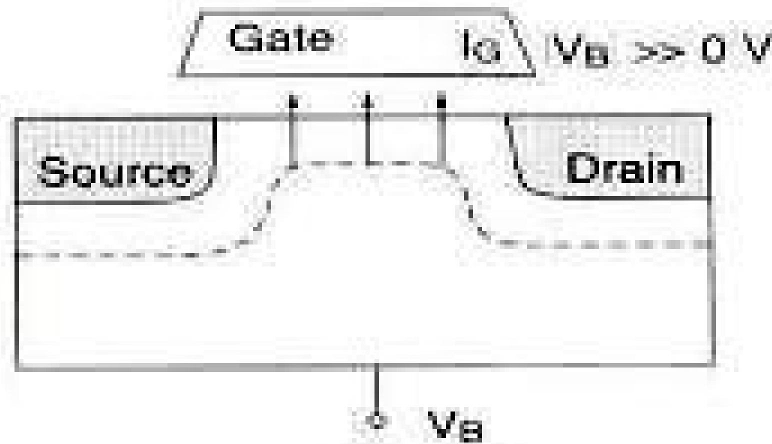


Figure 11 SHE Injection

It occurs when the substrate back bias is very positive or very negative. Carriers of one type in the substrate are driven by the substrate field toward the Si-SiO_2 interface. These energized carriers injects into the SiO_2 and creates the interface states. The threshold voltage shift will essentially affect the speed and power dissipation of the circuits.

2.3.2 Negative Bias Temperature Instability (NBTI)

At the elevated temperature BTI is observed in the MOSFET with p-channel (i.e. n type substrate) more severely with negative gate voltages. When the gate oxide electric field is around 6MV/cm and temperature is between 100-300 C, the stress due to NBTI is dominant. If electric fields is high then it may create further deterioration because of the hot carriers. When the stress conditions are diminished NBTI has capability to recover to a certain extent.

The following performance parameter of MOS can be deteriorated due to NBTI:

1) trans-conductance g_m is reduces
2) linear drain current and saturation drain current I_d reduces
3) mobility (μ_{eff}) in the channel decreases
4) sub-threshold slope S decreases
5) OFF current I_{off} increases
6) Magnitude of threshold voltage V_{th} increases

The NBTI reduces switching speed of a circuit as charging times for interconnect lines or load capacitances are increased.

Before four decades the effects of this phenomena was reported, but in the higher process nodes the impact of NBTI was not serious. In the recent technologies it is playing its role significantly. The following aspects makes the NBTI more susceptible.

1) Higher electric fields in the SiO2 due to scaling,
2) due to higher power dissipation temperature of the chip increases,
3) use of surface devices instead of MOS devices with buried channel
4) elevating the importance of p-channel MOSFETS and
5) higher permittivity nitrided oxides.

2.4 Process Variation

As device dimensions shrink towards the sub micron scale. The performance of Integrated circuit is becoming less predictable. There is a very less control of the physical geometry like length, width, thickness of devices and interconnects during the manufacturing. The more variations in these geometrical parameter, the more variations in the electrical behavior of circuits. These are inter-die and intra-die components. Variations in the inter wire spacing may cause a significant degradation in the signal integrity.

Process variation is naturally occurring variation in the attributes of transistor when integrated circuit is fabricated. It becomes critical in sub-micron regime (<65nm process node). As the variation becomes a larger percentage of full length or width of device and a feature sizes approach the fundamental dimensions such as size of atoms and wavelength of usable light for patterning lithography masks.

The sources of variation are gate-oxide thickness (tox), random dopant fluctuations, device geometry (length and width of the transistor), junction depth (Xj) etc.

2.4.1 Geometry variations of transistor:

The process variation related to the physical geometry MOSFET and other devices like resistors and capacitors in the circuit. These includes following.

Thickness variations: The gate oxide is a very important parameter. When the oxide is deposited over the surface of the silicon wafer the thickness of that SiO2 is not constant across the periphery of the wafer but it will vary this will causes the variation in the device to be fabricated on that.

Lateral dimensions variations: The variation in the dimensions like length and width of the transistor typically arise due proximity effects during the lithography step, mask, lens or photo system deviations or plasma etch dependencies. MOSFETs are quite sensitive to effective channel length as well as gate oxide thickness and to some extent the channel width. Out of all these, the channel length variation is generally considered. This is because the variation in the lateral dimensions have direct effect on the drain current (Id) characteristics.

2.4.2 Device material parameter variations:

The material anomalies can be account for doping of impurities, deposition of oxide and thermal annealing variations.

The dose, energy, angle can affect junction depth (Xj) and anomalies in the profiles of source/drain may modify effective channel length of the transistor during fabrication. Also other electrical parameters such as Vt will also be affected. During the thermal annealing and doping in the poly (or metal) gate the amount of depletion in a device can cause variation in the effective oxide thickness underneath the gate. These deviations can lead to some loss in the matching of NMOS versus PMOS devices.

2.4.3 Device electrical parameters variations:

Vt (threshold voltage variations): Vt of MOS device varies due to:

(i) oxide thickness variation
(ii) variations in the impurity level of polysilicon, substrate and implant
(iii) variations in the charges on the surface of devices

Process variation may increase or decrease the length and width of the transistor. So the aspect ratio (W/L) of the device changes as the variations

in this parameter are not correlated during the lithographic process. Width is defined while forming filed oxide whereas length is defined in during the diffusion of source and drain.
In the Static Random Access memory (SRAM) the variation in the V_t is caused by random dopant fluctuations

2.4.4 Classification of process variation

1) **Random Variations and Systematic Variations**

   Random Variations: These occurs without regards to locations and patterns of transistor within the IC. The variation in the threshold voltage of chip caused by density variations of impurity particles.

   Systematic Variations: It is related to locations and patterns. The corner edges in the layout patterns are deliberately kept slightly thicker as when the sharp edges are there in the layout, during the chemical mechanical polishing step the line edges may get deteriorated. These are due to resolution limit in the instruments like SEM (Scanning Electron Microscope) used in photolithography.

2) **Intra-die variations and Inter-die variations**

   Intra-die variation: It accounts for variations that arise between different devices and interconnects that resides within the same chip.

   Inter-die variation: It accounts for variations that arise between chips in the same wafer or different wafer.

2.4.5 Process variations in interconnects

The metal interconnects are having three parameters: length, width and thickness. When all these three are scaled down by (1/α), the cross sectional area of interconnect will be scaled down by its square. (Since $R=\frac{\rho l}{A}$) The length of interconnect is scaled down by (1/ α) so, the resistance is increased by α.

One remedy to this problem is that we can use the multilayer routing of interconnection with more thickness, wider conductors and thicker separating layers. One more way is to use optical interconnection where a very high level of integration is necessary.

When there is a variation in the cross sectional areas of interconnects then the "on chip variation" comes into picture. It results in both resistance and capacitance variation along the interconnect.

Use of multiple die-electrics, use of different metal on different levels, result in significant variation. Chemical mechanical polishing (CMP) and proximity effect in photolithography and etch process are also the source of variation

When there is a difference in hardness of the two metals or that of dielectric then during CMP step in the fabrication variation will be there in sheet resistance and capacitance. The purpose of CMP process is to remove the unwanted copper from lines and vias.

2.5 Power dissipation in CMOS

2.5.1 Current components causing leakage

The growth in semiconductor technology is enable by fabrication of very large circuits with complex functionalities on a single chip. With increase in transistor density, power dissipation also increases thereby making power design a valid design metric.

There are two main components that determine the power dissipation in CMOS.

1) **Static power dissipation** due to leakage current.
2) **Dynamic power dissipation** due to switching activity and charging/discharging of load capacitance.

Leakage power dissipation is due to flow of current in the absence of input transitions and when transistor has reached the steady state. In deep submicron regime static or leakage power becomes comparable to total power dissipation.

The main sources of leakage current in MOS circuits are subthreshold conduction current (I_{sub}), gate direct tunneling (I_g), gate induced drain leakage (I_{GIDL}), reverse-biased junction leakage current (I_j), among these, I_{sub} is the dominant leakage current component. So, it becomes necessary to adopt effective techniques to minimize the leakage power.

First, the gate leakage current (I_G) through thin gate oxide layer, it becomes the dominant leakage source for MOS technologies beyond 45nm. Second, the junction leakage current (I_j) due to reverse-bias junction leakage is attributable to the high doping concentrations in today's devices that causes tunneling of electrons across p-n junctions. The junction leakage occurs from source or drain to substrate through the reverse biased diodes when a transistor is in OFF state. This leakage current is an exponential function of doping concentration and reverse biasing voltage across the junction. Third, the gate induced drain leakage current (I_{GIDL}) which is due to high field effect in the drain junction of MOS transistor. Both I_{GIDL} and I_j decrease dramatically with V_{DD}. The fourth source of current leakage is the sub threshold leakage current (I_{sub}) that comes into play when gate-to-source voltage (V_{GS}) is lower but near to threshold voltage of the transistor.

Chapter: 3

Validation of Clock Distribution Block

3.1 Introduction of clock distribution block

In the clock distribution (CD) block we have three different types of clocks referred as clock1, clock2 and clock3 as shown in the figure. The frequency of the clock1 and the clock2 are same with the exception that clock2 is delayed compared to clock1. It is needed to synchronize the operation of all the circuits placed on the chip we have provide the clock signal to each of the blocks the according to the timing requirement. The operating frequency we are using is 3GHz for clock1 and clock2. The frequency used for clock3 is 600MHz.

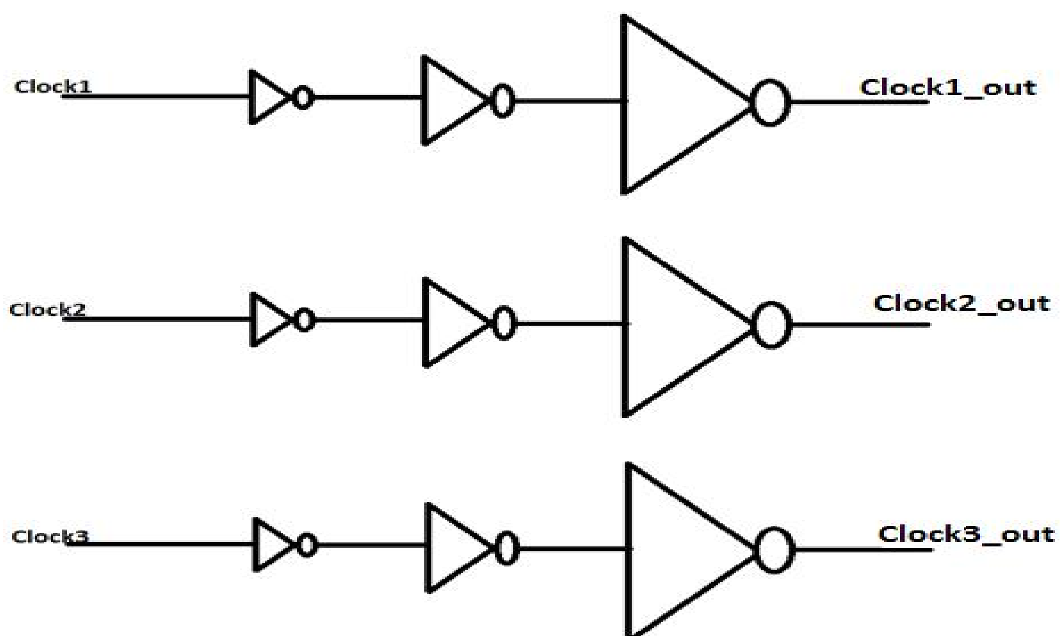


Figure 12 Generic arrangement of the clock distribution block

3.2 Difficulties in validating the CD block

In this block we are increasing the frequency from 2.7GHz to 3GHz. Here, we are using the three different clocks and we must have to maintain the rise time and fall time at each node of the circuit to 10% of the period of the input signal. If this constraint does not match then there will be degradation in the resultant output. We have to check the functionality of the CD block at three different corners named slow, fast and typical.

In the given SOC we have millions of transistors and very long routing path. So, the arrival of rising and falling edges of the clock signal will not be the at the exact time interval. There will be $\pm\Delta$ variation in the arrival of rising and falling edges of the clock signal which is referred as Duty Cycle Distortion. General requirement for the duty cycle is around 48% to 52%. The duty cycle distortion will lead to the timing jitter.

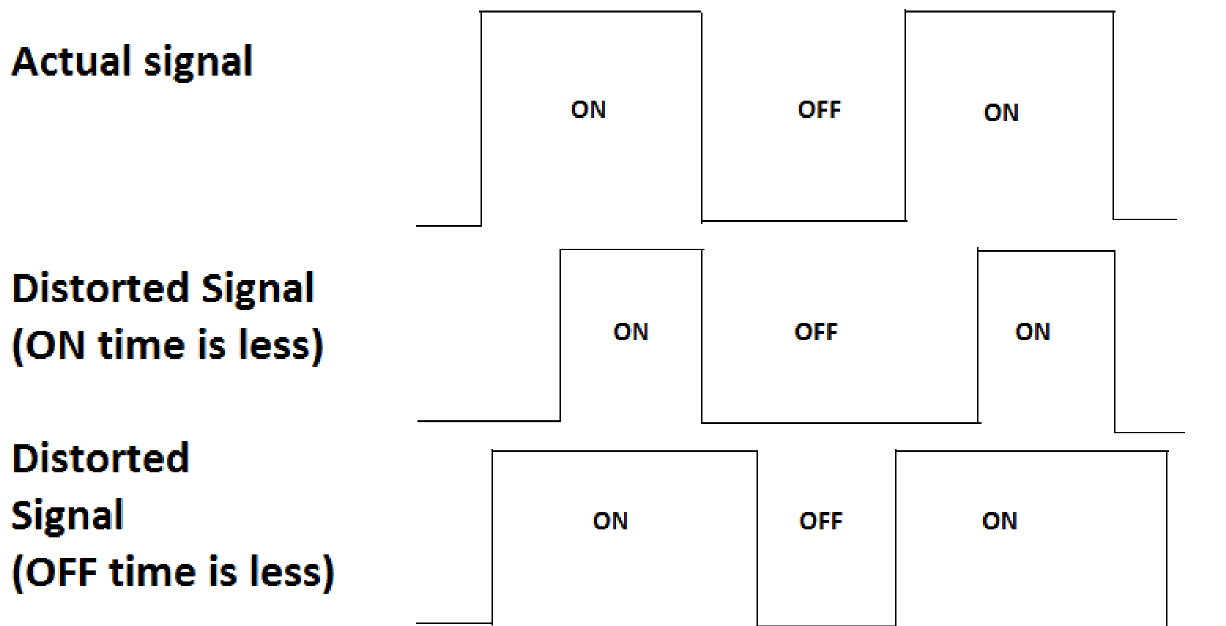


Figure 13 Effect of Duty cycle distortion on ON-OFF period

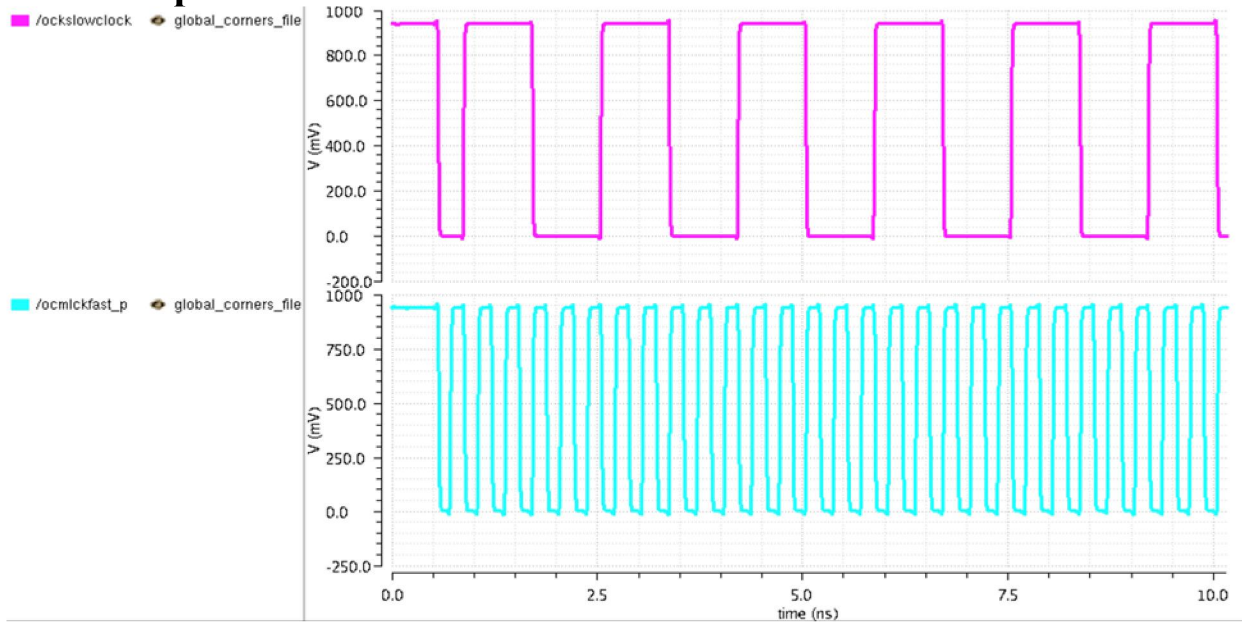
3.3 Simulation results for the CD block

Table 2 Constraints for the CD for functional simulations

Clocks	**Parameters**	**Specs**
Clock1	Rise Time	<10% of C.P.
	Fall Time	<10% of C.P.
	Duty Cycle_TX0	48-52
	Duty Cycle_TX1	48-52
Clock2	Rise Time	<10% of C.P.
	Fall Time	<10% of C.P.
	Duty Cycle_TX0	48-52
	Duty Cycle_TX1	48-52
Clock3	Rise Time	<10% of C.P.
	Fall Time	<10% of C.P.
	Duty Cycle_TX0	48-52
	Duty Cycle_TX1	48-52

All specs are meeting the requirements. The performance parameter for this block is well under the constraints for slow, fast and typical corners.

3.3.1 Output waveforms



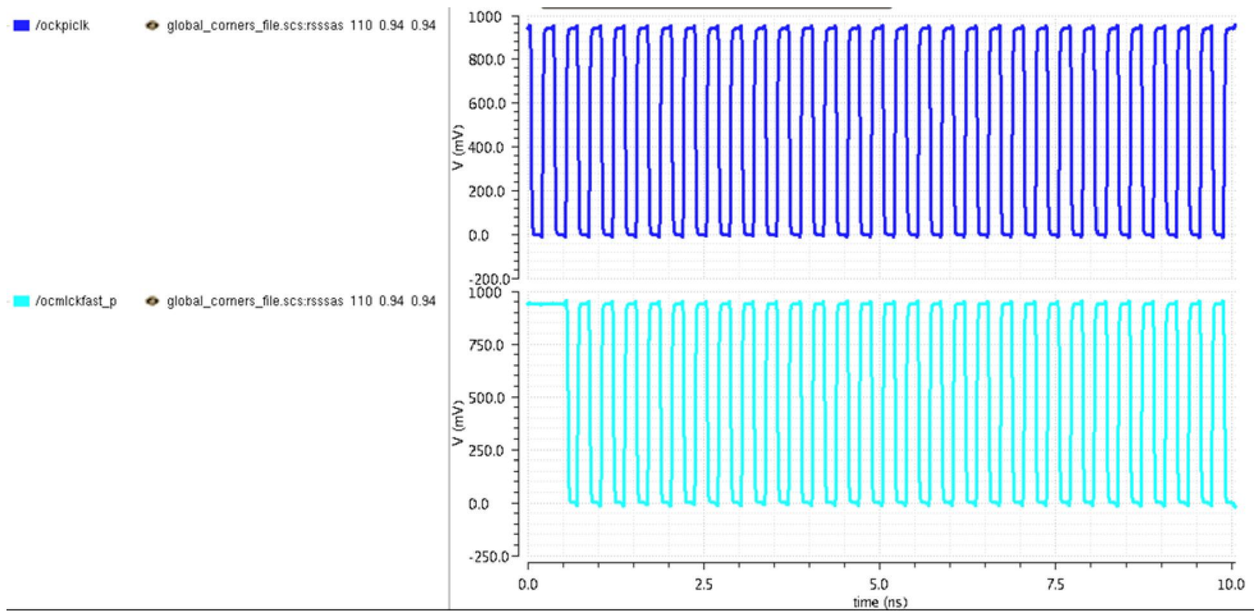


Figure 14 Waveforms of operating clocks

Chapter: 4

Reliability Validation for Devices and interconnects

4.1 Why reliability validation of interconnects is imperative?

As we know the number of devices are increasing immensely on the given chip. When we have millions of devices on the chip the current in the each net has to be maintain such that the during the operating life time of the circuits interconnect metal line can sustain the required amount of current. If the current is higher from that particular value than it will damage the metal line due to the phenomena like electromigration.

We are increasing the operating frequency to 3GHz. Due to higher frequency number of switching activities on the metal line will increase. So, in the given interval of time the current will increase. We have to control this current as it can destroy the metal line if it raise beyond its extreme limits.

4.2 How to do the reliability validation of interconnects

For doing the reliability measurement Intel proprietary tools are being used. In which each net of the circuits will be scanned to measure the value of current flowing through it. Then the files will be generated which has all information of current.

There are different types of file generated which contains information of current flowing in pre-layout and post-layout simulations. This file will be used as input for the layout engineers and they will decide the type and width of the metal which can carry the required amount of current. There is file which has the collection of FiSH (FinFET Self Heating) currents. Based on that file the layout engineers will add the parallel path of transistor to adjust the width of the device. Other way of doing this is to put more number of dummy transistors around the device which is heated up due to excessive current flowing through it. The dummy transistors are cooler compared to the active transistor. By that way the ambient temperature of the active device can be bring down.

4.3 Quality and Reliability of the Devices

When the circuits are being operated under hazardous environment the reliability of devices is imperative. When the circuits are used for longer period of time say for 10 years it possible that its performance may degrade. During this type of longer period circuits is subjected to the high temperature and supply voltage fluctuations. So we need to qualify the circuits such that deterioration in its performance parameters like rise time, fall time, propagation delay, duty cycle etc must be minimal i.e. within the constraints.

4.4 Aging, Burn in and EOS simulations

These simulations are carried out to test the quality of the devices for the longer period of time.

Aging

In this we have to qualify the circuits for 10 years. For that there are three types of simulations are incorporated named as fresh, stress and playback.

In the fresh simulation circuit will be subjected to normal operating condition in terms process, voltage and temperature. After that device will be stressed at the elevated temperature and supply voltages. At the end stress will be removed and circuit will be analyzed to find the remnant effect of given stress on the devices. This is called playback or aged simulation.

In the aging the transistors are stressed at 3% higher than the nominal supply voltage. If Vnom is 1.05V then stress voltage for aging analysis will be (1.05+ (0.03*1.05)) V.

Burn-in

In this analysis we need to qualify the circuit for the continuous operation for 10 hours. This analysis will also be carried out in post silicon validation.

This is similar to aging simulation but here the devices will be stressed for shorter amount of interval. Sometimes in the circuits due to fluctuations in supply voltages, due to IR drops the performance of the circuits can degrade.

So, to analyze such kind of hazardous conditions this simulation is incorporated.

In the burn in the stress voltage will be 30% higher than the nominal supply voltage. If Vnom is 1.05V then stress voltage for burn in analysis will be (1.05+ (0.3*1.05)) V. Such a large amount of increase in supply voltage is realistically not possible but by giving such high stress on the transistors we can mimic their performance at high temperature and extreme stress condition when circuit is functional for longer periods like for 8-10 hours.

EOS (Electrical Over Stress)

This analysis is performed only at elevated temperatures and high supply voltage. In this the transistor will be stressed and the potential difference of each of its four terminals (i.e. drain, source, substrate and gate) will be calculated. So, the violations for vgs, vgd, vds, vsb, vdb is dumped to the text file.

In the EOS only stress analysis is perform on the circuit the other two analysis (fresh and playback) are not performed. This is because in EOS analysis our goal is to find out transistor reliability under high supply voltage. According to specifications provided from the process engineers, the degradation in the saturation current of each devices must be less than 20%.

As the data rate increases i.e. operating frequency increases the reliability of the devices decreases. The reason being number of switching activities on the terminals of the transistor are more.

In the EOS technique the supply voltage signal will be given as ramp signal as shown below.

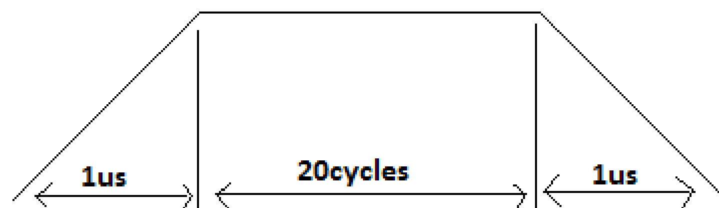


Figure 15 power supply ramp

Here initially the supply is ramp-up for 1us than the stress voltage is given for 20 cycles of the input waveform at particular data rate then the signal is ramp-down to low level in 1us. This is done to validate the behavior of circuit to range of the supply voltage. Unlike digital circuits in analog circuit the voltage of any terminal is not at any particular value during power down mode of chip so in that period if we are ramping up the supply voltage then circuits like biasing - current mirror will be turn on and we may have violations in terminal voltages.

4.5 How to do the Quality and Reliability simulations

For this simulation Intel proprietary tools are used. The model library files consisting of stressed device information are available from the fab. This model files are invoked using EDA tools of cadence virtuoso to Intel specific tools. Using this model files the simulations are incorporated one after another i.e. first fresh simulation are carried out then stress and at last playback simulations are carried out by the tool. The results of these all the simulations are stored in the text file.

Table 3 Constraints for aging, burn in and EOS validation

Parameters	Specs
FREQ_clk1	3GHz
FREQ_clk2	3GHz
FREQ_clk3	600MHz
FALL_clk1	<10% of C.P.
RISE_clk1	<10% of C.P.
FALL_clk2	<10% of C.P.
RISE_clk2	<10% of C.P.
FALL_clk3	<10% of C.P.
RISE_clk3	<10% of C.P.
DC_clk2_in	48-52
DC_clk1_in	48-52
DC_clk3_in	48-52
DC_clk1TX1_AVG	48-52
DC_clk1TX0_AVG	48-52
DC_clk2TX0_AVG	48-52
DC_clk2TX1_AVG	48-52

DC_clk3TX0_AVG	48-52
DC_clk3TX1_AVG	48-52

The performance parameters mentioned in the table have to meet in three different simulation fresh, stress and playback. The fresh simulation are at nominal temperature and supply voltage. In the stress the device will be stressed at high power supply and at elevated temperatures. In the playback simulation the stress conditions are removed and circuit is simulated to measure the remnant effect of stress. The results of fresh and playback simulations are compared to see the degradation of the devices.

These three simulations will be carried out for aging, burn in and EOS. The circuit satisfy the all constraints of performance parameter in each of these three simulation.

Chapter: 5

Power simulation

5.1 Importance of power measurements

As moving further into the deep submicron technologies the number of challenges we have to deal with like signal integrity, power dissipation due to leakage, IR drops etc. One of the major concern is the power dissipation of the IP.

If the IP consumes more amount of power from sources then devices like mobile phone, tablets, laptops will discharge sooner and this is reduce the battery life. So, the individual power dissipation has to be calculated for each of the circuits in the whole IP to find the total power budget of IP and SOC.

In the power simulation measurement two types current has to be measured.

1) Active current
2) Leakage current

1) **Active current:** when circuit is in functional mode and all the inputs are applied to the circuit
2) **Leakage current:** when the circuit is in the standby mode and all input signals like enable, clocks are deliberately turned off

- Both of these current are measured from the power supply.

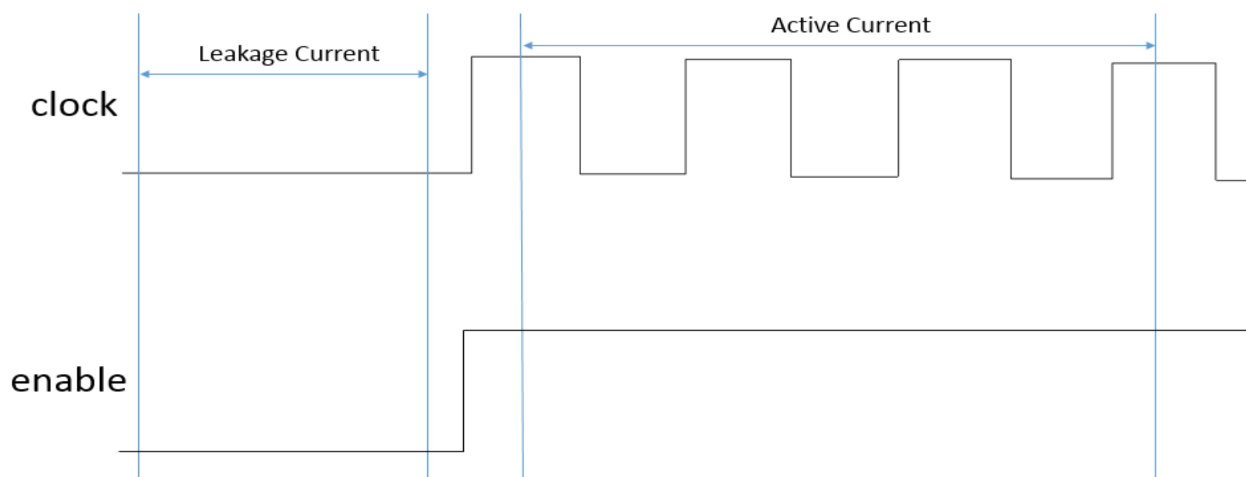


Figure 16 power simulation measurement

5.2 Low power techniques

5.2.1 Power gating

- This technique is used in VLSI circuit to reduce the power dissipation of the circuit in the standby mode. This can be done by shutting off the current flow from supply when the block are not in use.
- This technique is for single power supply domain. Large amount of current is required to drive the different IP in the SOC.
- Power gating uses high Vt (threshold voltage) pMOS transistor as power gate switch to shut off the flow of current to part of a design in standby or sleep mode. nMOS footer transistor can also be used as sleep transistor
- This large current is provided by power gate as shown in the following circuit. The range of Id is in 20-25mA. To carry this substantial amount the pMOS will be of very large size.

The following is an example of power gating technique.

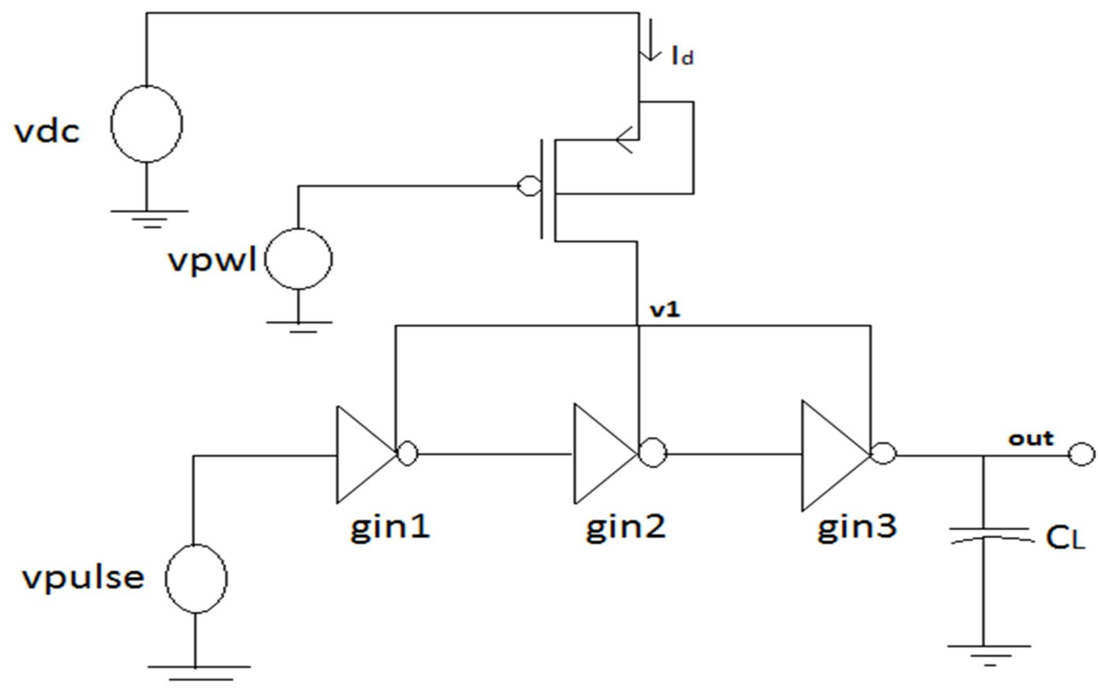


Figure 17 Power gating

The inverter chain consist of three inverter, the pulse train is applied at the input **vpulse** and with a load of C_L=100fF. The pMOS transistor used to control the active and leakage currents.
The active mode: 1ns to 18ns
The standby mode: 22ns to 48ns

The pMOS device is designed with the aspect ratio of m=5, m=10 and m=15.
The simulation result for m=5.

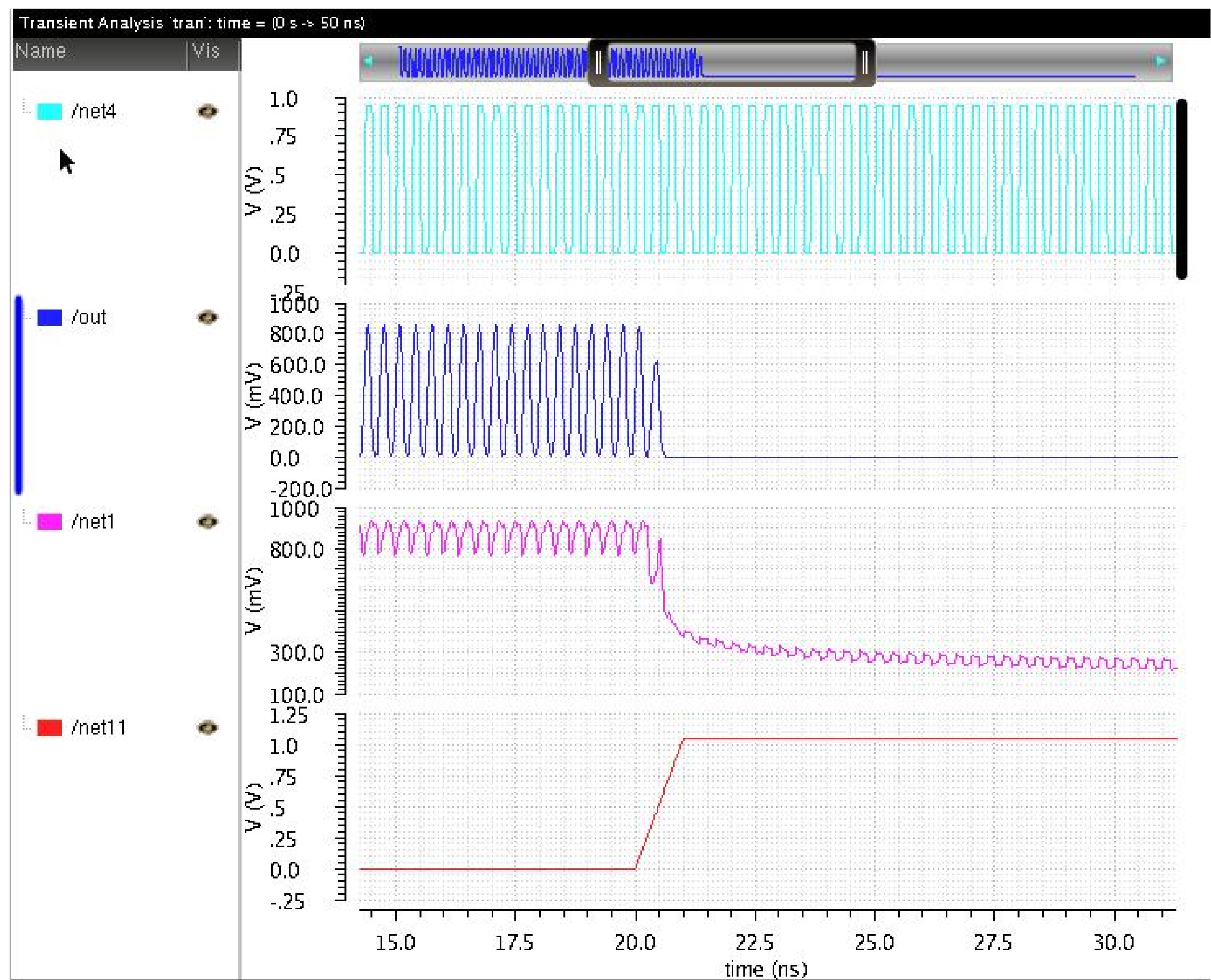


Figure 18 o/p waveforms for m=5

The value of the active and leakage current are following.

Table 4 Simulation result for m=5

	Process: Slow Temperature:130 C Voltage: 900mV	Process: Fast Temperature: -60 C Voltage: 1.2V	Process: Typical Temperature: 40 C Voltage: 1V
Active current	350.2u	440u	417.5u
Leakage current	4.018n	65.73n	11.75n
V1	834mV	1.16V	950mV

The simulation result for m=10.

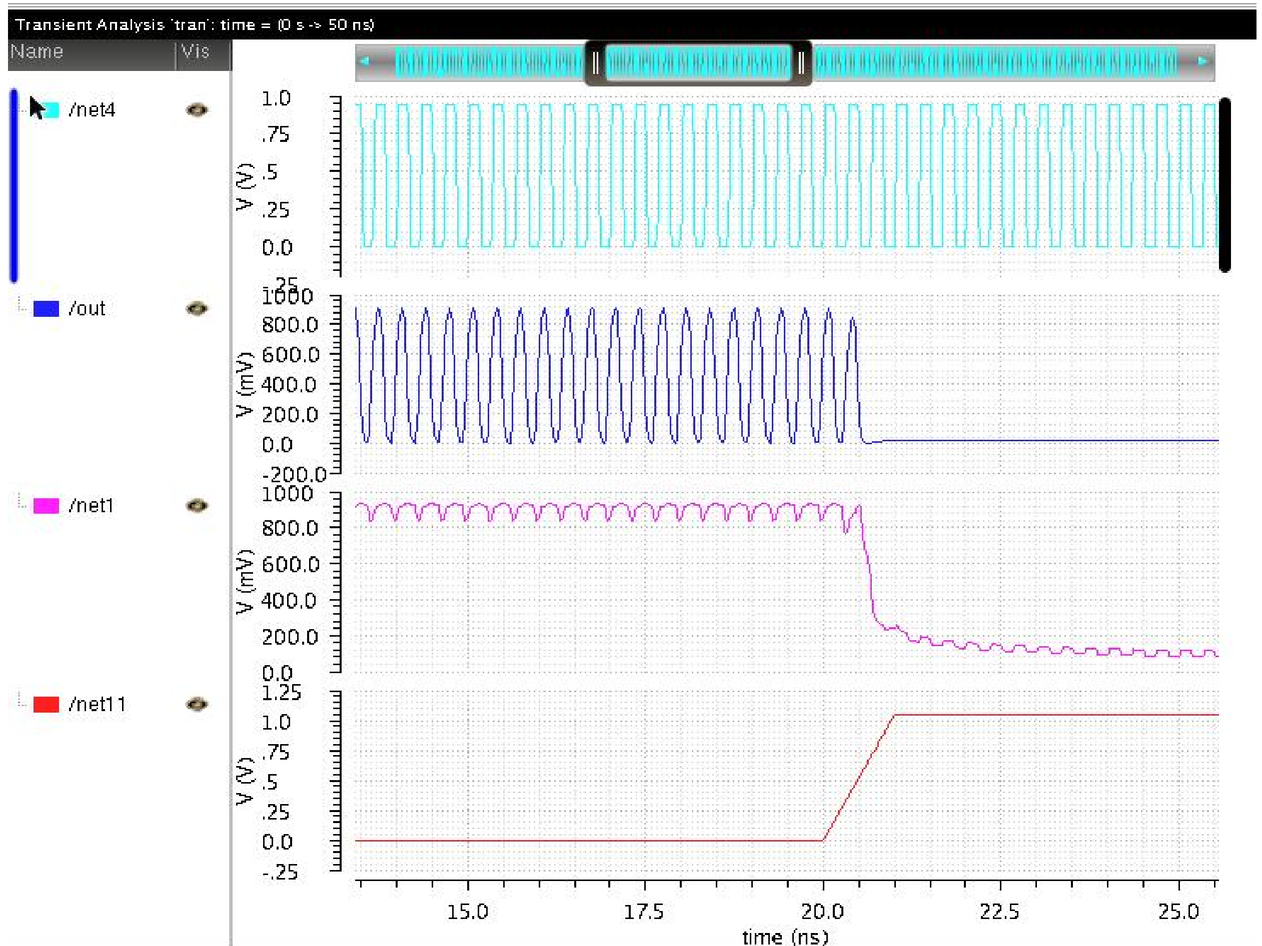


Figure 19 o/p waveforms for m=10

Table 5 Simulation result for m=10

	Process: Slow Temperature:130 C Voltage: 900mV	Process: Fast Temperature: -60 C Voltage: 1.2V	Process: typical Temperature: 40 C Voltage:1V
Active current	370u	445.2u	423.8u
Leakage current	14.69n	152.7n	20.81n
V1	866mV	1.18V	975mV

The simulation result for m=15

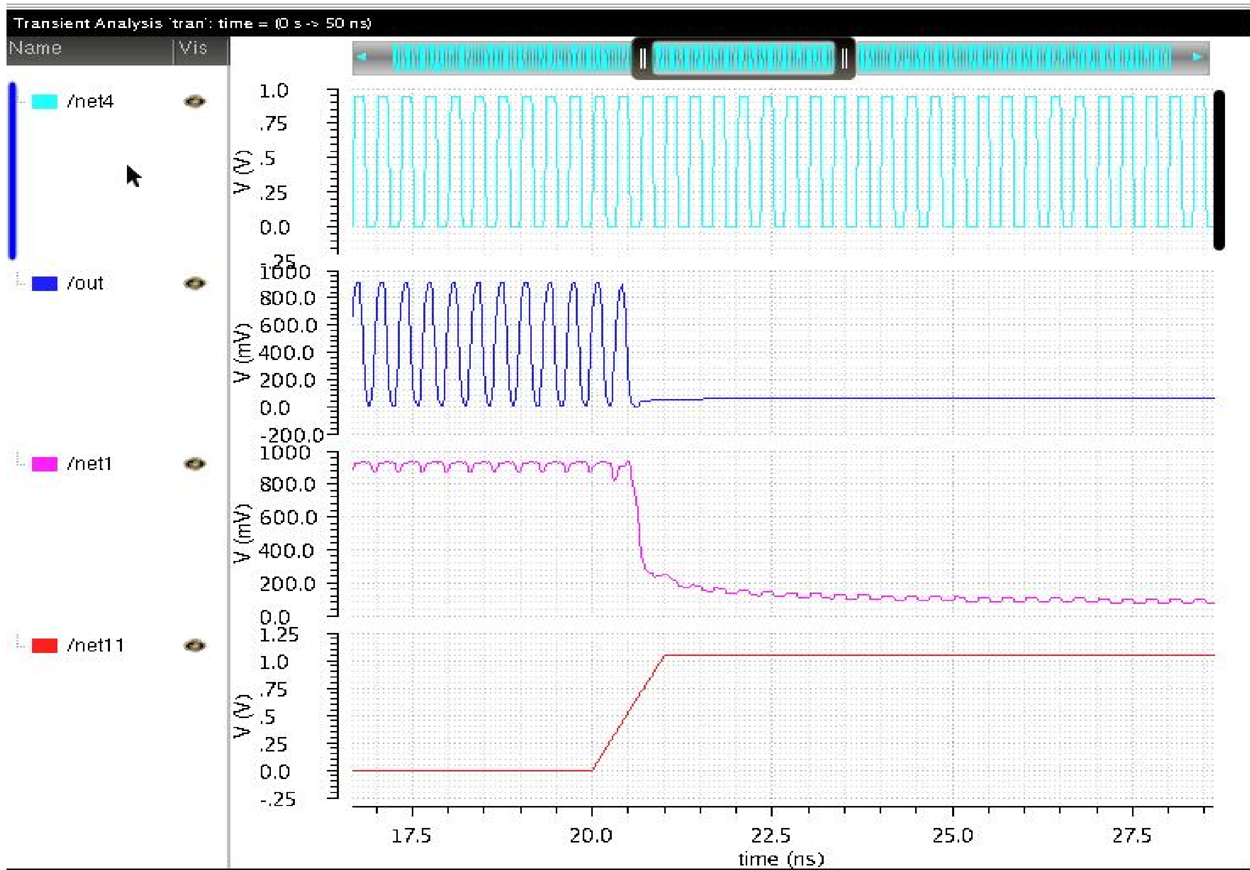


Figure 20 o/p waveforms for m=15

Table 6 Simulation result for m=15

	Process: Slow Temperature:130 C Voltage: 900mV	Process: Fast Temperature: -60 C Voltage: 1.2V	Process: typical Temperature: 40 C Voltage:1V
Active current	375.1u	447.5u	425.3u
Leakage current	20.83n	224.8n	29.71n
V1	877mV	1.187V	1.14V

5.2.2 Power Sequencing

This is technique is deployed when there are more than one power supply is present in the architecture or design i.e. this is used for multiple power supply domain. If the power sequencing is improper then it can cause immediate fault in device or affects its long term reliability. When an active power supply and inactive power supply is fed to the device then it can stress electrostatic discharge protection and other interfaced which deal with multiple voltages.

If this technique is not incorporated in the design than it can create latch up in the device. As we know CMOS technology is used to fabricate most multi voltage devices and chips. Latch up occurs when output voltage of CMOS drops below ground level due to undesired noise spike. Due to this insufficient current flow inside CMOS that will create low resistance path and conduct a current. By removing power from device this current can be reduced.

Following is the example showing how the power sequencing can be incorporated. There two power supply Vdd1 and Vdd2 present in the following example.

CASE: I
Vdd2 is present, Vdd1 is not present.

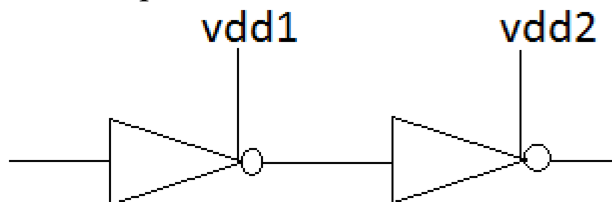


Figure 21 power sequencing example

If Vdd1 is not present then the output of first inverter can be anything between logic high and logic low i.e. the output is invalid. Now if the Vdd2 is present in this case so it will create a conducting path from power rail to ground rail in the second inverter. The current will be considered as leakage as output of Vdd1 i.e. input of Vdd2 is not valid. Hence, this leakage current will cause unnecessary power dissipation in the circuit.

In the IP there are hundred millions of such gate will be functioning so overall this will cause significant impact on power budget.

The following technique will be used to inhibit the leakage power dissipation.

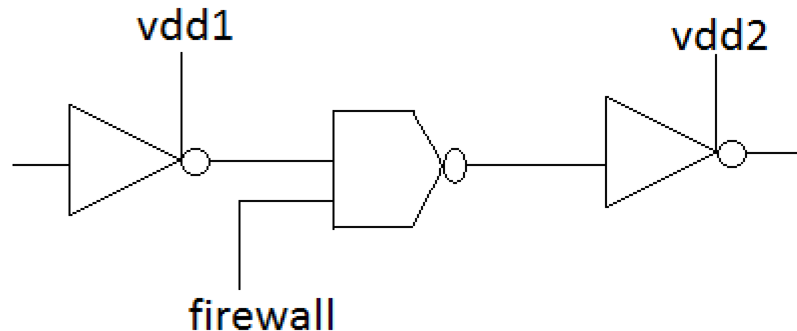


Figure 22 power sequencing with firewall mechanism

The NAND gate used between the two inverter is will provide a valid logic state at the input of the second inverter. Due to valid state (either logic '0' or logic '1') at the input only one of the device i.e. either pMOS or nMOS in the inverter will turn on and we have valid logic state at its output. As there is no conducting path from power and ground rail there will not be any power dissipation in the circuit. The power supply for the firewall gate (NAND gate) is Vdd2.

CASE: II

Vdd1 is present, Vdd2 is not present.

In this case not firewall mechanism is required. The reason is, if Vdd2 is not present then even if we have a logic state at the output of first inverter (input of second inverter) due to absence of Vdd2 there is no scope of conducting path between power rail and ground rail, so not leakage current hence no power dissipation.

Half adder example

The half adder circuit as shown in fig below consists of one XOR and one AND gate. The outputs of the adder sum and carry are stored in the flip flops, one each for sum and carry. Here, two different kind of power supply domain has been used. For processing the input to the gates we are using a power supply which is being controlled by a pMOS transistor. It means the pMOS transistor will be used to supply the current from power supply when we are processing the inputs. Once the inputs are processed and outputs are generated the “sum” and “carry” will be stored in the flip flop. Finally the output sum and carry referred as “sum_out” and “carry_out” are generated at output pin according to clock applied to the flip flops.

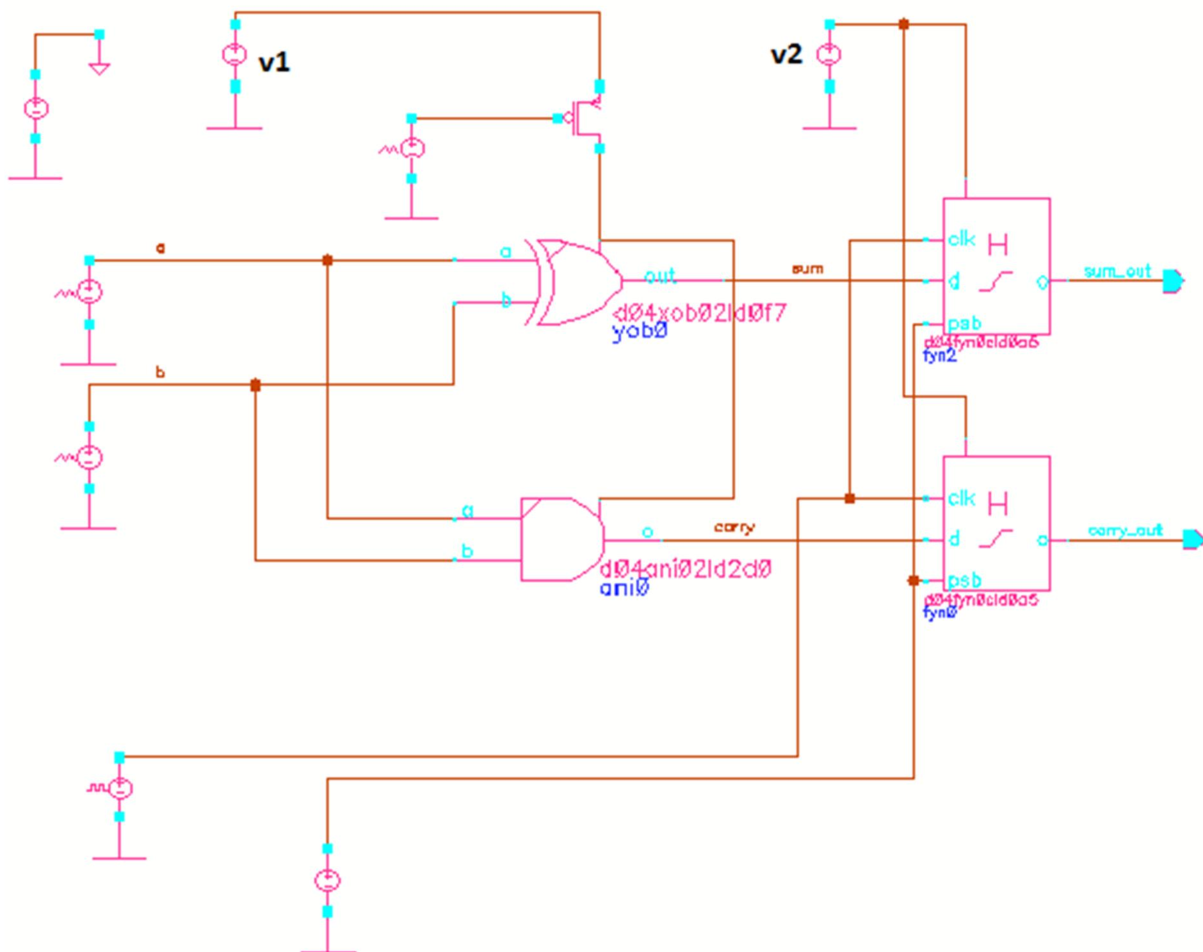


Figure 23 schematic of full adder for power dissipation analysis

Here, to store the data i.e. the output of adder the supply has to constantly given to the flip flops. Whereas for on the processing side i.e. the XOR and AND gate need the supply when they are processing the inputs ‘a’ and ‘b’.

By this technique we can relatively reduce the overall power dissipation of the chip because in the chip if there is 32-bit adder is there and if apply power constantly to that then it will consume significant amount of power. Rather than we can shut off the current from the power supply once the output are generated and then store them in the flops after processing. Of course there will be an area overhead due to use of flops.

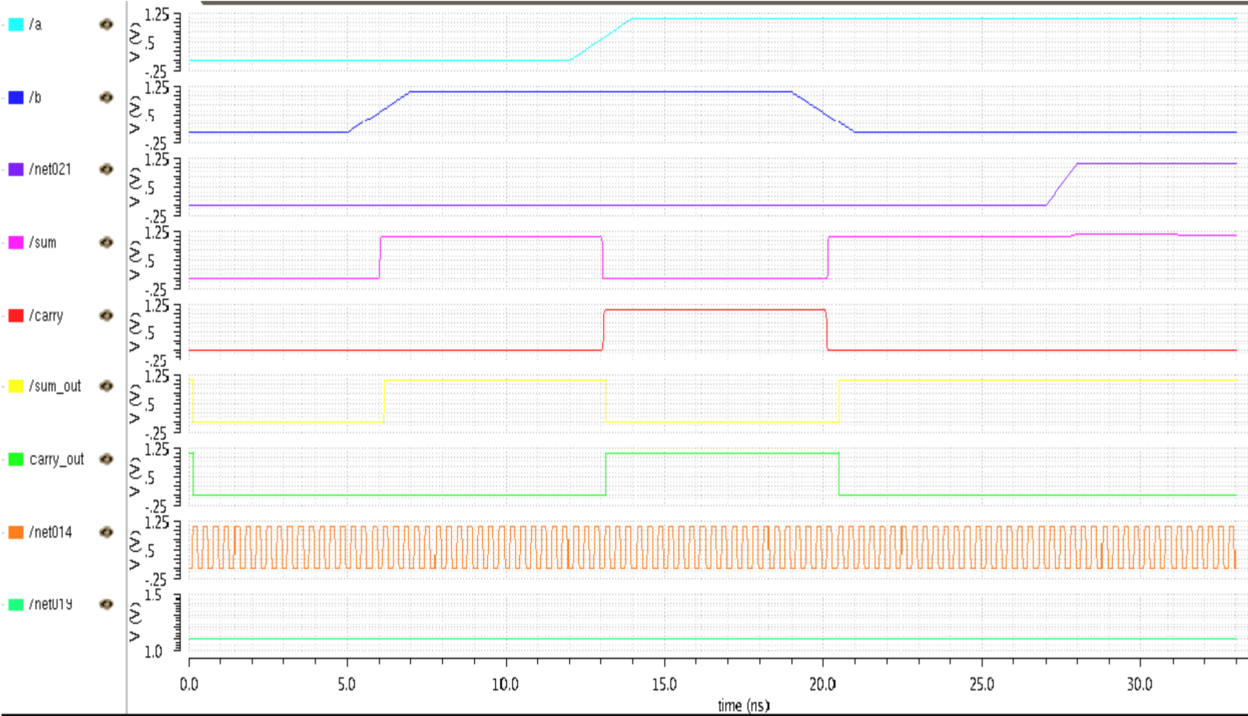


Figure 24 waveforms for full adder (inputs, outputs & control signal)

Here the "net021" is used as control signal which is applied to the gate of the pMOS transistor which is being used as power gate here.
As shown in the waveforms the net voltage is LOW on control signal till 27ns and after that it is becoming HIGH.
The duration in which control signal is LOW referred as active mode and when it is HIGH it is referred as standby mode. These modes are corresponds to "v1" in the schematic. For "v2" this mechanism is since it is constantly supplying current to the flip flops.

Value of currents in active and standby mode for "**v1**"

Table 7 value of currents for “v1” supply

	Process: slow Voltage: 900mv Temp: 130 C	Process: fast Voltage: 1.2V Temp: -60 C	Process: typical Voltage: 1 Temp: 40 C
Active current	1.9u	17.13u	6.99u
Leakage current	34.46n	4.83n	15.45n

Value of currents in active and standby mode for “**v2**”

Table 8 value of currents for “v2” supply

	Process: slow Voltage: 900mv Temp: 130 C	Process: fast Voltage: 1.2V Temp: -60 C	Process: typical Voltage: 1 Temp: 40 C
Active current	11.77u	14.78u	12.82u
Leakage current	11.04u	13.99u	12.1u

Conclusion

In the submicron technology as device dimensions becomes smaller and thinner, the criteria for the performance parameter becomes more stringent. Owing to this different kinds of second order effects like short channel effect, narrow channel effect, channel length modulation, punch through, tunneling, mobility degradation, velocity saturation, leakage etc. we have to consider while validating the functional performance of the circuits.

The reliability of the each device and interconnect will be prerequisite before the actual physical placement of circuits on the silicon. The reliability measures we considering for are hot carrier injection, negative bias thermal instability, electrical over stress, electro static discharge for the devices whereas electro-migration is considered for the interconnect reliability.

The reliability measures for analog circuit like biasing circuits like current mirrors are very critical as during the power down modes the terminal of transistor may have any non-zero value during this if the supply ramp signal is comes to the transistor then it can turn on the transistors unnecessarily. So this type of reliability analysis are very critical. The aging and burn in analysis will quality the reliability of transistors for longer periods of time.

The clock distribution block has been validated to match all constraints like rise time, fall time, duty cycle etc. It went through the quality and reliability validation and satisfied the specifications under impact of elevated temperature and power supply fluctuations. At the same time it has been simulated for different types of process skew corners.

The power simulations are very much of importance for very small feature size (<28nm). The leakage current do a significant impact on over all power budget because the geometry of transistor gets smaller leakage will be more in the transistor due to different second order effect. The subthreshold current will be significantly higher. In the inverter chain as the header pMOS size increases the amount of current flowing through it will also increases that will also add to the power dissipation of the circuit.

BIBLIOGRAPHY

[1] www.intelpedia.intel.com

[2] www.wikipedia.com

[3] http://www.semiconfareast.com/hotcarriers2.html

[4] VESA, "DisplayPort Proposed Standard," Version 1.0, August 15th, 2005

[5] CEA, "A DTV Profile for Uncompressed High Speed Digital Interfaces, CEA 861-B," May 2002

[6] www.vlsi-expert.com

[7] "An Introduction to Electromigration Aware Physical Design", J. Lienig, Proc. of the Int'l Symposium on Physical Design (ISPD), April 2006

[8] "Hybrid IR/EM Analysis Flow with EM Rule Extension", Gary Chan, TSMC; 2011 Synopsys User Group (SNUG) Conference, Taiwan

[9] www.iue.tuwien.ac.at/phd/entner/node24.html

[10] www.ece.tamu.edu/~spalermo/ecen689/lecture25_clocking_arch.pdf

[11] Comparison of NMOS and PMOS Hot Carrier Effects From 300 to 77 K -Miryeong Song, Kenneth P. MacWilliams, Member, IEEE, and Jason C. S. Woo, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 44, NO. 2, FEBRUARY, 1997

[12] An As-P(n'-n-) Doublk Diffused Drain MOSFET for VLSI'S -EIJI TAKEDA, MEMBER, IEEE, HITOSHI KUME, YOSIII[NOBU NAKAGOME, TOHACHI MAKINO, AKIHIRO SHIMIZU, AND SHOJIR.0 ASAI, MEMBER, IEEE , IEEE TI. TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-30, NO. 6, JUNE 1983

[13] A New Mode of Hot Carrier Degradation in 0.18pm CMOS Technologies- C.T. Liu, E.J. Lloyd, C.P. Chang, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, R. Liu, C.S. Pai, H. Vaidya, and J.T. Clemens Bell Laboratories, Lucent Technologies, 700 Mountain Ave., Murray Hill, NJ 07974

[14] Analysis of gate oxide thickness hot Carrier effects in surface channel P-MOSFET's "Doyle, B.S. Mistry, K.R. Cheng-Liang Huang, IEEE Transactions on Electron Devices, Jan 1995.

[15] Hot-carrier degradation of sub micrometer p-MOSFETs wit Thermal/LPCVD composite oxide "Lee, Yung-Huei, IEEE transactions on electron devices, Jan 1993

[16] Three hot-carrier degradation mechanisms in deep- Submicron PMOSFET's Woltjer, Paulzen, Pomp, Lifka, Woerlee, IEEE transactions on electron devices, Jan 1995.

[17] Positive Oxide charge generation during .25µm PMOSFET hot carrier degradation Woltjer, Paulzen, Pomp, Lifka, Woerlee, IEEE Electron Device Letters, Oct 1994.

[18] Hot-Electron and Hole-Emission Effects in short n-Channel MOSFET's - KARL R. HOFMANN, MEMBER, IEEE, CHRISTOPH WERNER, WERNER WEBER, AND GERHARD DORDA, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-32, NO. 3, MARCH 1985

[19] Performance and Hot-Carrier Reliability of 100 nm Channel Length Jet Vapor Deposited Si3N4 MNSFETs –S. Mahapatra*, Student Member, IEEE*, V. Ramgopal Rao*, Member, IEEE*, B. Cheng, M. Khare, Chetan D. Parikh, J. C. S. Woo, and Juzer M. Vasi*, Senior Member, IEEE ,* IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 4, APRIL 2001

[20] Effect of oxide field on hot carrier induced degradation in CMOS gate oxide- S.P. Zhao and S.Tayfor , 1995 IEEE 91 *5th IPFA '95: Singapore*

[21] Performance and Hot-Carrier Reliability of 100 nm Channel Length Jet Vapor Deposited Si3N4 MNSFETs –S. Mahapatra*, Student Member, IEEE*, V. Ramgopal Rao*, Member, IEEE*, B. Cheng, M. Khare, Chetan D. Parikh, J. C. S. Woo, and Juzer M. Vasi*, Senior Member, IEEE ,* IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 4, APRIL 2001

[22] Deuterium Post-Metal Annealing of MOSFET's for Improved Hot Carrier Reliability -I. C. Kizilyalli, J. W. Lyding, and K. Hess , IEEE ELECTRON DEVICE LETTERS, VOL. 18, NO. 3, MARCH 1997