VERIFICATION OF ANALOG IP: POWER MANAGEMENT UNIT (PMU)

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Niranjani Mayankkumar H.

(13MECV14)

Electronics & Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
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Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Niranjani Mayankkumar H.

Certificate

This is to certify that the Major Project entitled **"Verification of Analog IP: Power Management Unit (PMU) "** submitted by **Niranjani Mayankkumar H. (13MECV14)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in VLSI Design , Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

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- Niranjani Mayankkumar H.

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Abstract

Nowadays electronics circuits are really an important part of the Automotive products. The requirement fuel efficiency, security and safety in automotive field have increased to a great extent. So to achieve these requirements, electronics products are development with greater accuracy and efficiency. Vehicles, which used to be only mechanical in earlier days, now contains more than thousand electronic components most of which happen to be sensors and microcontrollers.

A complete System-On-Chip for these products are developed which have many different IPs including both Analog and Digital IPs like memories, ADCs, DACs, different sensors, etc and microcontroller based circuits to control all of these. All these circuits require a specific regulated voltage and current. There comes the requirement of Power Management Unit (PMU).

PMU not only provide required power or current it is also continuously measures various sensors' outputs and generates signals and accordingly sends it to the core. During this project work I have worked two different versions of PMU with different specifications. In this thesis report I have explained PMU architecture, different modes of PMU, PMU operation with different operating conditions the simulation results which show how PMU is verified using RTL simulation and SPICE level simulation.

Contents

List of Figures

Chapter 1

Introduction

In earlier days electronics involved in cars was only music systems and digital clocks. But as technology evolves now electronics is an important part of the automotive products. For example, the engine. The engine is the heart of a car. The circuit that automates how much fuel should enter the engine is governed by the electronic control unit (ECU). The ECU consists of sensors and microcontrollers, which govern the flow of fuel into the engine. It decides the amount of fuel to be injected inside the engine with the help of the pressure sensor, throttle position sensor, oxygen sensor, fuel injector and many other components. The main aim of using the ECU is to increase the fuel efficiency of a car.[8]

The second example is transmission. Typically, there are two types of transmission used in cars -manual and automatic, also referred to as manual gearing or automatic gearing. Electronics plays a more significant role in automatic-transmission cars. Herein, the automatic transmission of a car is controlled by the transmission control unit (TCU). The TCU collects information from the sensors attached to the vehicle. It further uses the data to do gear shifting at the right time, which helps to increase the car‘s performance and efficiency.

Electronics is also involved in breaking systems. Anti-lock brake systems (ABS)

are becoming increasingly popular in cars. These have two main advantages: they let you stop faster and they let you steer even while you have applied the brakes. Other applications like parking sensors, auto sensing wipers, auto sensing lights, security applications, in-vehicle communication systems, etc. increases great demand of electronics in the world of automobiles.

Now to operate all this electronics we need a regulated voltage and current. There comes the Power Management Unit (PMU). PMU is not only intended to provide voltage and current, it also senses voltages from different sensors. And it warns the controller when the output of the sensor is not in the required range of voltage. The IP includes different Power-on-reset (POR) and Voltage detectors (monitors) to manage power supply sequence during power-up/power-down of the SoC, functional and test-mode operation of the SoC and the PMU itself.

In this project report I have explained two versions of PMU namely PMU8 and PMU9. Main changes in PMU8 and PMU9 are of the Current requirement. PMU8 can provide maximum of 150 mA and PMU9 can provide current upto 400 mA. There are also some other changes which is explained in detail in chapter 2 and chapter 3 respectively.

1.1 Block Diagram of PMU

Figure 1-1 describes the top level block diagram of PMU8. Following is the description of different blocks.[5]

- POR: - This block is Power On Reset. POR generates a signal which goes high at value of 2V of high voltage supply and at value of 30mV of low voltage supply. These blocks are to indicate sufficient voltage levels of both voltage supplies.

- Low to high level shifters: - This module converts the low voltage signals coming

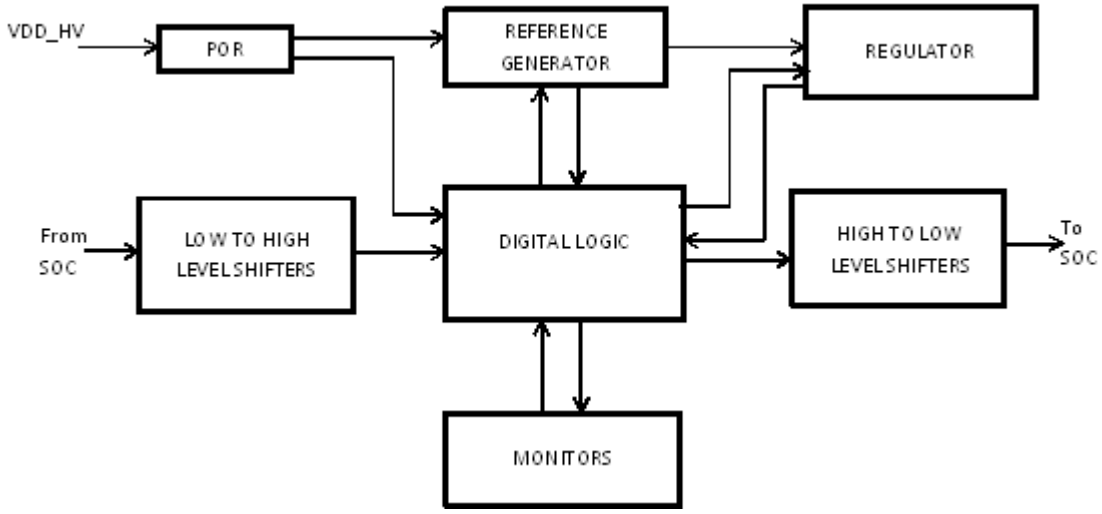

Figure 1.1: block diagram of PMU

from core to high voltage. The outputs "digital output" are going to almost every module inside PMU.

- High to low level shifter: - This module converts high voltage output signals from analog blocks to low voltage signal and sends out these signals to SoC.

- Digital Logic: - It contains digital logic using gates for generation of different signals using signals coming from SoC through high to low level shifters e.g. Enable signals for different analog blocks. Some signals from digital block also goes to SoC through low to high voltage level shifters.

- Regulators: - This is a very important block of PMU. This block provide regulated low voltage and required current for the SoC. There are two regulators, one for the main mode and one for standby mode of the PMU. It contains the regulator amplifier & softstart-up block. This block generates gate control signals for the ballasts which are placed inside IOring. Ballast is the pMOS with high W/L which provides the required current for the SoC.

- Reference modules: -This module contains three bandgap blocks which are used to generate different references for voltage monitors & regulator. Separate

bandgap blocks are used to generate reference for monitors & regulator. Two different bandgaps are used to generate reference voltages for main regulator and standby regulator. Also regulator bandgap block generates references for bist modules.

- Monitors: - Monitors are voltage detectors. This module contains all high voltage & low voltage monitors. There are many monitors in PMU which compares the sense signals coming from the SoC with the reference voltages generated from the reference generator block and generates signal accordingly.

Chapter 2

PMU8 Architecture

2.1 Introduction

In this chapter different portion and modes of PMU8 is explained in detail. PMU8 is responsible for providing regulated voltage of 1.2V and load current can be upto 150 mA. And in standby operation mode of PMU, it can give 1.06V output voltage and 10 mA of output current. This chapter includes main domain regulator and standby regulator. How monitors are tested in Test mode and Bist mode. And it also explain how PMU works in different modes of testing.

2.2 Main domain Regulator (PREG)

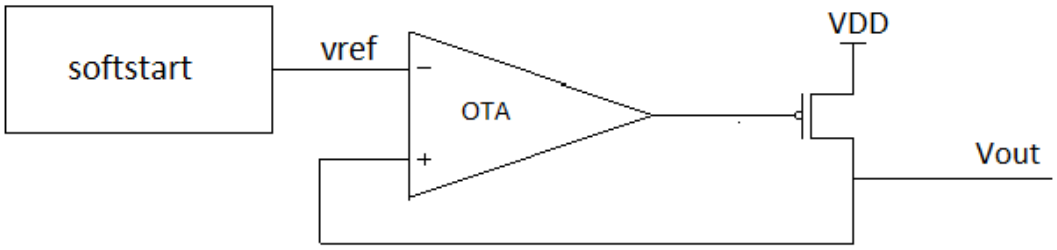

Figure 2.1: Representaion of PREG

Preg is the main regulator of Power Management Unit 8 (PMU) responsible for providing the regulated voltage of 1.2V and all the required current of SoC (upto 150 mA). As shown in figure 2-1 there is one Operational Transconductance Amplifier (OTA) which acts as Error Amplifier. Output of amplifier goes to Gate of a pMOS (Ballast). Ballast is the MOS which provides such a high current. It can provide a current of 150 mA. Drain of this pMOS is the output of the regulator which is fed back to the positive terminal of comparator. Negative terminal is at a reference voltage of 1.2. Reference voltage is generated by a bandgap reference voltage generator and comes through a soft-start block. Concept of soft-start is explained in next section in detail.

The ballast can be implemented using bipolar or MOS transistors. Since a MOS transistor is controlled by its gate voltage, it offers the advantage of smaller power consumption and consequently higher efficiency for the voltage regulator. The MOS transistor can be either N or P type. The nMOS transistor requires a gate voltage higher than the source voltage, and therefore it may be necessary a charge pump to increase the voltage level. The proper choice for low voltage systems is the use of a pMOS.

2.3 Detailed description of PREG

In figure 2.2 the detail schematic for the regulator is shown. Ibias is a constant current source for the OTA. The 'en' signal is the enable signal for the regulator. When 'preg_en' is 0 in starting M9 is on. And bandgap is not ready yet, so 'vbg_ready' signal is 0 and Ibias is OFF. Due to M9 ON, Vx point is pulled up to VDD and thus the ballast is OFF.[6]

Now when 'preg_en' is high, M9 turns off and the regulator is enabled. preg_en is high after bandgap is ready to give the reference voltage i.e. 'vbg_ready' signal is

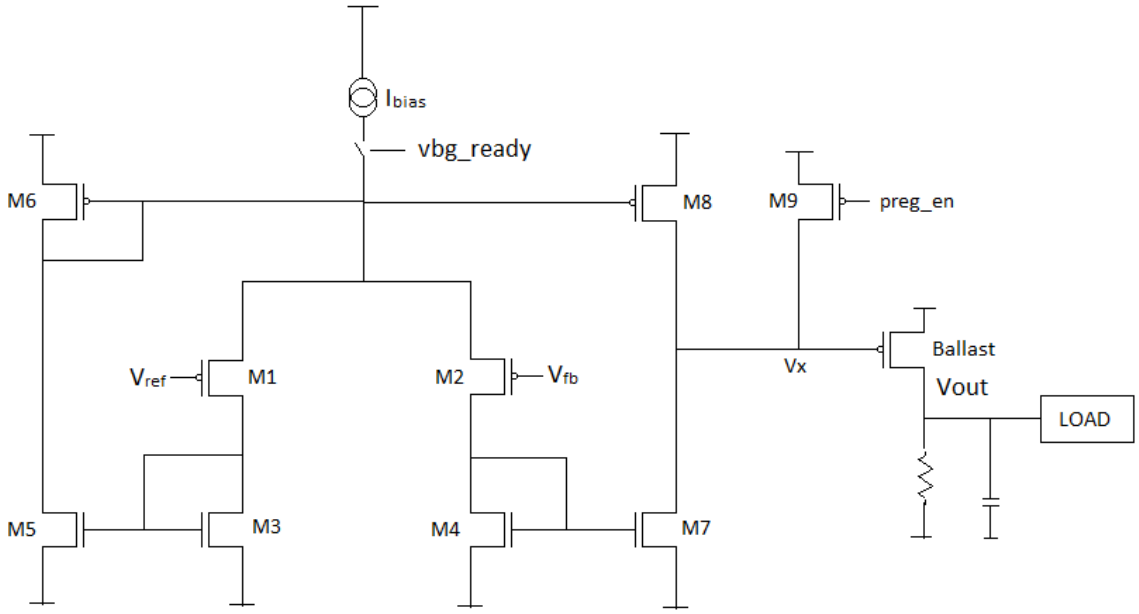

Figure 2.2: Detailed schematic of PREG

high. Now with 'vbg_ready' = 1 and 'preg_en' = 1 preg starts. Output voltage Vout shown in fig is fed back to the Vfb gate of M2. As Ballast is OFF initially Vout is 0. So Vfb is lesser than Vref. Hence current in M2 will be a little higher than current in M1. And I2 is mirrored in M7 so M7 will try to pull down the voltage at Vx. And so Vx is lesser than VDD and so Ballast starts. And Ballast will start to providing current and it will charge the capacitor. So Ballast will continue to flow current till Vout reaches equal to Vref i.e. 1.2V. So preg will start providing regulated voltage.

Now suppose load increases then Ballast will not provide current instantly so capacitor will start to provide current and will discharge very little. So voltage Vout decreases with few mV. This is fed back to Vfb and so again current from M2 will try to increase and so M7 will try to pull down the voltage Vx so Vsg for Ballast will increases and thus Ballast will provide the required current. There will be some constant voltage difference between Vref_preg and Vout in order to provide the required current. This voltage difference is called offset voltage of the regulator. This situation is shown the below figure 2.3. In the figure it can be seen that when the

load current is 0 mA, the output voltage Vout is very near to the reference voltage. So offset voltage is 0 during this period. Now when a current demand (Load current) increases from 0 to 75 mA. Then Vout will decrease with some milli volts, 20 mV in this case. And then when this current decreases again to 0 mA then Vout will again increses to 1.2 V (Vref_preg). Preg can provide upto 125-150 mA.

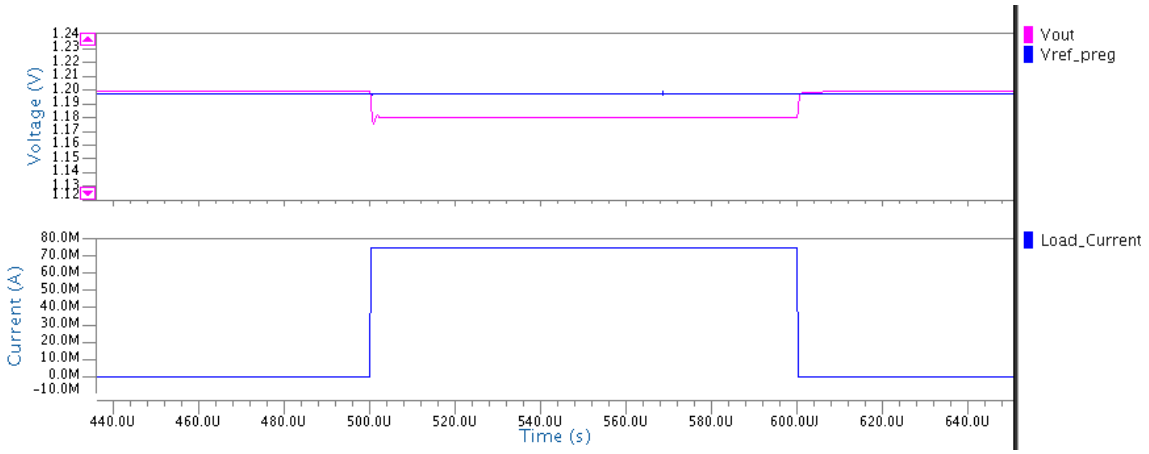

Figure 2.3: Current transients in PREG

2.3.1 Concept of soft-start

In order to avoid sudden big difference at the input of the differential amplifier, concept of soft-start is introduced. As shown in figure 2.4 the ramp generator will generate a ramp voltage which is compared to bandgap reference voltage. As output of ramp generator is below reference voltage 'cmp' is high. So 'S' input of SR latch is 0. Initially 'R' is high. So SR latch is reset and output is 0. 'ramp' is selected by mux which is buffered output of ramp generator. Now as output of voltage of ramp generator crosses the bandgap reference voltage, 'cmp' is 0. So 'S' of SR latch is high and its output is set. So bandgap voltage reference is selected by the mux. And output of this mux goes as reference voltage to the PREG.

So by using this concept of soft-start, reference voltage of preg will increase slowly

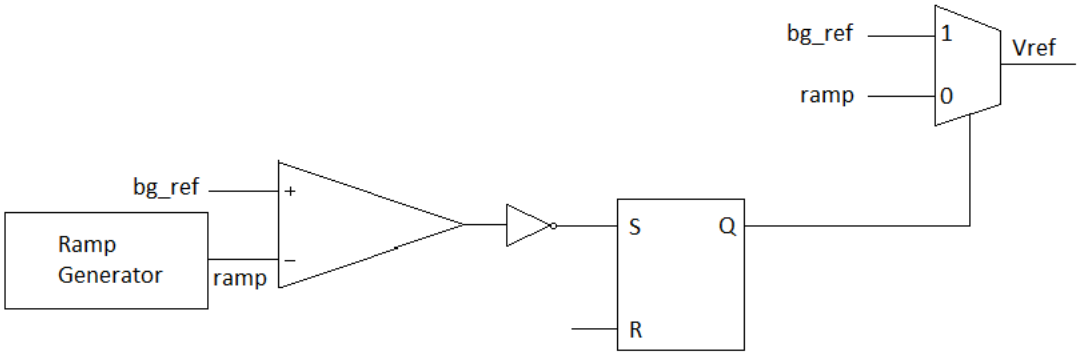

Figure 2.4: soft-start concept in PREG

instead of applying 1.2 volt directly. And once it reaches to 1.2, mux switches it to the main reference voltage coming from bandgap.

To understand importance of soft-start two simulation results are shown: start up with soft-start circuit and start up without soft-start. From fig it can be seen without soft-start amplifier of PREG will see the difference of 1.2V between its two input terminals. So amplifier will amplify this big difference and so it will reduce the gate voltage of pMOS Ballast to almost 0V. As pMOS Ballast is a very big MOS it will start providing a huge current of around 360 mA and it will charge output to 1.2V in less than 2 uS as shown in figure 2.5.

Whereas in case of soft-start circuit after enabling PREG, a ramp is applied to one terminal of amplifier and other terminal is connected to the final output voltage Vout. So Vout will follow this ramp voltage and thus the difference will be low and costant. So gate voltage of pMOS Ballast will not decrease much and a current of 20-30 mA will flow as shown in the figure 2.6.

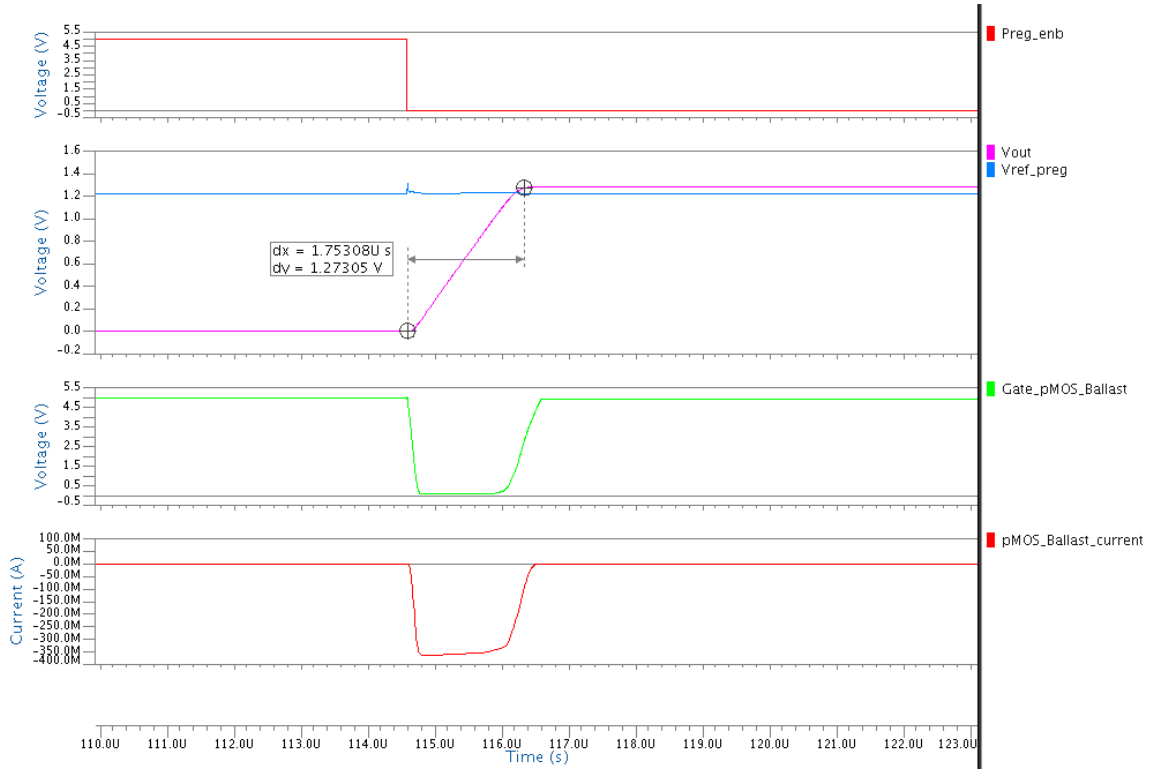

Figure 2.5: Start up with out Soft-start

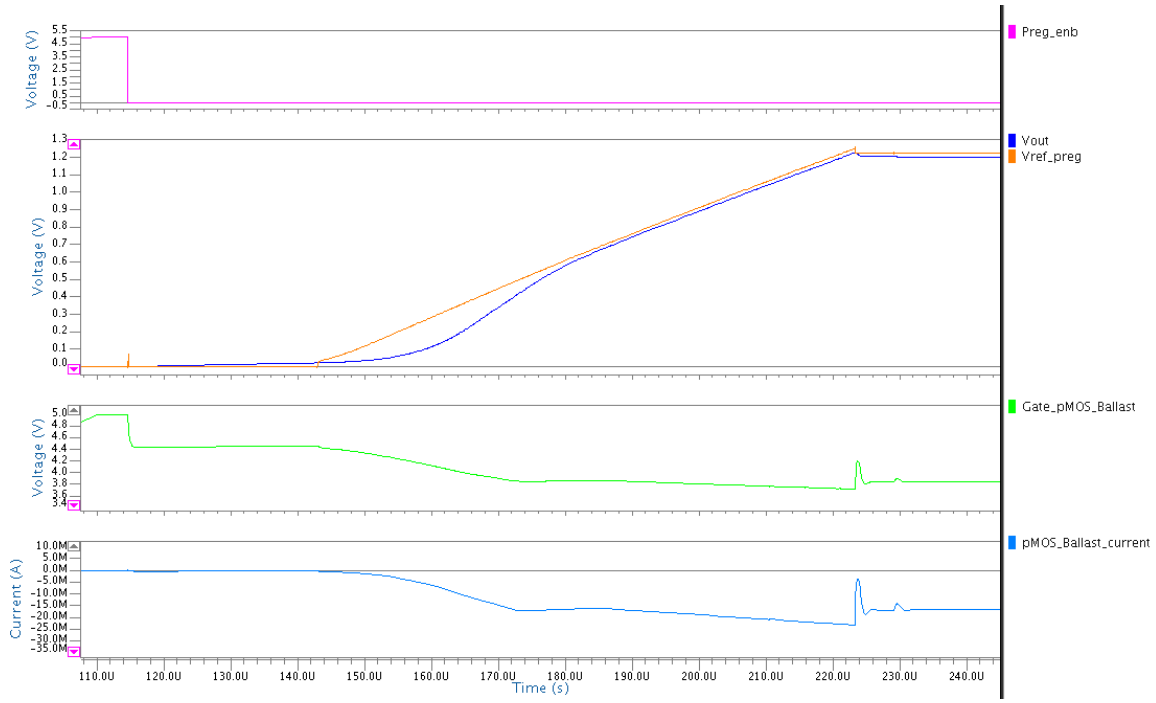

Figure 2.6: Start up with Soft-start

2.4 Low Power regulator (LPREG)

Lpreg is the low power linear regulator for the standby domain regulator which can provide only 10mA current and voltage supply of around 1.06V. In standby domain main regulator is turned off. And only Lpreg is turned on. The schematic for the Lpreg is shown below.

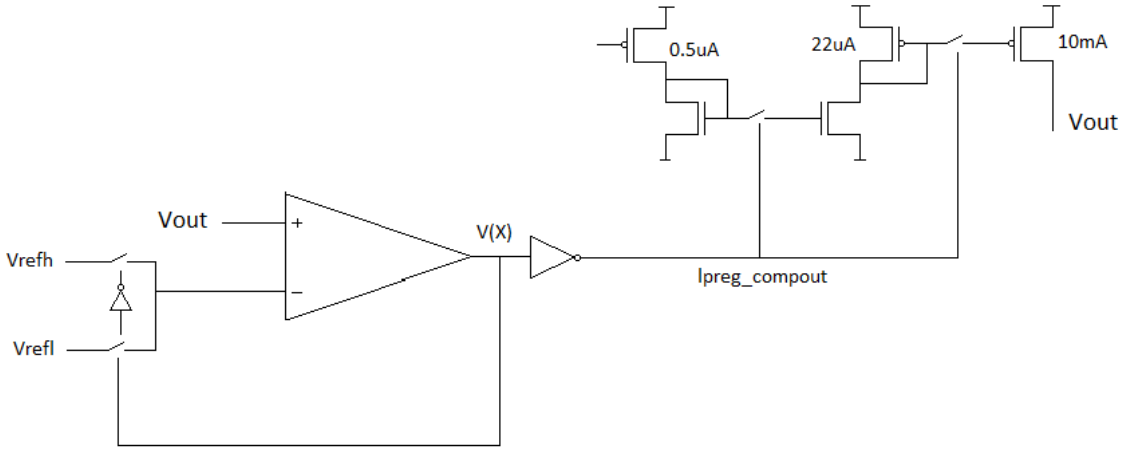

Figure 2.7: Schematic of LPREG

Now suppose we are entering into standby domain, so preg is turned off and hence low voltage supply will start to decrease. This is applied to the positive terminal of comparator shown by Vout in figure 2.7. Now in lpreg two reference voltages are used. So initially output of comparator is 1 and so vrefl = 1.06V will be selected. So Vout will keep decreasing till it reaches to 1.06V and when it just crosses 1.06V, V(x) will be 0 and vrefh = 1.064 will be chosen. And as V(x) = 0, lpreg_compout = 1 which will enable the switch. So the reference current of 0.5uA will be mirrored and according to ratio of w/l the mirrored current will be 22uA. And this current is further mirrored to 10mA. This provided to the load. And as shown in fig output point is Vout which is fed back to the comparator. So as long as Vout is less than 1.064V switches will be closed and current will keep charging the capacitor. So Vout

will rise from 1.06V to 1.064V. And when Vout crosses 1.064V V(x) will be 1 and so vrefl will get selected and the switches shown in fig will be closed and so Vout keep decreasing from 1.064V to 1.06V. So this procedure continues and Vout will keep oscillating between these two voltages.

In the figure 2.8, simulation result for lpreg is shown. After entering in standby mode, Vout will start discharging which can be seen in figure. Vref in figure is the reference voltage selected out of two values as explained above. So whenever Lpreg_comp_out is high output current will be flowed as shown in the figure.

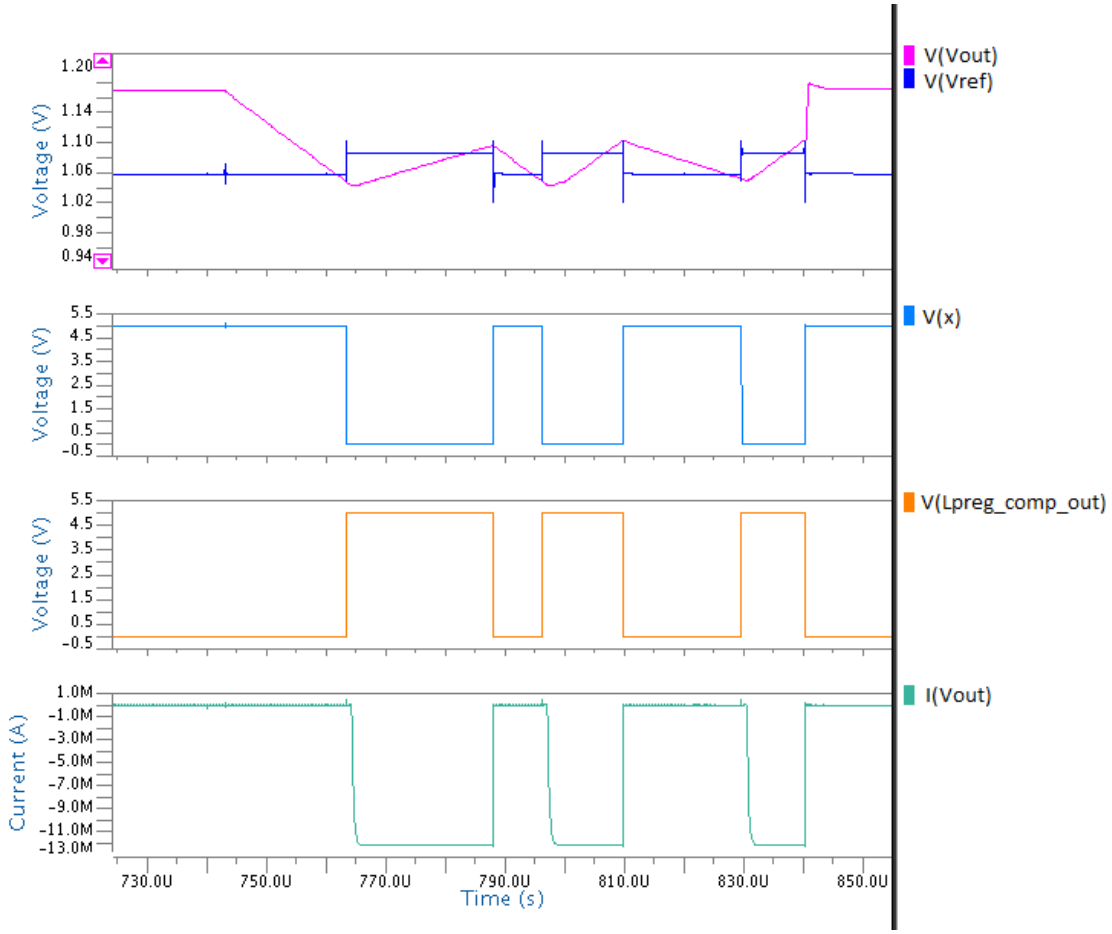

Figure 2.8: waveform showing working of LPREG

2.5 Testing of PMU

In testing of PMU there are three modes possible. (1) Test mode. (2) Bist mode. (3) Bypass mode.[7]

2.5.1 Test Mode

In Test mode all monitors are tested. Reference voltages from the bandgap voltage reference are also tested. The logic for the test mode is as below figure 2.9. A test

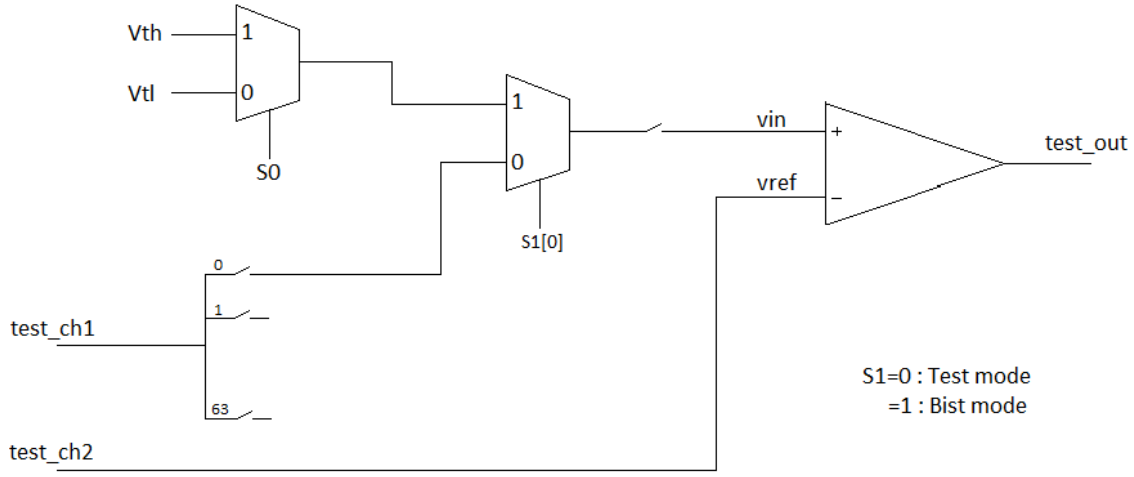

Figure 2.9: Logic for the Test mode and Bist mode

input voltage is applied at the test_ch1. There are many voltage detectors (monitors) in the PMU, so in test mode one by one all monitors is tested. And to choose the monitor there is 6 bits input pin, which through a decoder goes to switches and select a particular channel for the particular monitor. Now there is a separate 6 bits input pin for the bist mode. So in test mode these bits are 0. And these bits go to the selection line of all the multiplexer which is responsible for the selection of input between test mode and bist mode. So in test mode S1[i] = 0 for all i. where i is the number of multiplexer. So now as S1 is 0, the applied test input goes to the comparator of the particular monitor and its output comes to the output pin 'test_out'.

So while testing 2 voltage levels are given i.e. first voltage lower than the reference voltage is given than a voltage level higher than the reference voltage is given so its input switches from low to high and it should reflect at the output of the comparator by switching low to high. And again lower voltage is applied to the input so output again switches from high to low. Thus monitor is tested for both cases when input goes from low to high monitor output goes high and when input goes from high to low monitor output goes low which indicates that the voltage is dropped below a particular level. Reference used for the monitor can also be measured at the 'test_ch2' which is an output pin.

Figure 2.10 shows the testing of monitor in the test mode. Vin is applied externally to the test channel input and is transferred to the input of the monitor as explained in the test mode section. Vin is applied as 101 sequence so that when it crosses the reference voltage comparator will change its state and monitor can be tested. Different

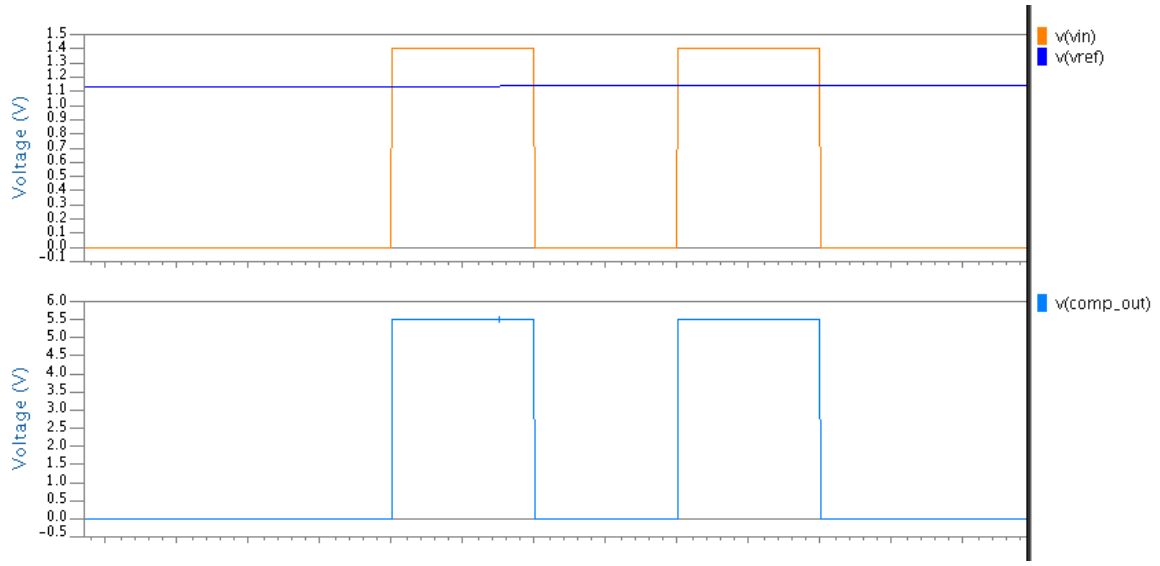

Figure 2.10: Monitor testing in Test mode

reference voltages of regulators or monitors can also be tested in the test mode. And if its value is not as desired due to some variations it can be corrected using trimming logic which is explained in detail in separate section.

Trimming

Due to process variation in fabrication there may be some difference of the reference voltage due to bandgap circuit, the regulated output of the regulator or monitors. Trimming is process of applying some trim bits to the circuit so that the variation in voltages due to process variation can be compensated. The logic for the trimming is shown in the figure 2.11. Take an example of bandgap circuit. On 'test_ch1'

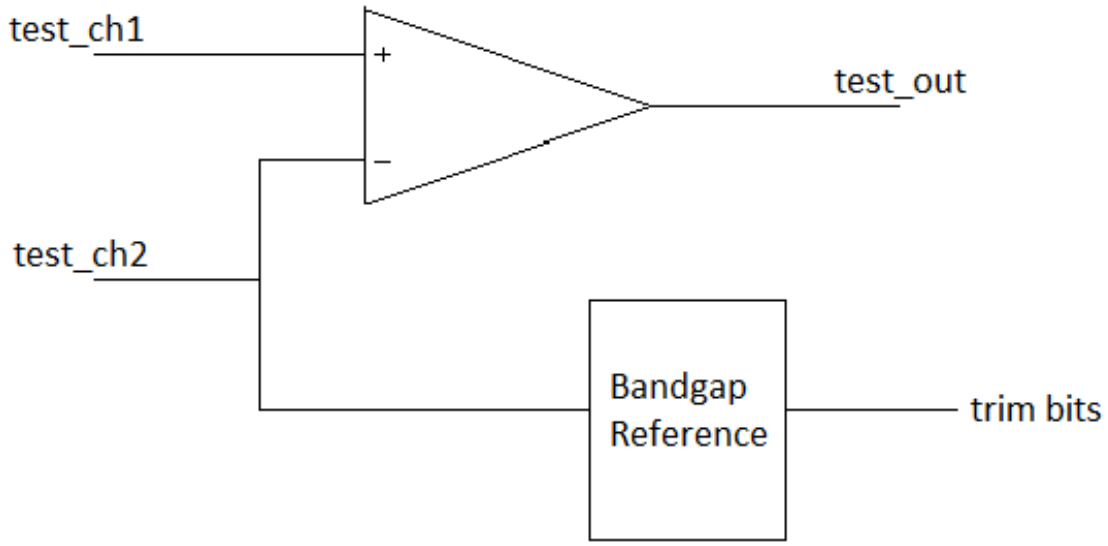

Figure 2.11: Bandgap strategy

desired input voltage is applied, which goes to a comparator. The second input of the comparator comes from the bandgap circuit. For example instead of the giving the reference voltage of 1.2V it is giving 1.18V. Now at the positive terminal of the comparator an input voltage of 1.2V is applied which is the desired voltage from the bandgap. The comparator will give the output '1'. Now some trim bits are applied to the bandgap circuit which was 0 till now, now to correct the output of the bandgap, trim bits are changed. So the input at the negative terminal of the comparator will change and so the output of the comparator will also change. Trim bits keeps changing until the output of the comparator just switches to 0 from 1. Similarly if the output of the bandgap is more than the desired voltage i.e.1.2V than

comparator's initial output would be 0 and trim bits are set such that it switches to 1.

Thus when output comparator trips we can say that the output of the bandgap is at the desired value. So these trim bits are stored in the registers. And every time the PMU starts, these trim bits are applied to the bandgap from the register. Thus for every single IC trim bits are different and is decided at the time of the testing of the IC by this process. So trimming is a one-time process. Similarly for monitors and regulators trimming process is done.

2.5.2 Bist Mode

PMU has Bist mode to check the status of all the voltage monitors after power up. The bist pattern runs after every power up. In bist mode a 6 bit input pin is set to a particular value, which is applied to the decoder and output of the decoder goes to 64 multiplexers' selection line which is shown in figure 2.9 (S1[i]). So in bist mode for the particular monitor the selection line of the multiplexer is 1 and channel 1 is selected.

Now in bist mode from a threshold voltage generator two voltages i.e. vth and vtl, are generated. These two voltages go in inputs of a multiplexer. The selection line of this multiplexer S0 is connected with a pin 'bm_vt_sel'. This pin stays at 0 for some time than goes 1 for a particular time and then again it goes to 0. Here vtl is lower than the threshold voltage and vth is higher than the threshold voltage of the monitor. Output of this multiplexer goes to next multiplexer which is kept to choose between test mode and bist mode. This further goes to the positive terminal of the comparator. At negative terminal of the comparator reference voltage is applied.

So when S0 = 1 vth gets selected, which is higher than threshold voltage of the monitor, comparator gives 1. Then S0 switches to 0, vtl gets selected, which is higher

than threshold voltage of the monitor, comparator gives the output 1. Thus output of comparator is measured and the voltage comparator can be tested. Like this every other monitor is selected one by one and tested.

Figure 2.12 shown below explains how a monitor can be test in Bist Mode. In Bist mode as explained earlier a signal called bm_vthsel will be given a sequence of 101 so it will select input voltage between two voltages generated by a voltage generator. So the input applied to monitor is shown with bm_vt in below figure. And a reference voltage is shown. So when this bm_vt changes the comparator output changes accordingly and monitor can be tested.

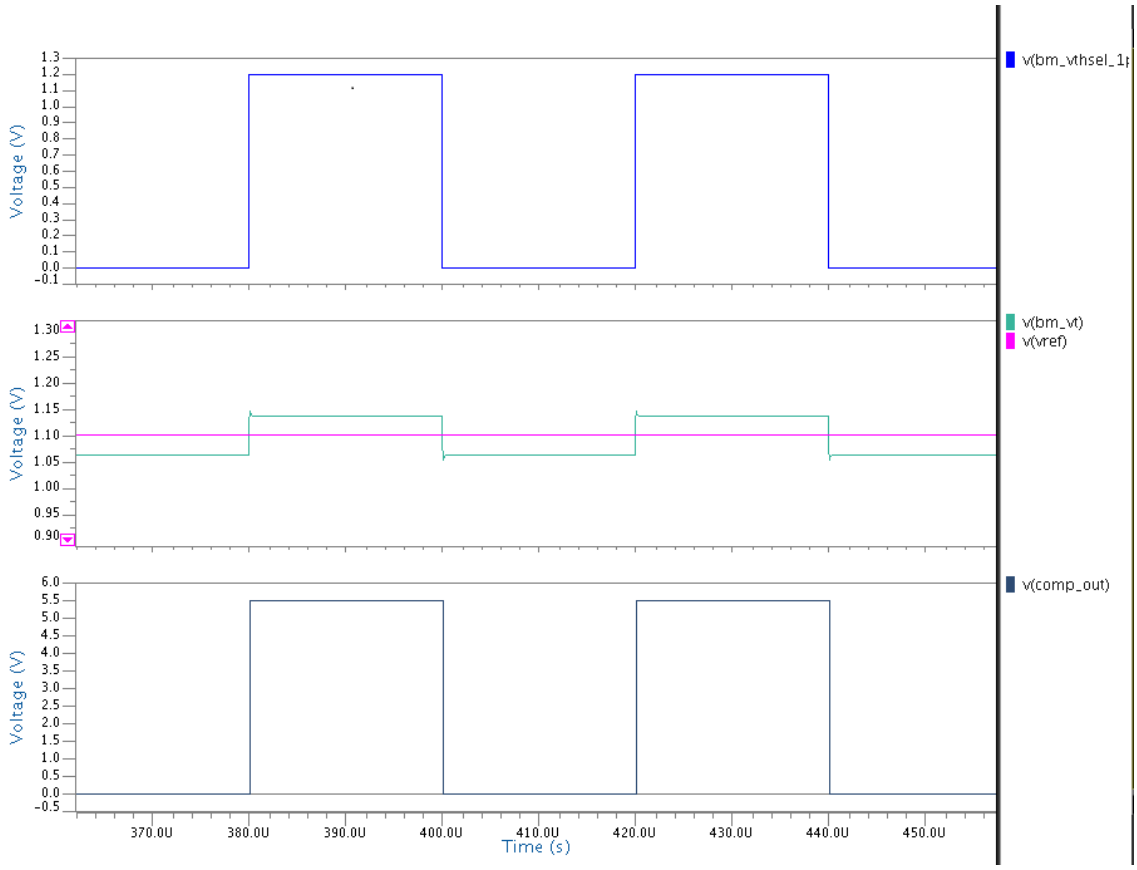

Figure 2.12: Monitor testing in Bist mode

2.5.3 Bypass Mode

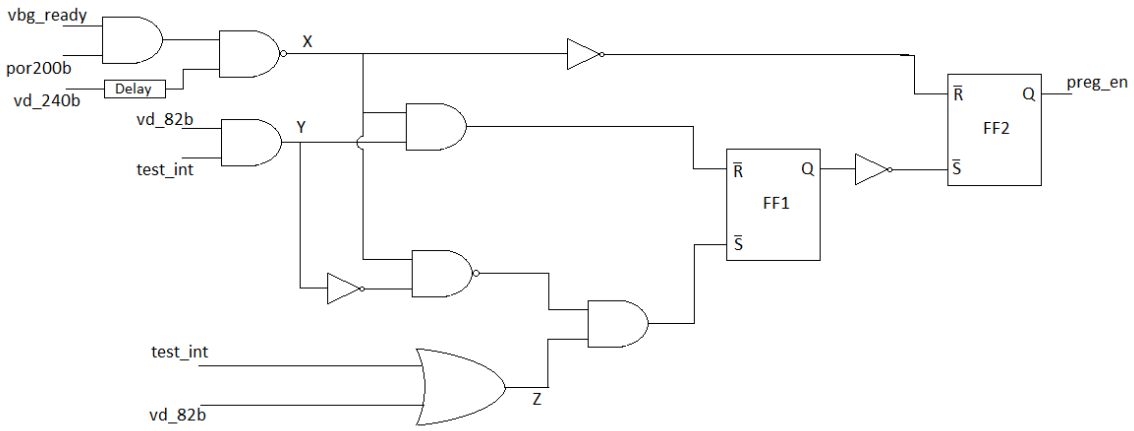

Figure 2.13: Configuration for entry and exit in Bypass mode

In bypass mode low voltage supply is given externally and regulator inside PMU is off. Low voltage supply is given before the high voltage supply whereas in normal mode high voltage supply is given earlier than low voltage supply.

Initially bandgap is off and so vbg_ready = 0 so X = 1. Now in bypass mode test_int signal is set to 1 externally. All monitors in PMU are enabled only after bandgap reference voltage is ready and vbg_ready signal is high. So as vbg_ready is 0, vd_82b = 0. Thus Y = 0 and so set input for FF1 is 0 and reset input is also 0, hence FF1 is in 'No change' mode.

Now after bandgap is ready, vbg_ready is high and hence all monitors are enabled so vd_82b and vd_240b are high. vd_240b is applied through delay. So Y will be 1 but X will be still 1 because of delay. Therefore set input is 1 and reset input is at 0 so FF1 is in reset mode. So Q of FF1 will be 0 and set input for FF2 will be 1 and reset input for FF2 is 0 so FF2 will be in reset mode. Therefore output of FF2 is 0 and so preg is disabled. Then after X becomes 0 and reset input is 1 of FF2. And set input for FF1 will be 0 so Q is high and so set input for FF2 is high, and hence

FF2 will be in 'No change' mode. Thus preg is disabled.

Exit from Bypass Mode

To exit from Bypass mode we need to set the FF2 and for that we need to set FF1. So any two of the three input i.e. test_int, vd_082b and vd_240b, are 0 then we can exit from bypass mode. The possible for exit from bypass is shown below:

Exit_1: test_int = 0 & vd_240b = 0 => X = 1, Y = 0.
Exit_2: test_int = 0 & vd_82b = 0 => Z=0.
Exit_3: vd_82b = 0 & vd_240b = 0 => X = 1, Y = 0.

So in all above combinations FF1 will be set and so Q of FF1 will be 1. And so set input for FF2 is 0 and hence output of FF2 will be high so preg is enabled.

Chapter 3

PMU9 Architecture

3.1 Introduction

PMU9 is mainly differed in current capability. To increase current capability BJT is used which can provide very high current. But transient response is not so good of BJT so PMOS is also used as in PMU8. Detailed description of Regulators scheme is shown further in this chapter. Standby mode sequence and standby domain regulator is also changed.

Other than regulators there are also some other changes like number of Low Voltage Detectors (LVDs). Other features of PMU like test mode, bist mode and bypass mode, etc. are same as PMU8 only.

3.2 Regulators

In PMU9 there are total 5 regulators: (1) High Power Regulator (HPREG), (2) pMOS Regulator (PREG), (3) nMOS Regulator (NREG) and (4) Low Power Regulator (LPREG).

HPREG is the main regulator which provides all the required current. Current ca-

pability of HPREG is very high, because the current providing element (Ballast) is BJT. BJT is capable of providing very high current. Current capability of HPREG is 400 mA. But the drawback of this regulator is that transient response of BJT is very slow. So if current demand increases suddenly then this regulator can not provide immediate current.

So for this purpose PREG is used. This PREG is same as used in PMU8. Here a pMOS is used as Ballast. pMOS is much faster than BJT. So PREG can provide sudden requirement of current upto 150 mA in 100 ns. NREG is current sink regulator. It continuously checks that the regulated output is below 1.22V or not. If somehow the output voltage increases to 1.22V then NREG will start sinking current which will further down the output voltage by discharging the output capacitor.

LPREG is the regulator for standby mode only. The output current capability of LPREG is 10 mA. All other regulators are turned off in standby mode except PREG. And if current requirement increases further in standby mode than PREG is turned on in standby mode to provide required current

3.2.1 High Power Regulator (HPREG)

As stated earlier in HPREG the Ballast used is BJT. BJT can provide high current of 400 mA. As shown in the figure 3.1 there is an error amplifier which is an OTA. This OTA is the same as explained in the PREG of PMU8. As shown in the figure on one input reference voltage of 1.98V is given, and on second input the final regulated output voltage is fed back.

If Vfb is lower than vref (1.98 V), then output of the amplifier will be pulled down from VDD. So the pMOS M1 will start conducting and it will start providing current, which

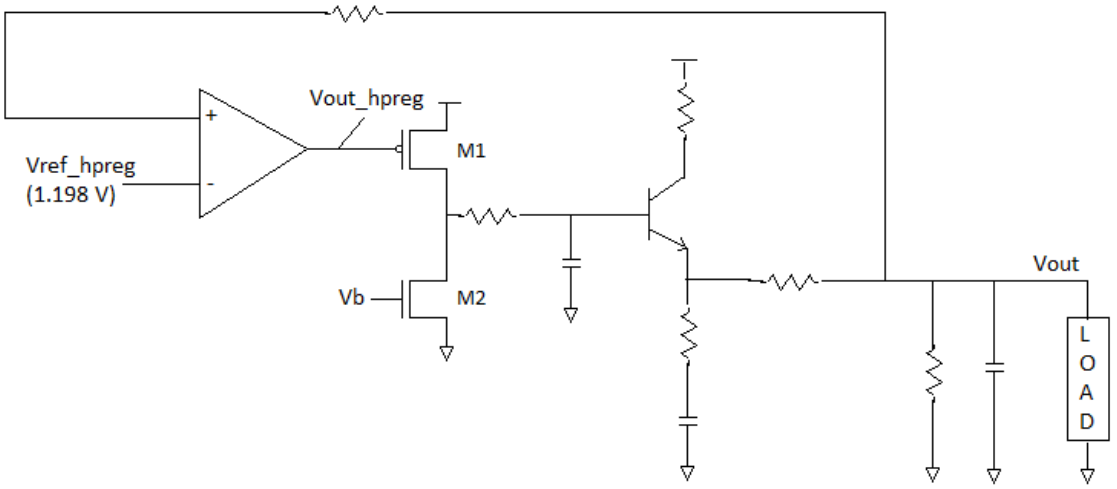

Figure 3.1: Schematic of High power Regulator

is applied to the base of BJT. So due to this base current, BJT will start providing emitter current. This high current of BJT will start charging the capacitor. And when the voltage across capacitor will reach just above the reference voltage of the regulator, output of the amplifier will increased and so the Vsg for M1 will decrease so base current will also decrease and thus output voltage is settled at 1.2V, just above the reference voltage.

3.2.2 PMOS Regulator (PREG)

PREG design is same as in PMU8. But the role of PREG is somewhat different. Here the PREG is responsible for the transient requirement of the current. For example if a sudden rise in current demand of 75mA or 100 mA in about 100ns then BJT can not act this fast. So the moment current demand increases, output voltage will decrease slightly. So when this output voltage decrease below reference voltage of PREG which is 1.173V, the PREG will come in picture. Error amplifier of PREG will detect this decrease in output voltage and it will amplify this voltage difference. So the output node of the amplifier will be pulled down. So Vsg for the pMOS (Ballast) will increase and so the output current will start providing current. And capacitor will be charged

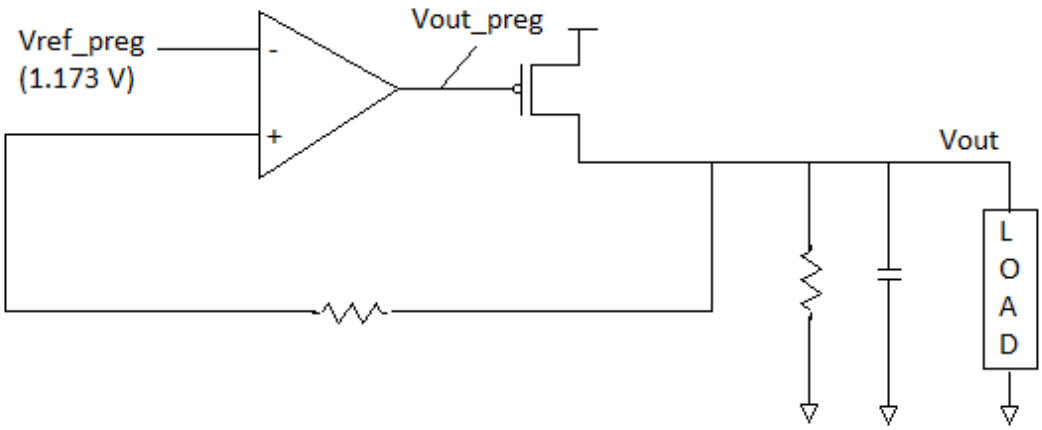

Figure 3.2: Schematic PREG

again and output voltage will again start to increase and so output voltage will not go below 1.17V (Vref_preg) meanwhile by this time HPREG will also detect this current requirement and decrease in voltage because PREG can give only output of 1.17V not 1.2V. So HPREG will start acting and will increase output voltage to 1.2V from 1.17V. And the moment output voltage is increased above Vref_preg RPEG will be out of the picture because output of amplifier will be pulled high and this will turn of the pMOS Ballast.

So the PREG is needed only to ensure that output voltage do not decrease too much due to high current demand. Because as BJT is slow there may be the case that a sudden current demand comes and before HPREG starts providing the current the output capacitor will discharge and output voltage will decrease to much lower value. So in this case PREG is really very usefull.

3.2.3 NMOS Regulator (NREG)

NREG is the opposite of PREG, PREG is current source while NREG is the current sink. And instead of pMOS Ballast, nMOS Ballast is used. An error amplifier

is also used to detect the output voltage. Reference voltage for NREG is 1.22 V. Vref_nreg is given at the negative terminal and output voltage is fed back to the positive terminal. So when regulated output is below Vref_nreg the output of amplifier is 0 and hence the nMOS Ballast is off. Now suppose suddenly current require-

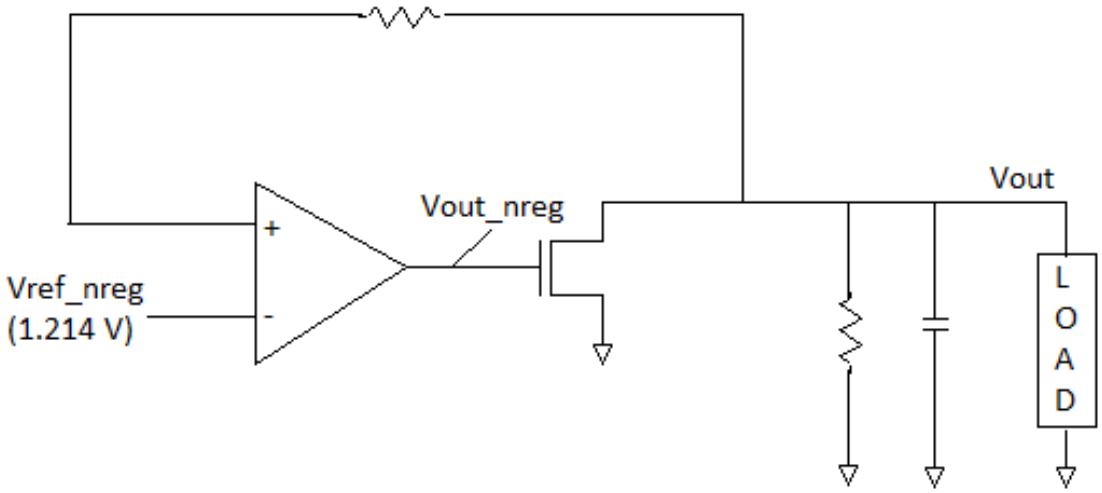

Figure 3.3: Schematic NREG

ment decreases. For example from 400 mA, suddenly current demand decreases to 150 mA. Then BJT will not decrease the output current immediately. Now as load current is now decreased, all the emitter current will start charging the capacitor. And the output voltage will start increasing. So if the output voltage reaches above Vref_nreg (1.22V) then output of amplifier will increase and nMOS Ballast will be on and it will sink some amount of the current and it will decrease the output voltage.

Thus NREG ensures that the output voltage do not increase above a certain level i.e. NREG will only come into act when the load current decreases suddenly with huge amount, because HPREG will not decrease its output current immediately so there should be one current sink which can sink this current.

3.2.4 Working of HPREG, PREG and NREG together at boot up & after settling

Start Up

At start up (boot up) reference voltage for PREG is kept higher than HPREG. Here also the concept of soft-start is used just like in PMU8. So this reference voltage of PREG will start ramping from 0 to 1.22V. So with increase in this reference voltage, final output voltage will also start rising, because initially Vout is at 0. And this Vout is fed back to the error amplifier as shown in the figure 3.4. So when Vref_preg increases, output of amplifier (Vout_preg) will decrease from VDD. So pMOS Ballast (M1) will start providing the current and will charge the output capacitor. So the final output Vout will start increasing and it will follow the reference voltage.

Reference voltage will keep increasing till it reaches to 1.22V. After that it will be constant 1.22V. So output voltage will also reach to 1.22V. Till now HPREG is out of picture, because at start up only PREG is turned on, HPREG is off. After settling output voltage at 1.22V HPREG is turned on. But as Vout is at higher value than Vref_hpreg, HPREG is still out of picture. Then reference voltage of PREG is stepped down to 1.17V. Thus final output voltage will also decrease to 1.17V.

So now HPREG will start acting. Vref_hpreg is 1.2V and Vfb is 1.17V. Therefore output of the amplifier will be pulled down and M2 will be on. So it will start flowing current. And base of BJT will start charging from 0V. Base will take some finite time to get charged at sufficient level. Once Vbe gets pass to the threshold voltage, BJT will start providing current and it will increase the output voltage to 1.2V. This situation is shown in figure 3.5.

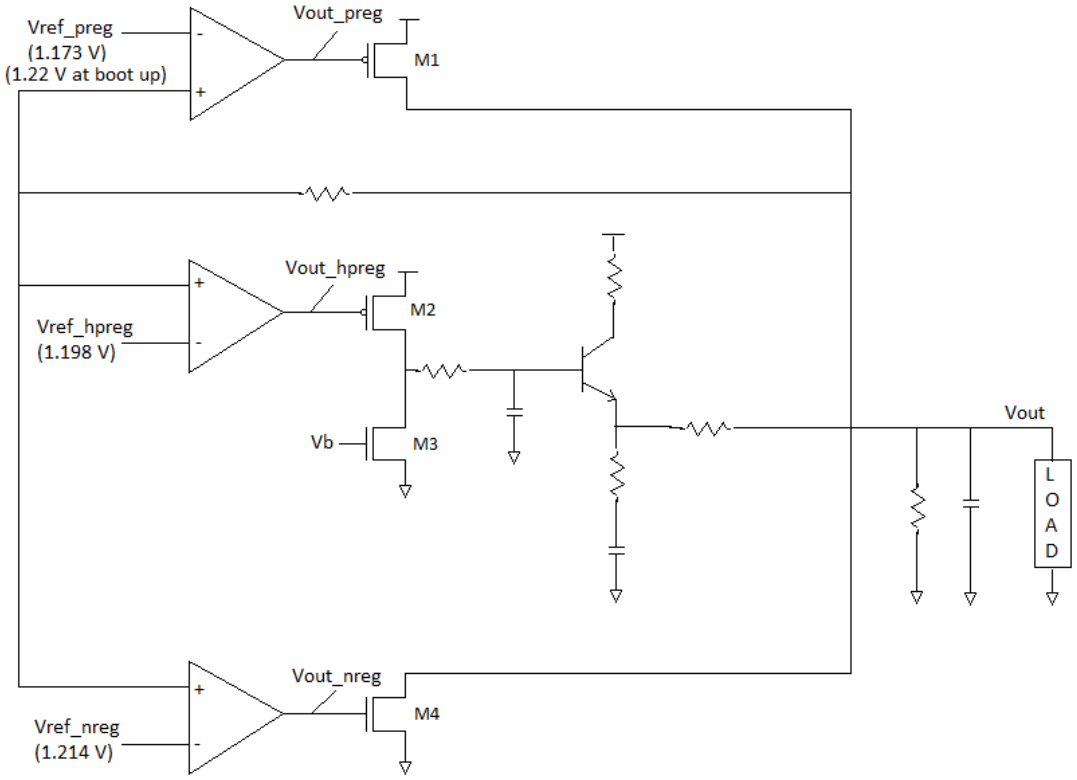

Figure 3.4: Schematic of HPREG, PREG and NREG

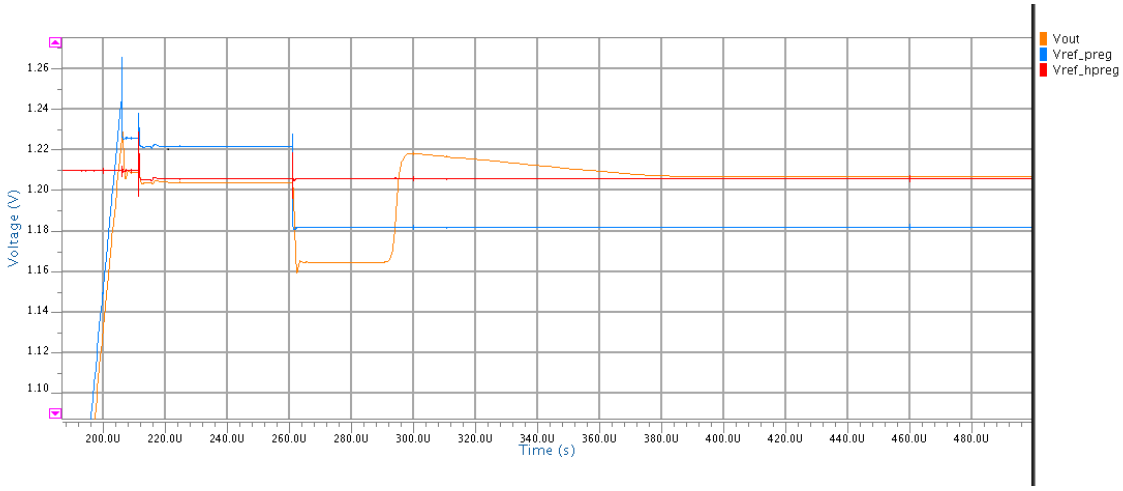

Figure 3.5: Simulation result explaining Start Up condition

After Settling

1. **Small Increase in the load current:** After settled down if small current demand increases then Vout will not decrease too much. So it will not go below Vref_preg. So PREG need not to act and only HPREG will take care of this current transient.

2. **Big increase in the load current:** If If the current demand is high in short time than before HPREG provide this current the capacitor will start discharging and so Vout will decrease with a few mV. So once this voltage goes below the reference voltage of PREG, its amplifier output will decrease and pMOS ballast (M1) will be on. And it provides immediate current. So PREG will not allow the Vout to decrease further.

3. **Small decrease in the load current:** If the load current decreases by small amount i.e. small transient, then HPREG will detect this decrease in the load current and it will decrease the base current of BJT. But it will take some time to react. So before HPREG decreases the emitter current, this extra current of emitter other than load current will start charging the capacitor to a higher value than 1.2V. And once HPREG reacts to this change in current it will decrease the emitter current and so Vout will also decrease.

4. **Big decrease in the load current:** If the decrease in the load current is high then as HPREG will take time to react and so high emitter current will start charging the capacitor because load current is low. Thus as the decrease in current is big capacitor will charge at very high value, and there may be chance of increasing this voltage above the 1.22V, which is the reference voltage of the NREG. Then NREG will come into act only when the Vfb is higher than 1.22V. Hence output of the amplifier of NREG will increase and it will turn on the nMOS Ballast (M4) and it will sink all the extra current. The moment Vout decreases below the reference voltage of NREG, it will be out of the picture.

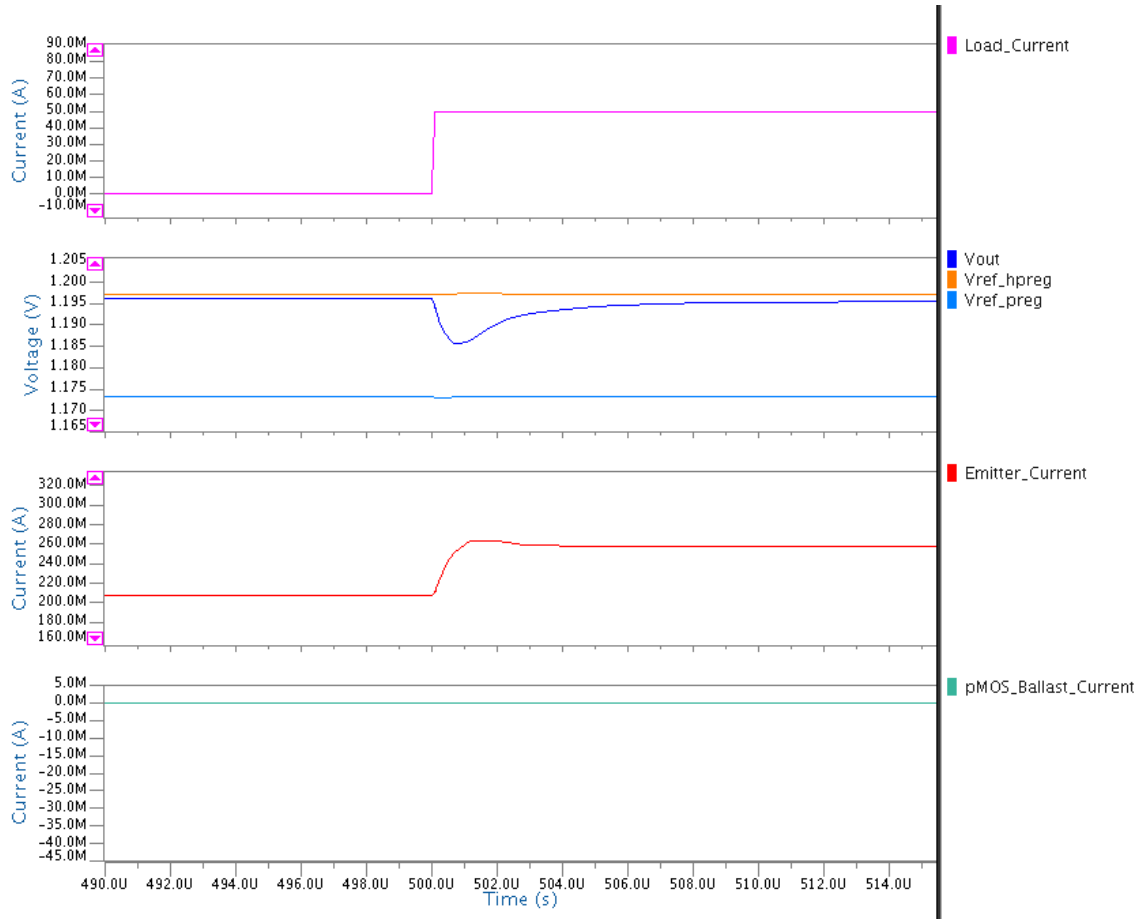

Figure 3.6: Small increase in Current

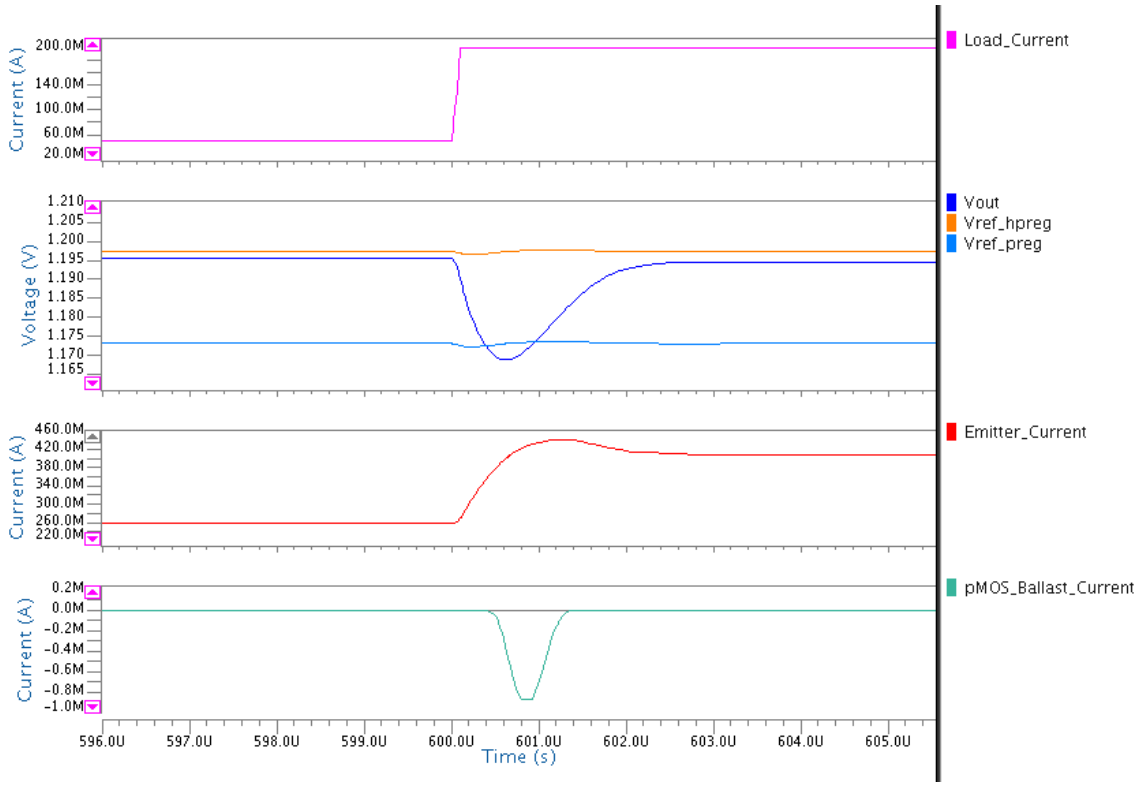

Figure 3.7: Big increase in Current

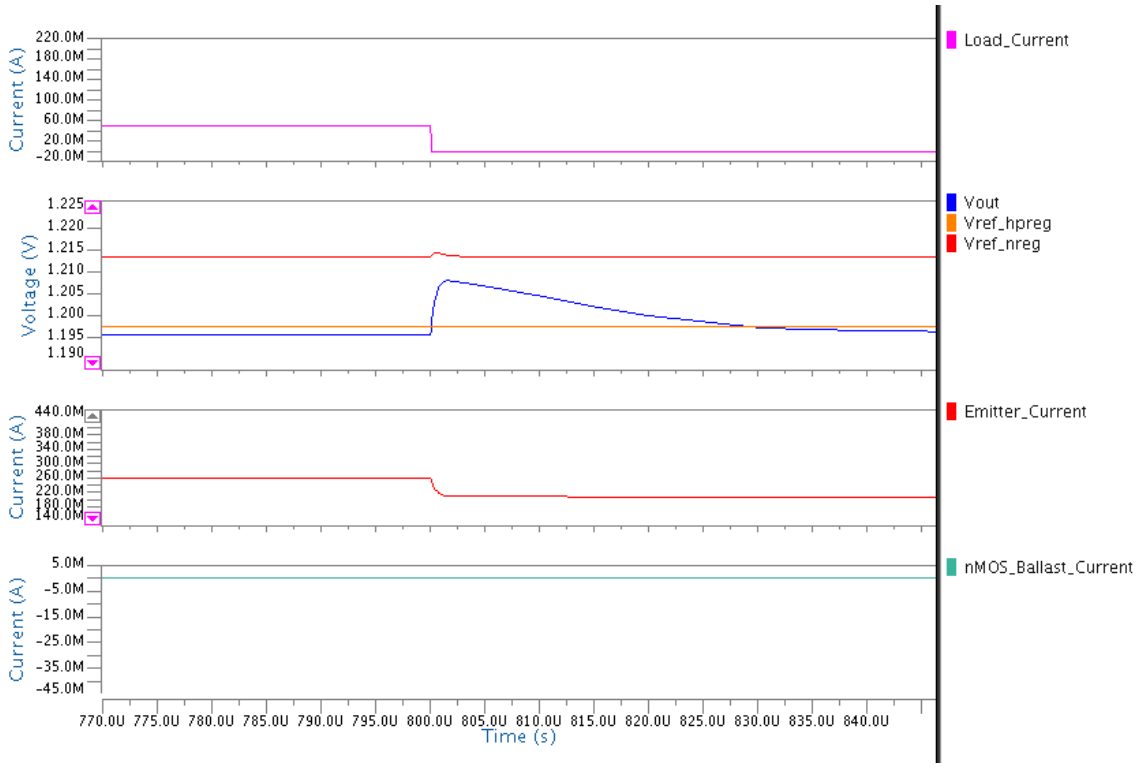

Figure 3.8: Small decrease in Current

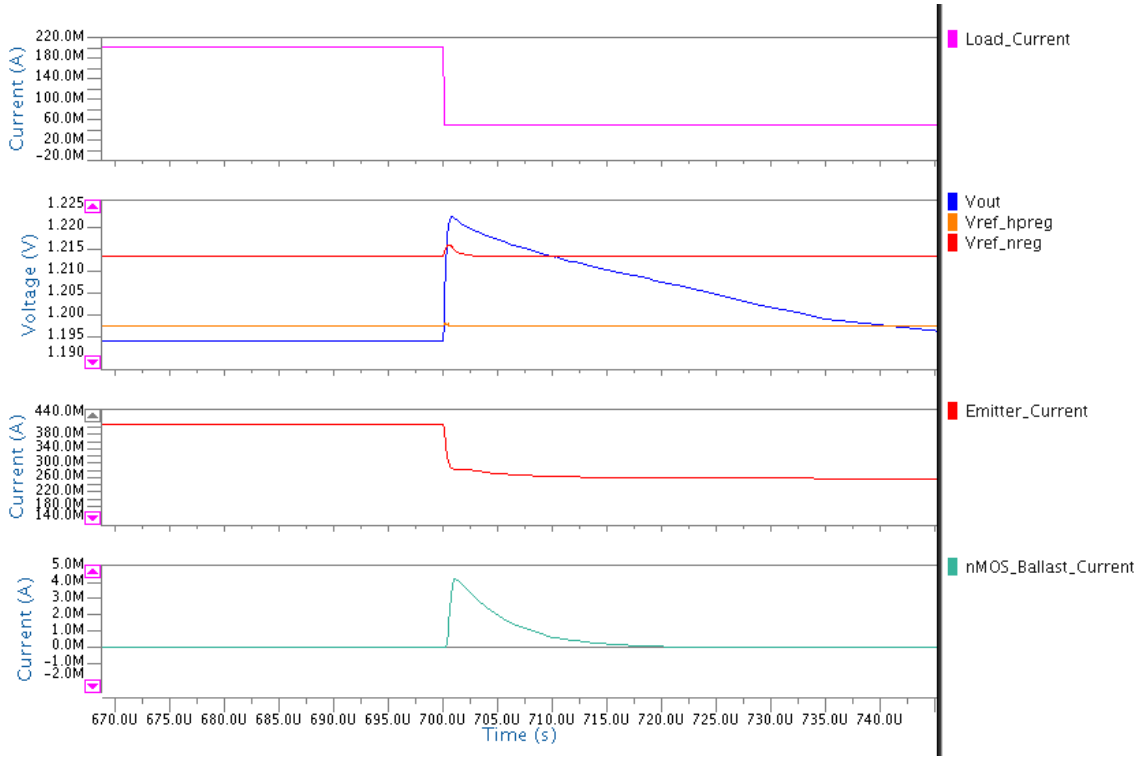

Figure 3.9: Big decrease in Current

Hence from above discussion it is clear that PREG is used in start-up of the PMU. And after settling PREG and NREG are only used to handle the transients. PREG takes care that Vout do not go below 1.17V and NREG takes care that Vout do not go above 1.22V. So Vout will always be between these two values, which is the main aim of PMU that irrespective of the load current the regulated output should not change much.

3.2.5 Importance of PREG

To understand importance of PREG lets assume that there is not PREG, and only HPREG is present. Now if a current transient comes, for example load current increase from 0.4 mA to 75 mA. In the figure 3.10 simulation result for this situation is shown.

Now when the load current increase output capacitor will start discharging and thus output voltage Vout will decrease from 1.2V as shown in the figure 3.10. So when it goes below the reference voltgae of HPREG, the amplifier of HPREG will detect this decrease and will amplify this difference and it will increase the base voltage of BJT as explained earlier. So Vbe will increase and emitter current will also increase. Thus it will provide the required load current and also it will charge the output capacitor back to 1.2V. But in all this procedure it will take some time because BJT is slow device compared to MOSFET. So in this case the output voltage decreases upto 1.45V i.e. the undershoot in the output voltage is around 68 mV.

Now take the case if PREG is there to support HPREG. Here also when the current increase, Vout will decrease and capacitor will start providing current. But when it goes below the reference voltage of PREG (1.178V), the amplifier of PREG will detect this difference and it will decrease the gate voltage of pMOS Ballast. Bigger the difference higher decrease in the gate voltage. Thus due to decrease in Vsg of pMOS,

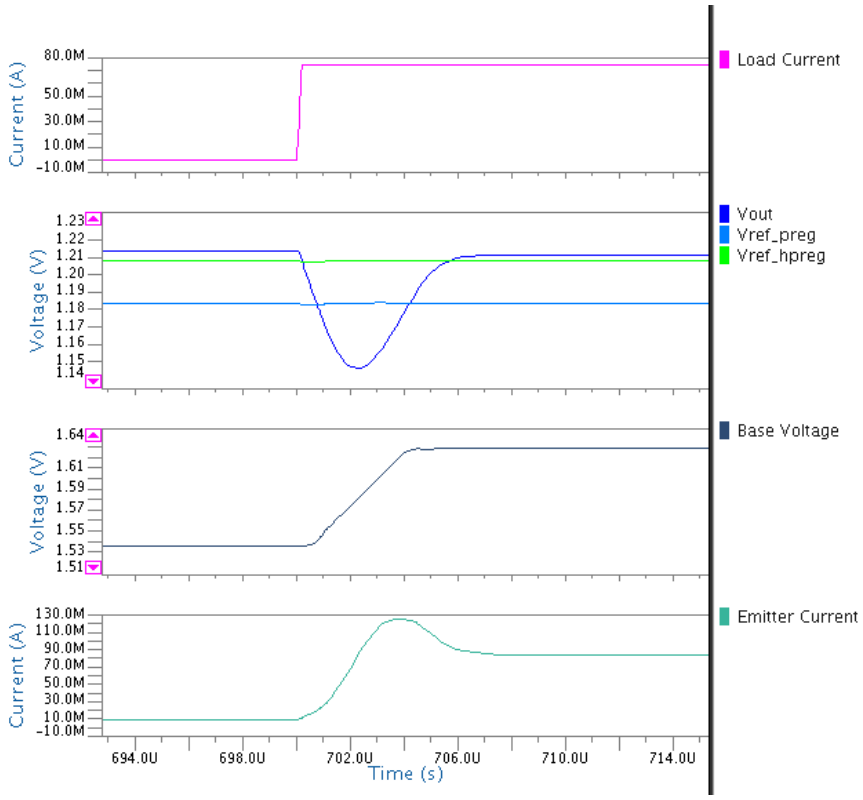

Figure 3.10: Current Transient without PREG

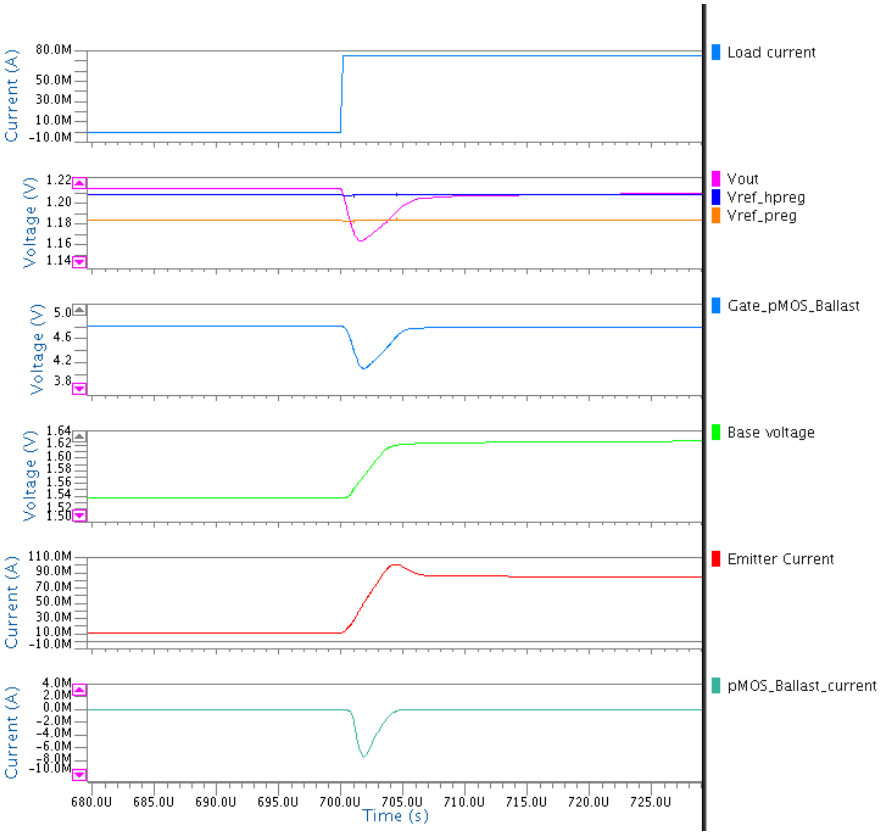

Figure 3.11: Current Transient with PREG

it will start providing current and also start to charge the capacitor. So output voltage Vout will increase, so when it increase above Vref_preg, PREG will be out of picture and the gate voltage of pMOS Ballast will increase back to VDD. So it will stop providing the current. Meanwhile HPREG will start acting and will see that the current requirement is increased. So it will start providing the required current. And PREG will be active only till HPREG is not able to provide the required current. So in this case the output voltage decreases upto 1.65V i.e. the undershoot is 50 mV. Figure 3.11 shows this situation with PREG. In the figure 3.12 the difference between Vout in both the cases is shown separately.

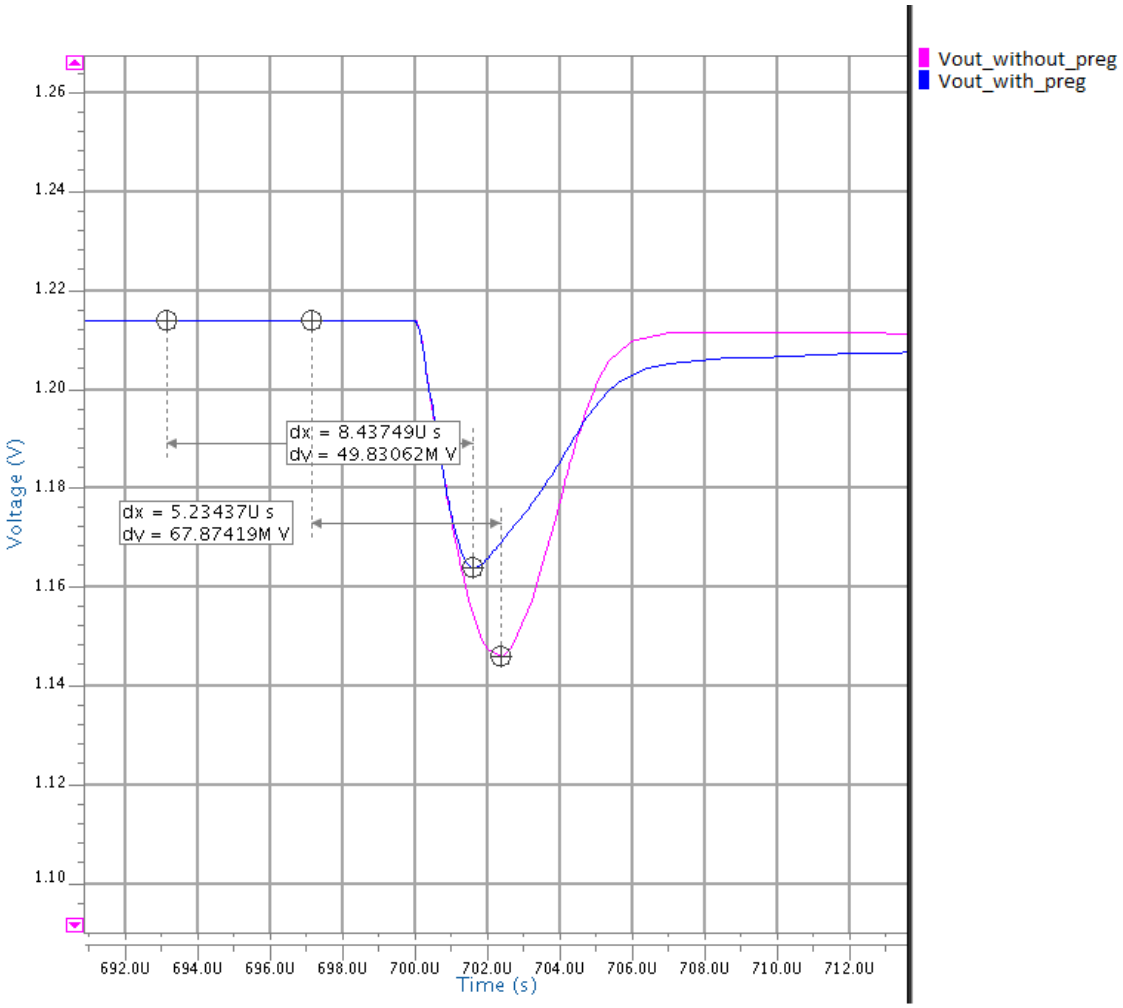

Figure 3.12: Difference in Vout with and without PREG

3.2.6 Importance of NREG

Now same as PREG, to udnderstand the need of NREG, lets take an example where the current demand decreases from 75 mA to 0.4 mA. In the figures 3.13 and 3.14 two cases of current transient with NREG and without NREG is shown.

In first case i.e. without NREG, if the current decreases suddenly from 75 mA to 0.4 mA. Now here HPREG has set the base voltage and base current to such a value that the emitter current is equal to the current demand i.e. 75 mA. Now suddenly current demand decreases but BJT is still giving the current. Now load current is very very small, so where all this emitter current will go? It will charge the output capacitor. So output voltage will start increasing. In the current example it is increasing upto 1.3V. This is happening because when current demand decreases amplifier of HPREG, shown in figure 3.13, will increase the gate of the pMOS so it will not provide any current. But the capacitor is charged to a particular value to provide sufficient voltage when the current was 75 mA. Now current demand is decreased but base voltage is still at the same value because the current sink at the base is very small. So due to this base voltage BJT will keep providing the current and it will charge the capacitor to high value.

Now lets see how NREG will solve this problem. When the load current decreases, in this case also emitter current is same and it will also start charging the capacitor. But when the voltage reaches upto the level of reference voltage of NREG i.e. 1.22V, amplifier of NREG will see this difference between Vout and Vref_nreg and it will increase the output of the amplifier which is the gate of the nMOS Ballast. Thus this nMOS Ballast will start sinking the current from Vout. So now all the extra current provided by emitter will be sinked by nMOS Ballast of NREG which was charging the capacitor to a very high value in the previous case. But in this case output voltage will go only upto 1.22V which is the reference voltage of NREG.

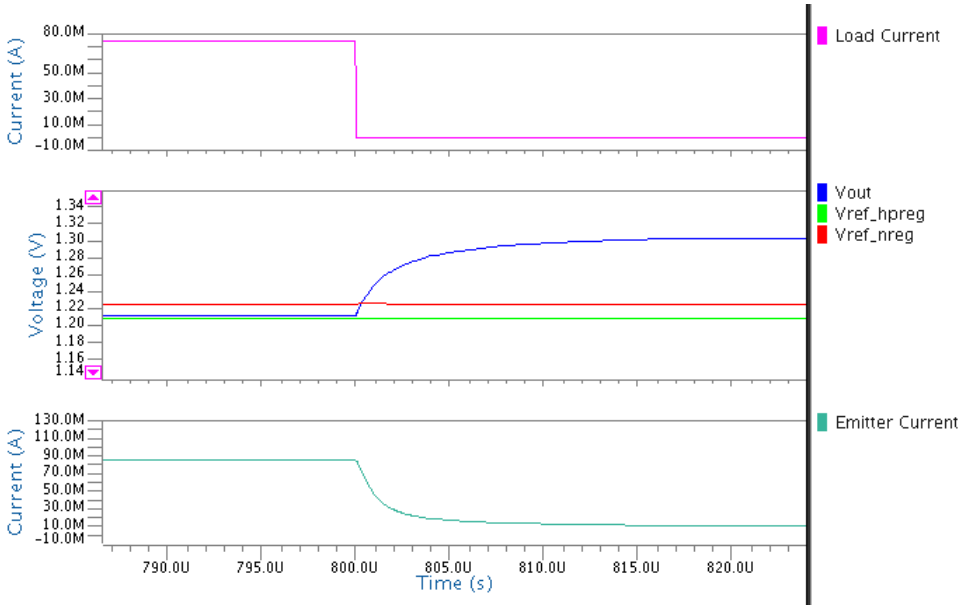

Figure 3.13: Current Transient without NREG

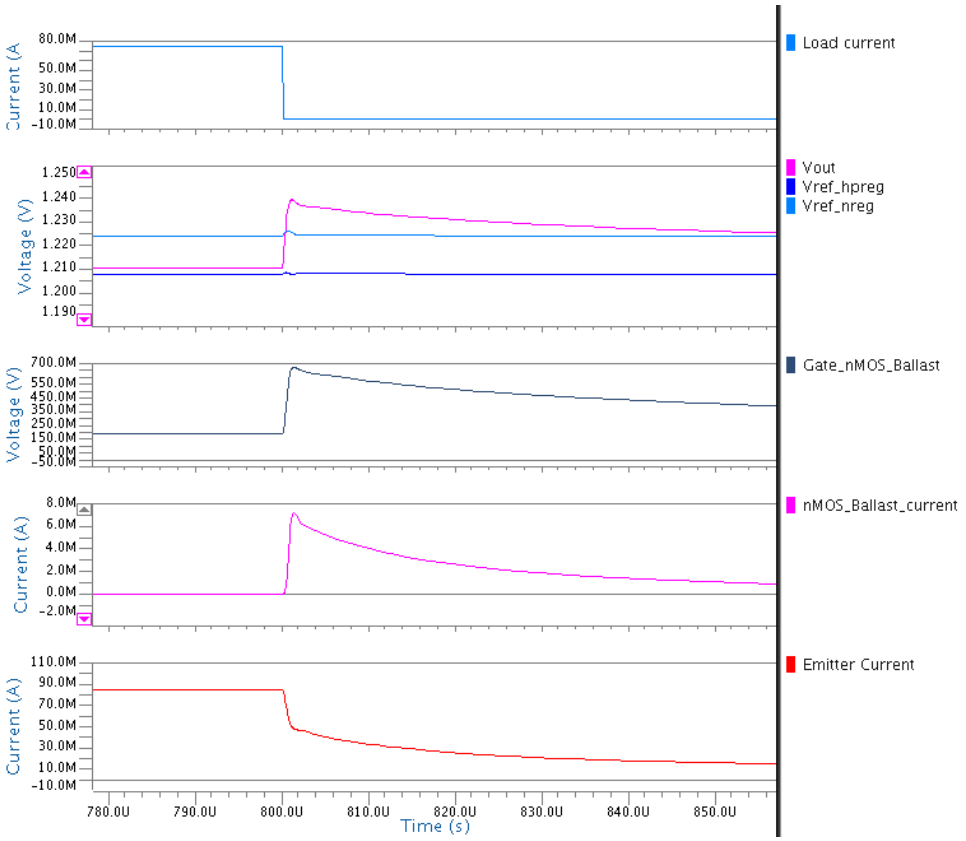

Figure 3.14: Current Transient with NREG

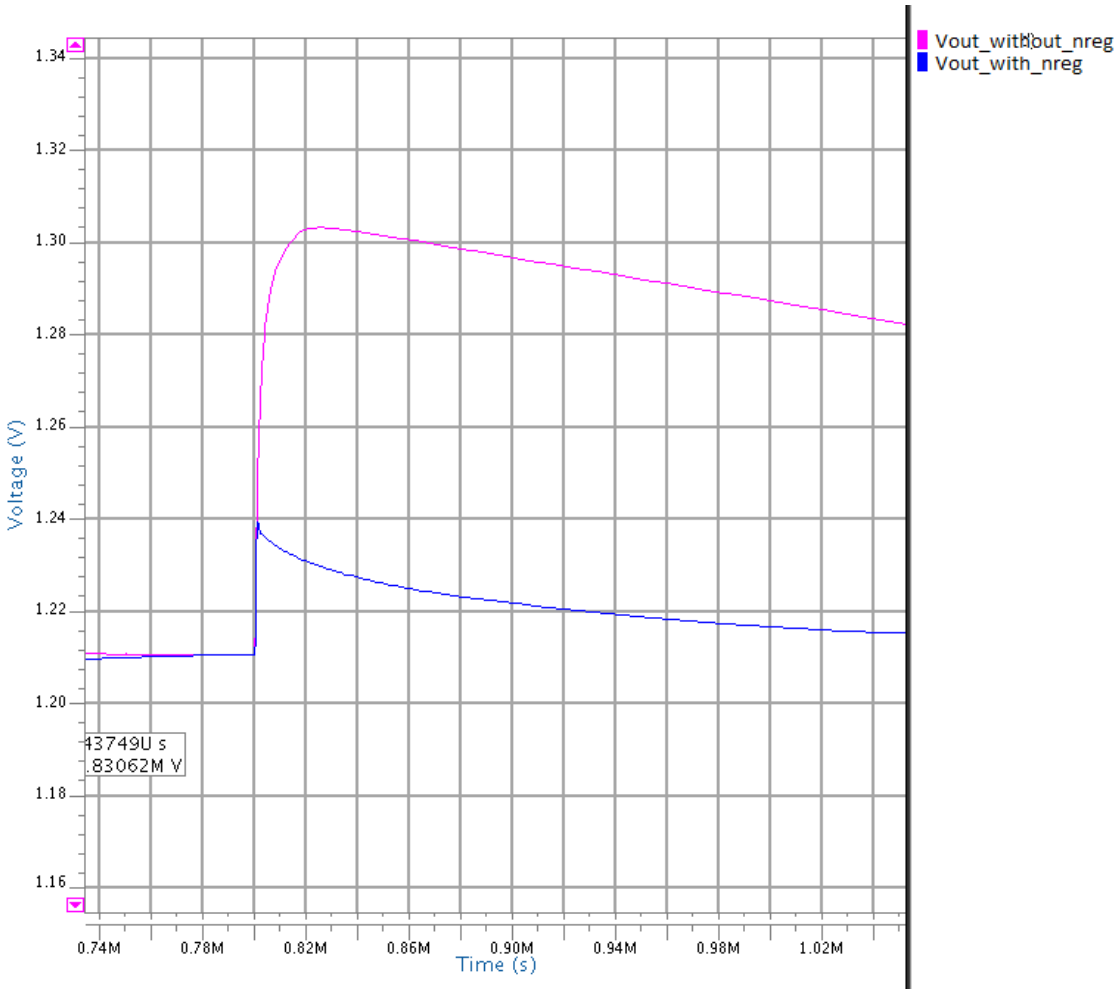

Figure 3.15: Difference in Vout with and without NREG

3.2.7 Low Power Regulator (LPREG)

Low Power Regulator is the regulator which provides the required voltage and current in stand by mode. Low Power Regulator design of PMU9 is very much similar to PMU8. In PMU8 case there was no BJT to provide the current. In main mode of PMU8 we have pMOS Ballast to provide the required current. So in Stand by mode also there is a big pMOS in the LPREG as shown in the PMU8 chapter.

Now in PMU9 case we have BJT Ballast, which can provide the required current. So here we do not require to have a big pMOS in LPREG such as in PMU8.

As shown in the figure 3.16 lpreg_compout signal generation is same as was in the PMU8 case. When lpreg_compout is high both the current mirrors will be on because of the switches shown in the figure so the final stage of the two mirrors will provide the base current to the BJT so that the BJT will provide the required current.

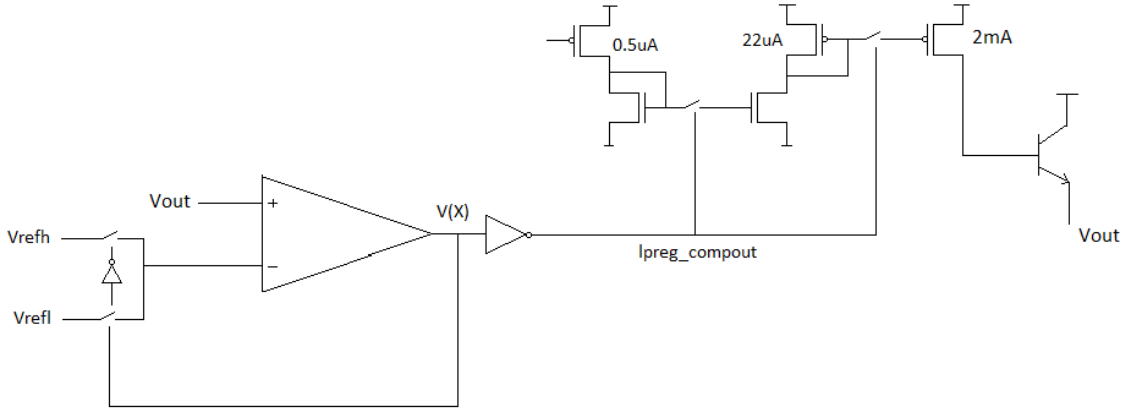

Figure 3.16: Schematic of LPREG

Chapter 4

PMU Sequencing

In this chapter different sequence of PMU like power up sequence, standby mode entry and exit sequence and bypass mode sequence. All modes are already explained in previous chapters. In this chapter only sequences are shown. All the sequences are really very important for the PMU and the sequence must be as given. So it is very imortant to verify the PMU sequence in all different cases. The result shown in this chapter is for PMU8. However the sequence for PMU8 and PMU9 are more or less same.

4.1 Power up sequence of PMU in normal mode

1. VDD_HV power up.
2. When it reaches 2 volts, signal por200b is generated from the POR block.
3. With por200b signal SoC enables all bandgap reference generators.
4. After settling of bandgap references, vbg_ready signals for each bandgap reference goes high. Vbg_reg_ready is ready signal for main bandgap of main regulator. Vbg_stby_ready is ready signal for bandgap for standby regulator and Vbg_vd_ready is ready signal for Voltage Detectors (monitors). So as shown below Voltage Detectors monitors are enabled when all this signals are on.

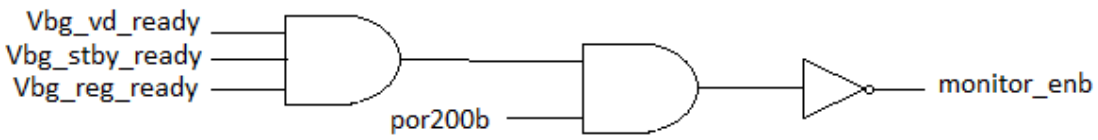

Figure 4.1: Logic to enable monitors

5. At VDD_HV = 2.9V, one VD's (VD_290) output goes high which indicates that high voltage supply reached to the level of 2.9 and now voltage regulator can be start.

6. So preg_en which is enable signal for main regulator goes high and preg will give low voltage supply VDD_LV of 1.2V.

7. At VDD_LV = 0.31V signal from the POR block por031b goes high.

8. Then different Voltage Detectors will keep monitor the level of VDD_LV.

9. At VDD_LV = 1.0V, VD_100b will be high and with this signal 1, which indicates that the low level supply reached to the sufficient level.

10. Then SoC will give trim_en = 1, so trimming of bandgap will be done and reference voltages will be corrected.

11. After trimming is done, pmu_ready signal will go high. This indicates that PMU is now ready to work.

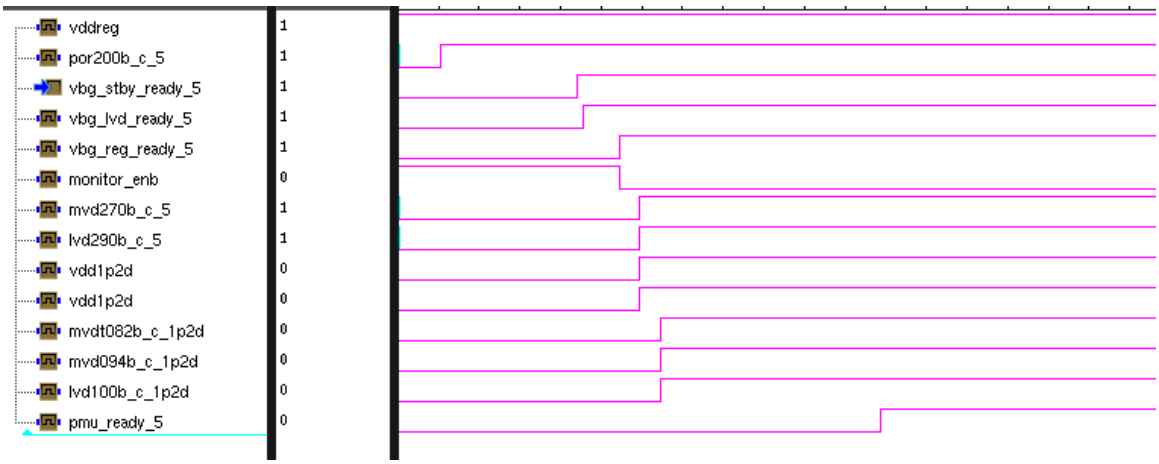

Figure 4.2: RTL simulation result for power up in Normal mode

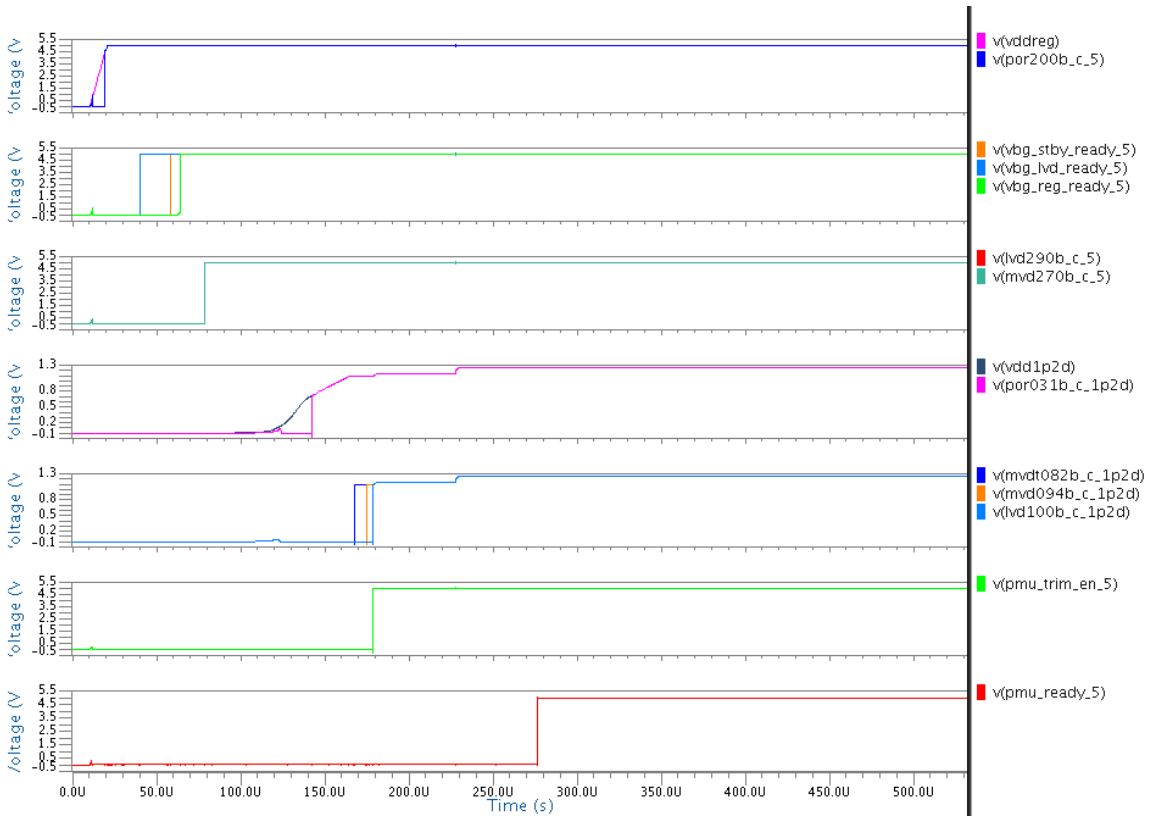

Figure 4.3: SPICE simulation result for power up in normal mode

4.2 Standby Mode sequences

4.2.1 Entry to standby mode

1. stby_mode = 1, control signal for the entry into standby mode.

2. pmu_ready = 0, which indicates main domain of PMU is OFF.

3. vreg1p2_stby_enb = 0, it is active low level enable signal for the LPREG, which is regulator for the standby domain.

4. switchoff_to_pmu = 1, signal from SoC to switch off the power switches.

5. Switchoff_from_pmu = 1, signal to SoC from PMU indicating that power switches are off now.

6. lpreg_ok = 1, means that low power regulator LPREG is ok to provide the required current.

7. vreg1p2_preg_enb = 1, after lpreg_ok is 1, SoC will off the main domain regulator.

8. hpbgap_enb = 1, after that SoC will disable the main domain bandgap reference.

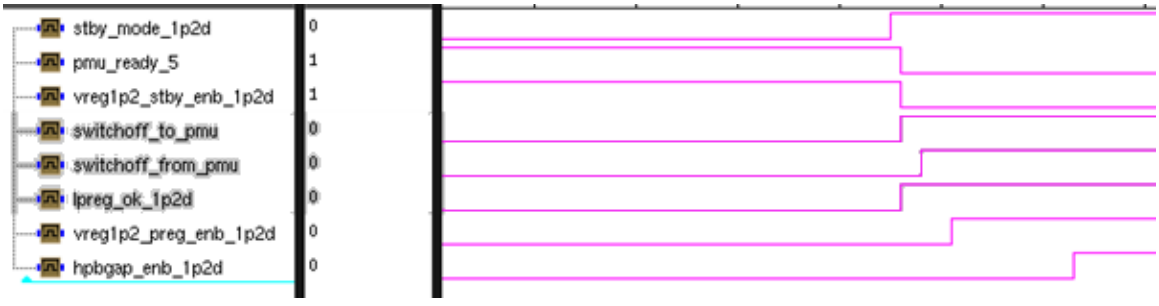

Figure 4.4: RTL simulation for the entry in standby mode

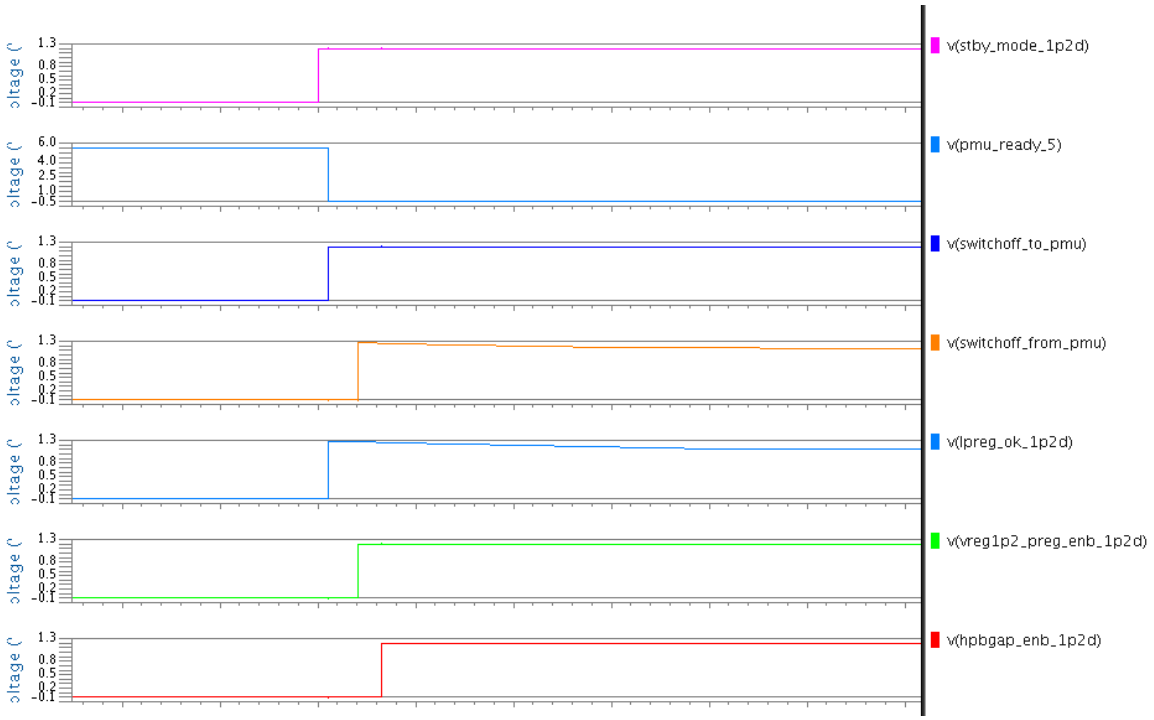

Figure 4.5: SPICE simulation for entry in standby mode

4.2.2 Exit from standby mode

1. stby_mode = 0, to exit from standby mode.

2. hpbgap_enb = 0, enables main domain bandgap reference.

3. vbg_lvd_ready, vbg_reg_ready goes to 1 from 0. vbg_stby_ready is already 1 as in standby mode bandgap reference is on.

4. vreg1p2_preg_enb = 0, then SoC will turn on the main domain regulator.

5. switchoff_to_pmu = 0, SoC will give this signal so that power switches can be closed.

6. pmu_ready = 1, which indicates that pmu is now ready to work in normal mode.

7. vreg1p2_stby_enb = 1, after entering into normal mode, SoC will turn off the standby domain regulator

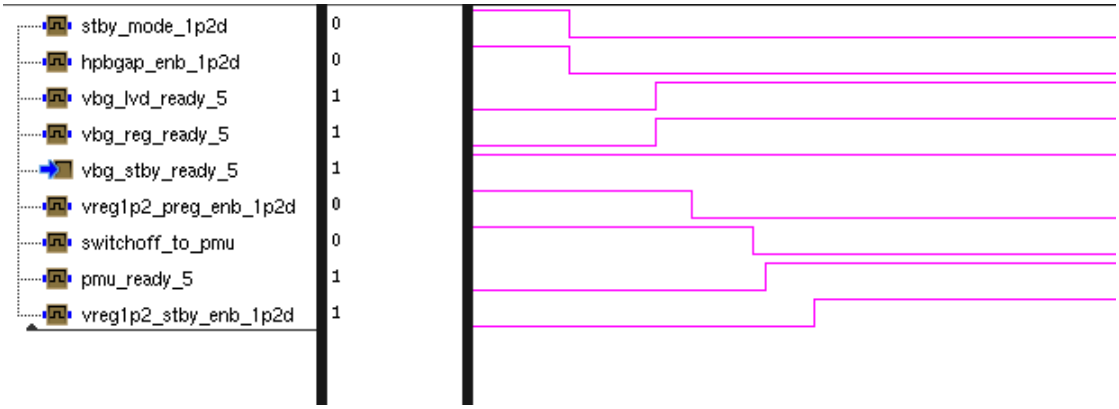

Figure 4.6: RTL simulation for exit from standby mode

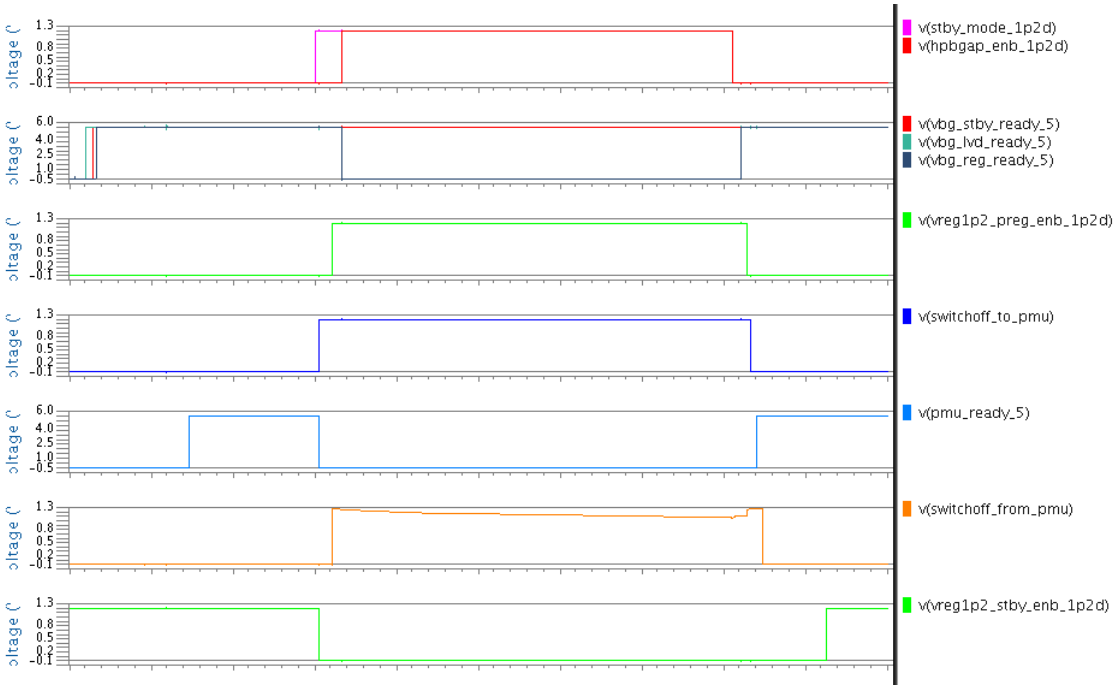

Figure 4.7: SPICE simulation for exit from standby mode

4.3 Bypass Mode

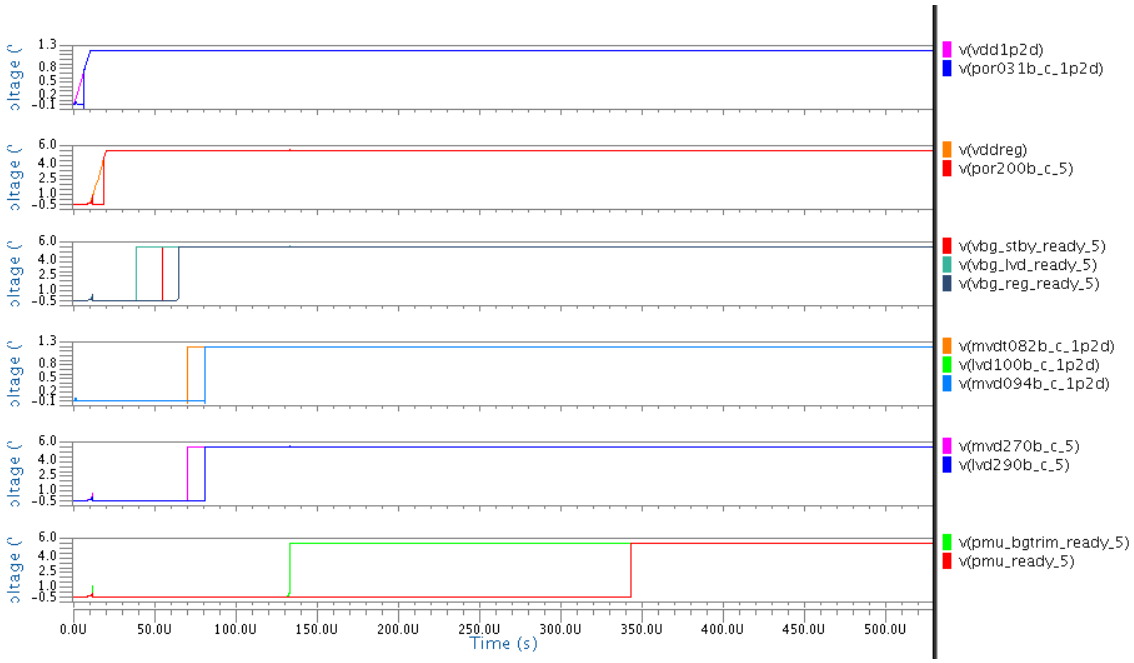

Figure 4.8: SPICE simulation for bypass mode

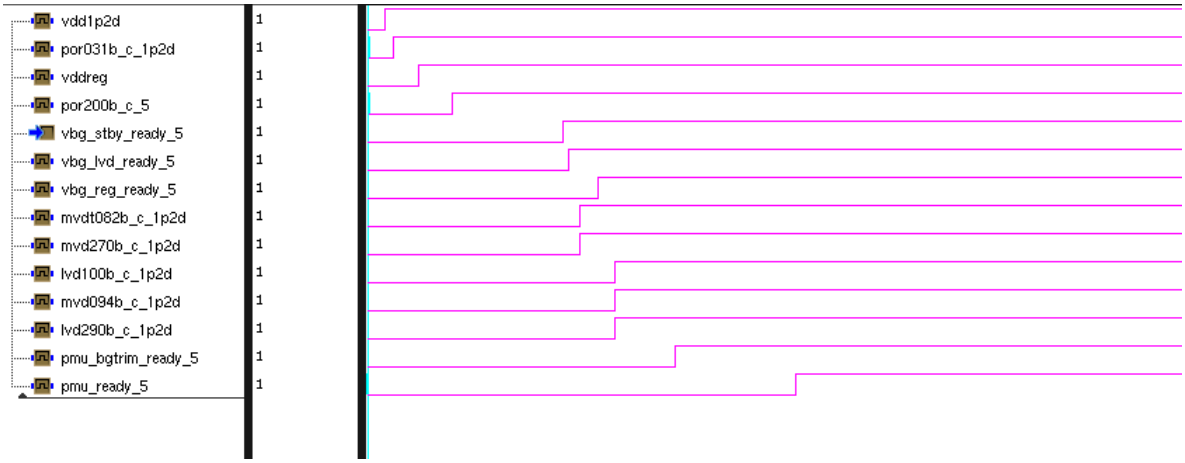

Figure 4.9: RTL simulation for bypass mode

1. vdd1p2d = 1, It is low voltage supply which is applied externally not provided by the regulator inside PMU. And it is appled before the high voltage supply.

2. por031b_c = 1, when vdd1p2d reaches 0.3V.

3. db_test = 1, it should be 1 for the Bypass mode and SoC will give this signal.

4. vddreg = 1, after that high voltage supply will be given.

5. por200b_c = 1, 1 when high voltage supply reaches 2V.

6. vbg_reg_ready, vbg_lvd_ready and vbg_stby_ready i.e. bandgap ready signals for the bandgaps, will be 1. v All monitors on.

7. Then normal sequence of normal mode is followed.

Chapter 5

Conclusion

After verifying this whole IP: Power Management Unit, I understood various features of the PMU, how it works in different modes like normal mode, test mode, bist mode, standby mode etc, what is the exact sequence of different signals of PMU in different modes. I also understood how the regulator can provide the required voltage and current. It is clear from chapter 2 and chapter 3 that how different current requirement can be satisfied with different regulators i.e. if the require load current is less only a regulator with big pMOS is adequate and if the required load current is high than a very big pMOS will be required if we want to use only pMOS. So instead to get this much high current BJT can be used which can provide high current.

And limitation of the speed of BJT can be overcome by using pMOS Ballast along with BJT as the main current provider. And nMOS Ballast is used as the current sink for the extra emitter current in case of transients.

The verification at Behavioral level is done to mainly check the sequence and connections of different blocks inside PMU. And SPICE level simulation is performed to check the sequence as well as all the different transients of load current possible in different critical PVT situations.

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