Dynamic Voltage Balancing of the Series Connected IGBTs

Major Project Report

Submitted in Partial Fulfillment of the Requirements for Degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

(**Power Electronics, Machines** & **Drives**)

By

Mandir Mansi Narendrakumar

13MEEP06

Department of Electrical Engineering

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

AHMEDABAD 382 481

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I, **Mandir Mansi Narendrakumar** Roll No. **13MEEP06**, give undertaking that the Major Project entitled **"Dynamic Voltage Balancing of the Series Connected IGBTs"** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in Power Electronics, Machines & Drives (Electrical Engineering), under Institute of Technology Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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Signature of Student

Date:

Place: Ahmedabad

Endorsed by

Industry Guide
Mr. Vinod Patel
(AGM, R&D)
Amtech Electronics(india)Ltd.
Gandhinagar.

Institute Guide
Prof. Dr. P. N. Tekwani
Department of Electrical Engineering
Institute of Technology
Nirma University
Ahmedabad.

Certificate

This is to certify that the Major Project Report entitled **"Dynamic Voltage Balancing of the Series Connected IGBTs"** submitted by **Ms. Mansi Narendrakumar Mandir (Roll No: 13MEEP06)** towards the partial fulfillment of the requirements for the award of degree in Master of Technology (Electrical Engineering)in the field of Power Electronics, Machines & Drives of Nirma University, is the record of work carried out by her, under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

Date:

Industry Guide
Mr. Vinod Patel
(AGM, R&D)
Amtech Electronics(india)Ltd.
Gandhinagar.

Institute Guide
Prof. Dr. P. N. Tekwani
Department of Electrical Engineering
Institute of Technology
Nirma University
Ahmedabad.

Head Of Department
Department of Electrical Engineering
Institute of Technology
Nirma University
Ahmedabad

Director
Institute of Technology
Nirma University
Ahmedabad

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Mandir Mansi N.

13MEEP06

Dedicated to My Family.....

Abstract

In the recent year, power electronics have increasing applications in high voltage power system which can be achieved by connecting lower rating power semiconductor devices in series connection to improve the power rating and voltage rating of power electronic converters. The main issue in series - connected insulated gate bipolar transistors (IGBTs) is the voltage balancing during dynamic and static states across each device. Voltage imbalance is mainly due to delay in gate drive signal, unequal leakage current of the device and mismatch in switching characteristics of the device. There are various methods for minimizing the voltage imbalance among the series connected devices in the string. Aim of this project is develop the voltage balancing circuit which will solve both static and dynamic voltage balance with simple structure, high reliability, low additional losses in the balancing circuit and number of devices can be easily connected in series.

Abbreviations

BJT ..... Bipolar Junction Transistor
DSP ..... Digital Signal Processor
DSC ..... Digital Signal Controllers
FACTS ..... Flexible AC Transmission System
FPGA ..... Field Programmable Gate Array
GTO ..... Gate Turn-Off Thyristor
HVDC ..... High Voltage DC Transmission System
IGBT ..... Insulated Gate Bipolar Transistor
IGCT ..... Insulated Gate Commutated Thyristor
IEE ..... Institution of Electrical Engineers
IEEE ..... Institute of Electrical and ElectronicEngineers
MOSFET ..... Metal Oxide Semiconductor Field Effect Transistor
RCD ..... Resistor, Capacitor, Diode
SCR ..... Silicon Controlled Rectifier
TVS ..... Transient Voltage Suppressors

Nomenclature

C ..... Capacitor

I_{CE} ..... Collector - Emitter current

I_L ..... Load Current

L_{Load} ..... Load Inductance

R_s ..... Series Resisitor

R ..... Static Balancing Resistor

Rg ..... Feedback Resistors

R_{Load} ..... Load Resistance

R_{off} ..... Off - state Resistor

t_f ..... Fall time

V_{CE} ..... Collector - Emitter Voltage

V_{cc} ..... DC Supply Voltage of IGBT

V_{dc} ..... DC Supply Voltage

ξ ..... Damping Ratio

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Chapter 1

Introduction

1.1 General Overview

In recent year, due to increase in the growth of power electronics in power semiconductors devices, and their application in high power modulators, control techniques, power converter circuit topologies, industrial drives and high-power traction drives, high voltage dc transmission system (HVDC) and flexible ac transmission system (FACTS). Transmission systems require a large number of switches to be connected in series which can handle high amount of power and voltage.

Generally, there are three types of method to improve the rated voltage of power electronic converter, which are employing transformers at the input and output of converter, adopting multilevel topology and applying devices in series connection. However, by employing transformers there is increase in size and cost of converter, adopting the multilevel topology with more voltage levels, the structure and controlling of converter becomes complicated. By employing series connection of power semiconductor devices which is equal to construct a device with higher voltage rating than normal device. Applying devices in series connection is the most effective, low-cost, highly reliable and direct measure to increase the rated voltage of power electronic equipment [1].

Compared to other power semiconductor devices such as silicon controlled rectifier (SCR), integrated gate commutated thyristor (IGCT) and gate turn of thyristor (GTO), insulated gate bipolar transistor (IGBT) is widely used. IGBT is a device which is a combination of metal oxide semiconductor field effect transistor (MOSFET) and bipolar junction transistor (BJT) with advantages such as high switching speed like MOSFET, less conduction loss like BJT, low driving complications etc. Therefore IGBTs are widely used in high power converters. Hence, series connection of IGBTs has been mostly used due it's following advantages:

- Higher switching frequency than other device.
- Self turn - off capability than silicon controlled rectifier (SCRs).
- Long life of switches.
- Simple driving circuit.
- Faster switching transient characteristics than GTOs.

1.2 Problem Identification

With growth of power semiconductor devices, IGBTs with higher rating of voltage have been developed which are used in high - power converters for traction drives, industrial drives etc. To obtain the higher rating of converters, numbers of IGBTs are connected in series.

The main problem for the series connected IGBTs is voltage unbalance during transient (dynamic) and static (steady) states. The operating voltage of series string of the IGBT modules is higher than individual operating voltage of IGBT modules and ideally the voltage should be shared equally in series string of the IGBT modules.

The unequal distribution of voltages in the series string of IGBT modules is mainly due to following parameters:

- Unequal leakage current of the device;
- Mismatch in the switching characteristics;
- Unequal gate drive delay signals.

Figure 1.1 shows the voltage unbalance due to parameters variation of IGBTs in the series connection and Figure 1.2 shows the voltage unbalance due to gate signals delay in which switch S represents the different positions.

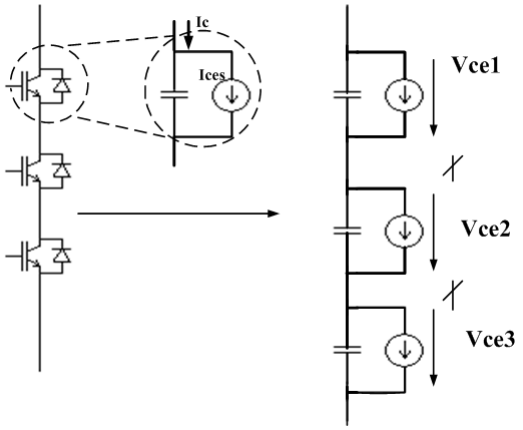

Figure 1.1: Unequal parameters of IGBTs

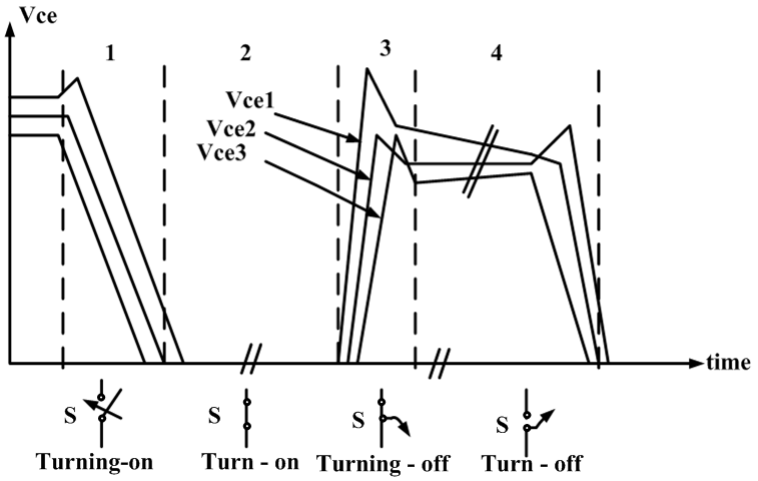

Figure 1.2: Voltage unbalance due to gating signal delay

Generally, the main problems with series connection of the IGBTs is unsynchronized timing of the gate signal, which leads to increase in the over voltage during transients (dv/dt) in different rates. Also, it reaches to unbalanced peak due to difference in the switching characteristics and its parameters. Steady - state voltage unbalance depends upon the difference in the leakage currents. This unbalance in the voltage may exceed the individual rated voltage of the device which leads to the failure of the device. As a result there is a failure of the entire series string of the IGBT modules.

1.3 Objective

The main aim of this project is to design and implement the simple active gate control circuits for series connected IGBT modules, which guarantee the safe operation and equal sharing of voltage during static and dynamic condition. Use of active gate control circuit with passive elements like resistors, capacitors and diodes has following advantages:

- Reduces the complexity of the driving circuits;
- No need of external snubber capacitors;
- Low cost;
- Compact in size ;
- It can be applicable to numbers series connected devices;
- No closed loop feedback sensing control is required.

1.4 Literature Survey

Recent growth of power electronics due to power semiconductor devices and their applications in the industrial drives, HVDC and FACTS requires series connection of the IGBTs to increase the power and voltage rating of the converter [1], [2]. Mainly there are three methods to increase the voltage of converter [1]:

- By employing transformers at input and output of converter;
- Adopting multilevel topology;
- Applying the series connection of the power semiconductor devices.

There are different types of voltage balancing topologies for series connected IGBTs which can maintained the voltage during steady and dynamic conditions. Mainly in the series connection of IGBTs, there are three types of voltage balancing circuits [2]:

- Voltage balancing by passive snubbers circuits;
- Voltage balancing by active gate control circuits;
- Voltage balancing by voltage clamping circuits.

Active gate control circuit is less used in compare with passive snubbers and active clamping, because passive snubbers can be easily implemented with less complexity. But active gate control circuit ensures voltage balancing with low switching losses of IGBTs [2].

As IGBT is the hybrid combination of MOSFET and BJT it has advantages such as high switching speed and low conduction losses. Hence IGBT is more preferred for series connection in compare to other devices. The main issues in series connection is to balance the voltage during static and dynamic condition. The voltage imbalance can be created by following parameters: [3].

- Unequal leakage currents;
- Unsynchronized gating signals;
- Due to variation in the output capacitance;
- Mismatch in the switching characteristics.

The passive snubbers circuits by using large value of snubber capacitors decreases the voltage imbalance but at the same time it increases the power losses and turn - off timings of the devices. Due to this the device is not operated at high switching frequencies. By using passive snubbers as voltage balancing circuit, the circuit become simple, it can be applicable to number of the series connected devices and the switching losses of the device is also reduced [4].

Voltage balancing through gate signal adjustments is to control the voltage imbalance during static and dynamic conditions. In this method closed loop feedback circuit is required which complicates the control circuit while the voltage balancing circuits is independent of the switching speed as all control action is done on the gate terminal [5].

The three different voltage balancing methods for series connected IGBTs with active clamping circuits on the gate side [6], [7]:

- Zener diode strings with resistor in series on the collector and gate of the device;
- Reference voltage method;
- Master-slave method.

A method with simple addition in the gate drive units for the series connected IGBTs by connecting the core with two windings between the gate drive units (GDU) and IGBTs which ensures the voltage balancing for collector - emitter (V_{ce}) [8].

A voltage clamping by zener diode which limits the V_{ce} and it also protects the circuits but at the same time it increases the power loss of the device [6], [9], [10], [12].

The voltage balancing circuit using active gate control circuit with passive elements which can balance the voltage during steady - state and dynamic state as it has following advantages: [11], [14].

- Less complexity in the control circuit;
- Automatic voltage balancing without closed loop control;
- No special gate drive units are required;
- Minimum losses in the control circuits.

Active voltage clamping using feedback loop with transient voltage suppressors (TVS) between collector and gate operates the IGBT in the linear region during turn - off transients which protects the device [15]. For series connection of IGBTs the overvoltage can be controlled by using a active gate circuit which amplifies the gate signals to reduce the switching transient and losses. This can be achieved by using closed loop control [16].

The optimum number of IGBTs connected in series string mainly depends on power loss along with reliability, switching frequency, cost, maintenance of device and voltage balancing circuit [17]. Comparative analysis has been carried out between series connected IGBTs and single high voltage - rated IGBT module in which series connected IGBTs have faster turn - on and turn - off timings then single IGBT module having high - voltage rating [18].

Voltage balancing during dynamic state of series connected IGBTs can be obtained using voltage clamping with slope regulation by adjusting its miller capacitance and gate current [19].

Voltage balancing circuits is designed with digital signal processor (DSP) and field programmable gate array (FPGA) for series connected IGBT [20]. Voltage balancing circuit using auxiliary clamp circuit made from passive (LC) for series connected IGBT with less complexity in driver circuit, low losses and high reliability [21].

Chapter 2

Voltage Balancing Topologies

2.1 Introduction

Presently, power electronics plays a very important role in the industry due to the availability of high power handling devices. The high rating of switch can be obtained by connecting the devices in series connection to attain the high power rating of the converters [2].

The main issue in series connected IGBTs is to equally distribute the blocking voltage across each switch connected in series string during static and dynamic state.

The series connection of IGBTs (self turn - off device) is not easy due to following reasons:

- Unequal leakage current of the device;
- Unequal switching characteristics;
- Due to variation in the output capacitance;
- Unequal gate drive delay signals.

There are various methods to minimize, voltage imbalance in series string of IGBTs, which can be classified into three main types:

1. Passive snubber circuits
2. Active gate control circuits
3. Voltage clamping circuits

The different types voltage balancing topologies available for series connected IGBTs is shown in the Figure 2.1.

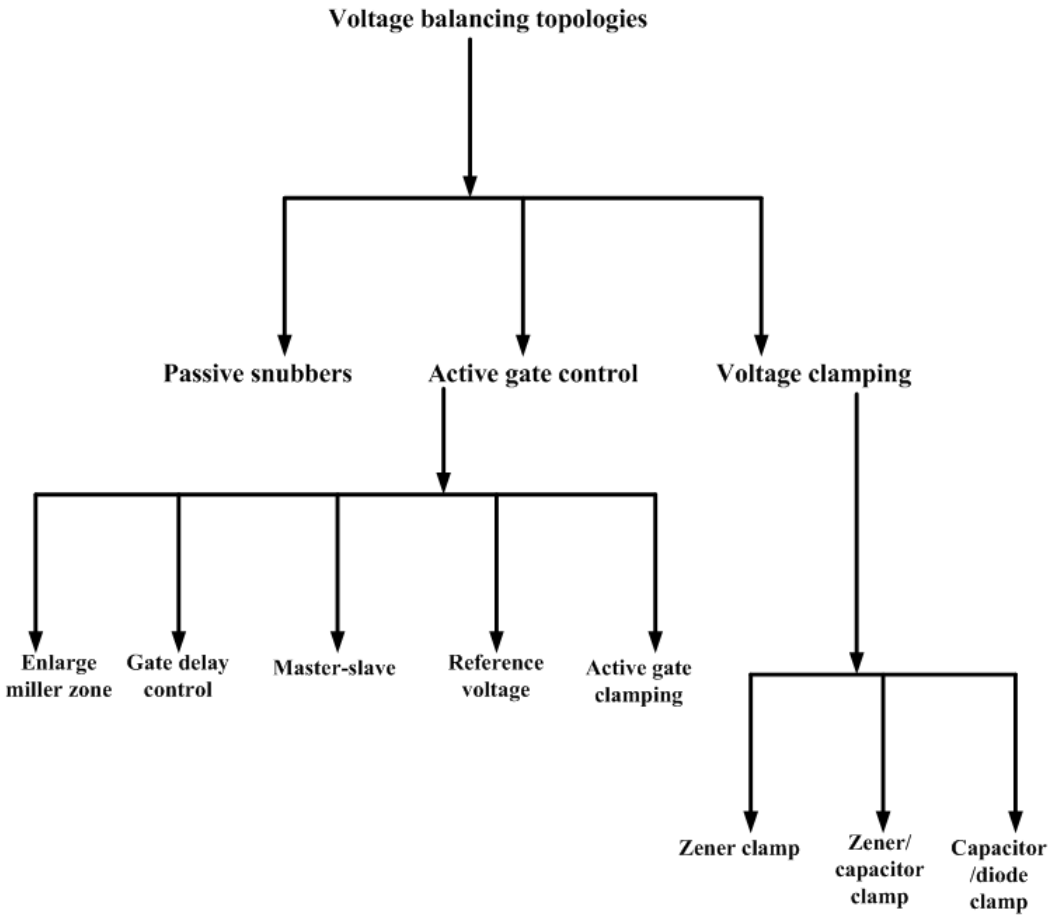

Figure 2.1: Voltage balancing topologies for series connected IGBTs

2.2 Voltage Balancing by Passive Snubber

The passive snubber is mostly used topology for series connection of IGBTs. A series resistor (R_s) is connected in parallel with IGBTs for static condition and resistor, capacitor and diode (RCD) or resistor, capacitor (RC) circuit is used in parallel with series resistors for dynamic condition.

The passive RCD snubber circuit is shown in Figure 2.2. The use of snubber capac-

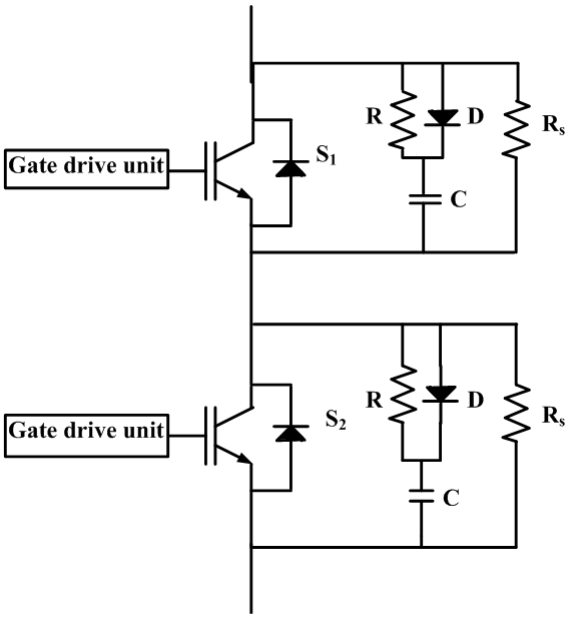

Figure 2.2: Voltage balancing by passive snubber

itors reduces the voltage imbalance but increases both turn - off time of the IGBT and power loss in the snubber circuit. It reduces switching losses of IGBT but the components used are too large in size to handle high currents and high voltages and therefore they are costly and bulky, it can be used in robust applications. The operating frequency used for snubber circuits is to kept quite low as it slows down the switching characteristics of the IGBT [4].

2.3 Voltage Balancing by Active Gate Control Methods

2.3.1 Voltage Balance by Enlarging Miller Effect Zone

In this method, a precharged capacitor is inserted to switch off the fastest device by applying a positive gate pulse. During dynamic condition, the timing of inserting capacitor and size of precharged capacitor is very important to achieve voltage balancing. Additional feedback circuit is required to sense the miller effect zone and to take comparative action across each device.
Main advantage of this method is that passive components are not used. However static balance can be achieved by connecting a series resistors in parallel with each IGBT.

2.3.2 Voltage Balance by Gate Signal Delay

In this method, voltage imbalance can be controlled by adjusting gate signal to control the steady and dynamic state. The difference in the gating signal creates a voltage imbalance in series connected IGBTs, to avoid this the gate signals are adjusted. To obtain voltage balancing during static and dynamic states individual voltage balancing controllers are used, which delays gate signals according to the level of voltage imbalance occurs. During dynamic state this method uses closed loop feedback, hence the drawbacks of above methods is nullified [5].
Gate delay control before adjusting and after adjusting in series connection is shown in Figure 2.3

2.3.3 Voltage Balance by Master - slave

In this method master device is kept as reference and the voltage between collector - emitter of the slave devices are controlled by referring to the voltage of the master device. The power losses and switching time are not increased as they are switched with timings of the master device.

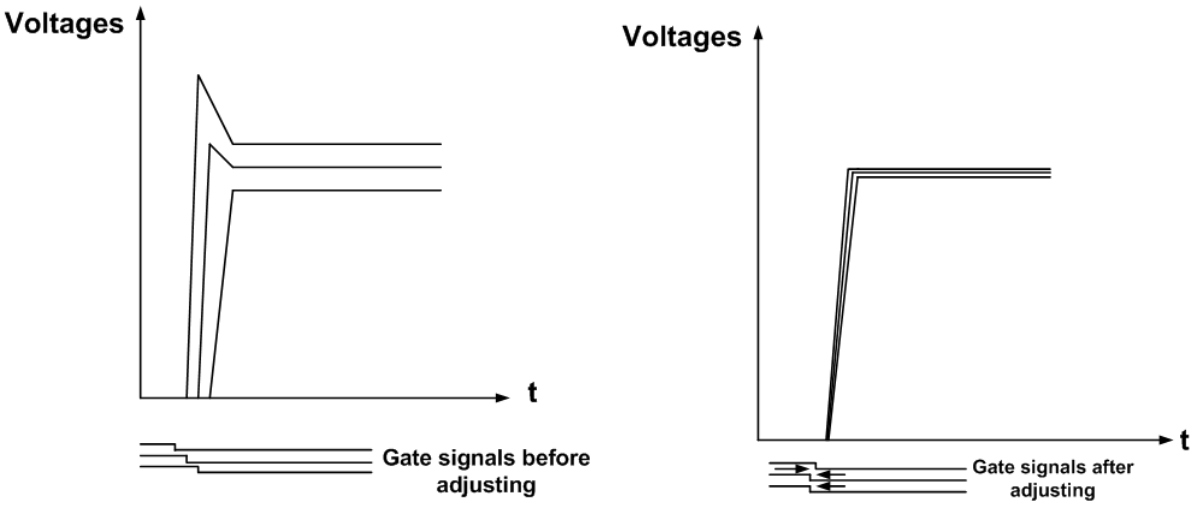

Figure 2.3: (a) Gate signals before adjusting, (b) Gate signals after adjusting

By this method, the voltage sensing circuits become complex and costly due to this it is only applicable to the limited number of series connected IGBTs. The control circuit of voltage error should be sensitive to detect minimum imbalance in voltage and should have fast reaction time. Voltage imbalance during the static condition can be controlled by connecting a series resistors in parallel with each IGBT [6], [7].

2.3.4 Voltage Balance by Reference Voltage Method

In this method, the common reference voltage slope is set during the transient state. High speed control circuits are required for each devices in series connection as device voltage has to track the reference voltage. The complexity in voltage sensing and control circuit is reduced as voltage of the device is not compared with each other. In this technique high operational amplifiers are used hence it increases the complexity of the gate driver circuit. The power loss of devices depends on rate of rise in the reference voltage. The static condition can be controlled by connecting a series resistors in parallel with each IGBT [6], [7].

2.3.5 Voltage balance by Active Gate Control using Resistor, Capacitor and Diode

A simple new voltage balancing circuit with passive elements along with active gate control is developed. R_1 and R_2 are used for static voltage balancing and C_1, C_2, D_1 and R_g are used for dynamic voltage balancing. The increase in C_2 voltage gives an effect of active gate controlling action on the IGBT. IGBTs in series connection shows oscillations in the voltages due to resonance between capacitances and stray inductance of the circuit. The switching losses and voltage balancing depends on value of capacitor in the auxiliary circuit [3], [14].

Active gate control circuit is shown in Figure 2.4.

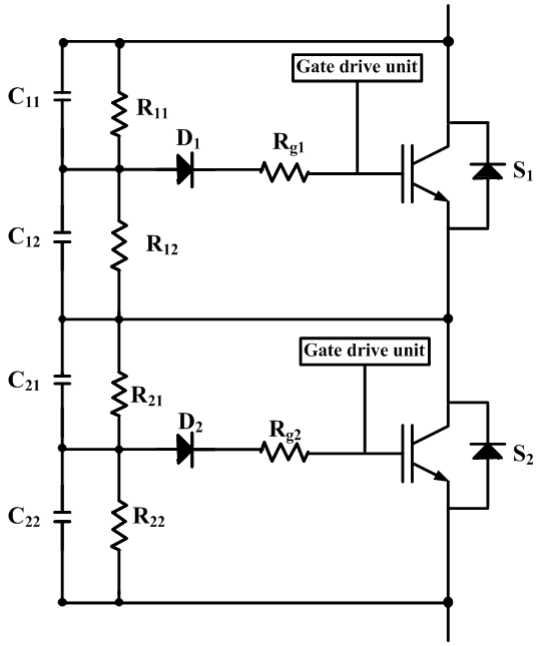

Figure 2.4: Voltage balance by active gate control

2.3.6 Voltage Balance by Gate Balancing Core

By this method, the disadvantages of active gate control circuits and snubber circuits are overcome. In this method gate wires of IGBTs connected in series are magnetically combined with cores. Gate balancing core is coupled with each gate drive unit which

provides a gate current whenever the delay is obtained in the switching signals. Since each gate circuit contain two balancing cores, which makes gate side circuitry complex and bulkier and the static condition can be controlled by connecting a series resistors in parallel with each IGBT [8].

Circuit structure for gate balancing core is shown in Figure 2.5.

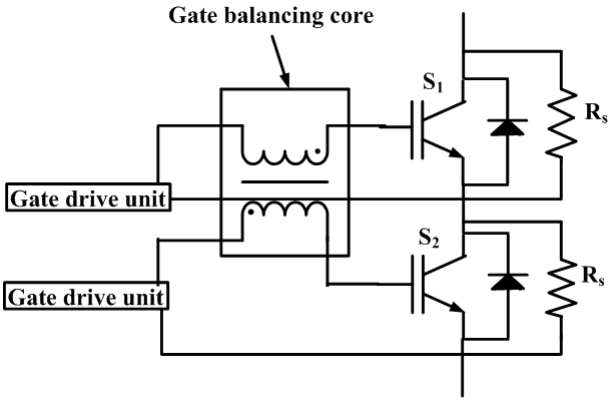

Figure 2.5: Voltage balancing by gate balancing core

2.4 Voltage Clamping Method

2.4.1 Voltage Clamping by Zener Diode

In this method, the zener diodes and protection circuits are used to clamp the over voltage of the IGBTs. In the active region, device has more power losses as the first device has to clamp both the higher voltage and current until other the devices are switched off, hence efficiency is reduced. This method has an advantage that it does not require a complex circuits.

2.4.2 Voltage Clamping by Zener Diodes and Capacitors

This method is the improvement of the previous method by adding capacitor and resistors in clamping circuit. The capacitor slows down the fastest IGBT to switch off state and when it reaches the zener diode breakdown voltage the IGBT voltage is

clamped [13].

Voltage clamping by zener diodes and capacitors circuit is shown in Figure 2.6.

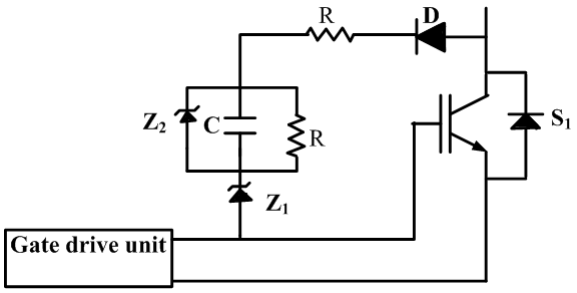

Figure 2.6: Voltage clamping by zener diodes and capacitors

2.4.3 Voltage Clamping by Diodes and Capacitors

In this method, clamping circuit made up of C_1, D_1 and C_2, D_2. In this method the excess energy is transferred to an external load which is stored in clamping capacitors. As the circuit contains some reactive components, hence the circuit becomes bulkier, costly and it also increase the commutation time of the device [9].The static condition can be controlled by connecting a series resistors in parallel with each IGBT. Voltage clamping by capacitors and diodes is shown in Figure 2.7.

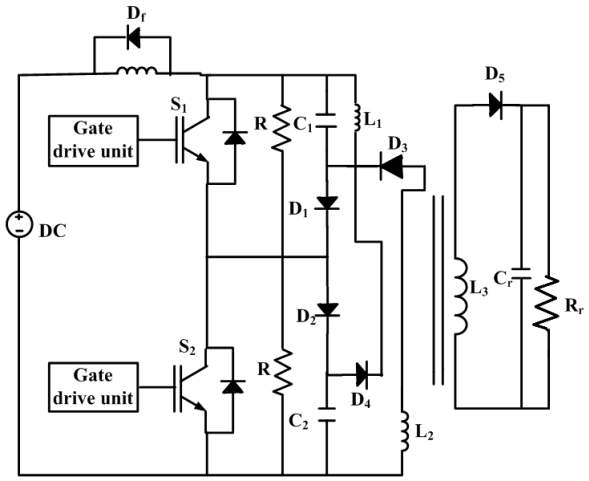

Figure 2.7: Voltage clamping by diodes and capacitors

2.5 Comparative Analysis of Voltage Balancing Topologies for Series Connected IGBTs

Comparison of voltage balancing topologies for series connected IGBTs is shown in Table I [2].

Table I: Comparison Table

Voltage balancing topologies	Loss in voltage balancing circuit	Complexity in voltage balancing circuit
Passive snubbers	High	Less
Voltage balancing by enlarging miller effect zone	Low	More
Gating signal delay	Low	More
Master-slave	Low	More
Reference voltage method	Low	More
Active gate control by (RCD)	Low	Less
Gate balancing core	Low	More
Zener diode clamping	Low	More
Voltage clamping by zener diodes and capacitor	Moderate	Less
Voltage clamping by capacitors and diodes	Moderate	More

Chapter 3

Adopted Topology

3.1 Introduction

With growth of power semiconductor devices, IGBTs with higher rating of voltage have been developed which is used in high - power converters for traction drives, industrial drives etc. To obtain the higher rating of converters numbers of IGBTs are connected in series.

The main problem for the series connection of IGBTs (self turn - off devices) is the voltage unbalance during transient (dynamic) and static (steady) states. The static balancing can be obtained by connecting a balancing resistor in parallel with each IGBT. The dynamic voltage balancing can be achieved by two methods:

1. Gate side balancing
2. Load side balancing

On gate side an active clamping is used while on load side clamp circuits or snubber circuits are used. By using snubber circuits loss is increased as it is proportional to switching frequency and value of snubber capacitors increases with increase in rating of switch. When gate signals are unsynchronized, the snubber circuits are not able to achieve voltage balance during transients states. However by using active gate control each voltage of devices has to be detected and fedback to active control circuit which causes the complexity of the driving circuit and reduces reliability of

the circuit, due to this it is only applicable to limited number of devices connected in series. A topology of active gate control by using resistors, capacitors and diode (RCD), which solves both static and dynamic voltage imbalance, is already proposed in [3]. The same topology is analyzed, used and implemented in this project for series connection of IGBTs. It consists of the three resistors, two capacitors and a diode which is attached to each device. Compared to other active control method, this method has simple structure as no external snubber capacitor are needed and high reliability, low additional losses and number of devices can be easily connected in series [3], [14].

The active gate control with RCD is shown in Figure 3.1

3.2 Features of the Adopted Topology

- **Automatic voltage balancing:**

  By this topology, the static balancing of voltage can be achieved by connecting a series resistors in parallel with each IGBT. The dynamic balancing of voltage can be achieved automatically by auxiliary circuit in which diode (D) and resistors (Rg) provides a feedback for the switch voltage which will again turn on the switch and this will limit the switch voltage to the normal value of the voltage. This action is similar to active voltage clamping. Hence the dynamic conditions can be achieved automatically without any special gate drive nor any additional control circuit. [3], [14].

- **Simple structure and low loss:**

  Auxiliary circuit consists of the all the passive elements which are of the small ratings then ratings of switch (IGBT), hence the loss in the auxiliary circuit is very low which make this circuit more efficient, economic solution and very reliable. In this topology any other control circuit or special gate drive circuit is not required and due to this features it can be applicable to number of series connected IGBTs [3], [14].

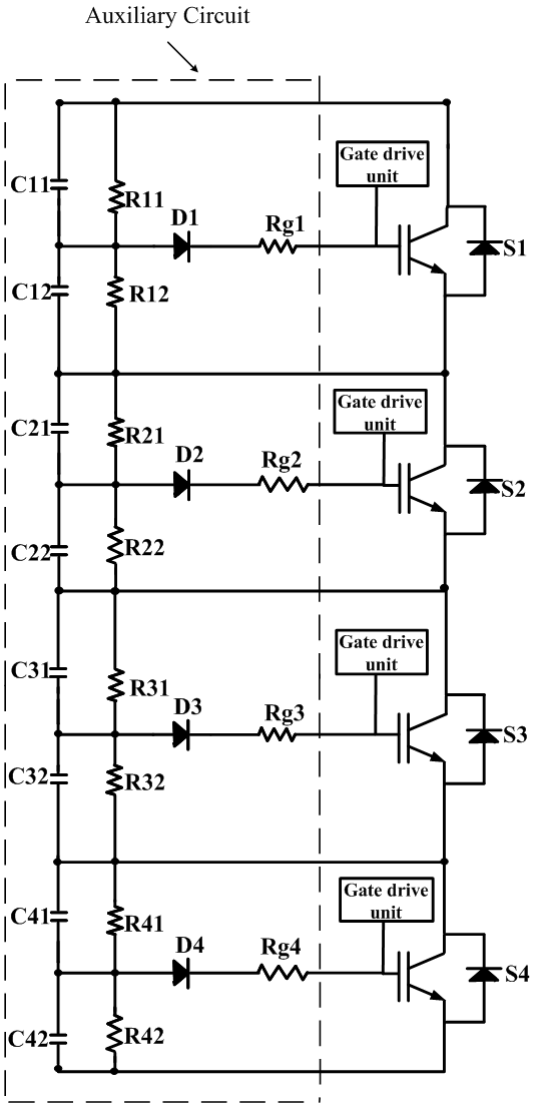

Figure 3.1: Active gate control

3.3 Operation Principle

Due to the difference in the delay time in the gate driving circuit, leakage currents, difference in capacitance can cause a over voltage of IGBT. This problem can be solved if the V_{ge} is controlled in the inverse proportion of the over voltage. Figure 3.2 shows the voltage difference of the IGBTs due to delay in the gate driving circuits.

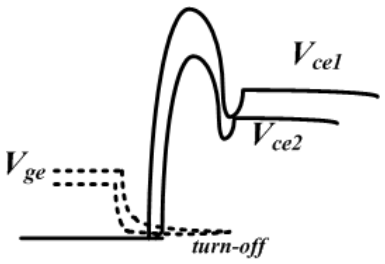

Figure 3.2: Gate voltage IGBT voltage waveform during transients

3.4 Modes of Operation

Modes of operation of series connected IGBTs are described during switching transients. Figure 3.3 shows operational waveform of active gate control for 4 IGBTs connected in series.

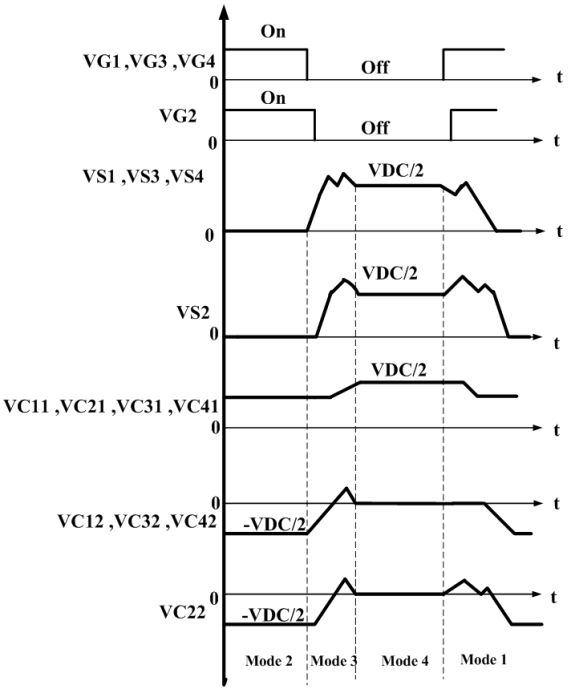

Figure 3.3: Operational waveform

IGBT $S2$ is delayed with respect to IGBTs $S1$, $S3$ and $S4$ (i.e IGBT $S2$ will turn on later compare to IGBTs $S1$, $S3$ and $S4$). Hence over voltage is applied across IGBT $S2$.

- **MODE 1 (Turning - on transients):**

  Figure 3.4 shows operation during turning on transients when gate signal is just applied to IGBTs, Figure 3.5 shows operation during turn on transients.

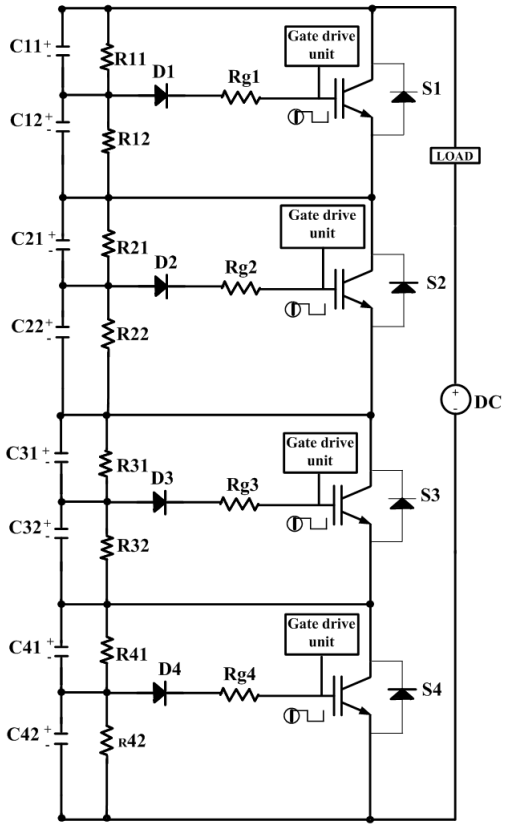

Figure 3.4: Operation during turning - on transients

During turn - on transients as IGBT $S2$ turns on little bit late then IGBTs $S1$, $S3$ and $S4$ hence overvoltage is applied across the IGBT $S2$ as IGBTs $S1$, $S3$ and $S4$ starts to turn on. The capacitor $C22$ will charge from zero to positive to reduce the overvoltage stress across IGBT $S2$ when IGBT voltage is higher then $C21$. The capacitor $C21$ is higher in the value then $C22$ so this voltage is applied across the gate terminal of IGBT $S2$ through $D2$ and $Rg2$ which will turn on the IGBT $S2$ slightly hence overvoltage across it is reduced significantly and the capacitor $C22$ discharges to turn it off again. At the end of mode1, voltage of IGBTs $S1$, $S3$, $S4$ and IGBT $S2$ reaches to zero and dynamic voltage balancing during turn - on is achieved.

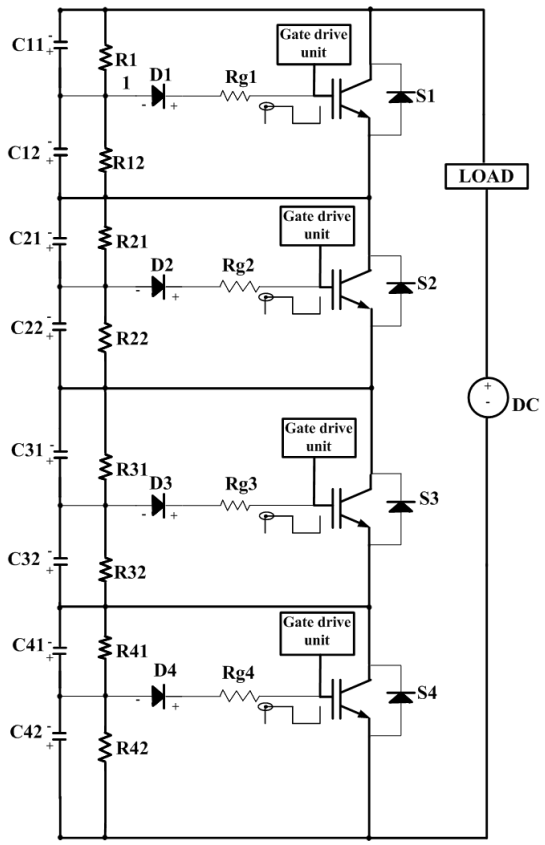

Figure 3.5: Operation during turn - on transients

- **MODE 2 (All switches are turned on):**

  Figure 3.6 shows operation when all switches are turn on

  When all IGBTs $S1$, $S2$, $S3$ and $S4$ are turned - on as gate voltage is high the capacitor $C11$, $C21$, $C31$, and capacitor $C41$ will discharge through IGBTs and charges the capacitor $C12$, $C22$, $C32$, and capacitor $C42$ with reverse voltage polarity and small discharging voltage through resistors $R11$, $R21$, $R31$ and $R41$ and diodes $D1$, $D2$, $D3$ and $D4$ blocks the reverse voltage. When all IGBTs are on the voltage ratio across capacitors will be maintained with respect to capacitance ratio at all time in this mode.

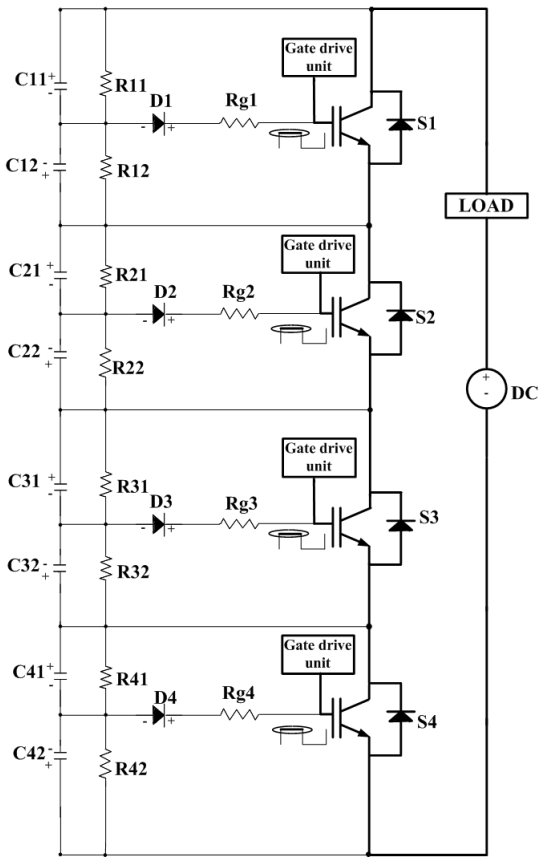

Figure 3.6: Operation during all switches are turn on

- **MODE 3 (Turning - off transients):**

  Figure 3.7 shows the operation during turning - off transients.

  During turning - off transients IGBTs $S1$, $S3$ and $S4$ will turn off little bit earlier then IGBT $S2$ as it has started earlier hence overvoltage is applied across IGBTs $S1$, $S3$ and $S4$. The voltage of the capacitor $C12$, $C22$, $C32$ and capacitor $C42$ will change from negative to zero and an additional signal is generated through $Rg1$, $Rg2$, $Rg3$ and $Rg4$. Hence the overvoltage is clamped to a reference value. Thus dynamic voltage balancing is achieved during turning - off transients.

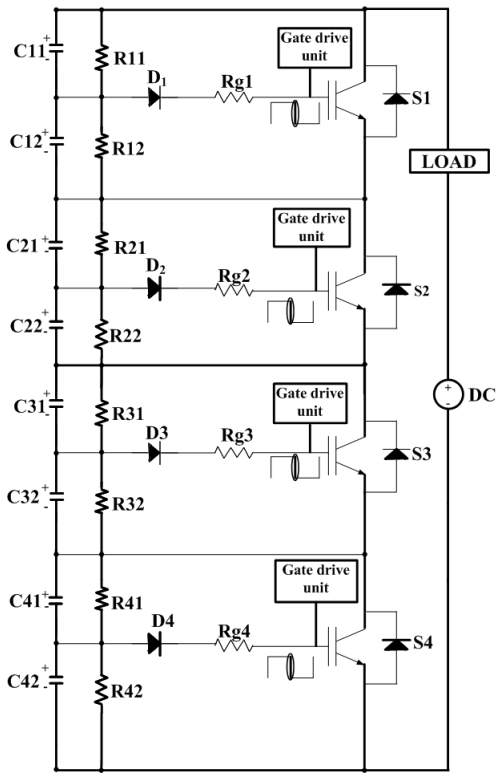

Figure 3.7: Operation during turning - off transients

- **MODE 4 (All switches are turned off):**

  Figure 3.8 show the operation when all the switches are turned off

  When all IGBTs $S1$, $S2$, $S3$ and $S4$ are turned - off gate signal is low. The switch current reaches to zero and load current will freewheel through load diode when inductive load is connected. At end of this mode the static balancing of voltage is achieved through resistors.

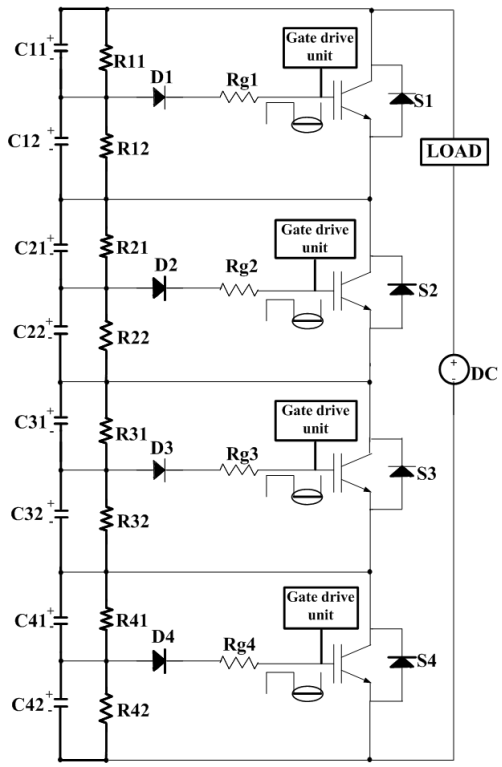

Figure 3.8: Operation during all switches are turned off

The voltage balancing of series connected IGBTs can be obtained by auxiliary circuit with active gate control during dynamic and steady states. Static balancing resistors (R) connected in parallel across each IGBTs to achieve the voltage balancing during steady state. Capacitors (C), diodes (D) and feedback resistors (Rg) are used to obtained dynamic voltage balancing.

The value of capacitors (C), static balancing resistors (R) and feedback resistors (Rg) is derived in the next chapter.

Chapter 4

Design Parameters of Adopted Topology

4.1 Design Criteria for Capacitors

Load current decreases linearly during turn-off transients of IGBTs.

Figure 4.1 shows the waveform of capacitor voltage and load current during turn - off.

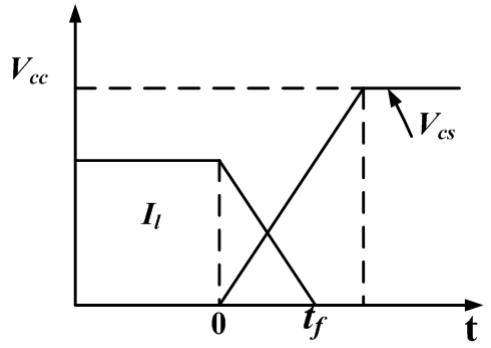

Figure 4.1: Capacitor voltage and load current during turn - off

The voltage of capacitor is designed with V_{cc} at t=t_f

$$V_{cc} = \frac{(I_L t_f)}{2 \times C} \tag{4.1}$$

hence minimum value of C can be obtained from equation 4.1

$$C > \frac{(I_L t_f)}{2 \times V_{cc}} \tag{4.2}$$

Damping ratio ξ is to be small to avoid large voltage peaks, where ξ cannot be so small otherwise it will damage device due to large surges. Damping ratio should not be larger then unity as it decreases switching times which will increase the time to obtain a stable situation. Hence ξ should be chosen less than unity [4].

$$\xi = \frac{R_{load}}{2}\sqrt{\frac{C}{L_{load}}} < 1 \tag{4.3}$$

Maximum value of C can be obtained by rearranging the equation 4.3

$$C < \frac{4L_{load}}{R_{load}^2} \tag{4.4}$$

Hence, the value of C can be obtained by combining equation 4.2 and equation 4.4

$$\frac{I_L t_f}{2V_{cc}} < C < \frac{4L_{load}}{R_{load}^2} \tag{4.5}$$

The capacitors value $C11$ should be greater than $C12$ as $C11$ should remain constant during small transition time and the voltage across $C11$ is considered as the reference voltage. In each switching interval there will be a charging and discharging of $C12$ as it has to generate an additional signal. When it charges from zero to positive a signal is generated to turn on switch at which overvoltage is occurred. If the value of $C12$ is chosen high it will create an impact on current during turn - on as a result the turn - off time will be longer and if the value of $C12$ is chosen too low it will create oscillations during turn - off time [4], [14]. Hence generally 10% of $C11$ is enough for $C12$.

4.2 Design Criteria for Resistors

For static balancing voltage - dividing resistors $R11$, $R12$ are used which are connected parallel across each IGBT. If dividing resistors $R11$, $R12$ are too small, the static balancing will be achieved as it will help to detect the overvoltage across IGBT by decreasing the voltage of $C11$ but losses would increase. If dividing resistors $R11$, $R12$ are too big, static balancing will not be achieved.

Generally, value of voltage dividing resistor $R11$, $R12$ is designed by $R11/\ R12 = 10$. The current to the IGBT is provided by feedback resistor Rg during transients and which reduces dynamic oscillations. If the of value feedback resistor Rg is too small, then it will increase the turn - off time of IGBT and if it is too big the feedback will not be provided [3], [14].

The fast recovery diode should be selected whose reverse - blocking voltage should be high. Diode separates the auxiliary circuit and gate terminal of IGBT during steady - state.

Chapter 5

Simulation Studies

5.1 Dynamic Voltage Balancing of Four Series Connected IGBTs

DC supply voltage source is generated by three - phase uncontrolled rectifier and its output is fed to capacitor bank to obtain pure DC voltage. Generated DC voltage is given to series link of IGBT modules with its auxiliary circuit. Gate signals for IGBT modules are generated by control card which generates the four gating signals where, three gating signals are same and one gating signal is delayed. Figure 5.1 shows the block diagram of series connected IGBTs.

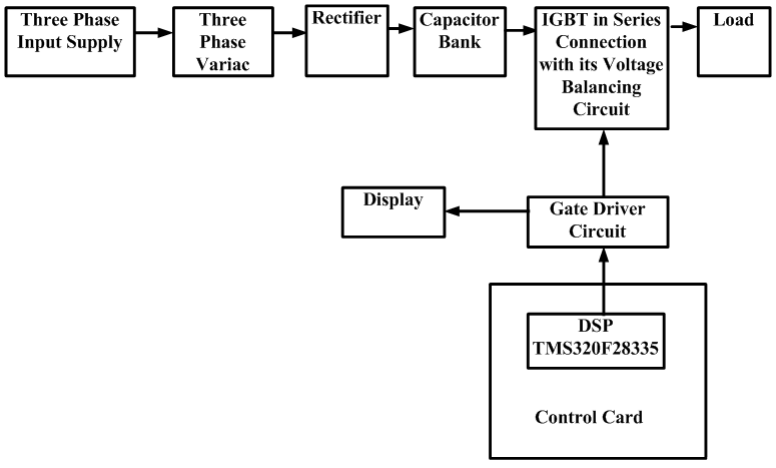

Figure 5.1: Block diagram of series connected IGBTs

5.2 Simulation Studies for 250V

Computer simulation is done in PSpice for dynamic voltage balancing of series connected IGBTs.

Simulation model for 250V is created with following specification is shown in Table I.

Table I: Specification of Simulation Model for 250 V

Parameters	**Value**
Supply DC Voltage V_{dc}	250 V
Load Current I_L	22.26 A
Switching Frequency	5 Khz
Delay time	300 ns
Load Resistor R_{Load}	11 Ω
Capacitor ($C11$, $C21$, $C31$, $C41$)	300 nF
Capacitor ($C12$, $C22$, $C32$, $C42$)	30 nF
Resistor ($R11$, $R21$, $R31$, $R41$)	3 kΩ
Resistor ($R12$, $R22$, $R32$,$R42$)	0.3 kΩ
Feedback Resistor ($Rg1$, $Rg2$, $Rg3$, $Rg4$)	56 Ω

Figure 5.2 shows the gating signals with same signals for switches $S1$, $S3$, $S4$ and gating signal for $S2$ is delayed by 300 nsec during turn - on time.

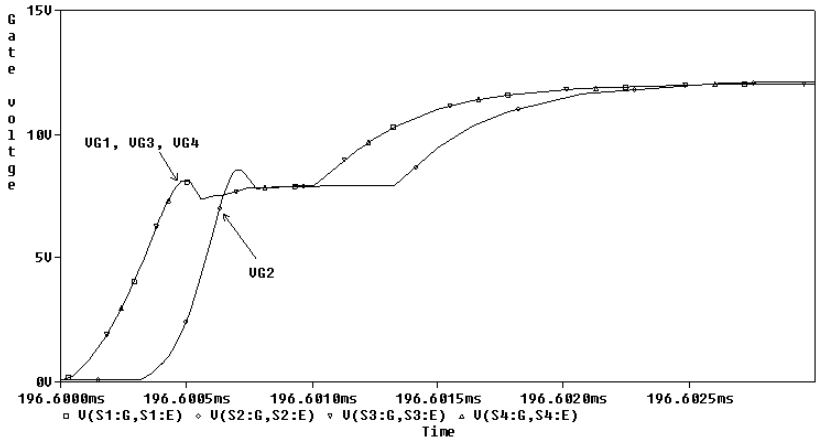

Figure 5.2: Gating signals with delay during turning - on time
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 5 V]

Figure 5.3 shows the simulated waveforms voltage across switches during turn - on,

where switch $S2$ is delayed by 300 nsec then $S1$, $S3$ and $S4$. Hence the overvoltage is obtained across $S2$. The voltage of capacitor $C22$ will charge from zero to positive, this voltage of capacitor $C22$ is applied across gate terminal of switch $S2$ through $D2$, $Rg2$ which will turn - on switch $S2$ slightly and overvoltage during turn - on time is reduced. In this way voltage balanced is achieved during turn - on time. Figure

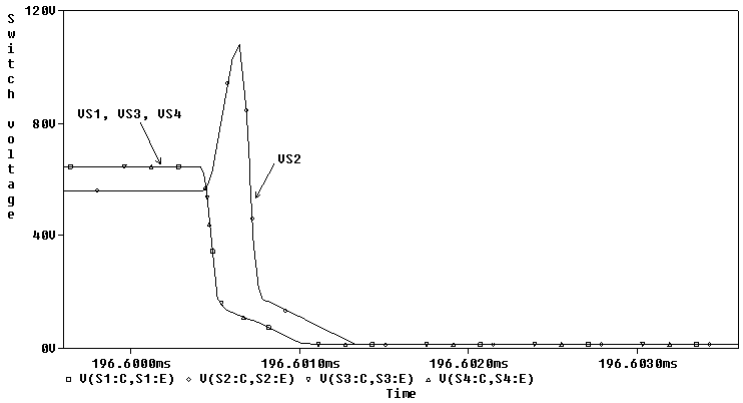

Figure 5.3: Switch voltages during turning - on time
[X-axis: 1 div: 1m sec, Y-axis: 1 div: 40 V]

5.4 shows capacitor voltage of $C12$, $C22$, $C32$ and $C42$ during turn - on time. The overvoltage across $S2$ charges capacitor $C22$ to clamp the overvoltage by providing an additional signal to turn on $S2$ again.

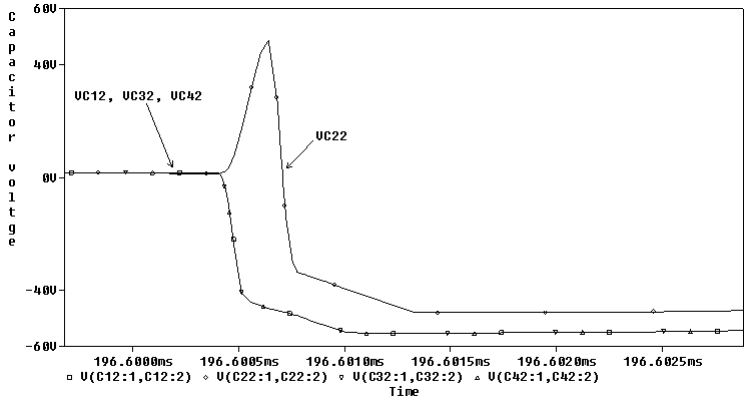

Figure 5.4: Capacitor voltages during turning - on time
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 40 V]

Figure 5.5 shows the gating signals for switches $S1$, $S2$, $S3$ and $S4$ during steady on state. Figure 5.6 shows voltages of switches $S1$, $S2$, $S3$ and $S4$ during steady on state.

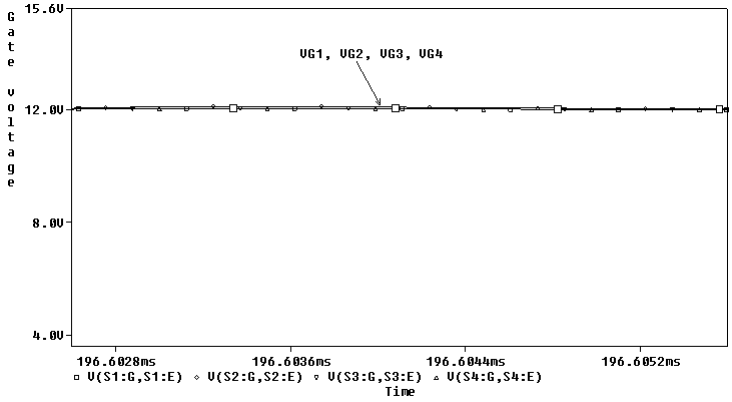

Figure 5.5: Gate signals during turn - on
[X-axis: 1 div: 0.8 μ sec, Y-axis: 1 div: 4 V]

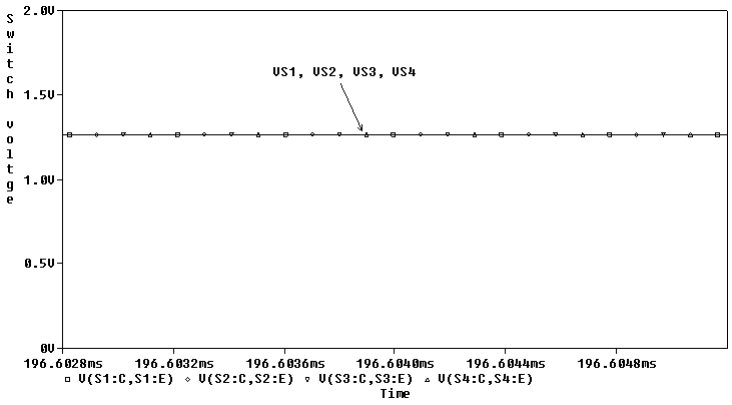

Figure 5.6: Switch voltages during steady on state
[X-axis: 1 div: 0.4 μ sec, Y-axis: 1 div: 0.5 V]

Figure 5.7 shows the gating signals with same signals for switches $S1$, $S3$, $S4$ and gating signal for $S2$ is delayed by 300 nsec during turn - off time. Figure 5.8 shows

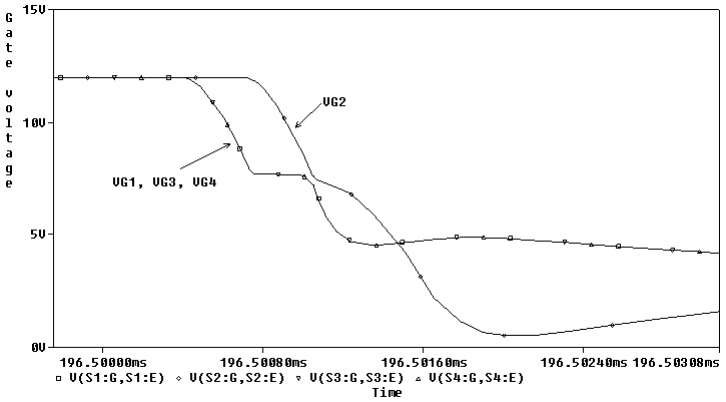

Figure 5.7: Gating signals with delay during turning - off time
[X-axis: 1 div: 0.8 μ sec, Y-axis: 1 div: 5 V]

the simulated waveforms voltage across switches during turn - off time, where switch $S2$ is delayed by 300 nsec then $S1$, $S3$ and $S4$. Hence the switches $S1$, $S3$ and $S4$ will turn - off earlier and overvoltage is obtained across them. If the overvoltage across them increases over the steady - state voltage then a gate signal is generated and voltage across them is reduced. This way voltage balanced is achieved during turn - off time. Figure 5.9 shows capacitor voltage of $C12$, $C22$, $C32$ and $C42$ during turn -

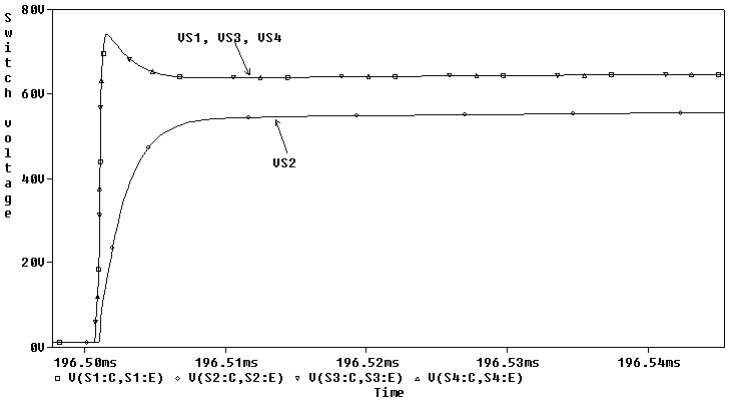

Figure 5.8: Switch voltages during turning - off time
[X-axis: 1 div: 10 μ sec, Y-axis: 1 div: 20 V]

off time. The capacitor voltage of $C12$, $C22$, $C32$ and $C42$ will change from negative

to zero to reduced the overvoltage across switches $S1$, $S3$ and $S4$. Figure 5.10 shows

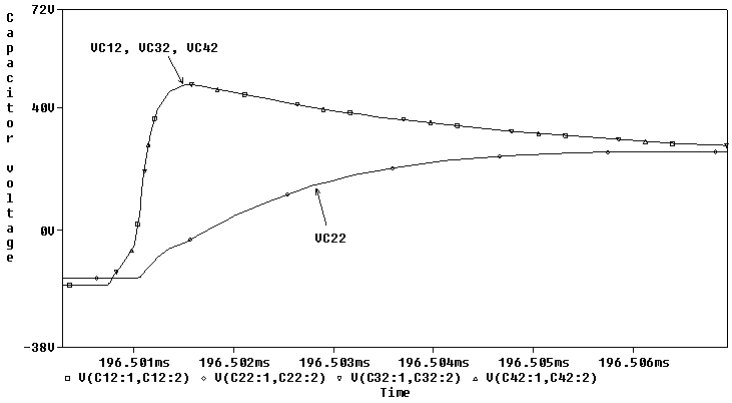

Figure 5.9: Capacitor voltages during turning - off time
[X-axis: 1 div: 4m sec, Y-axis: 1 div: 20 V]

gate voltage of switches $S1$, $S2$, $S3$ and $S4$ during steady off state.

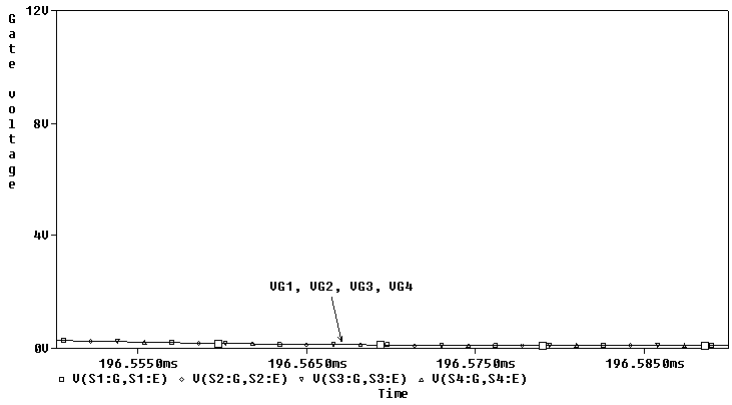

Figure 5.10: Gate signals during turn - off
[X-axis: 1 div: 10 μ sec, Y-axis: 1 div: 4 V]

Figure 5.11 shows voltages of switches $S1$, $S2$, $S3$ and $S4$ during steady off state.

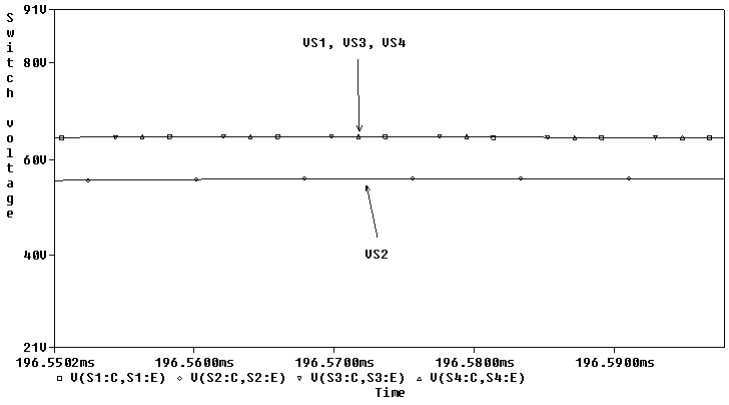

Figure 5.11: Switch voltages during steady off state
[X-axis: 1 div: 10 μ sec, Y-axis: 1 div: 40 V]

The voltage balancing during steady - state can be achieved by connecting a series resistors in parallel with each IGBT.

Figure 5.12 shows switch voltages of $S1$, $S2$, $S3$ and $S4$ with imbalance of 8.5V for 250V DC supply.

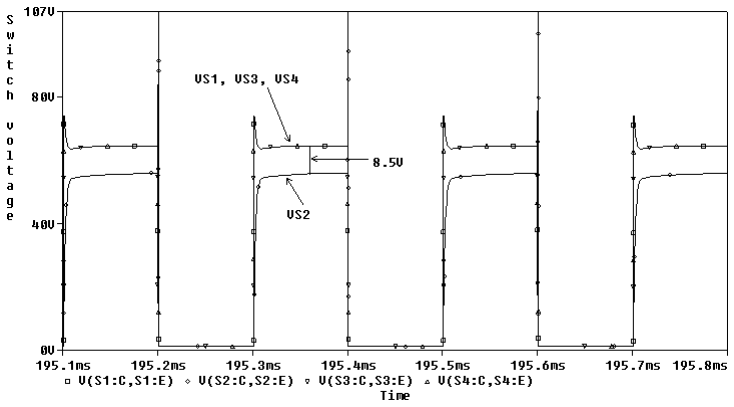

Figure 5.12: Switch voltages during steady - state
[X-axis: 1 div: 0.1m sec, Y-axis: 1 div: 40 V]

5.3 Simulation Studies for 500V

Simulation model for 500V is created with following specification is shown in Table II.

Table II: Specification of Simulation Model for 500 V

Parameters	**Value**
Supply DC Voltage V_{dc}	500 V
Load Current I_L	38.46 A
Switching Frequency	5 Khz
Delay time	300 ns
Load Resistor R_{Load}	13 Ω
Capacitor ($C11$, $C21$, $C31$, $C41$)	300 nF
Capacitor ($C12$, $C22$, $C32$, $C42$)	30 nF
Resistor ($R11$, $R21$, $R31$, $R41$)	3.2 kΩ
Resistor ($R12$, $R22$, $R32$, $R42$)	0.4 kΩ
Feedback Resistor ($Rg1$, $Rg2$, $Rg3$, $Rg4$)	56 Ω

Figure 5.13 shows the gating signals with same signals for switches $S1$, $S3$, $S4$ and gating signal for $S2$ is delayed by 300 nsec during turn - on time. Figure 5.14 shows

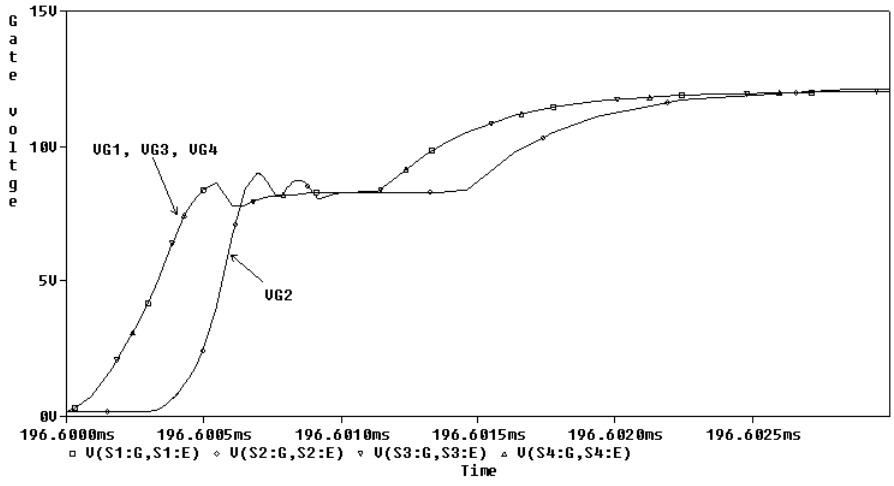

Figure 5.13: Gating signals with delay during turning - on time
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 5 V]

the simulated waveforms voltage across switches during turn - on, where switch $S2$ is delayed by 300 nsec then $S1$, $S3$ and $S4$. Hence the overvoltage is obtained across

$S2$. The voltage of capacitor $C22$ will charge from zero to positive, this voltage of capacitor $C22$ is applied across gate terminal of switch $S2$ through $D2$, $Rg2$ which will turn - on switch $S2$ slightly and overvoltage during turn - on time is reduced. In this way voltage balanced is achieved during turn - on time. Figure 5.15 shows

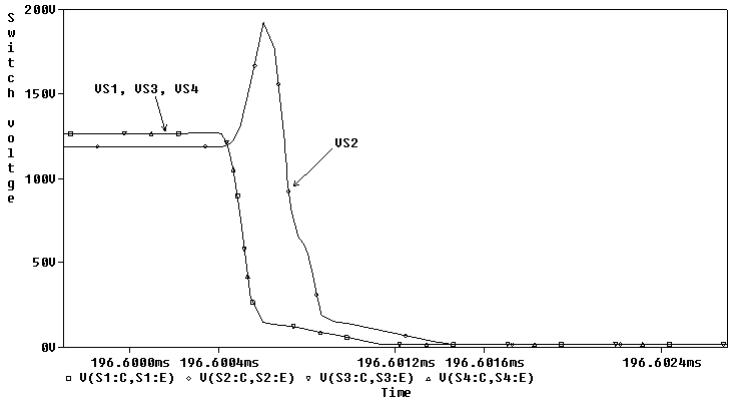

Figure 5.14: Switch voltages during turning - on time
[X-axis: 1 div: 0.4 μ sec, Y-axis: 1 div: 50 V]

capacitor voltage of $C12$, $C22$, $C32$ and $C42$ during turn - on time. The overvoltage across $S2$ charges capacitor $C22$ to clamp the overvoltage by providing an additional signal to turn on $S2$ again.

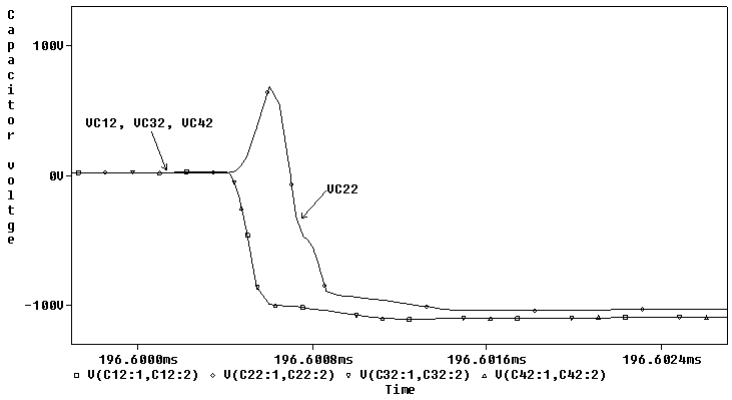

Figure 5.15: Capacitor voltages during turning - on time
[X-axis: 1 div: 0.8 μ sec, Y-axis: 1 div: 100 V]

Figure5.16 shows the gating signals for switches $S1$, $S2$, $S3$ and $S4$ during steady on state. Figure 5.17 shows voltages of switches $S1$, $S2$, $S3$ and $S4$ during steady on state.

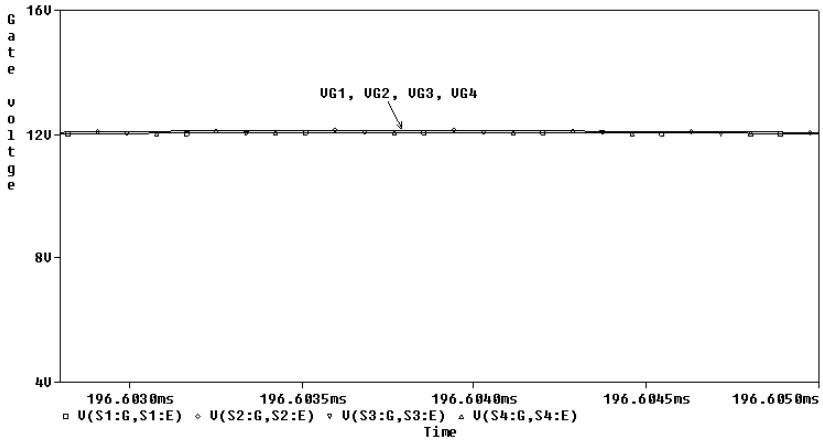

Figure 5.16: Gate siganls during turn - on
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 4 V]

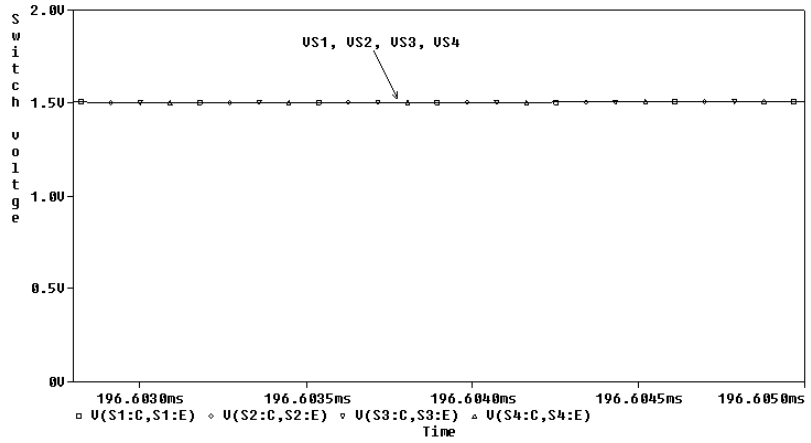

Figure 5.17: Switch voltages during steady on state
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 0.5 V]

Figure 5.18 shows the gating signals with same signals for switches $S1$, $S3$, $S4$ and gating signal for $S2$ is delayed by 300 nsec during turn - off time. Figure 5.19 shows

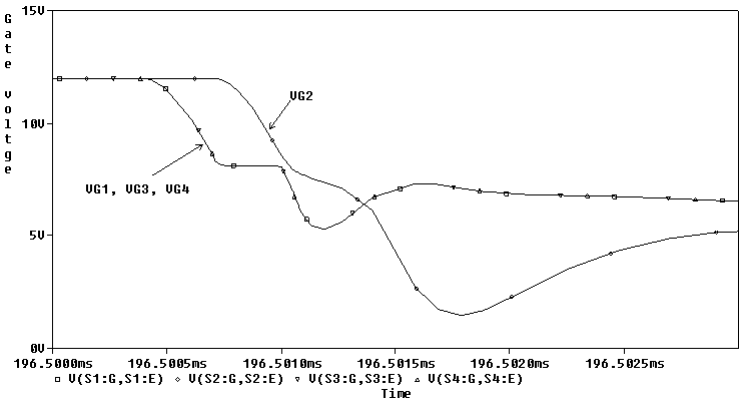

Figure 5.18: Gating with delay during turning - off time
[X-axis: 1 div: 0.5 μ sec, Y-axis: 1 div: 5 V]

the simulated waveforms voltage across switches during turn - off time, where switch $S2$ is delayed by 300 nsec then $S1$, $S3$ and $S4$. Hence the switches $S1$, $S3$ and $S4$ will turn - off earlier and overvoltage is obtained across them. If the overvoltage across them increases over the steady - state voltage then a gate signal is generated and voltage across them is reduced. This way voltage balanced is achieved during turn - off time.

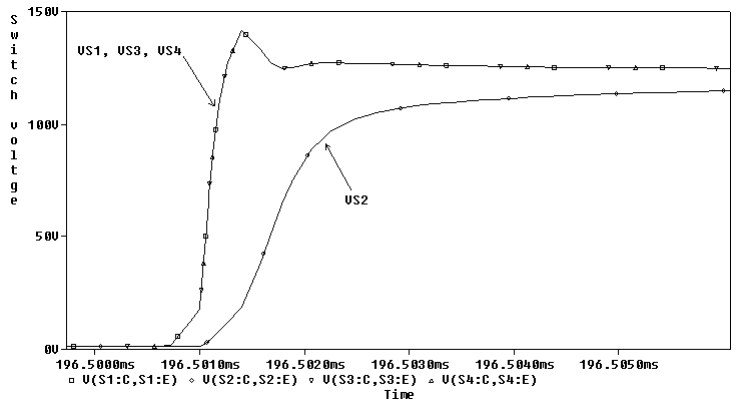

Figure 5.19: Switch voltages during turning - off time
[X-axis: 1 div: 1 μ sec, Y-axis: 1 div: 50 V]

Figure 5.20 shows capacitor voltage of $C12$, $C22$, $C32$ and $C42$ during turn - off time. The capacitor voltage of $C12$, $C22$, $C32$ and $C42$ will change from negative to zero to reduced the overvoltage across switches $S1$, $S3$ and $S4$. Figure 5.21 shows gate

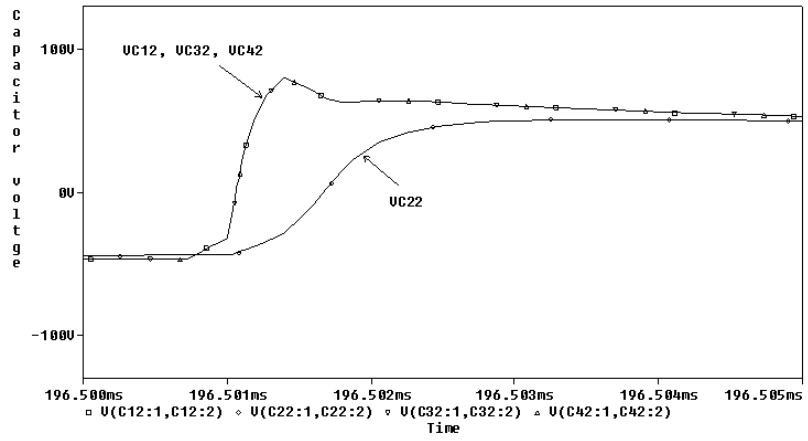

Figure 5.20: Capacitor voltages during turning - off time
[X-axis: 1 div: 1 μ sec, Y-axis: 1 div: 100 V]

voltage of switches $S1$, $S2$, $S3$ and $S4$ during steady off state.

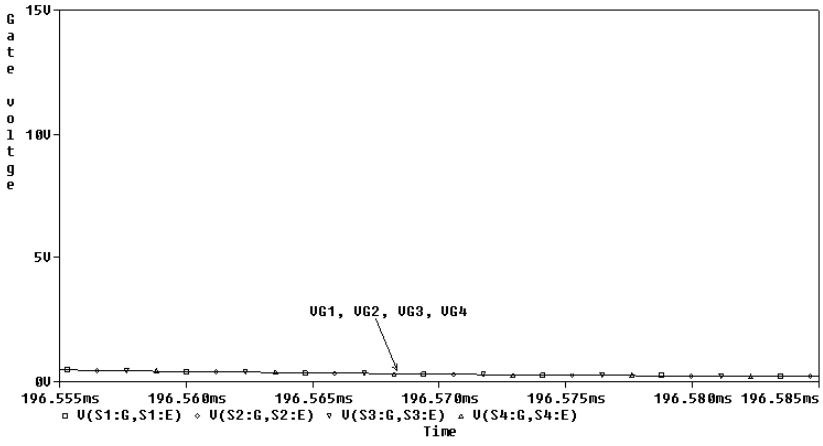

Figure 5.21: Gate signals during turn - off
[X-axis: 1 div: 5 μ sec, Y-axis: 1 div: 5 V]

Figure 5.22 shows voltages of switches $S1$, $S2$, $S3$ and $S4$ during steady off state.

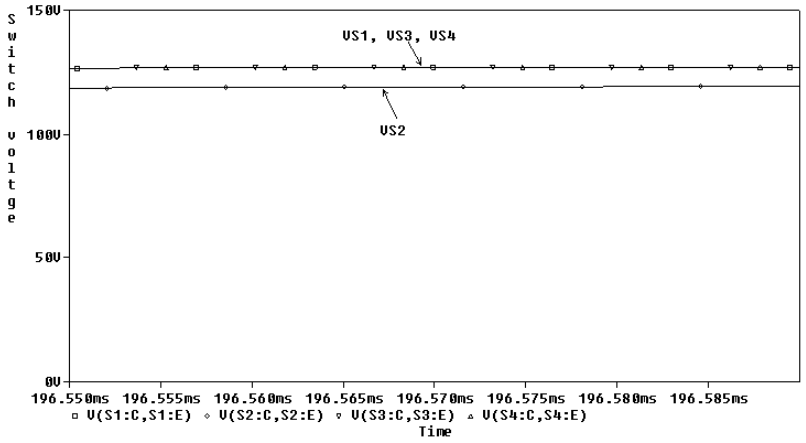

Figure 5.22: Switch voltages during steady off state
[X-axis: 1 div: 5 μ sec, Y-axis: 1 div: 50 V]

The voltage balancing during steady - state can be achieved by connecting a series resistors in parallel with each IGBT. Figure 5.23 shows switch voltages of $S1$, $S2$, $S3$ and $S4$ with imbalance of 7.5V for 500V DC supply.

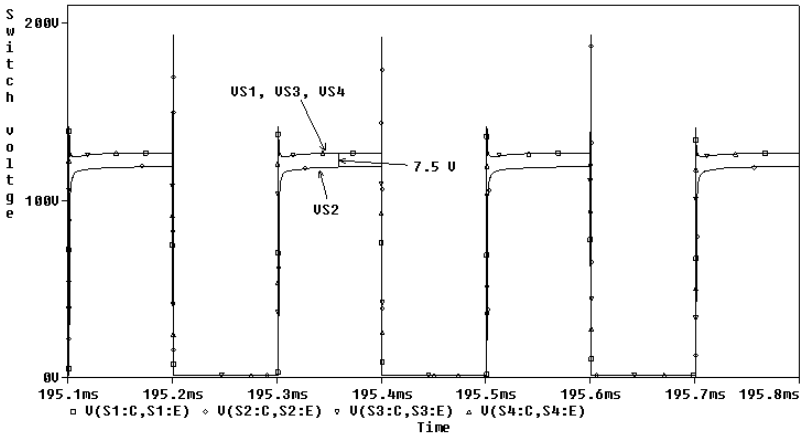

Figure 5.23: Switch voltages during steady - state
[X-axis: 1 div: 0.1m sec, Y-axis: 1 div: 100 V]

Chapter 6

Hardware Results

6.1 Dynamic Voltage Balancing of Four Series Connected IGBT

DC supply voltage source is generated by three - phase uncontrolled rectifier and its output is fed to capacitor bank to obtain pure DC voltage. Generated DC voltage is given to series link of 1200V,200A IGBT modules with its auxiliary circuit. Gate signals to IGBT modules are generated by control card which generates the four gating signals, where three gating signals are same and one gating signal is delayed. Figure 6.1 shows the hardware setup of series connected IGBTs .

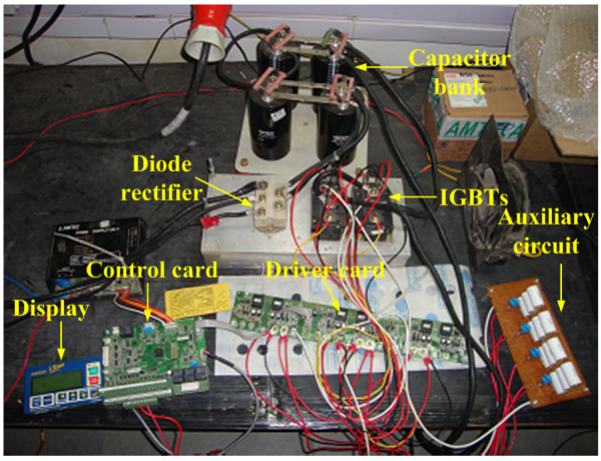

Figure 6.1: Hardware setup of series connected IGBTs

Figure 6.2 shows the gating signals of switches ($S1$, $S2$, $S3$ and $S4$) without delay.

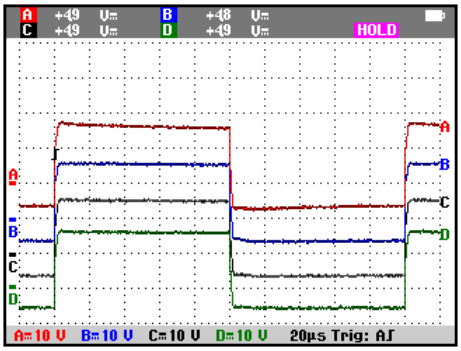

Figure 6.2: Gating signals without delay
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]
Blue Colour: Gate signal of $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]
Black Colour: Gate signal of $S3$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]
Green Colour: Gate signal of $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]

Figure 6.3 shows the switch voltage waveforms of $S1$ and $S2$.

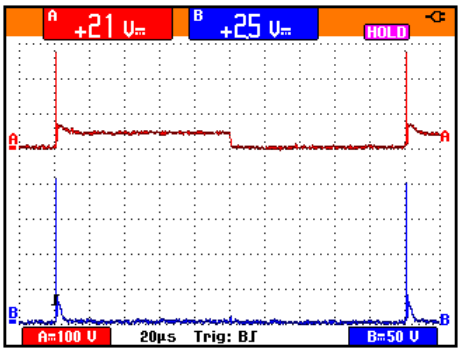

Figure 6.3: Switch voltages of switches $S1$, $S2$
Red Colour: Switch voltage of $S1$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100 V]
Blue Colour : Switch voltage of $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 50 V]

Figure 6.4 shows the switch voltage waveforms of $S3$ and $S4$.

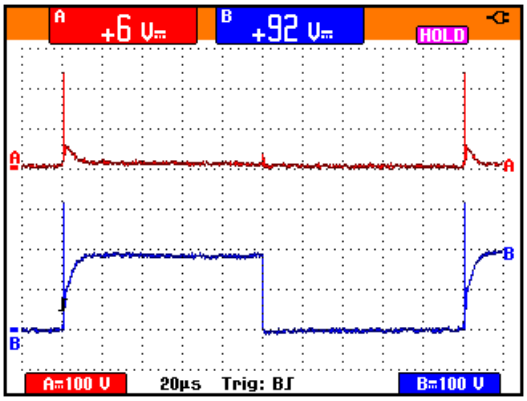

Figure 6.4: Switch voltages of switches $S3$, $S4$
Red Colour: Switch voltage of $S3$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100 V]
Blue Colour : Switch voltage of $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100 V]

Figure 6.3, and Figure 6.4 shows switch voltages of switches $S1$, $S2$, $S3$ and $S4$ without delay in the gate signals which shows unbalance in the switch voltages due to mismatch in the switching characteristics, unequal leakage currents and due to variation in the output capacitance.

Figure 6.5 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - on time.

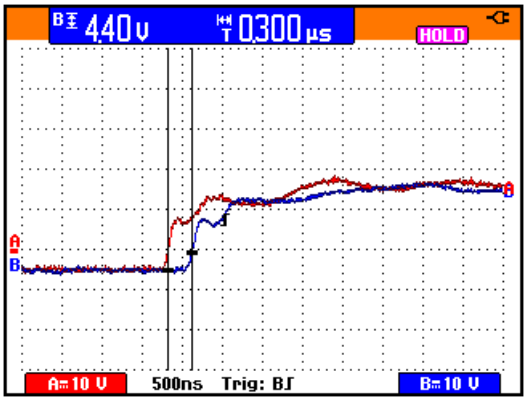

Figure 6.5: Gate signals of switches $S1$, $S2$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S2$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]

Figure 6.6 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - off time.

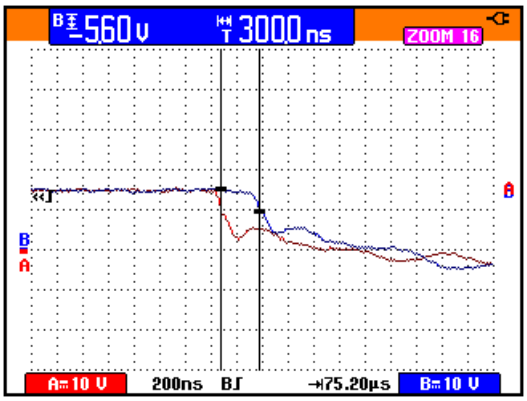

Figure 6.6: Gate signals of switches $S1$, $S2$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]
Blue Colour :Gate signal of $S2$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]

Figure 6.7 shows gating signals of switches between two switches $S1$ and $S3$ in which delay of few nsec is observed due to gate driving circuit parameters variation during turn - on time.

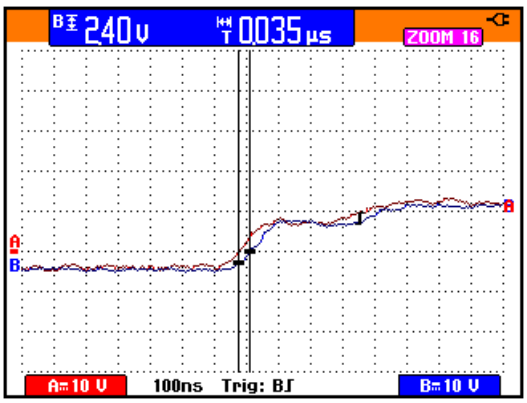

Figure 6.7: Gate signals of switches $S1$, $S3$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

Figure 6.8 shows gating signals of switches between two switches $S1$ and $S3$ in which delay of few nsec is observed due to gate driving circuit parameters variation during turn - off time.

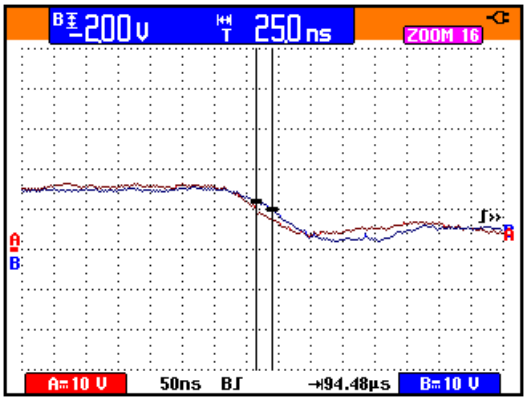

Figure 6.8: Gate signals of switches $S1$, $S3$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.9 shows gating signals of switches between two switches $S1$ and $S4$ in which delay of few nsec is observed due to gate driving circuit parameters variation during turn - on time.

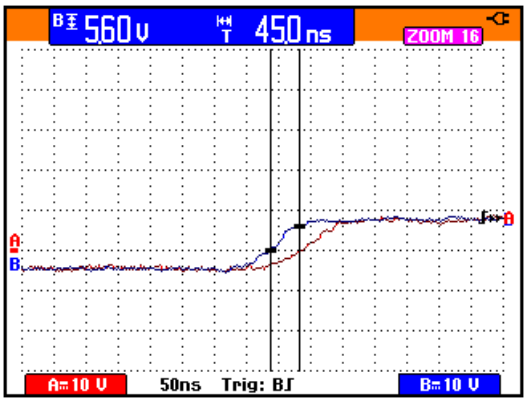

Figure 6.9: Gate signals of switches $S1$, $S4$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.10 shows gating signals of switches between two switches $S1$ and $S4$ in which delay of few nsec is observed due to gate driving circuit parameters variation during turn - off time.

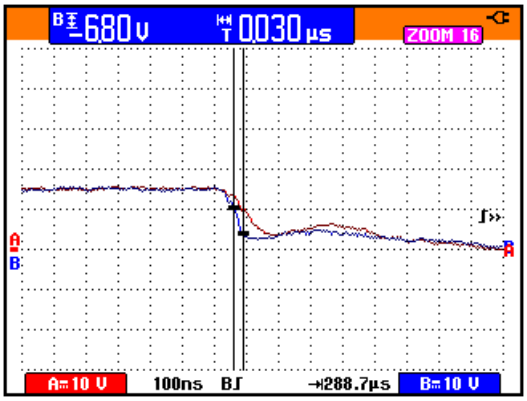

Figure 6.10: Gate signals of switches $S1$, $S4$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

Figure 6.11 shows the switch voltage waveforms of $S1$ and $S2$.

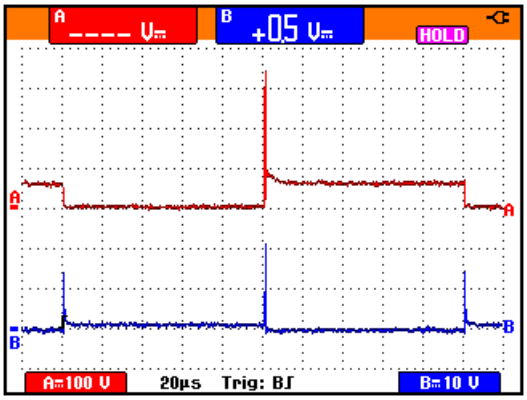

Figure 6.11: Switch voltages of switches $S1$, $S2$
Red Colour: Switch voltage of $S1$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100 V]
Blue Colour : Switch voltage of $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]

Figure 6.12 shows the switch voltage waveforms of $S3$ and $S4$.

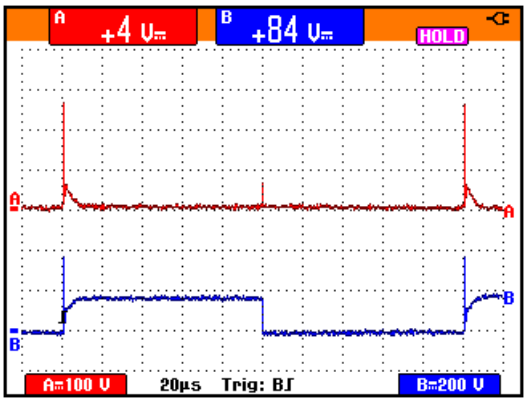

Figure 6.12: Switch voltages of switches $S3$, $S4$
Red Colour: Switch voltage of $S3$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100 V]
Blue Colour : Switch voltage of $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 200 V]

Figure 6.11 and Figure 6.12 shows switch voltage waveforms of $S1$, $S2$ and $S3$, $S4$ with delay of 300 nsec between switch two switches $S1$ and $S2$ during turn - on and turn - off time without auxiliary circuit. Hence their is unbalance in the switch voltages during turn - on, turn - off and steady - state time due to unsynchronized gate driving signals .

6.2 Hardware Results for 250 V

Hardware prototype is created with following specification is shown in Table I.

Table I: Specification of Hardware Model for 250 V

Parameters	**Value**
Supply DC Voltage V_{dc}	250 V
Load Current I_L	22.26 A
Switching Frequency	5 Khz
Delay time	300 ns
Load Resistor R_{Load}	11 Ω
Capacitor ($C11$, $C21$, $C31$, $C41$)	300 nF
Capacitor ($C12$, $C22$, $C32$, $C42$)	30 nF
Resistor ($R11$, $R21$, $R31$, $R41$)	3 kΩ
Resistor ($R12$, $R22$, $R32$, $R42$)	0.3 kΩ
Feedback Resistor ($Rg1$, $Rg2$, $Rg3$, $Rg4$)	56 Ω

Figure 6.13 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - on time.

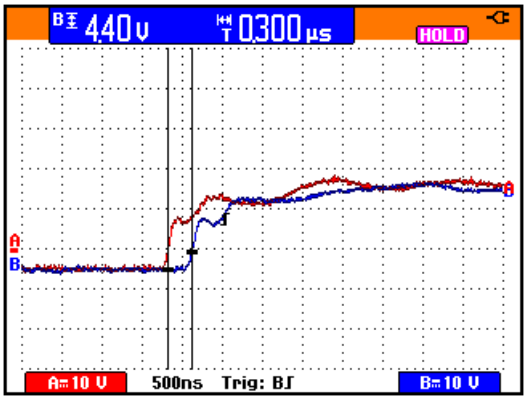

Figure 6.13: Gate signals of switches $S1$, $S2$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S2$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]

Figure 6.14 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - off time.

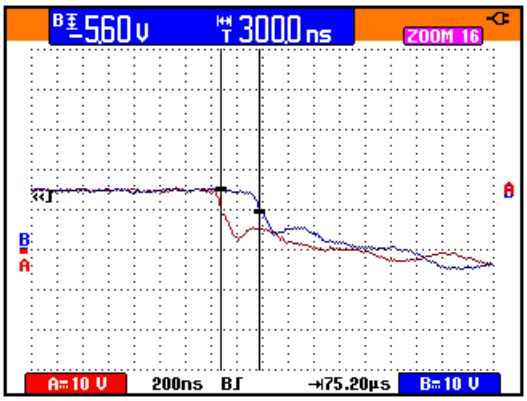

Figure 6.14: Gate signals of switches $S1$, $S2$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]
Blue Colour :Gate signal of $S2$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]

Figure 6.15 shows gating signals of switches between two switches $S1$ and $S3$ during turn - on time.

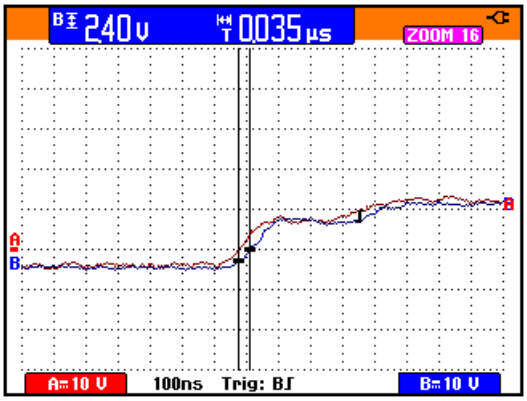

Figure 6.15: Gate signals of switches $S1$, $S3$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

Figure 6.16 shows gating signals of switches between two switches $S1$ and $S3$ during turn - off time.

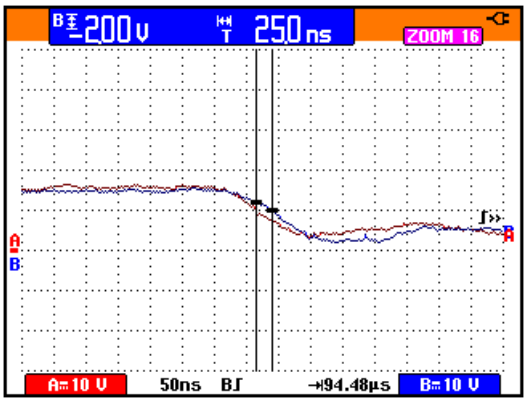

Figure 6.16: Gate signals of switches $S1$, $S3$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.17 shows gating signals of switches between two switches $S1$ and $S4$ during turn - on time.

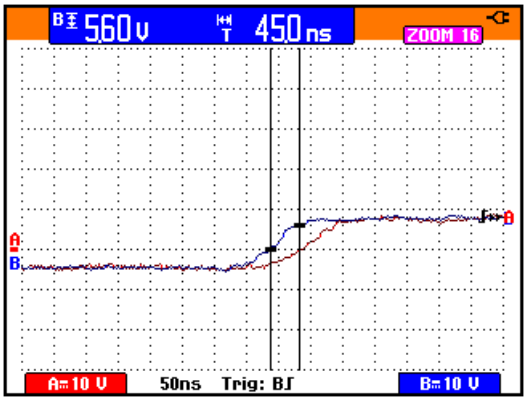

Figure 6.17: Gate signals of switches $S1$, $S4$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.18 shows gating signals of switches between two switches $S1$ and $S4$ during turn - off time.

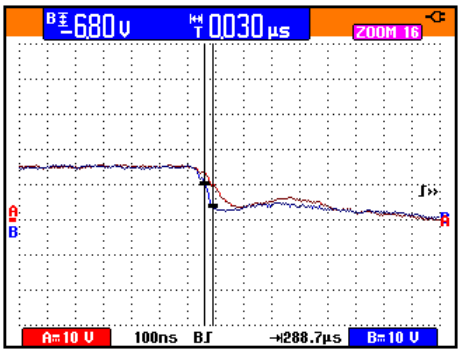

Figure 6.18: Gate signals of switches $S1$, $S4$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

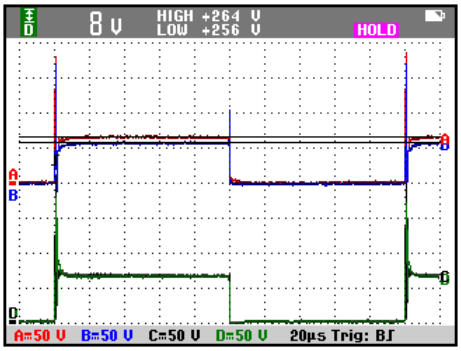

Figure 6.19: Switch voltages with auxiliary circuit
Red Colour: Switch voltge of $S1$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 50 V]
Blue Colour: Switch voltage of $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 50 V]
Black Colour: Switch voltage of $S3$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 50 V]
Green Colour: Switch voltage of $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 50 V]

Figure 6.19 shows switch voltage waveforms of $S1$, $S2$, $S3$ and $S4$ with auxiliary circuit. In which delayed gate signal is give to switch $S2$. Hence, voltage balance is achieved during turn - on time and turn - off time. During turn - on time the turn - on spike is reduced to 80 V and turn - off spike is also reduced. Voltage imbalance between switches is reduced to 8 V. Hence, dynamic and steady state voltage balance is achieved by connecting an auxiliary circuit.

Figure 6.20 shows gate voltages and switch voltages of $S1$ and $S2$

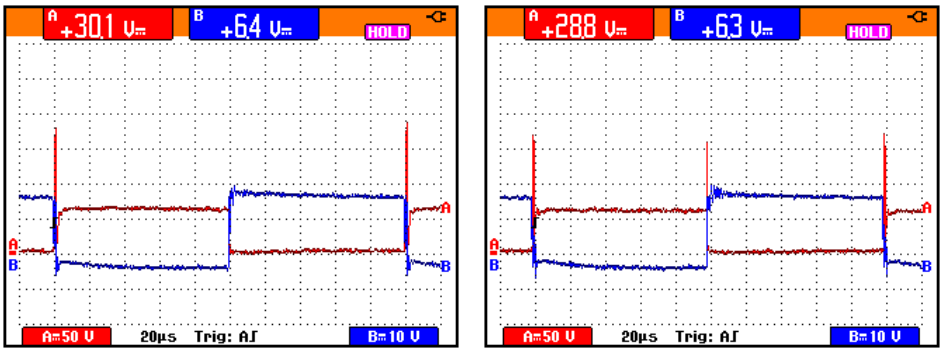

Figure 6.20: (a) Gate voltage and switch voltage of $S1$ (b) Gate voltage and switch voltage $S2$
Red Colour: Switch voltage of $S1$, $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div:50 V]
Blue Colour : Gate voltage of $S1$, $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]

Figure 6.21 shows gate voltages and switch voltages of $S3$ and $S4$

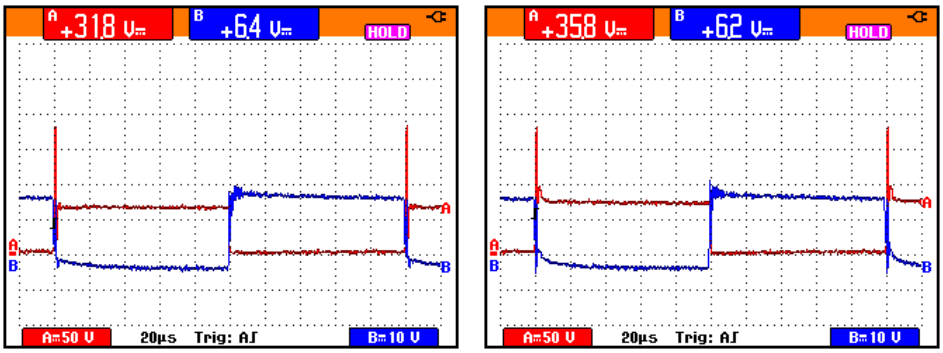

Figure 6.21: (a) Gate voltage and switch voltage of $S3$ (b) Gate voltage and switch voltage $S4$
Red Colour: Switch voltage of $S3$, $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div:50 V]
Blue Colour : Gate voltage of $S3$, $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10 V]

Figure 6.22 shows gate voltage and switch voltage waveform of $S1$ during turn - on and turn -off time.

Figure 6.23 shows gate voltage and switch voltage waveform of $S2$ during turn - on and turn -off time. As switch $S2$ is delayed by 300 nsec from switches $S1$, $S3$ and $S4$ overvoltage is applied across switch $S2$ during turn - on time. The voltage of capacitor $C22$ will charge from zero to positive, this voltage of capacitor $C22$ is applied across gate terminal of switch $S2$ through $D2$, $Rg2$ which will turn - on switch $S2$ slightly

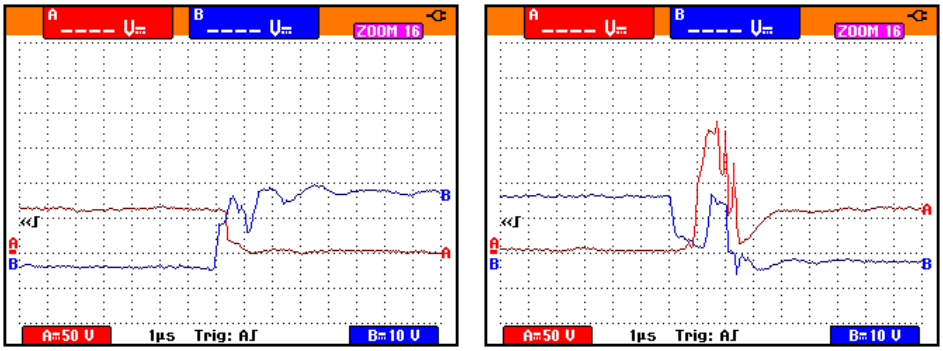

Figure 6.22: (a) Gate voltage and switch voltage of $S1$ during turn - on time (b) Gate voltage and switch voltage $S1$ during turn - off time
Red Colour: Switch voltage of $S1$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div:50 V]
Blue Colour : Gate voltage of $S1$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div: 10 V]

and overvoltage during turn - on time is reduced. During turn - off time as switch $S2$ is delayed by 300 nsec from switch $S1$, $S3$ and $S4$, overvoltage is applied across switch $S1$, $S3$ and $S4$ during turn - off time, the voltage of capacitor $C12$, $C32$ and $C42$ will charge from negative to zero and an additional signal is generated across gate terminal through $Rg1$, $Rg3$ and $Rg4$ to clamp the overvoltage. Hence, dynamic voltage balancing is achieved during turn-on and turn - off time by generating the feedback signal across gate terminal of the switches.

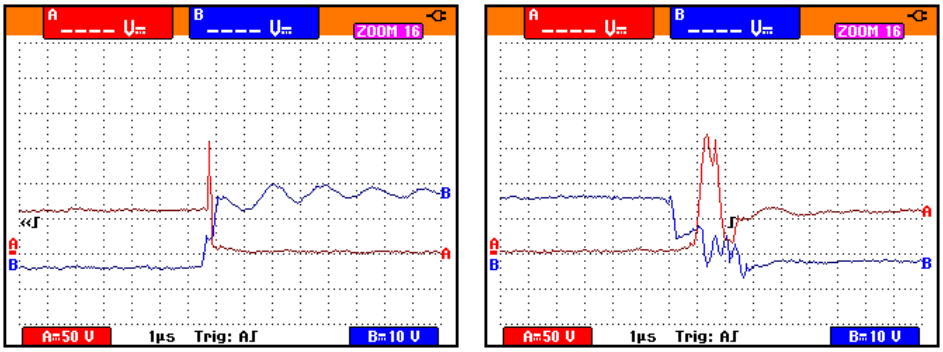

Figure 6.23: (a) Gate voltage and switch voltage of $S2$ during turn - on time (b) Gate voltage and switch voltage $S2$ during turn - off time
Red Colour: Switch voltage of $S2$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div:50 V]
Blue Colour : Gate voltage of $S2$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div: 10 V]

6.3 Hardware Results for 500 V

Hardware prototype is created with following specification is shown in Table II.

Table II: Specification of Hardware Model for 500 V

Parameters	**Value**
Supply DC VoltageV_{dc}	500 V
Load CurrentI_L	38.46 A
Switching Frequency	5 Khz
Delay time	300 ns
Load Resistor R_{Load}	13 Ω
Capacitor ($C11$, $C21$, $C31$, $C41$)	300 nF
Capacitor ($C12$, $C22$, $C32$, $C42$)	30 nF
Resistor ($R11$, $R21$, $R31$, $R41$)	3.2 kΩ
Resistor ($R12$, $R22$, $R32$, $R42$)	0.4 kΩ
Feedback Resistor ($Rg1$, $Rg2$, $Rg3$, $Rg4$)	56 Ω

Figure 6.24 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - on time.

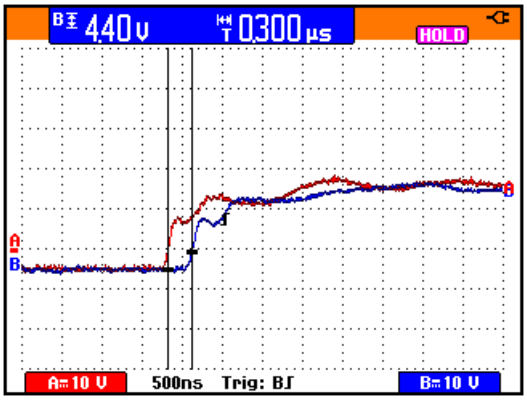

Figure 6.24: Gate signals of switches $S1$, $S2$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S2$ [X-axis: 1 div: 500 nsec, Y-axis: 1 div: 10 V]

Figure 6.25 shows gating signals of switches with delay of 300 nsec between two switches $S1$ and $S2$ during turn - off time.

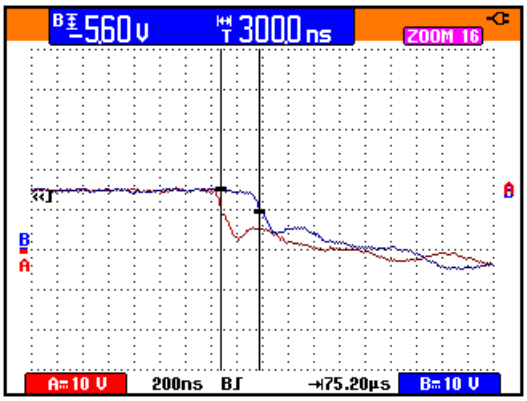

Figure 6.25: Gate signals of switches $S1$, $S2$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]
Blue Colour :Gate signal of $S2$ [X-axis: 1 div: 200 nsec, Y-axis: 1 div: 10 V]

Figure 6.26 shows gating signals of switches between two switches $S1$ and $S3$ during turn - on time.

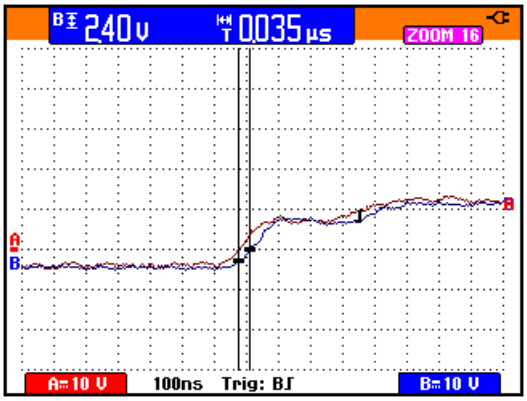

Figure 6.26: Gate signals of switches $S1$, $S3$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

Figure 6.27 shows gating signals of switches between two switches $S1$ and $S3$ during turn - off time.

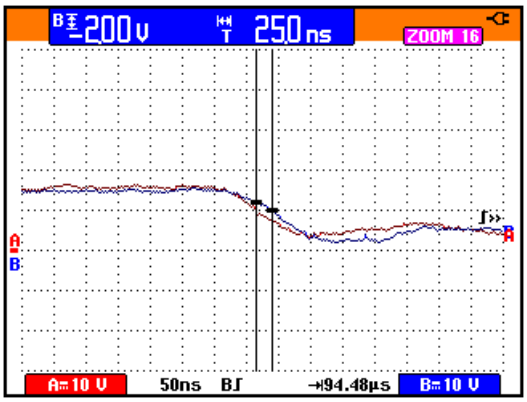

Figure 6.27: Gate signals of switches $S1$, $S3$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S3$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.28 shows gating signals of switches between two switches $S1$ and $S4$ during turn - on time.

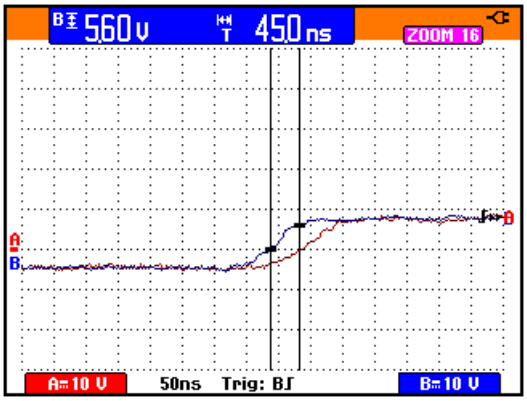

Figure 6.28: Gate signals of switches $S1$, $S4$ during turn - on time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 50 nsec, Y-axis: 1 div: 10 V]

Figure 6.29 shows gating signals of switches between two switches $S1$ and $S4$ during turn - off time.

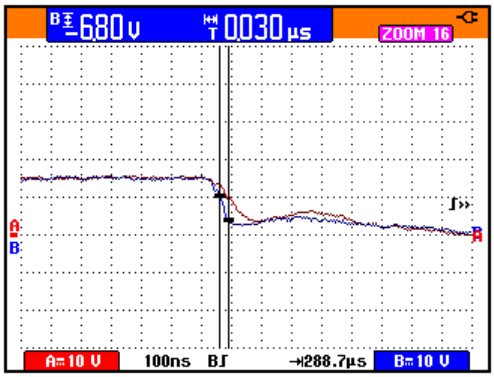

Figure 6.29: Gate signals of switches $S1$, $S4$ during turn - off time
Red Colour: Gate signal of $S1$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]
Blue Colour : Gate signal of $S4$ [X-axis: 1 div: 100 nsec, Y-axis: 1 div: 10 V]

Figure 6.30 shows switch voltage waveforms of $S1$, $S2$, $S3$ and $S4$ with auxiliary circuit. In which delayed gate signal is give to switch $S2$. Hence, voltage balance is achieved during turn - on time and turn - off time. The turn - off spike and turn - on spike is significantly reduced. Voltage imbalance between switches is reduced to 8 V. Hence, dynamic and steady state voltage balance is achieved by connecting an auxiliary circuit.

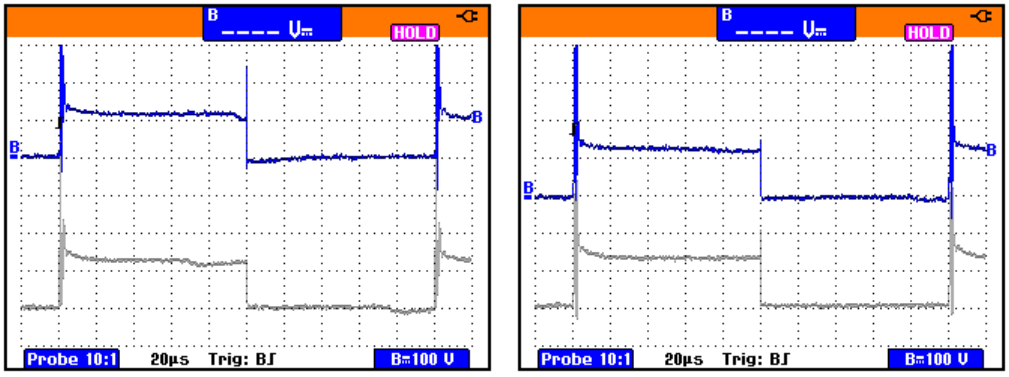

Figure 6.30: (a) Switch voltages $S1$, $S2$ (b) Switch voltages $S3$, $S4$
Gray Colour: Switch voltages of $S1$, $S3$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100V]
Blue Colour : Switch voltages of $S2$, $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100V]

Figure 6.31 shows gate voltages and switch voltages of $S1$ and $S2$

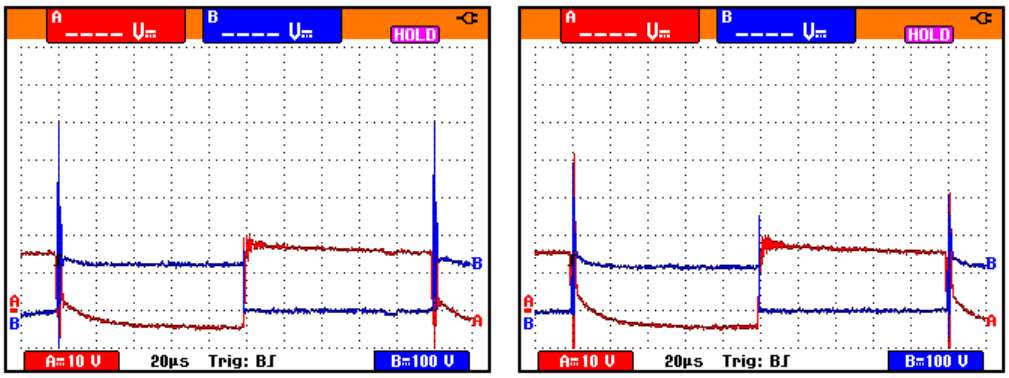

Figure 6.31: (a) Gate voltage and switch voltage of $S1$ (b) Gate voltage and switch voltage $S2$
Red Colour: Gate voltages of $S1$, $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10V]
Blue Colour : Switch voltages of $S1$, $S2$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100V]

Figure 6.32 shows gate voltages and switch voltages of $S3$ and $S4$

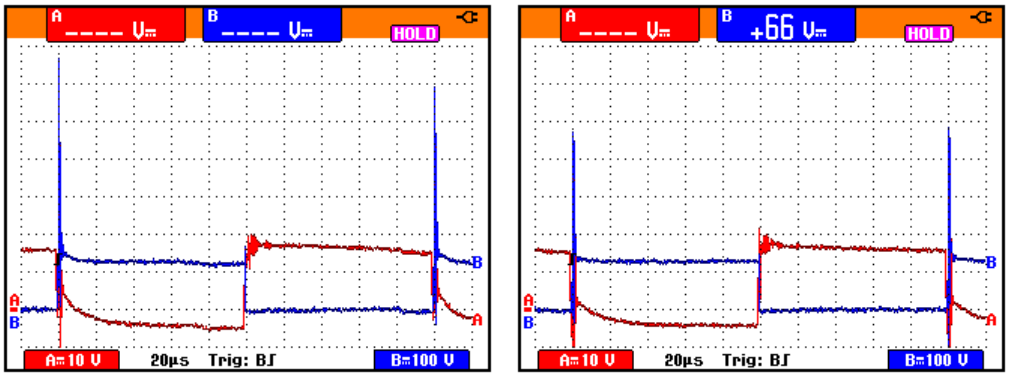

Figure 6.32: (a) Gate voltage and switch voltage of $S3$ (b) Gate voltage and switch voltage $S4$
Red Colour: Gate voltages of $S3$, $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 10V]
Blue Colour : Switch voltages of $S3$, $S4$ [X-axis: 1 div: 20μ sec, Y-axis: 1 div: 100V]

Figure 6.33 shows gate voltage and switch voltage waveform of $S1$ during turn - on and turn -off time.

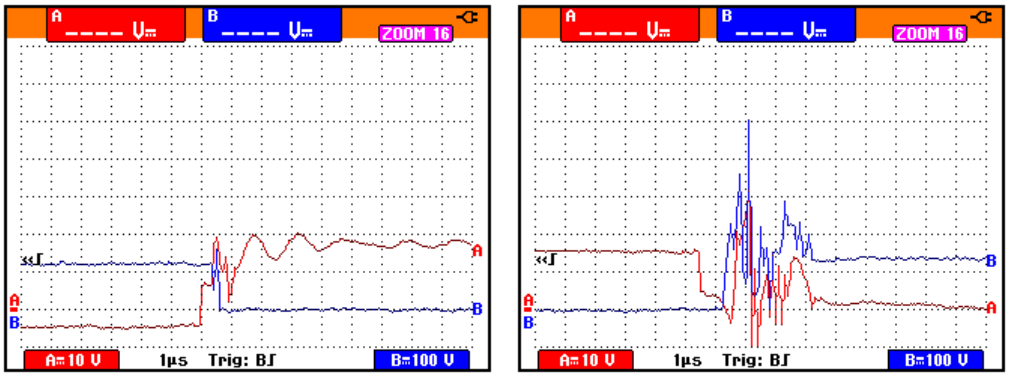

Figure 6.33: (a) Gate voltage and switch voltage of $S1$ during turn - on time (b) Gate voltage and switch voltage $S1$ during turn - off time
Red Colour: Gate voltage of $S1$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div:10 V]
Blue Colour : Switch voltage of $S1$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div: 100 V]

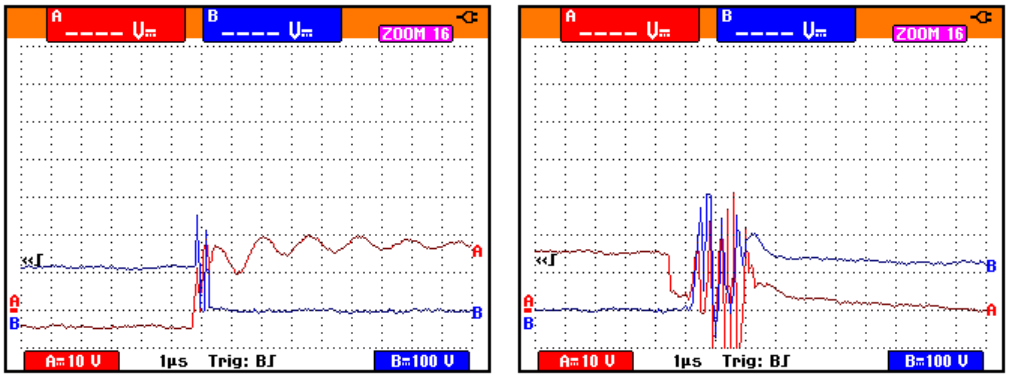

Figure 6.34: (a) Gate voltage and switch voltage of $S2$ during turn - on time (b) Gate voltage and switch voltage $S2$ during turn - off time
Red Colour: Gate voltage of $S2$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div:10 V]
Blue Colour : Switch voltage of $S2$ [X-axis: 1 div: 1μ sec, Y-axis: 1 div: 100 V]

Figure 6.34 shows gate voltage and switch voltage waveform of $S2$ during turn - on and turn -off time. As switch $S2$ is delayed by 300 nsec from switch $S1$, $S3$ and $S4$ overvoltage is applied across switch $S2$ during turn - on time. The voltage of capacitor $C22$ will charge from zero to positive, this voltage of capacitor $C22$ is applied across gate terminal of switch $S2$ through $D2$, $Rg2$ which will turn - on switch $S2$ slightly and overvoltage during turn - on time is reduced. During turn - off time as switch $S2$

is delayed by 300 nsec from switch $S1$, $S3$ and $S4$ overvoltage is applied across switch $S2$ during turn - off time, the voltage of capacitor $C12$, $C32$ and $C42$ will charge from negative to zero and an additional signal is generated across gate terminal to clamp the overvoltage. Hence, dynamic voltage balancing is achieved during turn - on and turn - off time by generating the feedback signal across gate terminal of the switches.

Chapter 7

Conclusions and Future Work

7.1 Conclusion

The simulation of four IGBTs connected in series is carried out with its voltage balancing circuit using active gate control circuit with passive elements like resistors, capacitors and diodes (RCD) in PSpice. During dynamic state when the auxiliary circuit is not connected a high voltage peak across delayed switch is observed however by connecting the auxiliary circuit the voltage peak has been reduced. The static voltage balancing is achieved by connecting a parallel resistors across switch (IGBTs), the value of the resistors should increases with the increase in the DC supply. As the static voltage balancing is well achieved with the lower value of resistors but the power rating of the resistors increases, which increases the significant loss in the resistors.
It has been observed that voltage balancing is achieved during static and dynamic state. Voltage imbalance between switches is reduced to 8V by using active gate control circuit voltage with passive elements like resistors, capacitors and diode which has following advantages:

- Reduces the complexity of the driving circuits;
- No need of external snubber capacitors;
- Low cost;
- Compact in size;

- It can be applicable to numbers series connected devices;
- No closed loop feedback sensing control is required.

7.2 Future Scope

- Testing of the hardware setup prototype for higher DC voltages;
- To reduce the high voltage peak during transients;
- Reduce the oscillations to improve overall reliability of the system.

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