Design and Implementation of CMOS Gm-C IF Filter Using Switching Capacitor Array For Dual Band Receiver

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Abstract

In wireless communication system where it is necessary to control the bandwidth of the signal path, filters are frequency-selective electronic circuits designed to pass a band of wanted signals and stop or reject unwanted signals, noise or interference outside the pass band. The pass band of a filter is the range of frequencies over which signals are transmitted from input to output without attenuation or gain. For higher frequencies, however, Operational amplifiers designs become difficult due to their frequency limit, so at those high frequencies, operational transconductance amplifiers (OTAs) replace operational amplifier as the building blocks. Using OTAs as the building blocks for analog applications and scaling-down semiconductor technologies, OTAs can work up to several hundred MHz. Currently, high frequency, high linearity, and low power are the three main concerns of CMOS OTAs. Tradeoffs have to be made among these aspects in designing practical OTAs. Amongst all the topologies of OTA, on the basis of literature survey, Folded Cascode OTA is chosen as it allows negligible swing limitations.

Continuous-time filters implemented with transconductance amplifiers and capacitors known as Gm-C Filter or OTA-C Filter. Rapidly growing mobile and wireless communication market, fully integrated filters for very high frequency and low power consumption applications have received considerable attention. In most continuous-time filters, an on-chip automatic tuning system is incorporated to overcome performance degradation due to process variations and fabrication tolerances as well as the effects of parasitic, temperature, and environment changes.

This research work involve research studies to realize CMOS Folded Cascode OTA and implement on chip High frequency gm-C IF Filter for Dual Band FM band and GSM band. An array of Band selection filters in a Multi Mode design is not power efficient and it would occupy large chip area, so it is decided to realize single band select filter that meets the requirement of dual band applications.

CMOS Folded Cascode OTA design is characterized to layout level based on TSMC 0.18μm process technology with the BSIM3V3 Level 49 MOSFET model. Designed folded cascode OTA has gain of 52 dB and a wide bandwidth of 400 MHz with phase margin of 50 degrees and power consumption 288μw.

Design of a 2^{nd} order gm-C dual-band IF filter to be used in a down conversion receiver for FM band and GSM band, as design is carried out in the TSMC 0.18 μm CMOS technology and the filter operates form 1.8V single supply. Designed 2^{nd} order gm-C dual-band IF filter Gm-C filter for GSM band work at a center frequency 70MHz(Bandwidth 5.10MHz) and for FM band work at a center frequency 10.6Mhz(bandwidth 1.73MHz) with power consumption 575μw

The designed filter has tuning ratio 6.6 and suitable for IF channel selection of Wireless System. Gm-C architecture also using an Automatic Tuning system for tuning purpose. The circuit does not need any external biasing circuit, only need to apply V_{DD} (1.8V).

Acknowledgement

To discover, analyze and to present something new is to venture on an untrodden path towards an unexplored destination is an arduous adventure unless one gets a true torchbearer to show the way. It is my profound privilege to express sense of gratitude to my guide **Dr.N.M.Devashrayee(PG Coordinator, VLSI Design, Institute of Technology, Nirma University)** for their constant guidance, inspiration and encouragement throughout this research work and for their critical reviews during the completion of this thesis. Without him valuable support, I could not have envisaged the successful completion of the thesis. The guidance provided by him has helped me in understanding the subject and associated research element.

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Kehul A. Shah

Table of Contents

List of Figures

List of Tables

List of Abbreviations

ADC	Analog to Digital Converter
DSP	Digital Signal Processor
CT	Continuous Time
OTA	Operational Transconductance Amplifier
OTA-C	Operational Transconductance Amplifier and Capacitor
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
GaAs	Gallenium Arsenide
MLF	Multiple Loop Feedback
LC	Inductor Capacitor
IF	Intermediate Frequency
SAW	Surface Acoustic Wave
Gm-C	Transconductance Amplifier and Capacitor
FM	Frequency Modulation
GSM	Global System for Mobile Communication
TSMC	Taiwan Semiconductor Manufacturing Corporation
CMOS	Complementary Metal Oxide Semiconductor
SoC	System on Chip
OP-AMP	Operational Amplifier
PC	Personal Computer
SC	Switched Capacitor
LTI	Linear Time Invariant
RF	Radio Frequency
LO	Local Oscillator
LNA	Low Noise Amplifier
VGA	Variable Gain Amplifeir
PLL	Phase Lock Loop
VCO	Voltage Controlled Oscillator
GBW	Gain Bandwidth

WLAN	Wireless Local Area Network
LHP	Left Hand Pole
LCMFB	Local Common Mode Feedback
CAD	Computer Aided Design
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ratio
SR	Slew Rate
THD	Total Harmonic Distortion
SFDR	Spurious Free Dynamic Range
ICMR	Input Common Mode Range
GVO	Gate Voltage Overdrive
LF	Leapfrog
PRB	Primary Resonator Block
FLF	Follow the Leader Feedback
WCDMA	Wireless Code Division Multiple Access
NSDR	Negative Source Degeneration
RF	Radio Frequency
WCM	Wilson Current Mirror
CCM	Cascode Current Mirror
LHP	Left Half Plane
RHP	Right Half Plane
VCF	Voltage Controlled Filter
VCO	Voltage Controlled Oscillator
PLL	Phase Lock Loop
CA	Capacitor Array
3G	Third Generation
4G	Fourth Generation
dB	Decibel
GBW	Gain Bandwidth

List of Symbols

f_{clk}	Clock Frequency
V-I	Voltage to Current Convert
T_s	Sampling Period
f_{IF}	Intermediate Frequency
Q	Quality Factor
C	Capacitance
ε_0	Permittivity
ε_r	Relative Permittivity
W	Width of Transistor
L	Length of Transistor
C_{ox}	Oxide Capacitance
g_m	Transconductance
A	Feedback Gain
V_i	Input Voltage
i_0	Output Current
I_D	Drain current
Φ_F	Fermi Potential
γ	Body Constant
V_{TH}	Threshold Voltage
V_{GS}	Voltage between Gate and Source
μ_n	Mobility of Electron
p	Pole
z	Zero
A_{DM}	Differential gain
A_{CM}	Common mode gain

φ_m	Phase margin
β	Feedback factor
$\frac{dV_{out}}{dt}$	Rate of change of output voltage with respect to time
p_n	Power of the nth harmonic
s_n	Spectral Density
H_n	Magnitude Response
P_{signal}	Signal Power
P_{Noise}	Noise Power
C_L	Load Capacitor
R_i	Input Resistance
R_0	Output Resistance
I_{SS}	Bias Current
f_t	Cutoff Frequency
C_T	Tail Capacitor
C_M	Mirror Capacitor
λ_P	Channel length modulation for PMOS
λ_N	Channel length modulation for NMOS
T	Temperature
K	Constant
q	Charge
K_f	Flicker Coefficient
Δf_n	Noise Bandwidth
I_{nd}^2	Drain Thermal Noise
V_{ng}^2	Gate Thermal Noise
$1/f$	Corner frequency

τ_{ϖ}	Delay
S_x^p	Sensitivity in p
N(s)	Numerator Polynomial
D(s)	Denominator Polynomial
S_{11}	Input Reflection Coefficient
S_{12}	Reverse Transmission
S_{21}	Forward Transmission
S_{22}	Output Reflection Coefficient

Chapter 1

Introduction

1.1 Motivation and Background

In any system that interfaces with the real world, the quantity which processed is always contaminated with noise and interferes. A filter is usually used to reject the surrounding interferes and unwanted noise. Though we are living in a digital age, any system that interfaces with the real world is the analog world, use continuous time filter. A typical digital processing system is shown in Figure 1.1

The physical quantity to be processed is converted to an electrical signal via a transducer. This signal is then converted to a digital signal via an ADC and further processing by the digital signal processor (DSP). According to Nyquist theory and to avoid aliasing, the input signal must be band limited before the A/D conversion. This is achieved by low-pass filters (anti-aliasing filter) that control the bandwidth of the signal which is half the sampling rate of the ADC. The processed digital signal coming out of the DSP is converted back to an analog signal via a low-pass reconstruction filter. Both the anti-aliasing filter and the reconstruction filter are analog filters operating in continuous-time.

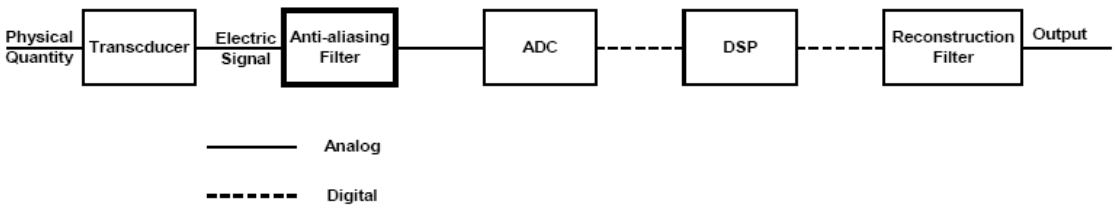


Figure 1.1 A Typical DSP System

The term continuous-time is somewhat confused with term sampled-data. Sampled-data filters do not work with the digital representation of the signal samples, as digital filters do. Thus these filters are discontinuous in time but continue in processed data values. The best example is switched-capacitor filters. Due to the sampling operation involved, continuous-time anti-aliasing filter and reconstruction filter are still needed in those kinds of switched-capacitor systems. Table 1.1 summarizes the properties of the filter categories.

Table: 1.1 Comparison of different types of Filter

	Digital	Sample-Data	Continuous-Time
Time Sample	Discrete	Discrete	Continuous
Data Sample	Discrete	Continuous	Continuous
Need Anti-Aliasing and Reconstruction Filter	Yes	Yes	No
Required Mathematical Transform	Z-Transform	Z-Transform	S-Transform (Laplace)

Filters can be also categorized according to the relative size of the elements used with respect to the wavelength of the signal into two categories: distributed and non distributed filters. In a non-distributed (lumped) filter, the physical dimensions of the used elements (resistance, inductance, or capacitance) are negligible compared to the wavelength of the signal. Thus they are considered as simple elements corresponding to physical element. This is in contrast to the distributed filter, in which the physical elements have dimensions comparable to the wavelength of the fields associated with the signal.

The main focus of this research is the design issues of high frequency continuous time integrated filters. High frequency continuous-time filters have been widely used, in cases where speed and low power dissipation are prime concern. Those applications, as shown in Figure 1.2, include video signal processing [1], hard-disk drive read channels [2], loop filters for phase-locked loops [3], and radio frequency wireless communication systems [4].Using digital filters is not feasible for high frequency applications because they are very power hungry at high frequencies, i.e., powerά $f_{CLK}\frac{(V_{DD}^2)}{2}$. Switched capacitor filters can have good linearity and dynamic range properties but its ability to process high frequency signals due to the sampling operation is limited. The sampling frequency should be chosen larger than the filter bandwidth to avoid inaccurate filter frequency response. That requires the use of operational amplifiers (Op-Amps) with very wide bandwidths, to provide proper settling, demanding large currents; it is required that the unity gain frequency of the used operational amplifier must be at least five times larger than the clock frequency used. Thus continuous-time filters became the only option in these types of applications. Continuous-time filters include two main categories: passive filters and active filters. A passive filter include among its elements resistors, capacitors, inductors, transformers. If the elements of the filter include amplifiers or negative resistances, this is called active.

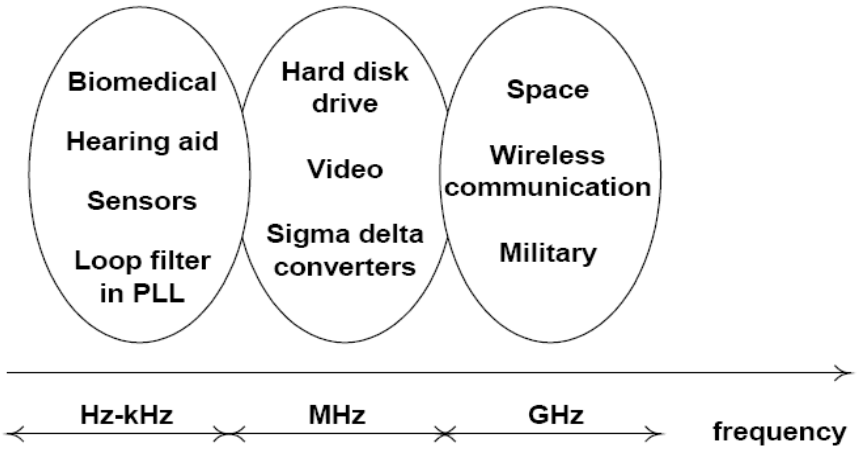


Figure 1.2 Applications of Filter

Active-RC filters have been widely used in low-frequency applications for a long time [5-16]. Discrete active-RC are filters also successful substitutes for passive-RLC filters at low audio frequencies for reasons of size and economy. However, they were found less suitable for high-frequency applications and fully integrated implementations due to the high frequency limitations of op-amps and the large chip area requirements of resistors. Consequently, many alternative active filter circuit topologies have been developed to overcome these drawbacks, for example the popular switched-capacitor filter.

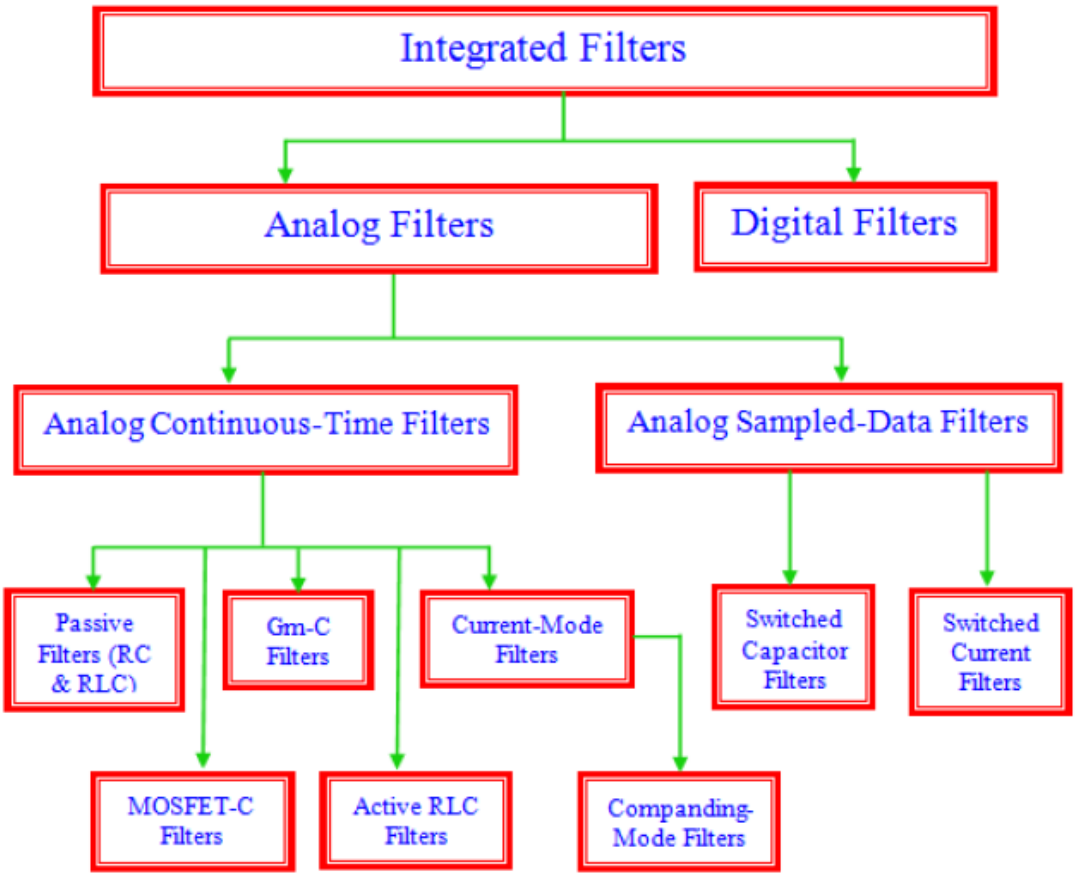


Figure 1.3 Classification of Integrated Filter

In switched-capacitor filter structures, MOS switches and capacitors effectively replace the resistors in active-RC filter structures. Nowadays, switched-capacitor filters can be fully integrated using all available IC technologies especially CMOS. In addition, precision frequency response is achievable without on-chip tuning, and high dynamic

range can be achieved. However, they are still not suitable for very high frequency applications due to the sampling mode of their operation, which would require very high clock speeds, along with the use of extra continuous-time (CT) input anti-aliasing filters and output smoothing filters.

CT filters based on the operational transconductance amplifier (OTA) (also referred to as V-I converter, transconductor, or transconductance amplifier) and capacitors, the so-called OTA-C, or gm-C, filters have received the greatest interest and attention in recent research [17-20]. OTA-C filters offer advantages over traditional active-RC filters in terms of design simplicity, high frequency capability, electronic tunability, suitability for monolithic integration, reduced component count, and potential for design automation. Although OTA-C filters are primarily aimed at high frequency operation (up to GHz range), they are also suitable for applications at low frequencies. Also, fully integrated OTA-C filters have been widely used in communication systems. The performance of a filter relies strongly on the circuit components, filter structure, design methods, and IC technology used. In particular, different circuit components and IC technology can result in very different performances for the chosen filter topology. The design of a high performance OTA-C filter is a complex task. It must simultaneously optimize different requirements, such as operating frequency range, power consumption, noise and dynamic range, sensitivity to device variations and fabrication tolerances, chip area, and cost. A number of IC technologies such as Bipolar, BiCMOS, and CMOS [21-29], GaAs, etc have been used for integrated filter design.

In most practical CT filters, an on-chip automatic tuning system is incorporated to overcome performance degradation due to device variations,fabrication tolerances as well as the effects of parasitics, temperature, and environment changes. Moreover, using the right filter structures can also reduce sensitivity. Low supply voltages have adverse consequences for active filter design. As the supply voltage shrinks, the linear signal range of the active devices also decreases. Consequently, the available dynamic range (defined as the ratio of maximum over minimum signal level) is reduced. The minimum

signal is restricted by noise, which is generated by active devices and resistors, and does not show a corresponding reduction at lower supply voltages.

Motivated by the rapidly growing mobile and wireless communication market, fully integrated filters for very high frequency and low power consumption have received worldwide attention. The most important filters for fully integrated high frequency applications are perhaps the OTA-C filters, which have been widely utilized. Design of high-order OTA-C filters based on the cascades of biquads, LC ladder simulation, and multiple loop feedback (MLF) methods have been explored. OTA-C filters also have significant limitations. Good overall linearity of the transfer function of OTA-C filters is only achievable with highly linearized OTAs. Increased linear range will unavoidably decrease the available range of transconductances of the OTAs at a given supply voltage, and increase OTA noise. As with other types of active filter, errors in the desired filter response may occur at high frequency, due to excess phase caused by device and layout parasitic at high frequencies. In common with other integrated filters, errors in filter response may be caused by device tolerances, process, and temperature and bias effects. Overcoming this problem requires the use of on-chip tuning circuits in most applications.

1.2 The role of IF filters in wireless receivers

Nowadays, wireless receivers for mobile phones mainly utilize the super-heterodyne structure to achieve good selectivity and to avoid the problem of DC offset in homodyne (Direct-down) receivers. IF band pass filters are then needed for the channel selection and Filtering. A simple block diagram of a wireless receiver is shown in Figure1.4. Most transceivers still use external filters such as surface acoustic wave (SAW) filters for IF filtering. The advantages of using external filters, especially SAW filters, are their high Q, stable center frequencies and no extra power is needed for operation. But in order to drive the 50Ω input impedance of these off-chip filters, much power (hundreds of mW) has to be supplied for the drivers. More noise is coupled into the external connections too. This

motivates the design of monolithic receivers with on-chip filters to avoid the extra power consumption for driving the 50Ω load and also to minimize noise coupling.

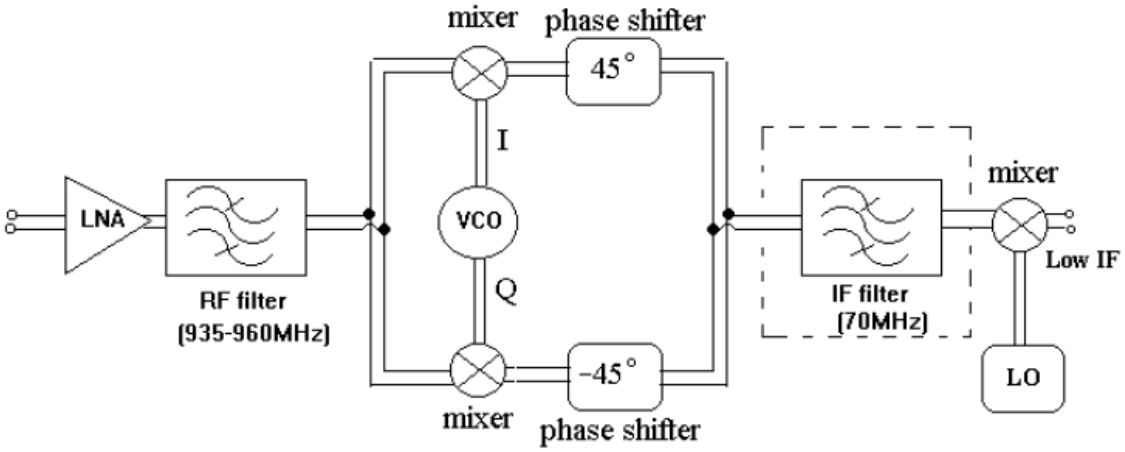


Figure 1.4 Basic Structure of Superhetrodyne Receiver

1.3 Scope of Work:

Today's transceivers employ a number of discrete filters; take up a large portion of space, and increasing the transceiver's overall size. To reduce the size, these filters need to be integrated on the same Silicon. In addition to area reduction, filter integration offers other advantages. The cost of an RF transceiver will be reduced because fewer external components will be required. Power dissipation will also be reduced, as RF signals do not need to travel off-chip thru package pins to an external filter. Signals traveling off-chip need to drive the large capacitances associated with the package pins and printed-circuit board and hence cause additional power consumption. In addition, integrating filters on-chip reduce the number of pins and thus the package can be smaller and less expensive. Finally, filter integration offers increased design flexibility. Also, filter impedance, which is typically 50 ohm to match the external standard, can be chosen during the design process to optimize RF performance.

Continuous-time filters implemented with transconductance amplifiers and capacitors known as Gm-C Filter or OTA-C Filter is best to design Intermediate Frequency (IF) filters in RF Receivers. Rapidly growing Mobile and Wireless communication market, fully integrated filters for very high frequency and low power consumption applications have received considerable attention. In most practical Continuous-time filters, an on-chip automatic tuning system is incorporated to overcome performance degradation due to device variations and fabrication tolerances as well as the effects of parasitics, temperature, and environment changes.

The scope of this research project involves research studies to realize CMOS Folded Cascode OTA and Implement on chip High frequency gm-C IF Filter for Dual Band (FM Band and GSM Band). The design is characterized to layout level based on TSMC 0.18 μm process technology.

1.4 Organization of Thesis

The thesis mainly concentrates on the design of Gm-C IF filter for Dual Band Receiver. The implementation of fully integrated, high-selectivity filters operating at tens of MHz provides benefits for wireless transceiver design, including chip area economy and cost reduction. The Operational Transcondutance Amplifier-Capacitor (OTA-C) technique is a popular technique for implementing continuous time filter and is widely used in many applications.

Chapter I give a very brief introduction about classification of integrated filter and role of IF in wireless receiver.

Chapter II discusses the background of analog continuous time filters. In this chapter, receiver architectures are briefly reviewed and requirements of continuous time channel selection filters are discussed. The most popular continuous time filters are briefly introduced and design requirements are also discussed. This chapter provides a general

review of CMOS OTAs. Three types of CMOS OTAs with different input/output configurations were described first, followed by current trends on high frequency, high linearity, and low power CMOS OTAs.

Chapter III discusses the basics of analog circuit design. The fundamental small-signal models and hand-calculation formulas are presented. Also, some important performance metrics in analog design are discussed.This chapter introduces Operational Transconductance Amplifiers (OTA), their different topologies, N-channel and P-channel differential amplifier, used in folded cascode OTA, with its small signal equivalent and parasitic capacitance. Practical folded cascode OTA is designed in TSMC 0.18μm CMOS technology and its pre-layout and post layout simulations are carried out. Cascode current mirror base folded cascode OTA simulation is carried out for getting large input-output swing.

Chapter IV focuses on the Gm-C IF filters for dual band (FM and GSM). First order and second order filter are designed with analysis. Because OTA-C filters are based on integrators built from an open-loop transconductance amplifier driving a capacitor, they are typically very fast but have limited linear dynamic range. This chapter presents the design of a dual band band-pass channel selection IF filter to be used in a direct conversion receiver for FM band and GSM band. Gm-C IF filter for dual band is designed in the TSMC 0.18μm CMOS technology and pre layout and post layout simulation is carried out. A unique Analog-Digital automatic tuning system is also implemented.

Finally, Chapter V summarizes the main contributions and summary of this research work with future enhancements

Chapter 2

Literature Review

2.1 Motivation

As various wireless communication systems emerge, average consumers want smaller and lower price mobile sets. A lot of research efforts have been dedicated to make standard CMOS technology applicate to System-on-Chip configuration (SoC). SoC is highly wanted by wireless Industry since it reduces the area of transceiver and price of product. For Integrated circuit technology(IC) integrating all analog circuitry on a single chip is very difficult. High frequency filters are still realized with discrete components in wireless communication systems because the required selectivity is infeasible with current integrated circuit (IC) technology. These discrete filters are not only expensive but are increasing the loss in the receiver chain.

To increase the integration rate of the analog circuitry, the use of discrete filters must be minimized; so as to achieve such goal minimum number of high frequency filters should be used. Number of external components and problem of power consumption can create major impact in radio architecture design [30]. Among so many types of receiver architecture available, the number discrete filter can be reduced and integration of analog filter is easy but other problems may arise. For example in direct conversion architecture channel selection is done at base band level(RF to direct baseband) with all intermediate frequency(IF) filters are eliminated, but this direct conversion architecture is susceptible to DC offset and flicker noise.

In low frequency, the integration of analog filter is feasible because the required selectivity is low but many difficulties arise in such integration because of limited

dynamic range (DR) and unwanted variation. Most low frequency range filters are based on operational amplifier (Op-amp) or operational transconductance amplifier (OTA). Since the active components are only linear in certain frequencies and signal range, there is a problem of dynamic range and linearity of filter with the use of active components. Tuning circuits must be used to compensate the frequency shift because integrated filter are sensitive to process and temperature variations. The tuning circuits sometimes affect the dynamic range (DR).

As wireless communication systems are required to process high data rate signals, baseband analog filters must have wide bandwidths, while maintaining high linearity, low noise, and low power consumption. In wide bandwidth system, it is not easy to achieve high linearity and low noise with low power consumption since linearity and integrated noise are increased with power consumption and bandwidth respectively. As the bandwidth increases, design of baseband filter is more complicated. Wide bandwidth filters are only possible when the active component achieves wide gain bandwidth, high linearity, and low noise.

The motivation of this thesis is to investigate and propose simple and robust CMOS Continuous time filter for Dual-band receivers. The analog continuous filter is essential block in the wireless communication system.

2.2 Analog Baseband Filter in Wireless Communication

Analog baseband filters can be divided into two different kinds: sampled data filters and continuous time filters. Sampled data filters are accurate and not sensitive to process variation. Because of the high clock frequency and settling time requirement of the amplifier, sampled data filters are not used in wideband signal processing. In contrast, continuous time filters are widely used in wideband signal processing, but they are very sensitive to process and temperature variations. The design and performance of continuous time filter is the main bottleneck in improving the performance of receiver

[31]. Due to problem of frequency variation, mismatch, and phase error in the baseband filter, performance of receiver is often limited

Nowadays, wireless communication systems are required to process not only high data rates but also multi-standard information. The reason for this is that second generation and third generation cellular phones or WLAN and Bluetooth will coexist for some time [32]. This implies that the filter in the receiver must have wideband cut-off frequency and multi-standard capability. High gain bandwidth is usually achieved at the expense of high current consumption, which is the main reason for the increase of power consumption in the filter. Multi-standard capability is usually obtained with parallel connection of passive components with switches. Since the bandwidth of different standard is determined by digital signal processor (DSP), programmable switches must be implemented to change the bandwidth.

There are still many problems in achieving wideband continuous time filter. Linearity is the main problem because desired signals are blocked in wideband filter due to inter-modulation products of two in-band signals. Parasitic near the cut-off frequency degrades the linearity and also increases the time constant of the filter. Since the size of passive components used in the filter is getting smaller as the filter bandwidth increases, mismatch or process variation of the passive components is more critical to the variation of the filter's time constant. Therefore, integration of wideband filter requires additional time for post design tuning.

2.3 Channel Select Filtering and Tradeoffs

The filter circuit used in any application can be of three different types depending on the type of signals handled. The general types of filters used in most applications are digital filters, continuous-time filters (Analog) and sampled-data filters.

2.3.1 Digital Filters

A digital filter [33] uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP chip. The analog input signal must first be sampled and digitized using an ADC. The resulting binary numbers, representing successive sampled values of the input signal, are transferred to the processor, which carries out numerical calculations on them. These calculations typically involve multiplying the input values by constants and adding the products together. If necessary, the results of these calculations, which now represent sampled values of the filtered signal, are output through a DAC (digital to analog converter) to convert the signal back to analog form. In a digital filter, instead of voltage or current sequence of numbers represent signal. Such setup of basic digital filtering process as shown in Figure 2.1 that combines the anti-aliasing filter and ADC together and the reconstruction filter with DAC to focus more on the digital filtering block.

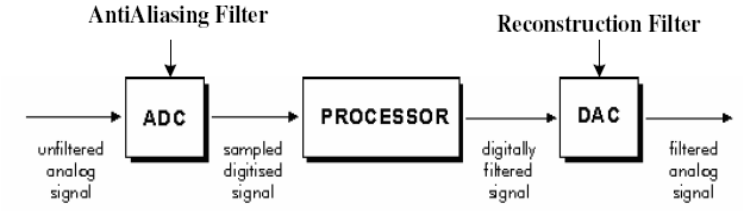


Figure 2.1 Digital Filtering Processes

2.3.2 Sampled-Data Filters

Sampled-data filters do not work with the digital representation of the signal samples, but operate on samples of the signal. Both the digital filters and sampled data filters are discontinuous in time but continuous in processed data value. Both the digital and sampled data filter are characterized in Z-domain. The best-known example of such an approach is that of switched-capacitor (SC) filters. An SC filter is a continuous-amplitude, sampled-data system. This means that the amplitude of the signals can assume any value within the possible range in a continuous manner. On the other hand, these values are assumed at certain time instants and then they are held for the entire sampling period. Thus, the resulting waveforms are not continuous in time but look like a staircase. Figure 2.2 describes how an input continuous time signal can be sampled. The sampling

operation extracts from the continuous-time waveform the values of the input signal at the instant *n·Ts (n = 1,2,3, …),* where *Ts* is the sampling period *(Ts = 1/Fs).*

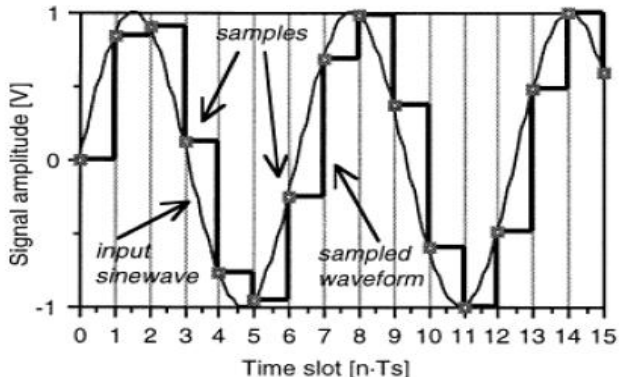


Figure 2.2 Sampling of Continuous Time Signal

The switched capacitor filter can be used in an application [34]-[35] similar to those shown in Figure 2.1 and Figure 2.2. Figure. 2.3 show the usage of SC filter in the standard application example. Due to the sampling operation involved, continuous-time (CT) anti-aliasing filter and reconstruction (smoothing) filter are requiring switched-capacitor systems.

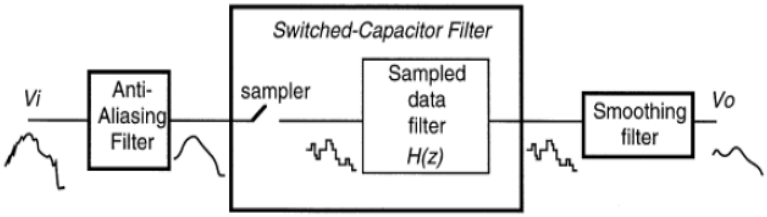


Figure 2.3: A Switch Capacitor Filter Application

2.3.3 Continuous Time Filters

An analog filter is any filter, which operates on continuous-time signals. In particular, Linear Time Invariant (LTI) analog filters can be characterized by their (continuous) differential equation. Instead of a difference equation as in digital and SC filters, analog filters are described by a differential equation. Instead of using the *z* transform to compute the transfer function, CT systems use the Laplace transform. In the real world, analog filters are usually electrical models, or ‘‘analogues", of mechanical systems

working in continuous time. If the physical system is linear and time-invariant (LTI) (e.g. consisting of elastic springs and masses which are constant over time), an LTI analog filter can be used to model it. Before the widespread use of digital computers, physical systems were simulated on so-called ``analog computers." An analog computer was much like an analog synthesizer providing modular building blocks (``integrators") that could be patched together to build models of dynamic systems.

Filters can be also be categorized according to the relative size (depending on the frequency of operation) of the elements used with respect to the wavelength of the signal into two categories: Distributed [36] and Non-distributed filters. In a non-distributed [37] (lumped) filter, the physical dimensions of the used elements (resistance, inductance, or capacitance) are negligible compared to the wavelength of the fields associated with the signal. Thus they are simple elements concentrated within the boundaries of the corresponding physical element. This is in contrast to the distributed filter, in which the physical elements have dimensions comparable to the wavelength of the fields associated with the signal and hence it is represented by a combination of physical elements.

2.3.3.1 Continuous Time Analog Filters

The main focus of this research is the design issues of continuous-time integrated filters. High frequency continuous-time filters have been widely used in various applications, in cases where high speed and low power dissipation are needed. Those applications include video signal processing [38], hard-disk drive read channels [39], loop filters for phase-locked loops [40], and radio frequency wireless communication systems [41]. The low frequency applications are in the bio-medical applications [42] like Hearing-aid and also for seismic systems [43].

Digital filter is not feasible for high frequency applications because they are very power hungry at high frequencies, i.e., $power = f_{clock} V_{DD}^2 / 2$. Although switched capacitor filters can have good linearity and dynamic range properties, they are not suitable because of their limited ability to process high frequency signals due to the sampling operation. The

sampling frequency should be chosen larger than the filter bandwidth to avoid inaccurate filter frequency response. That requires the use of operational amplifiers (Op-Amps) with very wide bandwidths,to provide proper settling, demanding large currents; it is required that the unity gain frequency of the used operational amplifier be at least five times larger than the clock frequency used. Another bottleneck is the inability of real switches to operate at high frequency and at low voltages. Thus continuous-time filters become the only option in these types of applications. Continuous-time filters are divided into two main categories: Passive filters and Active filters. All the components of passive filter are passive. Therefore, a passive filter may include among its elements resistors, capacitors, inductors and transformers. If the elements of the filter include amplifiers or negative resistances, this is called active.

2.4 Receiver Architecture

Earlier radio receiver cannot utilize frequency translation because they detected signals directly from radio frequency (RF), however such signal detection is not possible in modern radio receiver. Because the modulation schemes are used to deliver information effectively, a radio receiver must select a certain frequency band and translate the band to another frequency to detect the transmitted information [44]. Modern communication system is designed for efficient use of radio bandwidth. Received signal may contain adjacent channels, which have higher level of power than desired channel.

As an example, Figure 2.4 shows the GSM specification for the possible power levels of the nearby channels as a function of frequency offset. If the adjacent channel which is 600 kHz offset from the desired channel must be attenuated by 10 dB below the desired channel to detect the information, the adjacent channel must be attenuated by 65 dB according to the Figure 2.4. Since the desired channel is -98 dBm, the power of adjacent channel, -43 dBm, should be attenuated to -108 dBm. In the case of GSM, the desired channel has a bandwidth of 200 KHz with center frequency 900 MHz; the required filter must have a quality factor (Q):

$$Q = \frac{900MHz}{200KHz} = 4500$$

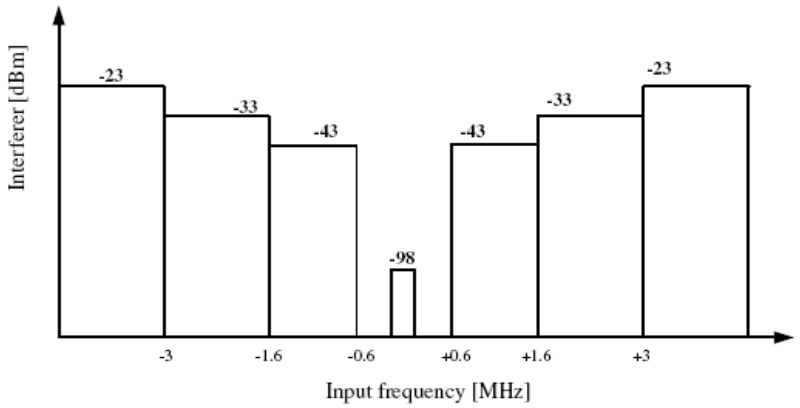


Figure 2.4 Power Level of different channel

This is not possible to realize with current technology [44]. The solution for this problem is to translate the frequency to lower or zero frequency for easier detection with feasible filters. In modern receivers, detection of information is usually done in low IF or zero IF. The analog filters in low IF or zero IF separate the desired channel from unwanted ones and surrounding interferers, which may be orders of larger than the desired signal. Accomplishing the same job without analog filters would require analog to digital converters (ADCs) with much larger number of bits to properly digitize and process large interferers [31]. Therefore, analog baseband filters are needed for the proper detection of the desired signal in radio receivers [45].

Analog channel selection filter's specifications are highly affected by receiver architecture. Therefore, it is important to understand the requirements of receiver architectures for the effective design of analog filters.

2.4.1 Superheterodyne receiver

A superheterodyne receiver removes the image component by filtering before each down conversion stage [46]. When the radio frequency(RF) signal is down converted to a non-zero intermediate frequency(IF), the image component which is at the same frequency offset from the local oscillator(LO) as the desired RF signal, but on the other side of the LO, is mixed to the same IF(Intermediate Frequency) as the desired signal. Before frequency translation, image frequency must attenuate by image rejection filter otherwise from desired signal, image frequency component cannot remove.

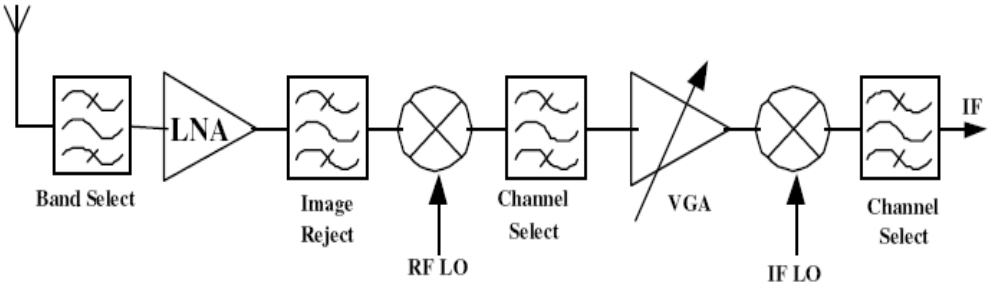


Figure 2.5 Superhetrodyne Receiver

First, a passive off-chip pre-select filter attenuates the signal outside the desired system band [47]. This filter suppresses out-of-band signals and thus reduces the dynamic range requirements of the next stages. It is desirable to suppress out-of-band signals as much as possible, but there is a tradeoff between stop band attenuation and pass band insertion loss [48]. The insertion loss of this filter is important because it directly adds to the receiver noise Figure. Usually, the band select filter is realized as a ceramic or a surface acoustic wave (SAW) filter. Above 1GHz, Ceramic filters are often preferred because of less insertion loss [48]. A low noise amplifier follows the preselect filter. The low noise amplifier (LNA) input must be matched to a specified impedance level, typically 50Ω, since the impedance matching is part of the preselect filter [47]. After the LNA, mixer converts the desired channel to a fixed IF.

The first IF frequency must be chosen carefully to allow the image at any possible LO frequency to lie outside the system band and to be attenuated enough by the pre-selection filter [44]. The first IF in a superheterodyne receiver must be given as:

$$f_{IF1} > \frac{B}{2}$$

----------(2.1)

where B indicate the bandwidth of the pre-selection filter. A high intermediate frequency relaxes the requirements on the preceding filter, but places higher demands on the circuitry of the subsequent IF stage. If the received radio frequency is very high when compared to the available filter technologies, it might be impossible to filter the signal. Such problem can be overcome by filtering and down converting several times. The number of down conversions depends on the frequency planning and on the selectivity of the filters. However, every down converting generates a new image frequency which must be rejected before the mixing, and the successive stages usually add a lot of noise which significantly impact on the dynamic range of the receiver.

After the down-conversion mixer, a passive off-chip channel-select filter attenuates the adjacent signals to a sufficiently low level. Therefore, the linearity requirements of the subsequent stages are drastically decreased. The first IF is typically between 30MHz and 100MHz [47]. The selection of the IF requires a trade-off. If a high IF is chosen, a less selective image-reject filter is sufficient at RF, but the required selectivity of the IF channel-select filter is increased. On the other hand, if a low IF is selected, the requirements for the channel-select filters are relaxed at the expense of tighter specifications for the RF filters. In most applications, the channel select filters cannot be implemented on chip with active components [47]. Therefore, power consumption is increased because input and output of the channel select filter should be matched to low impedance level. The channel-select filtering is usually divided between one or more IF filters and analog or digital base band filters. A variable-gain amplifier (VGA) decreases the dynamic range requirements of the following stages. After the first IF, the signal can be down converted to another IF or to DC using quadrature down conversion. The signal may also be sampled and digitized if the IF is sufficiently low. More than one IF can be used to divide the channel-select filtering and amplification between several stages.

The superheterodyne receiver architecture has dominated the field for decades since it offers an excellent performance [44]. The excellent sensitivity and selectivity come from the use of passive, highly linear off-chip filters. These filters provide a sufficient image rejection and selectivity at IF. The problems related to DC offsets and flicker noise can be avoided since the signal can be processed at an IF far from DC.

2.4.2 Direct Conversion Receiver

A direct conversion receiver converts the carrier of the desired channel to the zero frequency directly [46]. The direct conversion receiver is an alternative solution to the image rejection problem. The intermediate frequency is moved to DC making the desired channel an image of itself. Consequently, no image rejection filter is needed prior to mixing. Compared to superhetrodyne receiver, the direct conversion receiver implements external IF filters. The IF stages and the passive IF filters are eliminated so that the integrability of the direct conversion receiver is much higher than the super heterodyne. Furthermore, the direct conversion receiver is suitable for the multi-mode receivers since the bandwidth of the integrated low pass filters can be designed programmable. Figure 2.6 shows the schematic of the direct conversion receiver architecture.

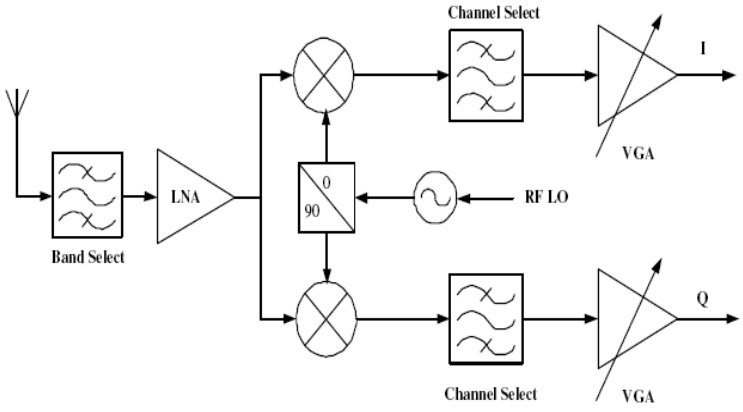


Figure 2.6 Direct Conversion Receiver

Two down conversion mixers must be used for demodulation at RF if a signal with quadrature modulation is received [46]. The pre-select filter is used to attenuate out of band signals before the LNA. Since there is no problem with image signal in the direct conversion receiver because the off-chip filter between LNA and mixer is not required.

Therefore, the output of the LNA drives on-chip load so that only input matching in the LNA is required. Also, a low pass filter with a bandwidth of half the symbol rate is suitable for channel selection and it can be implemented with an active on-chip filter [46].

The most serious problem of the direct conversion receiver after the down conversion stage is that of DC and time varying offset voltages [46-48]. Since the down converted band extends to zero frequency, static and time varying offset voltages can corrupt the signal [47-48]. The dc offset must be minimized to avoid the signal saturation. Even though automatic gain control can prevent the saturation of the incoming signal, the amplification will be very small. In such cases detection of a weak signal will be very difficult. If the offset is not removed, the DC offset component can be considered as in-band interferer.

One source of offset voltage involves transistor mismatches in the down converter and following baseband stages [48]. Such kind of offset voltage is constant and other dc offsets from the self-mixing of the local oscillator signal. This is caused by the leakage of local oscillator signal to the input of the mixers, which mixes with itself and produce a constant dc offset [48]. If local oscillator leak directly to the RF port of the mixers or to the input of LNA, the dc offset problem will be more serious [47-48]. The leaked local oscillator signal can also propagate to antenna because of the finite reverse isolation of the LNA and pre-selection filter and reflect back from the interfaces having mismatch. If the local oscillator radiates from the antenna and reflects from other objects back to the receiver, the offset due to self-mixing varies in time [47-48]. Figure 2.7 shows two cases of self mixing.

In case of Figure 2.7 (a) the local oscillator is mixed with itself, produce an offset voltage at the output of the down converter. This voltage is typically orders of magnitude larger than the desired signal, and if not removed, will cause saturation in subsequent stages [48]. As the antenna surroundings change over time and as leakage local oscillator reflect

from nearby moving objects, the local oscillator signal at the RF port of the down converter may vary with time and generate time varying offset voltage [48].

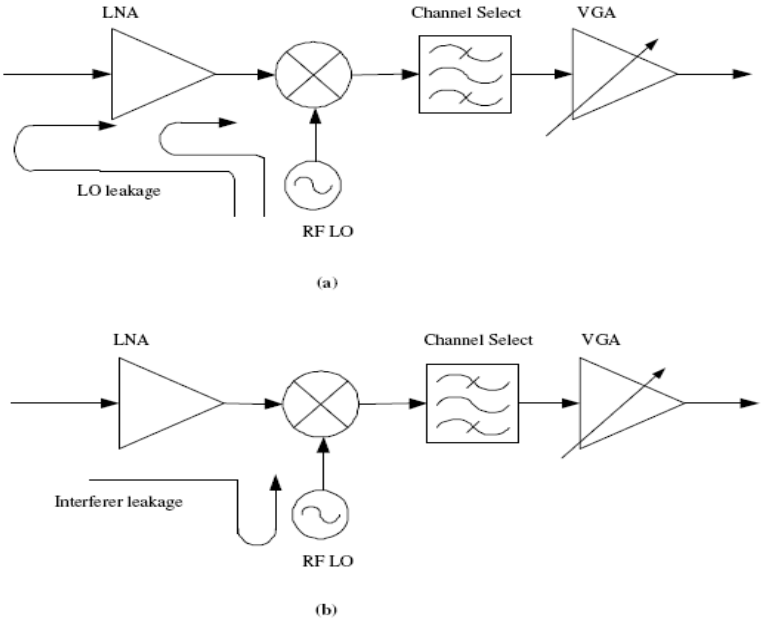


Figure 2.7 Two Different cases of Self Mixing

The other source of time varying offset voltage is self-mixing of a strong interfering signal as shown in Figure 2.7 (b). For example, the leakage signal from the transmitter itself mixed and creates a distorted signal at the baseband. This distorted signal will vary with time due to both the amplitude modulation of the transmitted signal and due to the power control in the up-link [47-48].

With better circuit design, magnitude of offset voltage can be reduced. Implementation of high pass filter or DC servo loop can remove the dc offset. However since the substantial information is contained at low frequency, the cutoff frequency of the high pass filter must be very low. This means that the capacitor in high pass filter must be very large.
Then the settling time of the filter will be slow that the high pass filter cannot remove the fast time varying dc offsets. The absence of passive IF filters places very stringent requirements on the active baseband filters. Both the linearity and the noise must be much lower than in a superheterodyne receiver as there is no significant amount of filtering or amplification in the IF. However flicker noise is high around dc and dc offset

is always present. Also mismatches between I and Q phase signal path cause significant problem. So the design of channel select filter in the direct conversion receiver should be done carefully.

2.4.3 Wide-Band IF receiver

Wideband IF receiver down converts a group of channels simultaneously [48] as shown in Figure 2.8. In most wide-band IF receiver, simple low pass filters are used at IF to suppress higher frequency components, allowing all channels to pass the second stage of down converters, where the required channel is converted to low intermediate frequency [48]. The second mixer and latter stages constitute a low-IF receiver [48]. A benefit of the wide-band architecture is the adaptation of a high IF in which the image is outside the pass band of the pre-selection filter. Another advantage of the wide-band IF receiver is that it eases full synthesizer integration [48]. The fixed frequency RF local oscillator is easier to implement, since a crystal controlled wide-band PLL with a high phase detector frequency can be used to clean up the phase noise spectrum of the VCO [48]. The requirements for high Q components are thus relaxed. The wide-band IF architecture uses the same frequency selection criteria as the first IF super heterodyne architecture. If the second mixer stage does not convert the signal directly down to base band, the secondary image can be a problem. However, most wide-band IF architecture use a zero IF after the mixers. As shown in the Figure 2.8, the low pass filters between the mixers are only necessary to suppress the up converted product generated in the first down conversion [46]. The channel selection filters are placed after the second down conversion. Typically, the limited output bandwidth of the RF mixers together with the interconnection to the second mixing stage attenuates the high-frequency products without any extra components [46]. In this architecture, the local oscillator to RF leakage is less important because the first local oscillator is outside the pass band of the preselection filter like in super heterodyne. The wide band IF topologies transfer the typical down conversion problems of a direct conversion into the second mixer stage [48], [46]. The distortion generated around dc in the first mixer is not significant because the portion, which passes the possible ac-coupling between the stages, is mainly up converted in the second mixers.

The most critical blocks are the second mixers which can handle all radio channels passing through preselection filter.

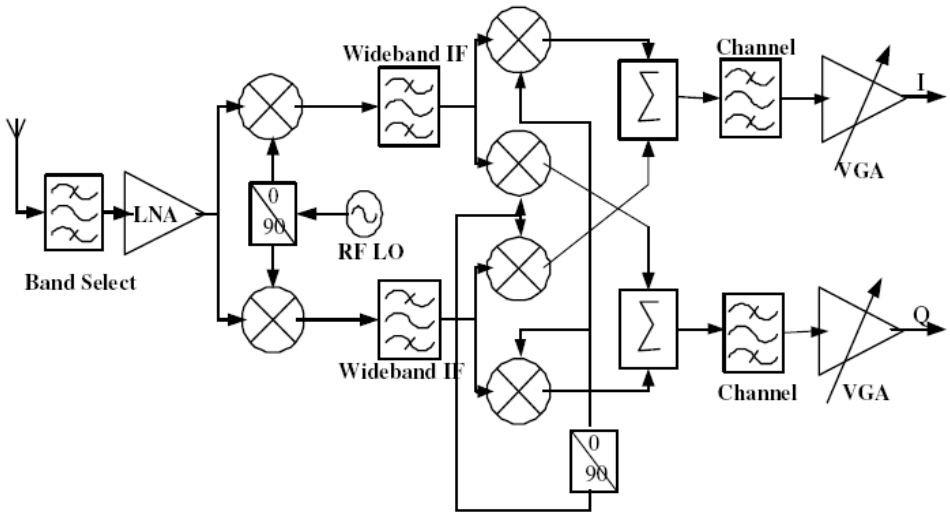


Figure 2.8 Wide Band IF Receiver

2.4.4 Digital IF receivers

Digital signal processing would provide significant benefits compared to analog circuitry [46]. When the down conversion to base band is performed digitally, dc offset, flicker noise or matching problems can be eliminated. However, due to the resolution or increased power consumption and sampling rate of ADC, direct RF to digital conversion is impossible with current technology. But low frequency operations, such as the second set of mixing and filtering in the dual IF heterodyne conversion, can be performed more efficiently in the digital domain. Figure 2.9 shows the digital IF receiver. In this Figure, the first IF signal is digitized, mixed with the quadrature phases of a digital sinusoid, and low pass filtered to yield the quadrature base band signals [49]. Problem of mismatch in I and Q is avoid by digital processing [49]. The issue in this architecture is the requirement of ADC. ADC dynamic range must be wide enough to handle the signal variations caused by path loss. Also band pass filter should have wide signal handling capability, dynamic range (DR) and need to suppress adjacent channel interferers effectively. Since the power consumption and requirement of ADC is too high for the mobile set receivers, this Digital IF receiver architecture is mainly used in the base station [49].

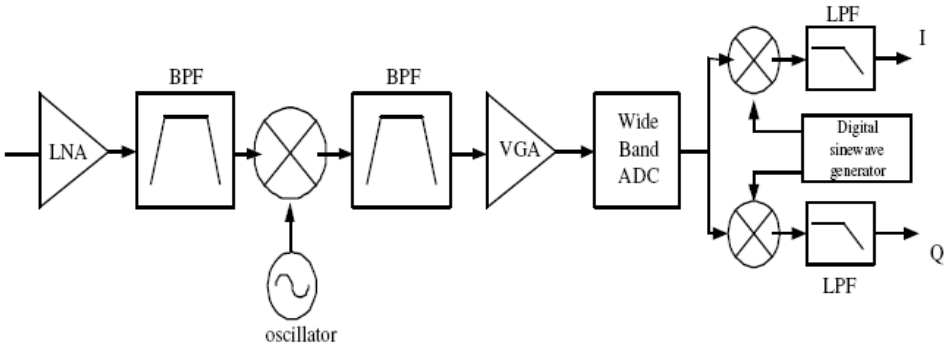


Figure 2.9 Digital IF Receiver

2.5 Channel Selection Filters

Channel selection filtering is dependent on the receiver's ability to suppress the adjacent channel interference and in-band blocking level. Received signal contains not only the desired channel but a multitude of neighboring channels or other interferers which must be attenuated before the detection [44].

The channel filtering can be done at an intermediate frequency, at base band or even over the A/D interface. In super heterodyne receivers, the channel filtering is performed at the intermediate frequency (IF) with a passive filter [44]. The passive filter is very linear and reduces the interferers without corrupting the desired signal. However, the passive filter must be used externally so it is not suitable for system on chip configure ration. In direct conversion or wide-band IF a receiver, the channel selection filtering is performed at the base band. The required quality factor of the filter is not high so that the channel selection filters can be integrated with other receiver blocks. However, the linearity requirement of the filter is high because adjacent channel interferers are unattenuated so that the filter must suppress the interferers without the production of significant intermodulation products [50].

When designing the channel selection filtering partition the filtering between the analog and the digital domain is main issue. Generally it is preferable to realize as much filtering as possible in the digital domain because this reduces the analog complexity. However, the penalty of pushing more filtering into the digital domain is that the requirements of ADC and digital complexity increase.

2.5.1 Channel Selection Filtering and ADC requirements

In modern communication system, the signal is eventually converted to a digital representation. Therefore, analog to digital converter (ADC) should be used to convert analog information to digital [47-48]. If the ADC is able to handle every interferers and noise generated by preceding blocks, channel selection can be done in digital domain [30], [47-48]. This is desirable case since digital filters are very accurate and do not require tuning circuitry. Also digital filters are readily integrated together with the front-end of the receiver [44]. However it is very difficult to design the ADC that has extremely high dynamic range (DR) and linearity with low power consumption. Even if the ADC can handle all the interferers, the power consumption would be very high due to the increased resolution requirements since the power of Nyquist rate ADC is proportional 2^N where N indicates number of bits [47]. Thus, this is not recommended for low power mobile receiver. In the other case, channel selection filtering can be done fully in analog domain. Since the channel selection filter in the analog domain reduces the power of interferers, the dynamic range requirement of the ADC is relaxed. As the order of analog channel selection filter increases, the requirement of ADC is more relaxed, but the increased order of analog domain filter increases signal delay and phase distortion [48]. Usually group delay and phase near the cut-off frequency are highly distorted than other region [48], [47], so the distortion should be compensated with extra circuitry such as all pass filter. Moreover, higher order filter increases the complexity of tuning circuit since the quality factor and attenuation rate of the filter are increased. In selecting analog low pass filters for the channel-selection filtering, three important parameters have to be determined: filter prototype function, 3 dB corner frequency, and filter order [48].

2.6 CMOS Continuous Time Filters

In CMOS technologies, the analog channel selection filter design techniques can be classified into continuous filters and sampled data filters [51-52]. The sampled data filters use many non-overlapping clock phases. Among the sampled data filters, switched capacitor filter is very popular. The main characteristics of the switched capacitor filters are determined by a clock frequency and by capacitor ratios [51-53]. The switched capacitor filter is used in low frequency such as audio frequency due to requirements of high speed clocks for switching and settling time of amplifier. In contrast to the sampled data filters, analog continuous time filters directly process analog signals. Owing to the continuous time nature, analog continuous time filters are most suitable for high frequency filtering [50]. A major disadvantage of continuous time filters is that the filter coefficients are sensitive to process and temperature variations along with aging. For this reason, tuning of the frequency is necessary. Regardless of the high sensitivity to the process and temperature variations, continuous time filter is receiving more interest due to fast data processing capability.

For the realization of fully integrated analog filters, there are many things which must be considered.

(I) First, the size of capacitor and resistor should be limited. Since integrated capacitors such as poly insulator poly capacitors or metal insulator metal capacitors occupy a large area so that the size of capacitor must be limited. For example, the capacitance can be expressed by

$$C = \varepsilon_r \varepsilon_0 \frac{A}{t}$$

----------(2.2)

Where A = area of the capacitor, t = thickness, "ε_0 = permittivity = 8.854×10−12F/m.

"ε_r = relative permittivity which is usually equal to 3.78 in CMOS. In CMOS, t is usually equal to 6×10−8m. To get the capacitance of 50 pF, an area of about $(300\mu m)^2$ is necessary [53], [45]. This area is relatively large compared to the area of other active

components. The capacitor also should not be too small because of the effect of parasitic capacitance [53]. Also large sizes of passive resistors often contain huge parasitic capacitances, which highly degrade the linearity of the filter. Therefore, optimum size of capacitors and resistors must be carefully decided.

(II) Frequency response of the filter must be stable. This means that every element in the filter should have accurate and stable values in the presence of fabrication tolerances and temperature variations, but this is almost impossible in an integrated circuit. In the integrated circuit, the ratio between same resistors or capacitors can be relatively accurate, but the absolute values are usually varied by ± 20 % [53]. This indicates that the RC time constant can be varied by ± 40 %. Furthermore, the quality factor of the filter is highly affected by small errors of the phase and component variation. Such process variations require tuning circuits for frequency and quality factor. This extra circuit often becomes a bottleneck in the realization of low power consumption and high dynamic range filter.

(III) Analog continuous time filters must be able to handle large signal because wide dynamic range required in radio receiver for large signal swings. However, these are increasingly difficult to achieve as power supply voltages are reduced and bandwidth is increased.

(IV) Analog IC filters are often located with data converters and digital circuits on the same chip. In this case, noise due to clock or switching is transferred to the analog filters through power supply line. This noise highly degrades dynamic range (DR) and signal to noise ratio (SNR) of the analog filter. Therefore, special design and layout techniques must require minimizing the effect of the noise [53].

In CMOS technologies, Active-RC, MOSFET-C and Gm-C filters are the most popular base band filters for wireless communication. Active RC filters usually apply lossy and lossless integrators to attenuate interferers. MOSFET-C filters have similar architecture

as Active-RC filters with replace passive resistors with a triode region transistor. Gm-C filters use transconductors and capacitors to attenuate interferers. Because of Gm-C open loop nature, it has been used for high frequency application. Each filter mentioned has its own advantages and disadvantages in terms of speed, linearity, and tunability.

2.6.1 Active RC Filter

The most popular continuous time filter is the active-RC filter which provides good dynamic range and low distortion. Thus, active RC filters are still widely used in low frequency application. However, low speed due to the negative feedback makes the filter difficult to apply for high speed wireless communication system. Usually, the gain bandwidth(GBW) of the amplifier for active RC filter needs to be around 20 - 30 times higher than the filter cut-off frequency to minimize phase error and any other non-idealities which occur near the GBW [54], [30], [47]. In the case of WLAN, this implies that the amplifier needs to have 300MHz GBW when the output load is connected. Active-RC filters are mostly applied in low frequency application even though the filters demonstrate superior performance.

Most active-RC filters are designed based on the active-RC integrator. In the active RC integrator, a capacitor is connected in negative feedback to function as the integrating element and a resistor is used to feed current into the capacitor [55]. Figure 2.10 shows the RC-OP amp integrator. If we assume an ideal operational amplifier is used, the relation between the input and output voltage in the s-domain is given by

$$\frac{V_{in}(t)-V^{-}(t)}{R}=C\frac{d[V^{-}(t)-V_{out}(t)]}{dt}$$

----------(2.3)

$$V_{out}=\frac{-1}{RC}\int_{0}^{\alpha}V_{in}(t)dt$$

----------(2.4)

$$V_{out} = -\frac{1}{RC}\int_{0}^{\infty} V_{in}(t)dt$$

----------**(2.5)**

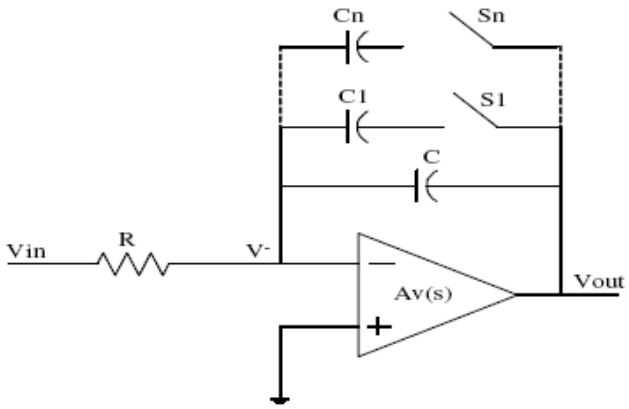


Figure 2.10 RC-OP amp Integrator

In the ideal integrator, the time constant is RC and the phase is 90 degrees. However, non-ideal op-amp gives an impact on the integrator transfer function and quality factor of the filter [55]. Since op amp has finite dc gain ADC and the finite gain bandwidth GBW, the transfer function of the op amp can be expressed as

$$A(s) = \frac{GBW}{S + \frac{GBW}{A_{DC}}}$$

----------**(2.6)**

$$V_{out(s)} \approx \frac{\frac{-1}{RC}V_{in(s)}}{(1+\frac{S}{GBW})(S+\frac{1}{RC}\frac{1}{A_{DC}})}$$

----------**(2.7)**

As an ideal integrator, GBW and DC gain of the amplifier must be infinite or very high [55]. However, it is difficult to obtain high GBW and DC gain at the same time since high DC gain is obtained with a multi-stage amplifier [56]. Therefore, the real integrator only works in a certain frequency range.

In an active RC integrator, the resistor transfers the input voltage into current, and the feedback capacitor integrates the input current because no current flows to the amplifier input [57],[55]. There are basically different integrators: lossy and lossless integrators. Figure 2.10 shows a lossless integrator with binary weighted capacitor array. Adding a resistor in parallel with integrating capacitor, lossy integrators are formed [57]. Usually op-amp is used as an active element, but OTA with high output impedance and large gm can also be used for an integrator [58]. In the ideal case, the active RC filter is insensitive to parasitic capacitance because it is connected to a virtual ground or driven by a voltage source [53]. But due to the limited DC gain, unity gain bandwidth, and output resistance, the parasitic capacitances affect the transfer function of the integrator slightly.

As shown in equation 2.5, with R and C the time constant of the integrator is determined. The time constant typically varies by ±50 %, due to variations in process and temperature. The time constant of an active RC integrator can be tuned using series or parallel capacitor or resistor matrices. The series resistor and parallel capacitor matrices occupy less area [59], [55]. In practice, parallel capacitors as shown in Figure 2.10 are used because the switch on resistance produces a LHP zero without shifting the integrator time constant [55]. The sizes of the switched capacitors are binary weighted in order to simplify the digital control of time constants. Whether the CMOS-switches locate at the input or the output of the amplifier based on the requirements. At the inverting input node, the switch on-resistance has almost no effect on the linearity, but the parasitic capacitances of the switch are added to the inverting input [47], [55]. Alternatively, at the output node, the switch on resistance degrades the linearity, particularly at high frequencies, but the parasitic capacitances of the switches have minimal effect on the performance of the integrator.

In the parallel capacitor array, the limited on-resistance of the CMOS switches used have a minimal effect on the high frequency performance of the integrator since any resistance which is in series with the integrating capacitor has a phase lead at high frequencies [55].

This phase lead reduces the high frequency phase lag deriving from the limited bandwidth of the amplifier [45].

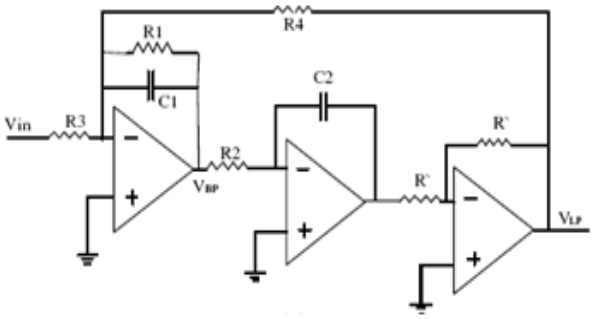
There are many different active RC filters. Among them, Tow-Thomas filter, Ackerberg Mossberg, and Sallen-key filter are the most well known filters. The second order Tow-Thomas and Ackerberg Mossberg filters are usually a combination of lossy, lossless integrators and adder. Adder is simply designed with parallel connection of input resistors at the integrator. Figure 2.11 shows the Tow-Thomas and Ackerberg Mossberg filters. The Sallen-Key filter uses one amplifier, resistors, and capacitors to realize 2nd order filter. Since the structure is simple and only one amplifier is necessary, Sallen-key filters are generally used as antialias filters. Figure 2.12 shows the Sallen-key filter.

2.6.2 MOSFET-C Filter

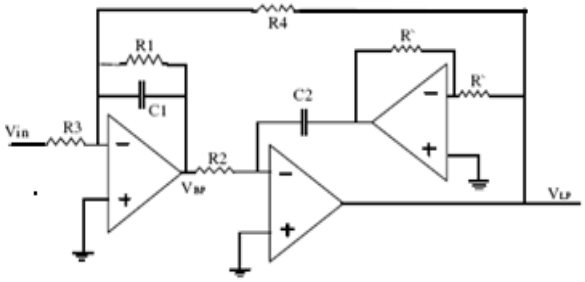
The MOSFET -C Filters are basically active RC filters but in place of resistor, tunable CMOS triode region transistors is placed. [47][53]. so, the time constant can be tuned by controlling the gate voltage Vc [53], [60].

The advantage of the MOSFET-C filter is that the resistance is controlled by a control voltage, V_C, resulting in an extended tuning range as the resistance increases to infinity [50], [61]. However, very high resistance values cannot be used in practice because of device mismatches and noise. In addition, rather high control voltage, V_C is required for the triode region operation of the transistor. Due to this, it is difficult to get large signal swing when supply voltage is low. Moreover, MOSFET-C filtering technique is based on voltage mode op-amp so that high-frequency operation is achieved [52], [60], [61].

The tunable CMOS resistors eliminate the use of capacitor matrices for time constant tuning. However, the triode region MOS resistor produces harmonics when the input signal is increased [53], [51]. Generally, the voltage difference between drain and source, V_{DS} should be smaller than 20 % of the voltage difference between gate and threshold voltage, $V_G - V_{TH}$ [53], for low harmonic components. If $V_G - V_{TH}$ is 1V, V_{DS} should be smaller than 200 mV. However, if a fully differential structure as shown in Figure 2.13 is used, the even order harmonics can be eliminated and increase the linearity [53], [45], [61]. In triode region, small signal current i^+_{DS} and i^-_{DS} are



(a)



(b)

Figure.2.11 (a) Tow-Thomas Filter (b) Ackerberg-Mossberg Filter

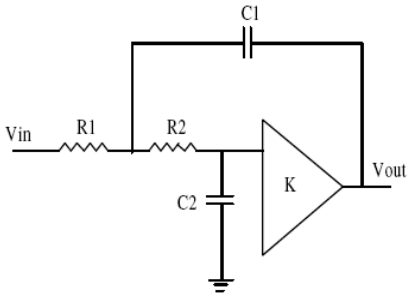


Figure.2.12 Sallen –Key Filter

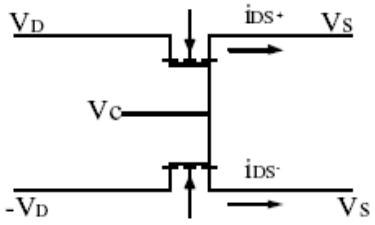


Figure.2.13 Fully-Differential MOS Resistor

$$i^{+}_{DC} = \mu C_{ox} \frac{W}{L}[(V_C - V_{th} - V_s)(V_D - V_S) - \frac{1}{2}(V_D - V_S)^2]$$

----------(2.8)

$$i^{-}_{DC} = \mu C_{ox} \frac{W}{L}[(V_C - V_{th} - V_s)(-V_D - V_S) - \frac{1}{2}(-V_D - V_S)^2]$$

----------(2.9)

$$i = i^{+}_{DS} - i^{-}_{DS} = \mu C_{ox} \frac{W}{L}(V_C - V_{DS})2V_{DS}$$

----------(2.10)

$$R = \frac{2V_{DS}}{i^{+}_{DS} - i^{-}_{DS}} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_C - V_{th})}$$

----------(2.11)

So, the second order equation is cancelled and the current difference is proportional to V_{DS} and controlled by V_C. As long as the transistors are in the triode region, linear resistance can be achieved.

MOSFET-C filter is required with passive resistor which can be replaced with triode region MOSFETs [53][62] but parasitic capacitance of triode region transistor can affect the characteristic of filter. Filter architecture is insensitive to parasitic C_P which can be minimized when it is connected to virtual ground or output of Op-amp [45].Figure. 2.14 show the suitable filter structure for MOSFET-C filter realization. Charge and discharge of C_{P1} by V_S do not affect the performance. Also, the top and bottom plates of C_{P2} are connected to virtual ground and signal ground respectively. Therefore, this parasitic capacitance does not affect the performance. Output parasitic capacitance C_{P3} is connected to low impedance output node so the charge and discharge of the parasitic

capacitance do not affects the filter much. According to Figure 2.14, a Tow thomas filter or a Sallen-key filter is a generally used structure for MOSFET-C filter [53], [63].

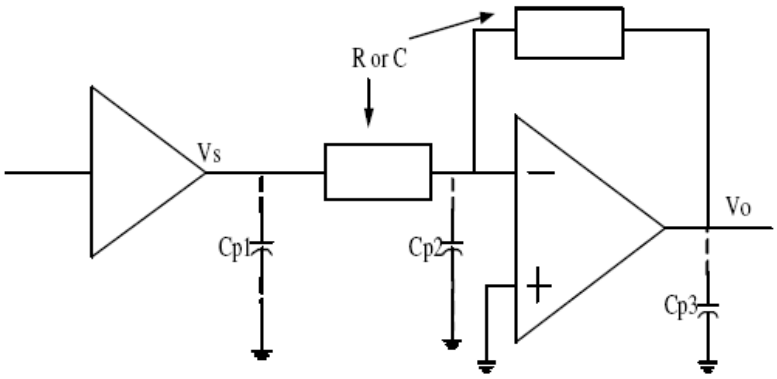


Figure.2.14 Filter Structure for MOSFET-C filter

2.6.3 OTA-C filter

OTA-C filters are more suited to high speed applications as opposed to the active RC and MOSFET-C filters described in the previous sections since they can be used in an open-loop configuration and it need not constrained by the stability requirement [64], [61], [31]. OTA-C filter is generally known as Gm-C filter. OTA is basically different from a transconductor. OTA is an op amp without a low impedance output stage, ideally operating with a virtual ground at its input and whose transconductance value is mostly irrelevant, because its voltage gain is high [61]. A transconductor is a simply voltage controlled current source [61]. However, OTA-C or Gm-C filters usually have identical filter structures and functions, OTA-C filter in this section also includes Gm-C filter.

The drawback of using OTA in an open loop configuration is that the circuit is limited to very small input levels which is required to operate the transconductor in linear region [65], [61]. Even though many different techniques have been reported to increase the

input range while maintaining linearity, these techniques often degrade the frequency response due to additional parasitic [52], [65]. Even with the linearization technique, the input signal swing range is still less compared to the active -RC filters. Another drawback of OTA-C filters is their dependence on the parameter gm which makes them highly susceptible to process variations. This drawback can be accounted by including some kind of automatic tuning [52].

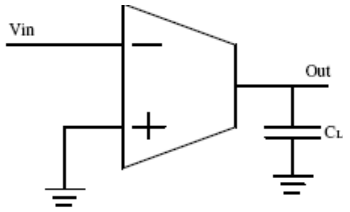


Figure.2.15 Gm-C Integrator

Gm-C integrator is a key block of the OTA-C filter. In a Gm-C integrator, the transconductance (gm) and integration capacitor C determine the unity gain frequency of the integrator. Instead of a simple transconductor, the operational transconductance amplifier (OTA) can be used. Figure 2.15 shows a Gm -C integrator. The input is fed into the transconductor of transconductance Gm and the output current of the transconductor is integrated by a capacitor.

$$V_o(s) = \frac{g_m}{sC_L} V_{in}(s)$$

----------(2.12)

In a Gm-C integrator, the integration is a passive operation because the Transconductor transforms the input signal into another form [44]. So, in case of summing operation, to add N inputs N transconductors required.

Figure 2.16 shows the 1st order OTA-C filters. One advantage of the OTA-C filter is that passive components like the resistor and inductor can be realized with OTA and capacitor [53], [45]. As shown in the Figure 2.16, the resistor is realized by connecting negative input of OTA to positive output and the function of inductor can be realized in certain frequency by using two OTAs and a capacitor. However performance of OTA is dependent on linearity of resistor and inductor, so when high linearity is required passive resistor is used. Figure 2.17 shows the fully differential OTA-C biquad filter. As shown

in the Figure 2.16, low pass and band pass functions can be obtained from the biquad OTA-C. In this filter, the passive resistor is replaced with OTA by negative feedback connection. This filter is 2nd order. For the higher order filter, this biquad filter can be cascaded.

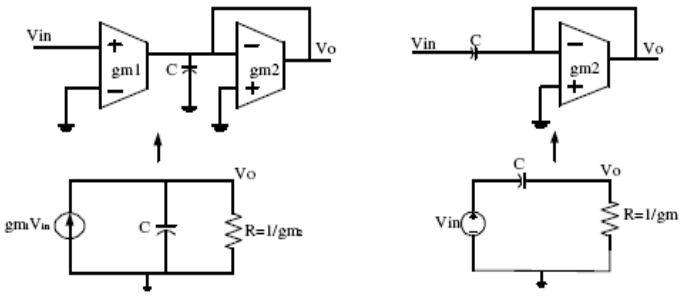


Figure.2.16 OTA-C filter

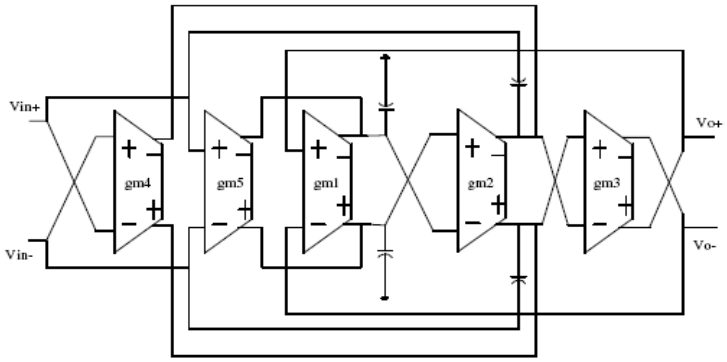


Figure 2.17 OTA-C Biaquad Filter

2.7 CMOS OTAs

CMOS technologies are very convenient for implementing OTAs because their MOSFETs are inherently voltage-controlled current devices. A variety of CMOS OTAs with different topologies have been designed and developed for different purposes so far. According to their input/output topologies though, they can be categorized into the previously mentioned three types, i.e., single input/output, differential-input single-output, and differential input/output. These three types of CMOS OTAs with their advantages and disadvantages are described below.

2.7.1 Single input/output OTAs

Figure2-18 presents some common CMOS topologies [66] to implement the single input/output OTAs. Figure 2-18(a) is a single-NMOS common-source transconductor. Although it is the simplest, it has relatively low output impedance due to its Miller effect (input-output coupling) and low linearity, deviating it from an ideal OTA. To alleviate this problem, a cascode topology in Figure 2-18(b) is suggested, where a common-gate transistor M_2 is introduced to provide isolation between the input and output. This unilateralization method increases not only the output impedance and linearity, but also the bandwidth and the available transconductance, at the expense of a higher voltage supply. The third topology in Figure 2-18(c) differs from the cascode topology in its common-gate transistor, where a PMOS transistor is applied instead of a NMOS one, resulting in a folded cascode topology. It provides the same isolation, but with a reduced voltage supply. Figure 2-18(d) is a regulated-cascode transconductor, which is an enhanced cascode transconductor. It replaces the gate DC bias of M_2 in Figure 2-19(b) with a negative feedback from its source. This feedback further improves the linearity and the output impedance by a factor of *(A+1)* compared to the cascode transconductor, where *A* is the feedback gain. The improvement mechanism behind the cascode and regulated cascode topologies will be further explained in the next chapter. The fifth one in Figure 2-18(e) utilizes a PMOS current mirror to convert a negative transconductor to a positive one.

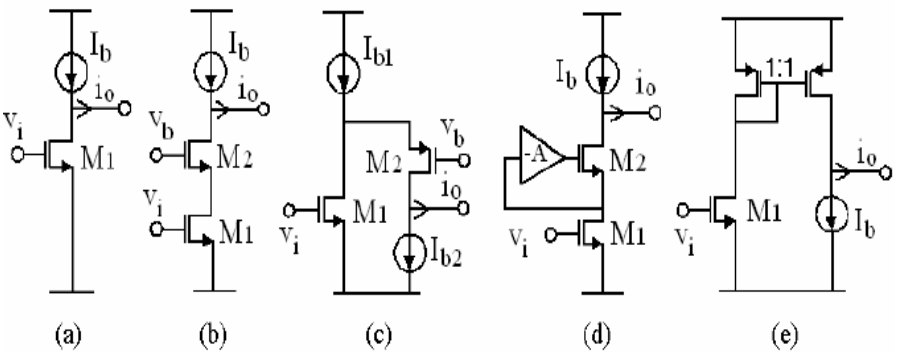


Figure 2.18 Single Input/output OTA [66] (a) Common Source Transconductor (b) cascade Transconductor (c) Folded Cascode Transconductor (d) Regulated Cascode Transconductor (e) Positive Transconductor

Ignoring the parasitic in cascode and regulated-cascode transconductors in Figure.2-18(b), (c), and (d), the output currents of their input common-source transistors (M_1) will propagate to their outputs (i_o) without any loss. Therefore, despite the different topologies of the transconductors in Figure 2-18, their transconductance g_m can be unified, where $g_{m,M1}$ is the transconductance of the input transistor M_1, and V_i and i_o are the input voltage and output current respectively. The sign ± is inserted to discriminate the positive transconductor in Figure 2-18(e) from the other negative ones. The transconductance in (2-1) can be tuned through the control of the DC current of each transconductor above. The more DC current, an OTA consumes, it has large tuning range and transconductance.

$$g_m = \frac{i_0}{v_i} \approx \pm g_{m,M1}$$

----------(2.13)

2.7.2 Differential OTAs

Figure 2-19 depicts two typical CMOS implementations of the second-type OTA with the differential-input single-output topology [66]. They both contain a source-coupled differential-pair input stage, which can provide high input impedance, high gain, and high common-mode rejection simultaneously without much sacrifice. A scrutiny of their signal paths after the input stages reveals the important role that current mirrors play in these two implementations.

In Figure 2-19(a), the current mirror CMp transfers the left output current of the input differential pair, i_d^+ , to the right to combine with its right output current i_d^- ,from which the transconductor output current is twice, so does its transconductance:

$$g_m = \frac{i_0}{v^+_i - v^-_i} = g_{m,M1}$$

----------(2.14)

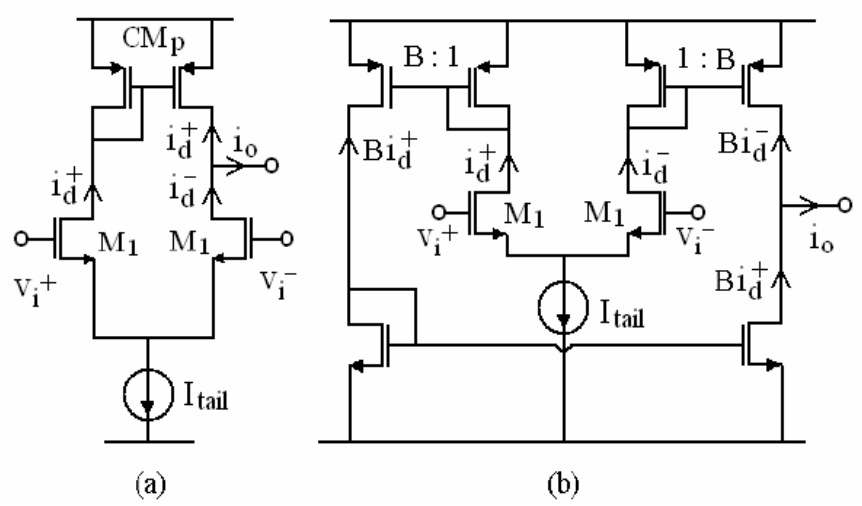


Figure 2.19 Differential Input and Single Output [66]
(a) Simple OTA (b) Balance OTA

The balanced implementation in Figure 2-19(b) is different from Figure. 2-19(a) in that two PMOS current mirrors are added after the input differential pair improves the balance between its differential inputs. Furthermore, these two PMOS current mirrors can be set in such way that they have a size ratio of B between their (i) reference transistor and (ii) controlled transistor. This boosts their output currents by B times [67]. The boosted currents are combined at the output using a NMOS current mirror at the bottom, resulting in a transconductance as large as B times of the previous one's:

$$g_m = \frac{i_0}{v^+_i - v^-_i} = -Bg_{m,M1}$$

----------(2.15)

The transconductance in (2-14) and (2-15) can both be tuned by changing the DC tail currents I_{tail} in Figure. 2-19(a) and Figure 2.19(b). Equations (2-14) and (2-15) manifest the significant improvements of the transconductance by using the current mirrors compared to those in which single output is taken. The two equations, assume the ideal combination so that the two differential output currents arrive there at the same time. It is not exactly the fact because the output current from the left in each implementation in Figure. 2-19 requires an additional current mirror to combine itself with the right one, which introduces a time-delay difference between the two combined currents. Therefore, equations (2-14) and (2-15) are valid only when the time delay of the current mirrors for

the current combinations is negligible compared with operating signal cycle. As the operating signal cycle decreases, the time delay will become comparable and the improvement from using the current mirrors will be lessened.

The CMOS OTAs in Figure 2-20 illustrate two OTA implementations for the third-type fully-differential topology [66]. One can see that their structures are similar to that in Figure.2-20(b), but their two output currents remain. The aforementioned size ratio of B can also be applied in the current mirrors to increase their transconductance and therefore their current efficiency. The two OTAs in Figure 2-20 have the same transconductance, as can be derived below,

$$g_m = \frac{i_0}{v^+_i - v^-_i} = Bg_{m,M1}$$

----------(2.16)

Again, the DC tail currents I_{tail} in Figure 2-20 can be used for the above transconductance tuning. Compared to the OTA in Figure 2-20(a), the one in Figure.2-20(b) has an additional common-mode feed forward (CMFF) circuit comprising M_{C1}, M_{C2}, and M_{C3} to further enhance its common-mode rejection. The sizes of M_{C1}, M_{C2}, and M_{C3} should be properly selected to achieve a common-mode transconductance gain of $Bg_{m,M1}$, in order to optimize its common-mode cancellation with the B-size PMOS transistors at the outputs, which have a common-mode transconductance gain of - $Bg_{m,M1}$.

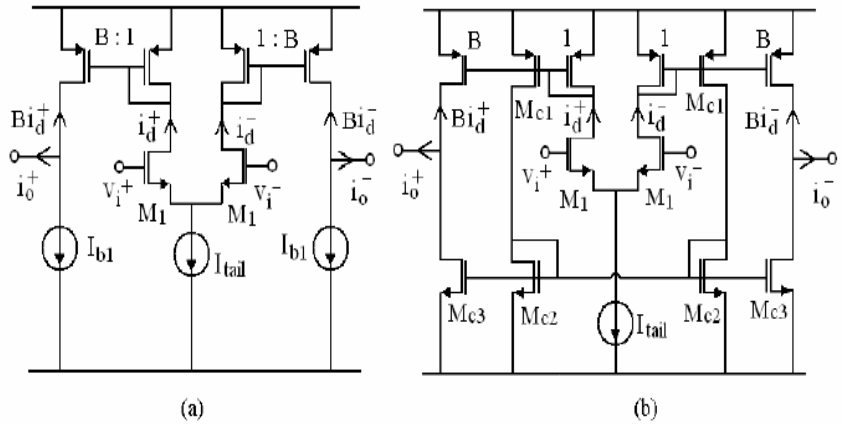


Figure 2.20 Differential Input/output OTA [66]

2.7.3 OTA Trends

Currently, high frequency, high linearity, and low power are the three main concerns of CMOS OTAs. With many efforts, researchers have made significant progress in these three aspects of CMOS OTAs, especially the latter two. Meanwhile, there are lots of problems in each aspect as well as in combining all three aspects. Tradeoffs have to be made among these aspects in designing practical OTAs. The current trends on these aspects are reviewed below.

2.7.3.1 High Frequency

As mentioned previously, OTAs are regarded as a good candidate to replace OPAMPs for high-frequency applications. OTAs that can operate up to several hundred MHz have been reported [68-78]. For higher frequencies, such as those above 1 GHz, new technologies and techniques are required.

CMOS scaling technology is one driving force behind the high-frequency OTAs. OTAs are built using transistors which mainly determine the OTA frequencies. Transistors with high cutoff frequency (f_T) and high maximum oscillation frequency (f_{MAX}) are desired. Most OTAs developed using long-channel CMOS technologies (>0.5 μm) had frequencies limited to 100 MHz or less according to [66] and its references. As the lengths of CMOS devices are scaled down, both channel delays and parasitic capacitances are reduced, which increases the cutoff frequencies of the transistors. Current CMOS 0.18 μm technology with f_{MAX} up to 40 GHz has been well commercialized [79], and 0.13 μm, 90 μm, 65nm, and even 45nm technologies are also available to researchers, all with much higher f_{MAX} than the 0.18-μm technology [80], [81]. These submicron and deep-submicron advanced technologies offer significant potential for various OTAs to be implemented at RF and even microwave frequencies. However, the study of RF/microwave OTAs circuits using these advanced technologies is still in its infancy.

Besides the scaling technology, OTA topologies are also very important for high-frequency OTAs. For an OTA in a given CMOS technology, capacitive parasitics can be

reduced by optimizing its topology in order to maximize its frequency. To this end, simpler topologies are preferable. Those OTAs with multiple stages [82-83] are complicated structures and not suited for high-frequency purpose. As previously discussed for the second-type OTAs, the use of current mirrors to combine one differential output current with the other results in different time delays for the two paths, which is also not suitable. The simplest topology is single-transistor common-source transconductor that probably has the least parasitics in all possible topologies which has been used in RF circuits. This simplest topology has low output impedance, low linearity and small transconductance. The described cascode topologies are a good solution, which have an excellent balance between complexity and performance. They have been widely used in low noise amplifier designs at RF and microwave frequencies [84]. It will be shown in the rest of this thesis that the cascode topologies are also very useful for high-frequency OTAs.

2.7.3.2 High Linearity

Linearity is a common issue of OTAs. When small input signals are applied then the output currents of a CMOS differential pair depend linearly on its input gate voltages only when small input signals are applied. Otherwise, high-order nonlinear terms must be included in the expression of the OTA output current [66],

$$i_0 = \sum_{i=1}^{\alpha} a_i v_1^{\,i} + \sum_{i=1}^{\alpha} b_i v_2^{\,i} + \sum_{1}^{\alpha}\sum_{1}^{\alpha} C_{ij} v_1^{\,i} v_2^{\,i}$$

----------(2.17)

These nonlinear terms cause significant distortion of the transconductance, which reduces the desired fundamental signal and presents harmful inter-modulation products at the output of the OTA [85], [86].

To reduce the nonlinear problem, several techniques have been proposed. One simple way is to directly put a voltage divider before an OTA, such that the input voltage of the OTA itself is kept small for its linear operation. However, it also reduces the available transconductance as a tradeoff. Source degeneration illustrated in Figure.2-21 is a

common way to reduce the nonlinearity, which also reduces transconductance usually by an order of the source degeneration factor N [66]. The two topologies presented in Figure.2-21(a) and Figure.2-21(b) utilizes degeneration resistors at the sources which realize the same transconductance and degeneration, and it can be exchanged. Shown in Figure.2-21(c), (d) and (e) are three active source-degeneration topologies based on topology as shown in Figure. 2-21(b). The degeneration resistor is simply replaced by a triode MOSFET in Figure.2-21(c). The one in Figure.2-21(d) also uses triode-MOSFETs, but with an additional internal mechanism that increases its transconductance for large signals, hence its linear range is expanded [87]. The last topology in Figure.2-21(e) utilizes two saturated transistors (M_2) for the degeneration with their drain connected to gates. Its third-harmonic distortion can be reduced by a factor of N_2, compared to its transconductance reduction of N due to the degeneration [87].

Some intelligent ways were also developed by means of an algebraic sum of nonlinear terms so that the nonlinear terms were automatically cancelled, yielding only a linear fundamental term in the ideal case [66]. Figure.2-22 shows two cross coupled topologies for the nonlinearity cancellation at the top and their practical implementations using MOSFETs at the bottom. Both topologies come from the high-order nonlinearity cancellation techniques for multipliers [66], [88].

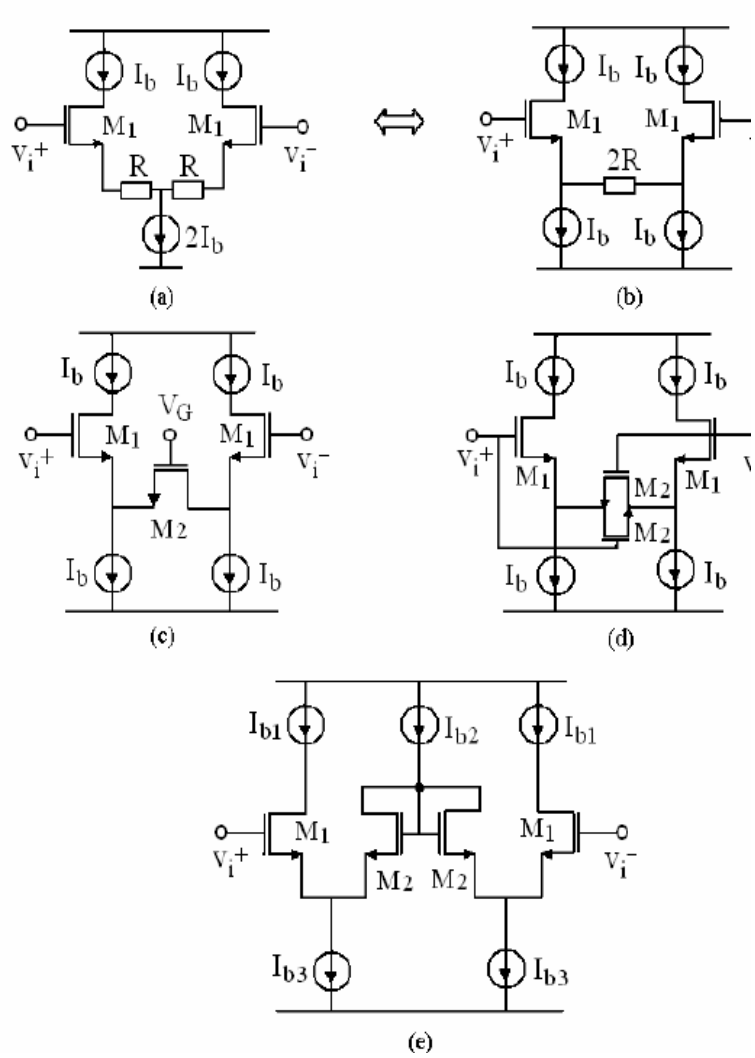


Figure 2.21 Source Degeneration Linear Technique [66]

$$(V_A V_1 - V_A V_2) - (V_A V_2 - V_A V_1) = 2V_A(V_1 - V_2)$$

----------(2.18)

$$[(V_1 + V_A)^2 + (V_2 - V_A)^2] - [(V_1 - V_A)^2 + (V_2 + V_A)^2] = 4V_A(V_1 - V_2)$$

----------(2.19)

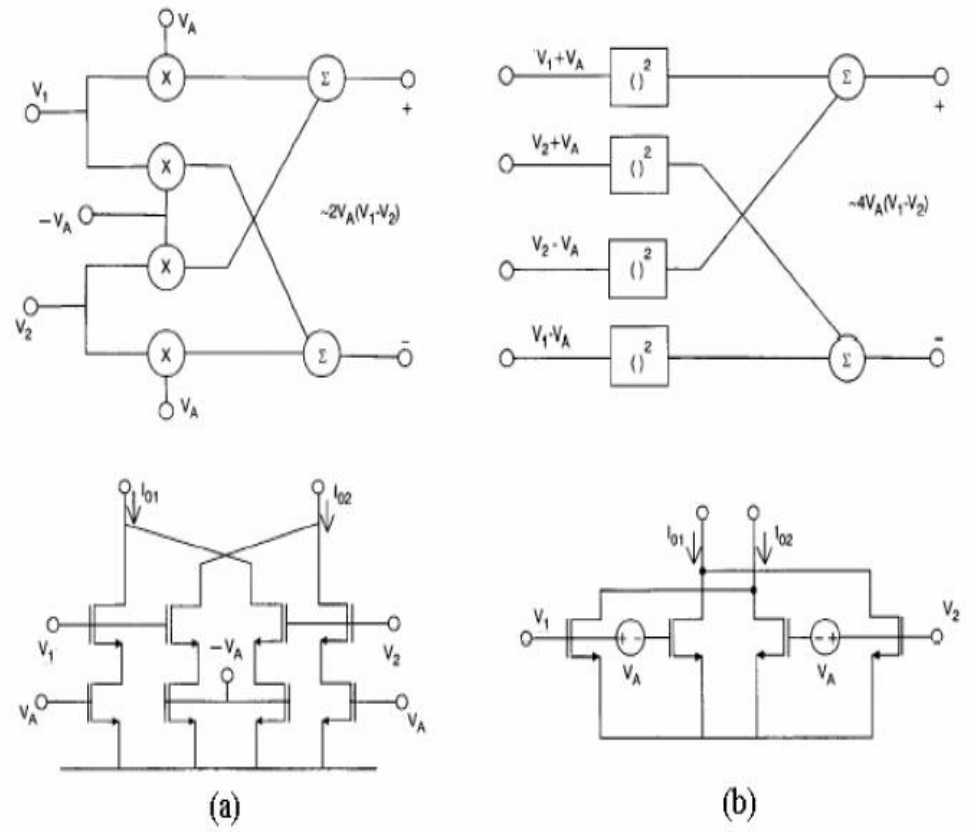


Figure 2.22 Linear techniques using nonlinear-term sum cancellation from [66]
(a) multiplication-sum technique, and
(b) squaring-sum technique (V1= -V2).

Techniques combining the above source-degeneration topologies and cross-coupled topologies also exist to further enhance the nonlinearity reduction [86-87]. Figure 2-23 presents one technique combining the topologies of Figure. 2-21(d), Figure. 2-21(e) and Figure 2-22, a complex combination technique. A byproduct of the linear techniques in Figure 2-22(d) and Figure 2-23 is a reduction in power consumption. The issue of power consumption is discussed in next section.

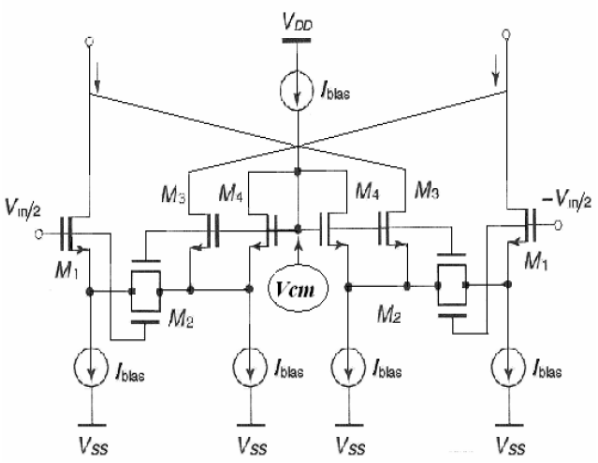


Figure 2.23 A complex combined linear technique from [87]

2.7.3.3 Low power

Mobile systems always require low power consumption in order to extend battery life. Non-portable devices also require low-power feature in order to save their energy costs as well as their thermal requirements. To use OTA circuits that contain several OTAs in such devices, low power operation of each OTA is required.

The power consumption of an OTA is determined by two factors: its DC voltage supply and its DC current. This indicates two possible choices to obtain low power requirement. The aforementioned CMOS scaling technology can enable low-voltage operations of the transistors, which allows the OTAs to operate at low voltage supplies, and it is one primary way to reduce the power consumption.

The other primary way is related to current-reduction techniques, which can reduce the DC currents flowing through the OTAs without change their transconductance, i.e., their power efficiencies can increase. Class-AB OTAs can accomplish this task. A class-AB OTA differs from a common OTA in that the class-AB has an adaptive bias circuit [67], [90-93]. A simplified class-AB OTA is shown in Figure. 2-24(a). The adaptive bias circuit can make the quiescent currents very low in order to dramatically reduce static power dissipation. When a large input signal is applied, it can automatically boost

dynamic currents well above the quiescent currents, yielding an intelligent way to make full use of the DC currents. Accordingly, the above linear topologies in Figure. 2-21(d) and Figure 2-23 are also class-AB OTAs. The adaptive bias circuit in Figure 2-24(a) is actually a local common mode feedback (LCMFB) network, which can be realized using the level-shifter in Figure. 2-24(b) The OTAs in [90-91] adopt two level-shifters with a cross-coupled structure for their two input transistors, while the work in [67] utilizes two level shifters to control the common-mode node of its input differential-pair. The latter has an advantage over the former in that the latter's lowest current in the differential pair is never less than the DC current of its level-shifter I_B, and input transistors is cutoff [67]. Using a single level-shifter also exists [92-93], but with a lower output current and a requirement for an extra common-mode sensing circuit.

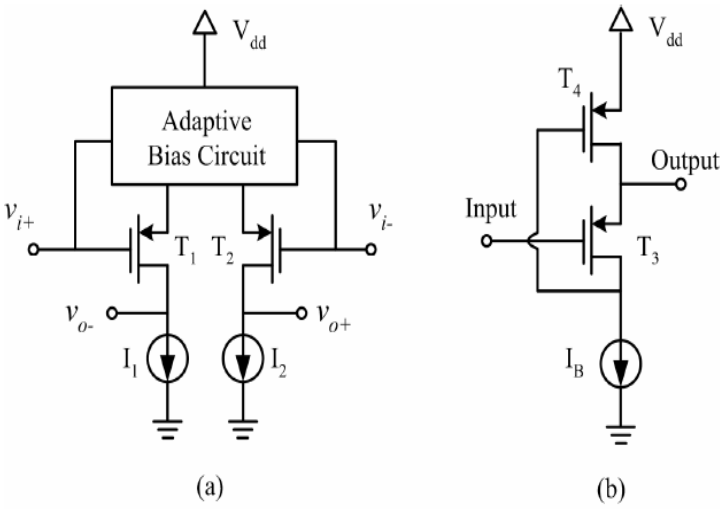


Figure: 2.24 (a) Simplified Class AB Amplifier and (b) Level Shifter [90-91]

2.8 OTA Topology

Operational Transconductance Amplifier (OTA) is usually an integral part of many analog and mixed-signal systems. OTA is a very important circuit that is used to realize functions ranging from DC bias generation to high-speed amplification or filtering depending on its levels of design complexities. There are numerous types of transconductor available in analog circuits; symmetrical CMOS OTA and folded cascode OTA are the two main types of OTA used widely in all designs. In this section, 3 types of OTA will be discussed.

2.8.1 Symmetrical CMOS OTA

A symmetrical CMOS OTA consists of one differential pair and three current mirrors as shown in Figure 2.25. The input differential pair is loaded with two equal current mirrors. The gain of such Op-amp is limited due to the gain per transistor can be quite small for nanometer MOS Transistor devices. The input devices see exactly the same DC voltage and load impedance, which give the best option in matching. Besides, this OTA gives large output swing as the output is only connected to a PMOS and a NMOS.

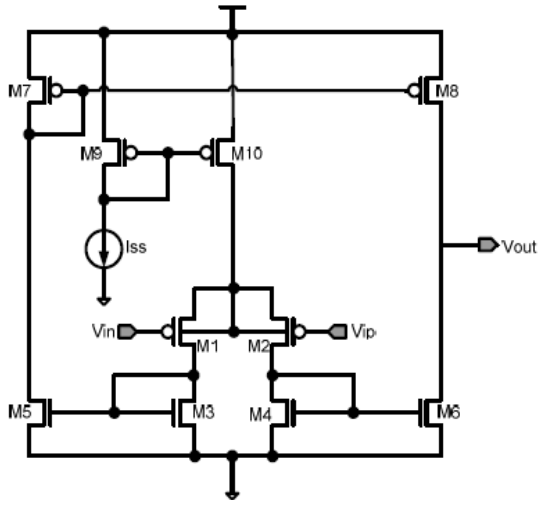


Figure 2.25 Symmetrical CMOS OTA

2.8.2 Telescopic CMOS OTA

In telescopic CMOS OTA, four cascode MOST are added M3-M6 in series with the input devices and current mirror to increase the gain as shown in Figure 2.26 Cascode M5 is included in the feedback loop around transistor M7 which allow larger output swing. Besides, telescopic has lower distortion at low frequencies and power consumption is not increase since there is only one biasing current source involved. However, the increased output impedance does not increase the GBW as the gain is increased but only at low frequencies.

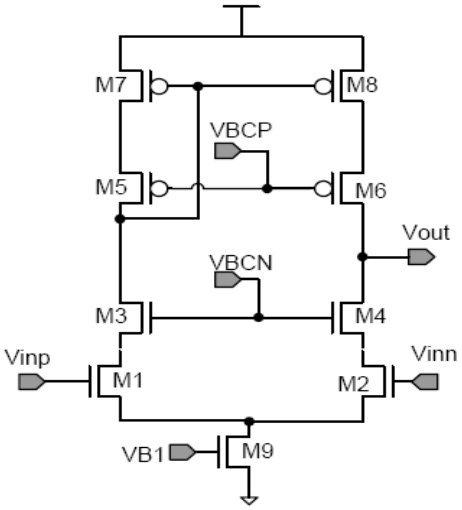


Figure 2.26 Telescopic CMOS OTA

2.8.3 Folded Cascode OTA

Folded cascode OTA consists of an input differential pair, two cascodes and one current mirror as shown in Figure 2.27. It utilizes the high swing current mirror hence output swing is higher than telescopic and high gain and GBW can be achieved because cascode at the output are used. However, the current consumption is twice of telescopic stage due to the additional current mirror. The main advantage of folded cascode OTA is that the input transistors can operate with their gate beyond the supply lines. The common mode input voltage range can include one of the supply rails and hence this can be used for single-supply systems.

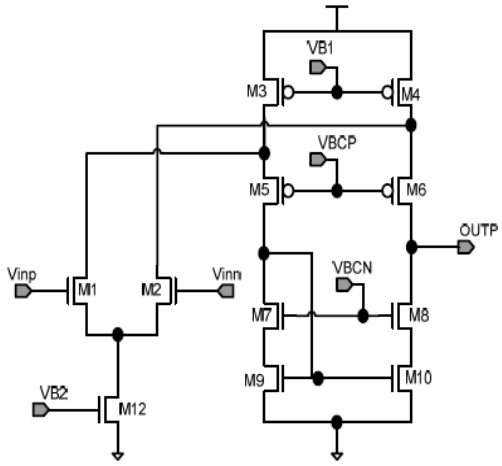


Figure 2.27 Folded Cascode OTA

The performances of 3 types of OTA can be summarized in Table 2.2. Folded cascode OTA is chosen as the base transconductance cell as it is compromising in overall performances.

Table 2.1 Comparison between various OTA Topologies

Topology	Gain BW	Output Swing	Power Dissipation	Noise
Symmetrical	**Medium**	**Highest**	**Medium**	**Highest**
Telescopic	**Medium**	**Low**	**Low**	**Low**
Folded Cascode	**High**	**Medium**	**Medium**	**Low**

2.9 Automatic Tuning Scheme

The frequency response of a filter is determined by the values of transconductances, resistances and capacitances. To maintain an accurate response of filter, absolute values of components are necessary. Absolute values on an integrated circuit can shift significantly due to process parameter variations, temperature and aging.

Depending on the accuracy of response desired, many schemes with varying complexities have been proposed and implemented. All these are collectively called "automatic tuning schemes." Since tuning of a high order filter is complex, integrated tuning schemes have generally relied on manipulating the response of basic filter building blocks like biquadratic sections. Tuning involves (i) Measure the filter response (ii) Compare the response with the desired response and (iii) Apply necessary tuning technique

Chapter 3

Design and Implementation of CMOS Folded cascade OTA

3.1 Analog Integrated Circuits

In the last few decades a revolution in the field of electronics is experienced in many fields. Starting from one single transistor to multimillion transistor circuits have provided us with the functionality that past generations could only dream of. The level of integration will continue to increase and the buzzword of today is “System- on-chip” (SoC).

With the rising level of integration the complexity of integrated circuits increases. More and more functionality can be added as new process technologies evolve. With the increasing complexity the use of CAD tools that supports design on a hierarchy of abstractions becomes more important. For digital circuit design there exist a large variety of tools and design methodologies that efficiently supports designs using several levels of abstraction. This is required in order to keep in phase with the new capabilities offered by technology.

For analog circuit design the situation is different. The level of abstraction is still kept at very low levels and there are not that many CAD tools available. The lack of a structured design flow is one of the major problems in analog circuit design. This becomes obvious when analog and digital circuits are put on the same chip, as in mixed-signal SoCs. In general, the digital parts account for about 90% of an integrated circuit while only 10% is analog. However, most of the time and effort are spent on the analog parts [94].

Even though the trend is to replace analog circuits with digital approach with possible ways, but there are still some functions where analog parts cannot be avoided. The most obvious are the communication with the “real” world outside the chip. Since the world consists of analog signals we must be able to interpret and convert these signals to something that can be fed as an input signal to a circuit, for example use a microphone to pick up variations in the air-pressure, a sensor to measure the intensity of light, or an antenna to transmit and receive radio frequency signals.

Some of the most important applications of analog circuits are to bridge the gap between the “real” world and the digital domain. The need to go from analog to digital processing has made the use of analog-to-digital (ADC) and digital-to-analog (DAC) converters indispensable. Requirements of high-speed communications have made these circuits some of the most critical components in mixed-signal chips.

Filters are other important components in such applications. Antialiasing filters are required whenever we sample an analog signal, thus an analog filter is necessary in all communication systems. Analog filters may also be found in hard disc drives where they perform antialiasing and equalizing of the signals read from the disc. Another important application of analog circuits are in radio frequency (RF) circuits. Here analog circuits are operating at frequencies in the range of several GHz in order to realize the functions required in modern wireless communication Systems.

In all of the above analog circuits, amplifiers are one of the most important building blocks. It is thus clear that analog circuits are important and necessary in a large range of applications. This is especially true when considering SoCs where the link between the analog and the digital domain will be required in practically every circuit. To conclude, analog circuits are, and will remain, an important component in many integrated circuits.

3.2 The Analog Design Flow

A simplified view of an analog design flow is shown in Fig. 3.1. The starting point is an idea of the functionality to implement.

The function is mapped onto an architectural description. In this process the functionality is decomposed into a set of high-level building blocks. The decomposition is continued until the functional block can be mapped onto a set of lower-level analog building blocks. The simulations done at this level are typically carried out using high-level models in order to validate the functionality of the concept. From these simulations, the specifications on the low-level blocks are extracted. Here the performance metric are measures of properties that are used to characterize the behavior of a cell. For example an amplifier must have at least a specific unity-gain frequency in order for a filter to work properly.

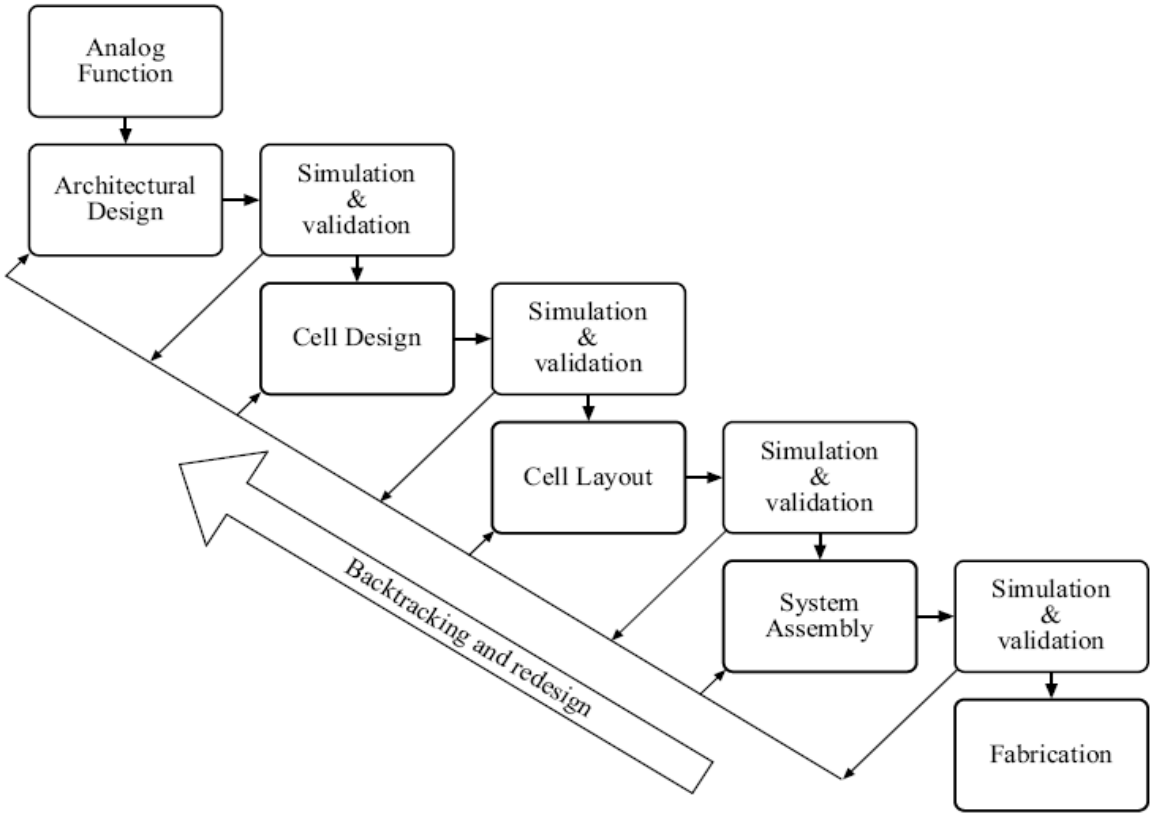


Fig3.1: The Analog Design Flow

In the next step these cells are realized by designing the low-level building blocks that previously derived performance specification. The cell design step includes choosing

between several possible realizations in order to implement the functionality in the most efficient way.

During the layout phase the geometries for the functional blocks is determined. Finally the building blocks are assembled to implement the desired functionality. Throughout the design process excessive simulations and validation steps are required. If the circuit fails to meet the specification at some level the proceeding design steps must be revised. This may include backtracking several steps in the design process.

3.2.1 The Manual Design Methodology

In Fig. 3.2 a flow graph for traditional manual cell-level analog circuit design is shown. The circuit specification puts lower and/or upper limits on some performance metrics while other may be less precisely specified.

Topology section

The designer has to choose a suitable circuit topology that is able to meet the specification. Usually there exist several topologies that implement a particular functionality. The designer have to decide upon one of them based on experience, simple hand calculations and rules of thumb. Also, the designer's choice may be influenced by other aspects than the actual performance of the circuit.

Device Sizing

In the component sizing step, the size of all transistors, resistors, capacitors, and biasing voltages and currents are determined. These parameters are referred to as the design parameters. Determining the values of the design parameters is a complicated task since the relation between the parameters and the resulting performance is a nonlinear function.

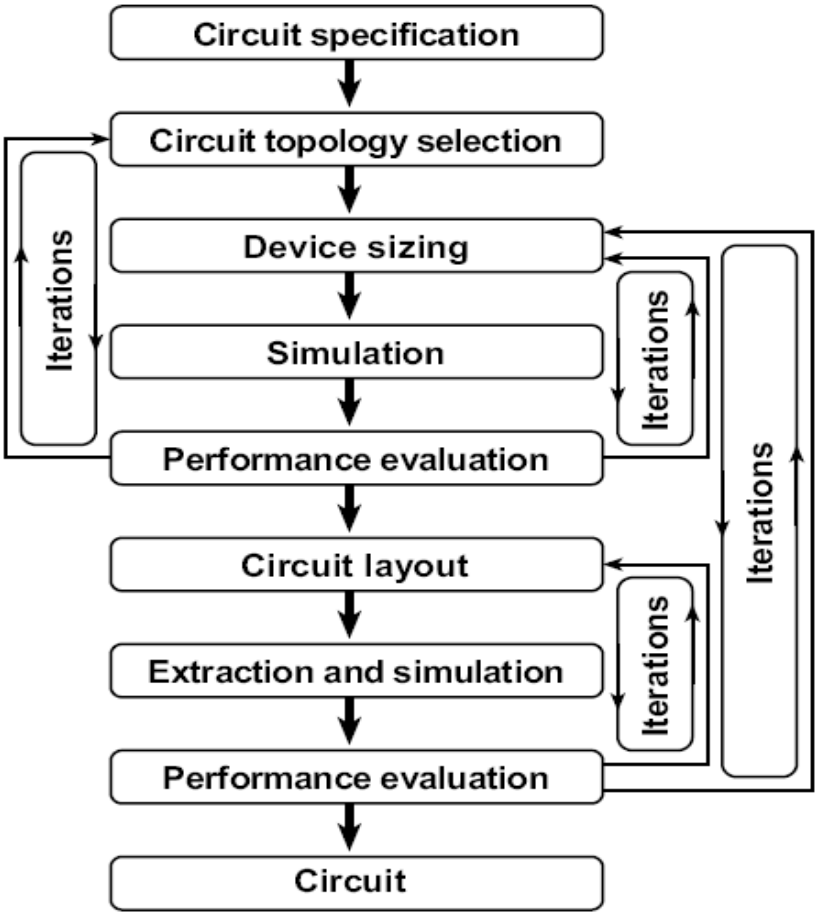


Fig. 3.2: cell-level manual analog circuit design.

To get the approximate sizes of the components simplified hand-calculation models may be used. The formulas are usually based on simple approximations of the transistor characteristics that may differ significantly from the real devices. The designer's previous experience with analog circuit design may give additional directions on what choices to make. Rules of thumb are also commonly used in order to reduce the large design space.

In order to evaluate the performance of the initial sizing of the devices a circuit simulator, such as HSPICE or Spectre, is used. A test bench is created where a set of suitable input signals are applied to the circuit in order to extract the performance metrics of interest.

Many circuit simulators offer the ability to sweep the value of the design parameters and determine their impact on the overall performance. Sweeping a large number of design parameters are, however, costly in terms of computational time. Thus, in practice, limited in the number of design parameters that can be swept.

Some simulators, e.g., Spectre, offer a simple form of performance optimization. Typically a few design parameters may be adjusted using optimization in order to fine-tune a set of performance metrics. However, in practice these optimization routines are only capable of handling a small number of design parameters. It also requires a good initial starting point. Thus, only minor improvements are achieved. The time required to perform the optimization task is also long, since the circuit simulator must be called repeatedly.

If no feasible solution is found after performing several iterations with parameter adjustment and the design process have failed, designer has to go back and select a different circuit topology. Thus, it is, important that a suitable topology is chosen at the beginning of the design process. In a worst case scenario the specification for a particular cell have been set to tight, if this occurs the overall performance specification must be revisited.

Layout Generation

Layout generation is a time consuming part in analog design. In the layout phase, the device sizes from the previous design step are mapped onto a physical implementation. The tools available at this level are, traditionally, basic module generators, tools for checking design rules. While the goal, in most cases, is to make the design as dense as possible other aspects such as the impact of parasitic effects on the final circuit performance, matching conditions, and yield degradation are also important.

In order to determine the layout-induced performance-shift an extraction tool is used. Given the geometries of the layout, the tool extract the interconnect parasitic of the circuit. In order to meet the performance specification the designer have to consider the degrading effect of the layout phase during the previous step. Thus, some extra design margins have to be added.

If the margin is made to small, changes in the layout as well as resizing of the devices might have to be performed. Such tasks are, of course, time consuming and even a small change in the size of some devices might require large changes in the layout. On the other hand, if the design margin is made to large, the penalty will be, e.g., increased power consumption and larger chip area.

3.3 Challenges in Analog Design

The traditional analog design flow suffers from several problems. In this section some of these issues will be discussed in more detail.

One of the most important aspects are the time spent on designing the low-level cells. The time required to design an amplifier might be in the order of weeks [95-96] when all design steps are considered. Since a large amount of all chips contains both analog and digital components this poses a severe bottleneck due to the gap between analog and digital design efficiency. Decreasing the time spent on the design of analog parts in a chip will have a large impact on the time-to-market for the whole chip.

Another important aspect is the circuit performance. A circuit specification may contain requirements on tens of different performance metric. When sizing a circuit manually the designer has to understand how these performances metric are affected by changes in the design parameters. In a worst-case scenario the designer will adjust the width of the transistors in order to meet the requirement on bandwidth; however, while doing this the requirement on distortion is violated. It is clear that with an increasing number of effects

and performance metrics taken into account the problem becomes difficult for a designer to comprehend.

Depending on the application some of the performance metric will not affect the actual function of the circuit. Two examples of such properties are the power consumption and the total area used by the circuit. Two amplifiers with different power consumption may have similar operation characteristics. For example a mobile application it is therefore important to find the amplifier with the lowest power consumption while still meeting the specification. Since each iteration in Fig. 3.2 is costly, the number of circuits that can be examined in order to minimize the power consumption is limited.

As shown in Fig. 3.3 it is assumed that there are restricted parameters spaces in which the device sizes can be chosen. With repeated iterations in which the device sizes are adjusted to meet the specification different points in the design space is visited. Continuing the process some part of the space where the performance specification is met can be found. Further, by exploring the feasible design space, e.g., the power consumption could be minimized.

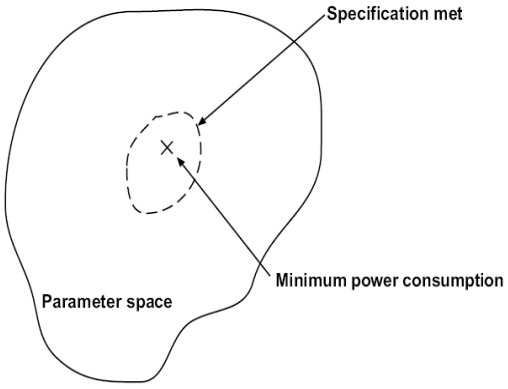


Fig.3.3: Design Parameter Space

Yield is an important factor when considering the cost of the chip. Usually, manual design is carried out using nominal process parameters. When the device sizes have been determined the design is simulated using worst-case process parameters in order to measure the effect of process variations. The worst-case design parameters are derived by the process vendor in order to simulate process corners. Also, Monte Carlo simulations,

where design and process parameters are varied according to statistical distributions, are used for this purpose.

This method provides a way of predicting the circuit yield. However, the Monte Carlo simulations are time consuming. Also when a simulation fails there is no way of identifying what design parameters is causing the failure. The use of multiple sets of worst-case parameters will produce a large number of simulation results to take into account, further complicating the design process. Consequently these approaches are only used at the end of the design procedure to validate the performance. The actual device sizing is carried out using nominal process parameters. Adjustments to the design parameters are usually required in order for the circuit to work under several sets of worst-case parameters.

During the layout phase many effects that will increase the yield and ensure good circuit behavior must be taken for consideration. The number of constraints on an analog layout can be huge and it is hard for a human designer to keep them in mind and make the appropriate choices. Also, the number of layout solutions that can be tried out is limited by the time consuming task of producing them.

When migrating from one process technology to the next, the process parameters determining the performance of the circuit are changed. Also, layout rules, such as minimum spacing rules and so on, change. This usually requires a complete redesign of the circuit, both with respect to the sizing and the layout. Thus, the level of reuse of analog circuits is low.

To conclude the following drawbacks of the manual design methodology are identified:

- Time consuming and therefore costly.
- Insufficient exploration of available design space, i.e., low utilization of existing process technology.

- Hard to reuse previous designs.
- High risk of errors being introduced.
- Yield is not taken into account during the design process.

3.4 The Process Technology

Today there exist several process technologies for realizing integrated circuits. The most popular of these is the complementary metal-oxide semiconductor (CMOS). CMOS is the dominating process technology for Analog and digital integrated circuits today.

In the CMOS process both n-channel (NMOS) and p-channel (PMOS) MOSFETs are used to realize the logical functions. Since the PMOS transistor is “on” when a low voltage level (zero) is applied to the gate, and the NMOS transistor is “on” when the gate potential is high (one) these devices can be used to form complementary circuits where the static power consumption is small.The low power consumption and the manufacturing cost of CMOS circuits is low compared to, e.g., bipolar circuits, has made CMOS the most popular process technology for digital circuits.

Even though the bipolar transistors can work at higher frequencies, and the fact that analog and digital circuits are used on the same chip have made the CMOS process important for analog design as well. Special processes, such as Bi-CMOS, combine the bipolar technology with the CMOS technology. In this way the designer can use bipolar devices for performance-critical analog parts and CMOS for digital parts on the same chip.

However, in this work the process technology considered is standard CMOS. Since our target is design analog amplifiers working at baseband frequencies, CMOS process technology is sufficient in most cases.

Bipolar Vs CMOS Transistor [57]

Category	Bipolar	CMOS
Turn on Voltage	**0.5V- 0.6V**	**0.8V- 1.0V**
Saturation Voltage	**0.2-0.3V**	**0.2V- 0.8V**
Analog Switch Implementation	**Offsets, Asymmetric**	**Good**
Power Dissipation	**Moderate to High**	**Low but can be large**
Speed	**Faster**	**Fast**
Number of Terminal	**3**	**4**
Noise(1/f)	**Good**	**Poor**
Noise Thermal	**OK**	**OK**
Offset Voltage	**<1mV**	**5-10mV**

3.4.1 The CMOS Devices

In this section, a simple model for the CMOS transistor is discussed. Even though this model do not predict the behavior of the sub-micron transistor accurately, the relations are still valuable to understand the relationship between different properties of the devices. Also, some of the concepts presented here are used in more accurate models as well. The equations presented are those normally used when performing hand calculations. They are also an integral part of the manual device sizing approach.

Large-Signal Model

The symbol of the NMOS and PMOS transistors are shown in Fig. 3.4. These symbols are the four-terminal version of the transistor. In this simple model the transistors are assumed to have three operating regions. Here the equations for the NMOS transistor are given. However, the corresponding relations and equations for the PMOS transistor are similar. For the NMOS transistor the cut-off, linear, and saturated regions are defined by the following relations

Cutoff: $V_{DS} < V_{GS} - V_{TH}$

Linear: $V_{DS} \leq V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$

Saturated: $V_{DS} \geq V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$

----------**(3.1**)

Here V_{TH} , the threshold voltage is the minimum gate to channel voltage required in order to create a conducting channel between the drain and source in the transistor. The threshold voltage is modelled by

$$V_{TH} = V_{THO} + \gamma(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}$$

----------**(3.2)**

(a) **(b)**

Fig.3.4: (a) NMOS and (b) PMOS Transistor symbol

Where V_{THO} is the threshold voltage when V_{BS} is zero. The additional terms are results of the body-effect. The body-effect is an increase in the threshold voltage due to the voltage difference between the substrate (bulk) and the source of the transistor. Φ_F is the difference between the Fermi potential at the gate and the Fermi potential at the substrate. γ is the body-constant determined by the process parameters. Depending on the operating region the current through the transistor, I_D is given

Cutoff: $I_D \approx 0$

Linear: $I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V^2_{DS}}{2}]$

Saturated: $$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2[1 + \lambda V_{DS}]$$

----------(3.3)

Where μ_n is the mobility of electrons near the silicon surface for the NMOS transistor, *Cox* is the gate capacitance per unit area, is the output impedance constant, and *W* and *L* are the width and channel length of the transistor. In analog amplifiers the transistors are usually biased to work in the saturated region. The reason for this is that when a transistor operates in that region the current is controlled mainly by the gate-source voltage.

Small-Signal Model

For large signal variations the large-signal model can be used to calculate the behavior of the circuit. However, if only small signal variations are considered the nonlinear large-signal model can be linearized. The small-signal model is a linearization of the large-signal model around the operating point of the circuit. This model is only valid for small perturbations from the operating point. The models can be used in order to simplify the calculation of, e.g., the frequency dependent properties of the circuit.

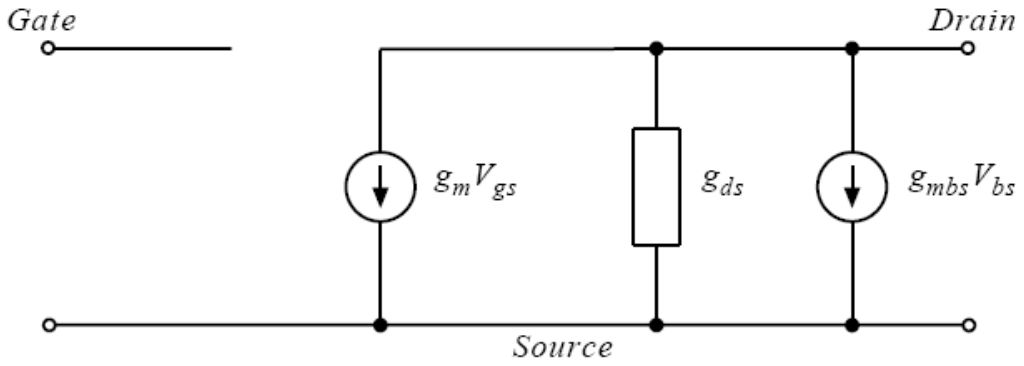


Fig.3.5 Small Signal Model of MOS Transistor

A simple small-signal model for the NMOS transistor is shown in Fig. 3.5. Here g_m is the transconductance and g_{ds} is the output conductance. The small-signal parameters are derived using the following expressions:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \lambda$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \frac{\partial V_{TH}}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} = \eta g_m$$

----------(3.4)

3.5 Performance Metrics in Amplifier Design

There are several important performance metrics that must be taken into account When designing an analog amplifier. The importances of these metrics are of course highly dependent on what application of the amplifier is intended to be used in. In this section some commonly used performance metrics for analog amplifiers are discussed. Depending on the application of the amplifier, other performance metrics might also be of interest. The purpose of this section is not to give a full coverage of all existing performance metrics in analog circuit design, but to introduce and explain some of the concepts used later on.

The general amplifier transfer function is:

$$A(s) = \frac{A_0(1+\frac{s}{z_1}).....(1+\frac{s}{z_n})}{(1+\frac{s}{p_1}).....(1+\frac{s}{p_m})}$$

----------(3.5)

Here *z* denotes a zero and *p* denotes a pole. A_0 is the DC gain, i.e., the gain when *s* is equal to zero. Further, the output signal of a differential amplifier can be written as:

$$V_{out}(s) = A_{CM}(s)[\frac{V_p(s)+V_n(s)}{2}] + A_{DM}(s)[V_p(s) - V_n(s)]$$

----------(3.6)

Where $A_{CM}(s)$ is the common mode gain and $A_{DM}(s)$ is the differential gain. Vp(s) is the positive input signal while Vn(s) is the negative input signal.

Bandwidth and Unity-Gain Frequency

In Fig. 3.6 the magnitude and phase response of an amplifier with two-poles are shown. The bandwidth of an amplifier is defined as the frequency band for which the amplitude is within 3dB of its maximum value.

The bandwidth for the amplifier in Fig. 3.6 is about 100 rad/s. Another performance metric is the unity-gain bandwidth (UGBW). The UGBW is defined as the frequency range for which the amplifier has a gain that is at least equal to unity. Further, at the unity-gain frequency, ωu, the amplification of the input signal is equal to unity, i.e., above this frequency the input signal is no longer amplified. The unity-gain frequency is defined as:

$$A(jw_u) = 1$$

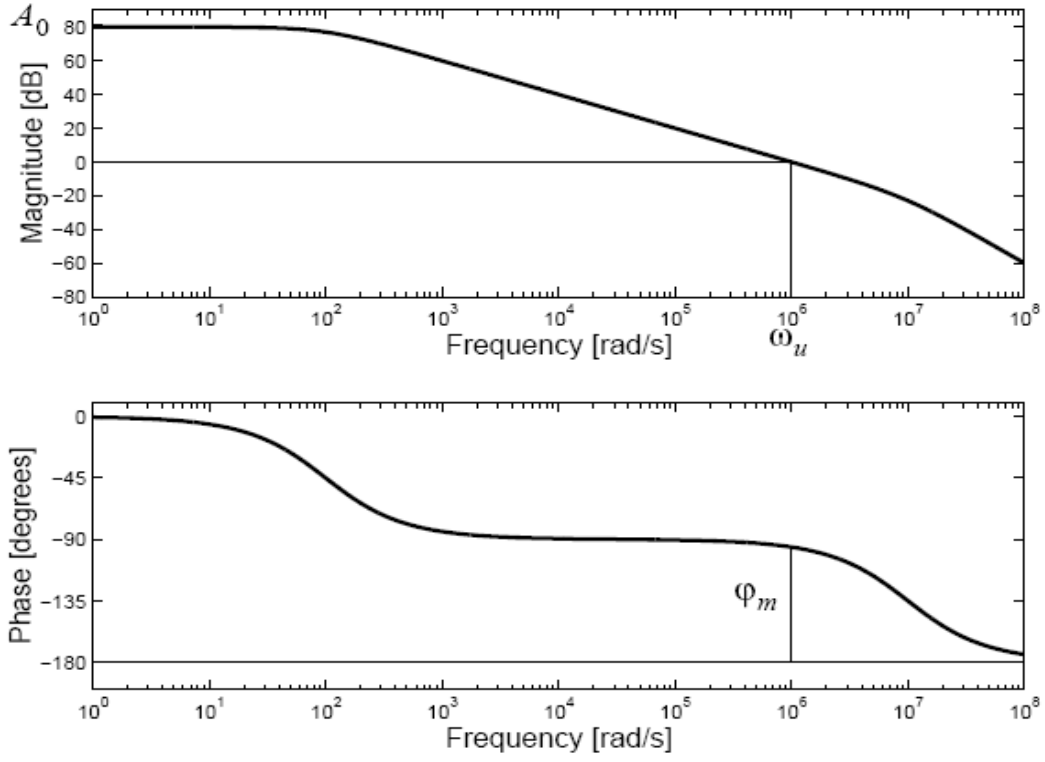


Fig. 3.6: Magnitude and Phase Response of Amplifier

Phase Margin:

The phase margin φ_m is defined as: $\varphi_m = arg(\beta A(jw_u) - (-\pi)$

Here β is the feedback factor in a closed-loop amplifier configuration. The phase Margin is a stability measure for the amplifier.

Positive and Negative Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) measures the amplifiers ability to suppress variations in the power supply voltages. In the ideal case, a change in supply voltage will not effect the performance of the amplifier. However, in reality, changing the power supply voltage will affect the bias levels and thereby the operation of the circuit. Both positive PSRR, i.e., the suppressions of variation in the positive power supply voltage, and negative PSRR, i.e., the suppression of variations in the negative power supply voltage are of Important. The definitions are

$$PSSR_p(jw) = 20\log\frac{A_{DM}(jw)}{A_{VDD}(jw)}$$

$$PSSR_n(jw) = 20\log\frac{A_{DM}(jw)}{A_{VSS}(jw)}$$

----------(3.7)

Where A_{VDD} is the magnitude of the frequency response from the positive power supply to the output terminal and A_{VSS} is the magnitude of the frequency response from the negative power supply to the output terminal.

Common Mode Rejection Ratio

The common mode rejection ratio (CMRR) is a measure of how unwanted common mode signals on the amplifier input terminal are suppressed. In

$$CMRR(jw) = \frac{A_{DM}(jw)}{A_{CM}(jw)}$$

----------(3.8)

the gain of the common-mode signal is compared to gain of the differential signal. In the ideal case the CMRR is infinitely large, i.e., the common-mode signal is not amplified of at all.

Slew Rate

The slew rate is defined as the maximum slope at an amplifiers output.

$$SR = Max[\frac{dV_{out}}{dt}]$$

----------(3.9)

It is measured by applying a large step to the input terminal and measure the slope at the output terminal. When slew-rate limitation occurs the amplifier will not act as a linear system. For example, if a large step is applied on the amplifiers input terminal, the output signal is a linear ramp with a constant slope (the SR).

Distortion

When a sinusoidal signal is used as the input to an amplifier the output signal, in the ideal case, is a linear amplification of that signal. However, in reality the shape of the output signal deviates from its input. This is due to that nonlinearities in the amplifier distort the signal.

There are several types of nonlinearities in analog amplifiers. First of all, the circuit elements, i.e., transistors, capacitors, and resistors are nonlinear elements. Secondly, other effects such as slew rate limitation causes nonlinear behavior.

Distortion appears as unwanted frequency components at the circuits output. One way of measuring the harmonic distortion, i.e., the effect of higher-order harmonics is by measuring the total harmonic distortion (THD). THD relates the fundamental and the higher order harmonics. It is calculated by summing the higher order harmonics and comparing them to the fundamental according to

$$THD = 10\log\frac{\sum_{2}^{\infty} P_n}{P_{Fundamental}}$$

----------(3.10)

Where P_n is the power of the nth harmonic while $P_{Fundamental}$ is the power of the fundamental. Other performance metrics for linearity are harmonic distortion, compression and intercept points, and inter modulation distortion [67]. The concept of intercept points is illustrated in the Fig. 3.7

The intercept points are computed by extrapolating the curves of the fundamental, second and third harmonic according to Fig. 3.7 Since the second harmonic increases quadratically, it will intersect with the fundamental at some point, *IIP*2. The higher the interception is located; the better is the suppression of the harmonic

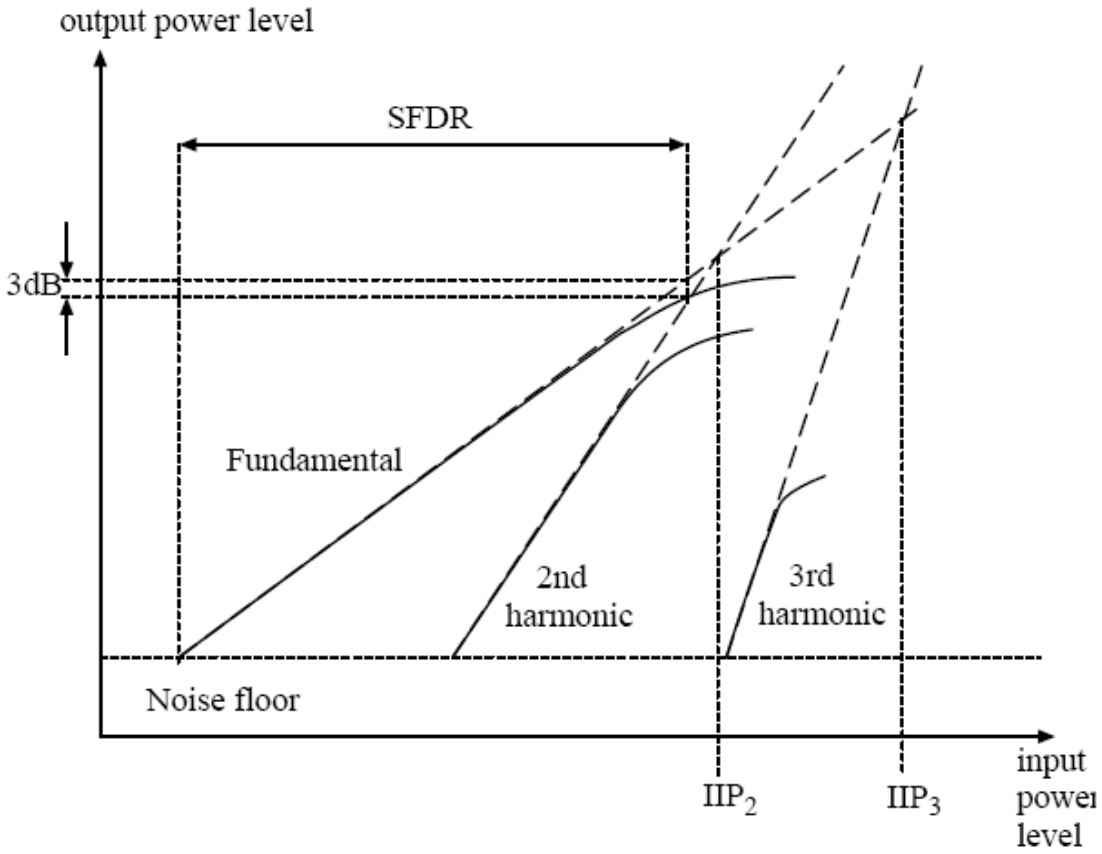


Fig.3.7: Intercept Point and Spurious Free Dynamic Range

Noise

In MOSFETs there are mainly two types of noise sources, thermal and flicker noise (1/*f* noise) [31]. Thermal noise arises in resistors and is the result of random motions of electrons due to thermal effects. Flicker noise is believed to be the result of charges being "trapped" in the device for various reasons and later released. Unlike thermal noise flicker noise is frequency dependent and decreases inversely with the frequency.

The noise spectral density at the circuit output is computed by summarizing the contribution of all independent noise sources in the circuit according to

$$S_{out}(\omega) = \sum_{1}^{n} S_n (H_n(\omega))^2$$

----------(3.11)

Here n is the number of noise sources, S_i is the spectral density of the noise source, and H_n is the magnitude response from the noise source to the output of the circuit. By integrating the noise over a frequency band the noise power is obtained.

A common performance metric for noise is the signal-to-noise-ratio (SNR) defined by

$$SNR = 10log\frac{P_{Signal}}{P_{Noise}}$$

It is defined for a specific frequency range over which the corresponding signal and noise power is integrated.

Common-Mode Range and Output Range

The common-mode range (CMR) is defined as the range of the common-mode level at which the circuit responds properly to differential input signals. In order to determine the CMR, an acceptable level of distortion at the circuit output may be defined.

The output range (OR) is defined as the range in which the output signal can vary, given that the distortion must be lower than some threshold value.

Circuit Area, Power Consumption, and Yield

Some performance metrics do not directly affect the functionality of the circuit but they are associated with its cost. A typical example of such performance metrics is the silicon area occupied by the circuit. The area of the chip directly affects the manufacturing costs and it is therefore of interest to make the circuit as small as possible.

The power consumption is more important because a large number of applications nowadays running on battery. The power consumption directly affects the operation times for such products and is therefore an important performance metric.

During the manufacturing process, a certain percentage of all circuits will, due to various reasons, not operate according to the specification. Yield is defined as the number of circuits, out of a set, that do operate according to the given specifications. Maximizing the yield directly affects the cost of manufacturing a chip. Designing for high yield is therefore important. Further, the yield is partly depending on the chip area since the number of process errors is approximately the same per unit area. Thus, a lower percentage of the chips will be affected by these errors if each chip is made smaller.

Trade-Offs in Analog Amplifier Design

It is clear that there is numerous performance metrics used for analog circuits. What makes the design process even more challenging is the nonlinear relation between them. In Fig. 3.8 some of these relations, present in analog amplifier design, is illustrated. For example, when trying to lower the power supply voltage the voltage swing is reduced. If the voltage swing is reduced the SNR is decreased and so on. Thus, determining the relations between the performance metrics is crucial in analog circuit design. Simple device models can give some information of possible trade-offs.

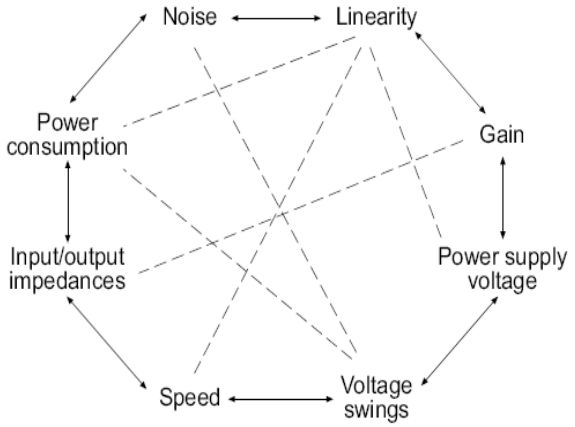


Fig.3.8: Tradeoffs in Analog Amplifier Design [49]

3.6 Operational Amplifiers

The evolution of very large scale integration (VLSI) technology has developed to the point where millions of transistors can be integrated on a single die or “chip”. Integrated circuits once filled the role of subsystem components, partitioned at analog-digital boundaries; they now integrate complete system on a chip by combining both analog and digital functions. Complementary Metal-oxide semiconductor (CMOS) technology has been the mainstay in mixed-signal implementations because it provides density and power savings on digital side, and a good mix of components for analog design. In a few years, from now, CMOS technology will overpower the whole electronic industry. Designing High Performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is Operational-Amplifier. At large supply voltages, there is a trade-off among speed, power and gain amongst other performance parameters. Often these parameters present contradictory choices for operational-amplifier architecture [57].

Operational Amplifiers (usually referred to as op-amps) have become one of the most versatile building blocks in analog processing system and are an integral part of many analog and mixed-signal systems. Ideally they perform the function of a voltage controlled current source, with an infinite voltage gain. Op-amps with vastly different levels of complexity are used to realize functions ranging from DC bias generation to high-speed amplification or filtering. The design of op-amps continues to pose a challenge as the supply voltage and transistor channel length scale down with each generation of CMOS technology.

Operational amplifiers are the amplifiers that have sufficiently high forward gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of op-amp [57]. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement the negative feedback concept.

Most of the CMOS op-amps that do not have a large enough gain require two or more gain stages.

The unbuffered operational amplifier better described as operational transconductance amplifier since the output resistance typically will be very high (hence termed “as unbuffered”). The term “buffered” and “unbuffered” is used to distinguish between high output resistance (operational transconductace amplifiers or OTAs) and low output resistance amplifiers (voltage operational amplifiers).

Table 3.1 Comparison of OPAMP Vs OTA

OPAMP	OTA
High input impedance and low out- put impedance.	High input impedance and high output impedance.
Modeled as a voltage controlled voltage source because of the above property.	Modeled as voltage controlled current source.
Used with external feedback for creating circuits. Used as an output buffer. Contains compensation capacitor in its circuitry between the 2 stages (Miller compensation).	All nodes are at low impedance except for the input and the output nodes.
Op-amp becomes unstable with larger load capacitances.	Better frequency capabilities than op-amp. As load capacitance increases the phase margin increases and the OTA is stable.
An OTA with output buffer is an op-amp.	Generally a single stage design
	For most on-chip applications as loads are capacitive the design of opamp is essentially design of an OTA

3.6.1 The Operational Transconductance Amplifier

Many modern Op-Amps are designed to drive only capacitive loads. In this case, it is not necessary to use a voltage buffer to obtain low output impedance. So it is possible to realize Op-Amps with higher speeds and larger signal swings than those that drive resistive loads. These Op-Amps are possible by having only a single high-impedance node at the output. The admittance seen at all other nodes in these Op-Amps are on the order of $1/g_m$, and in this way the speed of Op-Amp is maximized. With these Op-Amps, compensation is usually achieved by the load capacitance C_L. As C_L gets larger, these Op-Amps gets more stable but also slower. One of the most important parameters of these modern Op-Amps is gm (ratio of output current over input voltage), therefore they are sometimes referred to as Operational Transconductance Amplifiers (OTA).

The schematic symbol and equivalent circuit model for an Operational Transconductance Amplifier (OTA) are shown in Figure 3.9(a), (b) respectively**.**

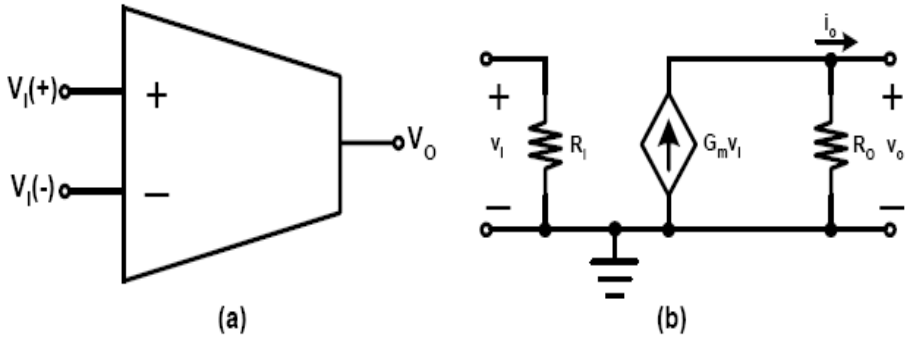


Figure 3.9 OTA and its Equivalent Circuit

The OTA converts an input voltage to an output current relative to a transconductance gain parameter $G_m=i_o/v_i$**. Ideally the input and output resistances are infinite (**$R_i=R_o=\infty$**) such that** $i_i=i_{Ro}$**=0 and the output current is absorbed solely by**

the load. The conventional OTA is classified as a class A amplifier and is capable of generating maximum output currents equal to the bias current applied.

The equivalent circuit model indicates the transconductance amplifier generates an output current (i_o) proportional to an input voltage (v_i) based on the transconductance gain G_m. The open circuit voltage gain of the conventional OTA model in Figure 3.9 (b) is given by $A=G_mR_o$.

3.6.2 Single Stage OTA

The entire differential amplifier can be considered as OTA. Figure 3.10 shows two such topologies with single Ended and differential outputs. The small signal, low frequency gain of the both circuit is $g_{mN}(r_{ON} \square r_{OP})$, where the N and P denotes NMOS and PMOS. The bandwidth is determined by load capacitance C_L.

The circuits of Figure 3.10 suffer from Noise Contribution from transistor $M_1 - M_4$. In all op amp topologies, at least 4 transistors contribute to the input noise: two from input transistor and two from load transistors.

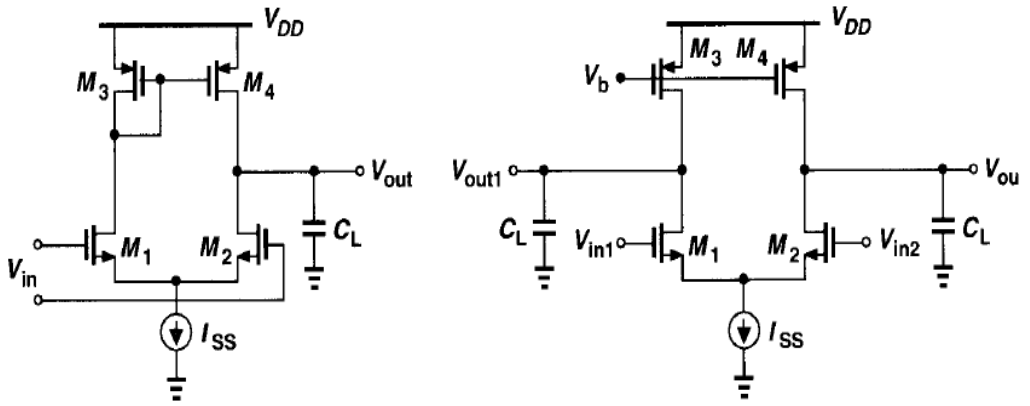


Figure 3.10 Differential input with Single Ended and Double Ended Output

3.6.3 Telescopic Topology

In order to achieve high gain, differential cascode topologies shown in figure 3.11 for single ended and differential output generation respectively. Such circuits show a gain on the order of $g_{mN}[(g_{mN}r^2_{ON} \square g_{mP}r^2_{OP})]$, but at the cost of output swing and additional poles. Such configuration called "Telescopic" cascode OTA. The circuit with single ended output suffers from a mirror pole at node X which creates issue of stability. In the fully differential version of Figure 3.10, output swing is given by:
$2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + V_{OD5} + V_{OD7})]$ .Another drawback of telescopic cascode is difficulty in shorting their inputs and outputs e.g to implement unit gain buffer.

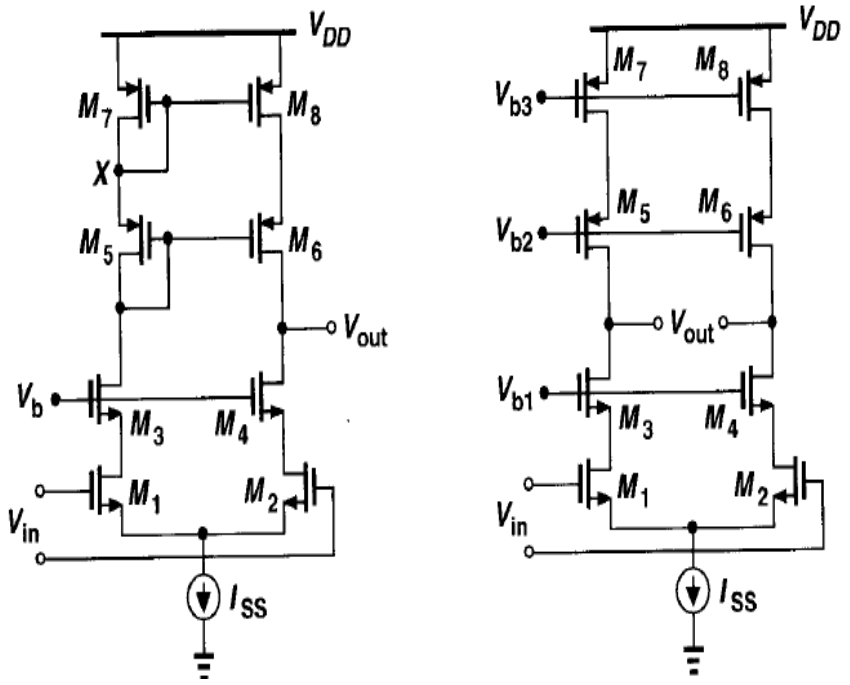


Figure 3.11 Cascode OTA with single ended and double ended output

3.6.4 Folded cascode Topology

In order to alleviate the drawback of telescopic cascode, namely, limited output swing and difficulty in shorting the input and output, a "Folded Cascode" can be used. In the circuit shown in Figure 3.12, the small-signal current generated by M_1 flow through M_2 and subsequently the load, which can produce an output voltage $g_{m1}R_{out}V_{in}$. The primary advantage of folded cascode structure lies in the choice of voltage level because it does

not stack the cascode transistor on the top of the input device. The idea in figure 3.11 shown Figure 3.13, the resulting circuit replaces the NMOS input pair with PMOS counterpart.

In figure 3.13(a), one bias current I_{SS}, provides the drain current of the both the input transistor and cascode devices, whereas n fig 3.13(b) input requires an additional bias current i.e. $I_{SS1} = I_{SS}/2 + I_{D3}$. Thus, folded cascode consume higher power. In figure 3.13(a) input CM level cannot exceed $V_{b1} - V_{GS3} \_ V_{TH1}$ where as in figure 3.13(b) in cannot be less than $V_{b1} - V_{GS3} \_ V_{THP}$.

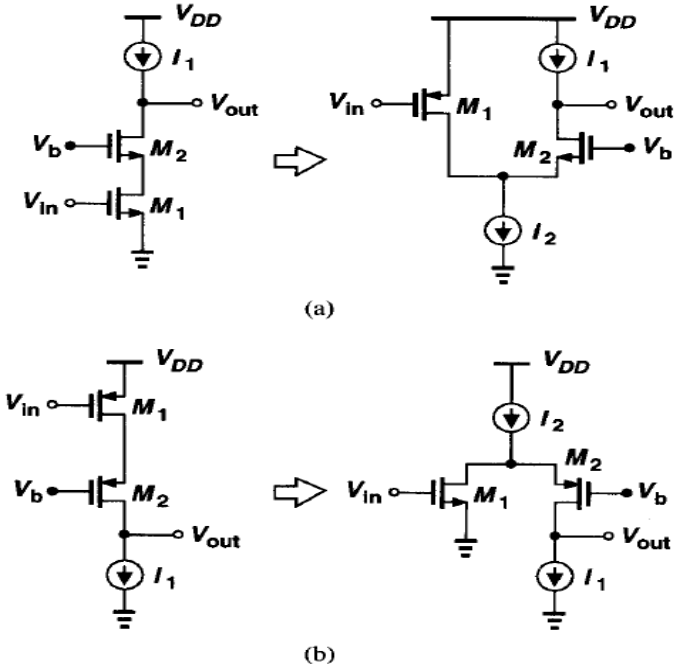


Figure 3.12 Folded Cascode Circuits

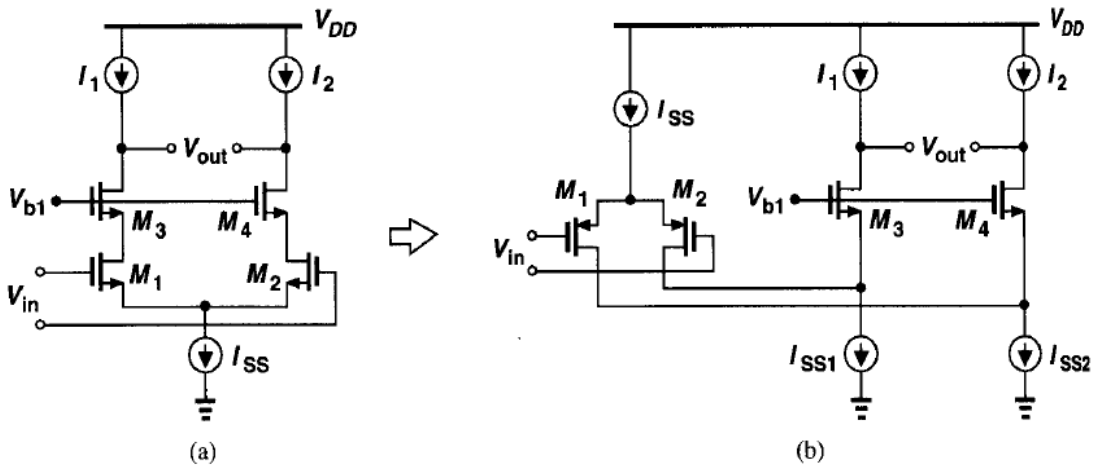


Figure 3.13 Folded Cascode Topology

3.6.5 Two Stage Topology

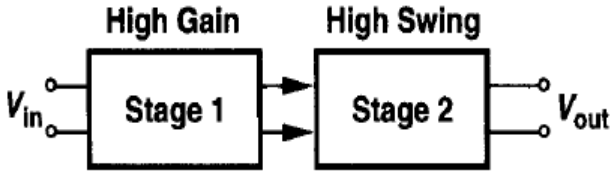


Figure 3.14 Two Stage op-amp

The gain of one-stage topologies is limited to the input pair transconductance and the output impedance. Two-stage op amps consist of first stage providing a high gain and the second providing large swing. The first stage incorporates various amplifier topologies, but the second stage is typically configured as a simple common- source stage to allow maximum output swings. Each stage in figure 3.14 can incorporate various amplifier topology but second stage is typically is simple common source stage, so allow maximum output swing.

In figure 3.15 two stage op amp, first and second stage exhibit gain which is equal to $g_{m1,2}(r_{o1,2} \square r_{o3,4})$ and $g_{m5,6}(r_{o5,6} \square r_{o7,8})$, respectively.

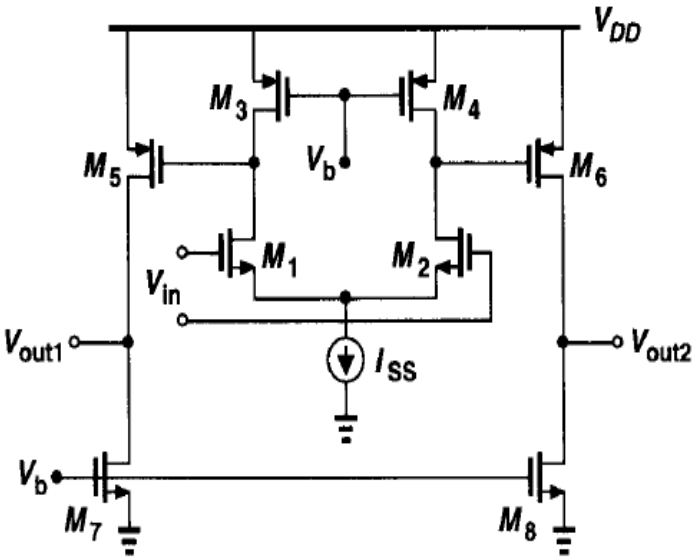


Figure 3.15 Simple Two Stage op-amp

The overall gain is therefore comparable with that of cascode op amp, but the swing at V_{out1} and V_{out2} is equal to $V_{DD} - V_{OD5,6} - V_{OD7,8}$. To obtain higher gain, first stage can incorporate cascode devices as in fig 3.16. The overall gain can be expressed as:

$$A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{o3,4}r_{o1,2}] \square [(g_{m5,6} + g_{mb5,6})r_{o5,6}r_{o7,8}]\} X [g_{m9,10}(r_{o9,10} \square r_{o11,12})]$$

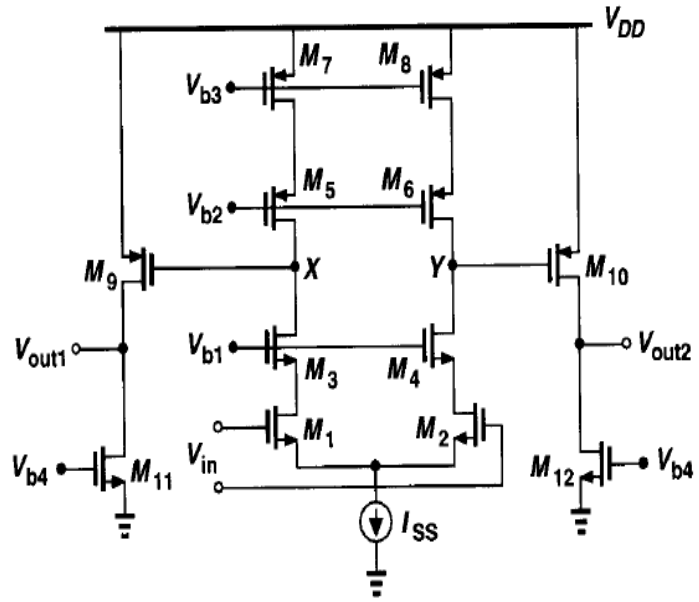


Figure 3.16 Two Stage op-amp with cascoding

Each stage introduce at least one pole in open loop transfer function, making it difficult to guarantee stability in feedback using op amp, so op amp with more than two stage is rarely used.

3.6.6 Two Stage, Telescopic, & folded-cascode Topology: Discussion

Two stage op-amp has high output voltage swing and high power consumption because if its two stage.

The overall voltage swing of a folded-cascode op-amp is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies, and higher noise.
Folded-cascode op-amps are used quite widely, even more than telescopic topologies, because the input and outputs can be shorted together and the choice of the input common-mode level is easier. In a telescopic op amp, three voltages must be defined carefully: the input CM level and the gate bias voltages of the PMOS and NMOS cascode transistors, whereas in folded-cascode configurations only the latter two are critical.

In folded-cascode op-amps, the capability of handling input CM levels are close to one of the supply rails. The folded cascode stage also has more devices, which contribute significant input referred thermal noise to the signal.Telescopic op-amp has severely limited output swing and hence the dynamic range. It is smaller than that of Folded Cascode because the tail transistor directly cuts into output swing from both side of op-amp.

Table 3.2: Comparison between Single and Multistage OTA

Single Stage OTA	Multi Stage OTA
• Single high impedance (voltage gain) node • Near maximum power efficiency • Limited gain and/or output range • Can be combined with cascodes, gain boosting **Examples:** **Telescopic OTA** • Maximum power efficiency • Limited input common-mode range **Folded cascode** • Large input common-mode range • Slightly improved output range • Folding adds noise and power penalty	**Advantages** over single stage OTA • Reduced interaction between gain and output range • Somewhat higher drive capability for given C_{in} **Disadvantages** • Increased power dissipation or reduced speed • Need for compensation **Examples:** • Miller-compensated 2-stage OTA • Nested Miller compensation

3.7 g_m / I_d Methodology

The present trend toward portable equipment as well as the increasing circuit density and size of integrated Systems tend to make low power consumption a primary concern [97], [98]. In CMOS analog circuits the minimum power consumption is achieved when MOS transistors operate in the weak inversion region [99]. However, the best compromise in terms of consumption and speed is achieved in moderate inversion.

Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (GVO) as the key parameter, where GVO = $(V_{gs} - V_{TH})$ V_{gs} being the gate voltage and V_{TH} the threshold voltage [100-101]. Micro power design techniques, on the other hand, exploit known weak inversion models [99, 102].Here,design methodology

that allows a unified synthesis methodology in all regions of operation of the MOS transistor. It provides an alternative taking full advantage of the moderate inversion region to obtain a reasonable speed power compromise. The method exploits the transconductance over dc drain current ratio (g_m / I_d) relationship versus the normalized current ($I_d /(W / L)$.

The long-channel design has different set of equations which govern each region of operation. The overdrive voltage Vov is a key parameter which defines the region the device is operating in. The g_m / I_d method characterizes the performance of a transistor in all regions of operation [103]. The following section develops the long-channel equations of the transistor. From these equations we derive the figure of merits for the g_m / I_d method. For the figure 3.17, assume device in strong inversion and saturation.

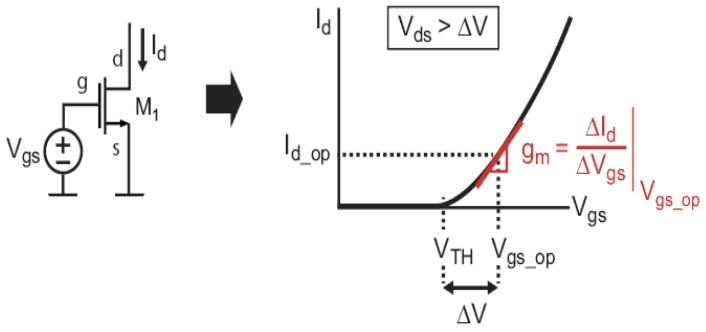


Figure 3.17 nMOS Device Operated in Strong Inversion and Saturation

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{TH})^2(1 + \lambda V_{ds})$$

----------(3.12)

$$\Rightarrow g_m \approx \frac{\partial I_d}{\partial V_{gs}} \approx \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{TH}) \approx \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}$$

----------(3.13)

$$\Rightarrow g_m \approx \frac{I_d \sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\sqrt{I_d}} \approx \frac{2I_d}{(V_{gs} - V_{TH})}$$

----------(3.14)

The maximum speed of an amplifier is limited by the the transconductance ratio of and the capacitance of a transistor.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{db}}$$

----------(3.15)

f_T is a key parameter for characterizing the achievable gain·bandwidth product with circuits that use the device with assumption that CMOS device follow the square law relationship.

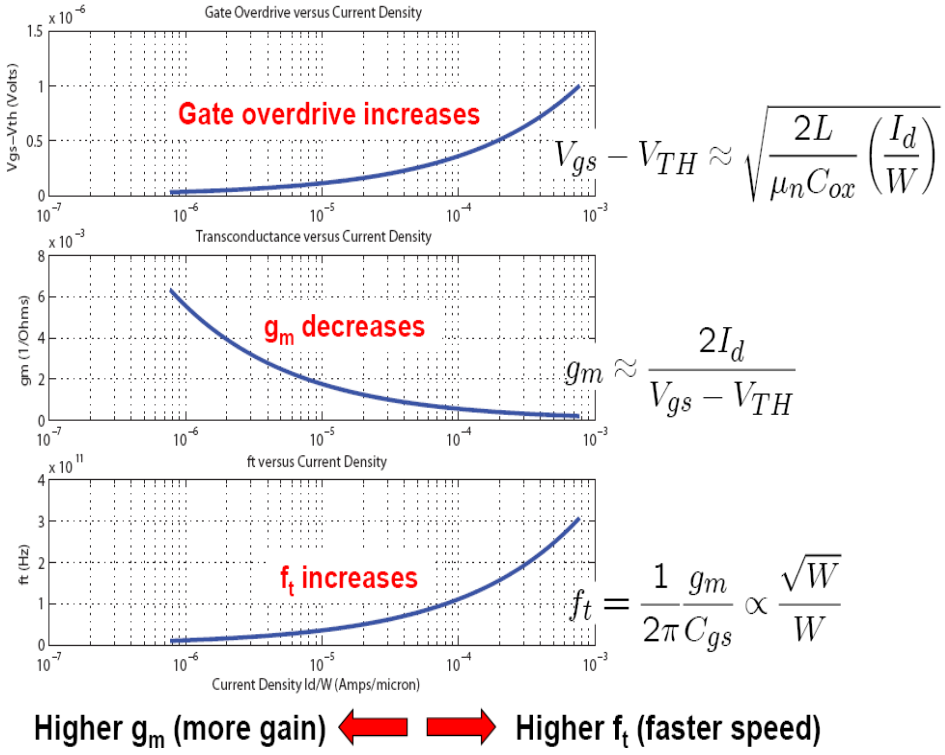
$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{TH})^2$$

$$\Rightarrow V_{gs} - V_{TH} \approx \sqrt{\frac{2L}{\mu_n C_{ox}} (\frac{I_D}{W})} \qquad g_m \approx \frac{2I_d}{(V_{gs} - V_{TH})}$$

----------(3.16)

These formulations are only accurate over a narrow region of strong inversion (with the device in saturation).

Strong Inversion($V_{gs} > V_{TH}$)	**Weak Inversion($V_{gs} < V_{TH}$)**
Poor g_m Efficiency (g_m / I_d Low) But Fast Speed	Good g_m Efficiency (g_m / I_d High) But Slow Speed
Key Device Parameter Calculated as: $g_m = \frac{2I_d}{(V_{gs} - V_{TH})}$ $g_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_F + V_{SB}}}$ $r_0 = \frac{1}{\lambda I_d}$	Key Device Parameter Calculated as: $g_m \approx (\frac{1}{n})\frac{I_d}{V_t}$ $g_{mb} \approx \frac{n-1}{n}(\frac{I_d}{V_t})$ $r_0 = \frac{1}{\lambda I_d}$
Moderate Inversion: Compromise Between the two	

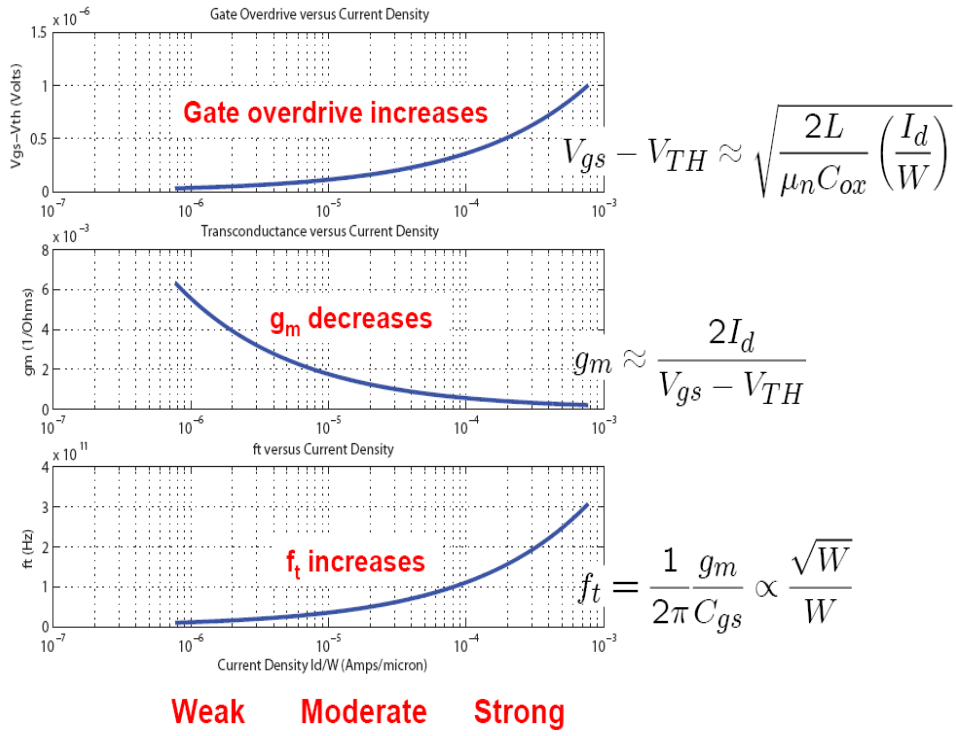


$$V_{gs} - V_{TH} \approx \sqrt{\frac{2L}{\mu_n C_{ox}}\left(\frac{I_d}{W}\right)}$$

$$g_m \approx \frac{2I_d}{V_{gs} - V_{TH}}$$

$$f_t = \frac{1}{2\pi}\frac{g_m}{C_{gs}} \propto \frac{\sqrt{W}}{W}$$

Figure 3.18 Transconductance Efficiency Vs f_T



$$V_{gs} - V_{TH} \approx \sqrt{\frac{2L}{\mu_n C_{ox}}\left(\frac{I_d}{W}\right)}$$

$$g_m \approx \frac{2I_d}{V_{gs} - V_{TH}}$$

$$f_t = \frac{1}{2\pi}\frac{g_m}{C_{gs}} \propto \frac{\sqrt{W}}{W}$$

Figure 3.19 Transistor "Inversion" Operating Region

The performance of any analog circuit can be broadly divided into its large signal and small signal characteristics. The current I_d determines the power dissipation; voltage V_{DS} the available signal swing, transconductance g_m signifies speed and voltage gain; the intrinsic capacitances $(C_{gs} + C_{gd} + C_{db})$ determine the speed and the output impedance; r_0 the voltage gain of the circuit.

The choice of g_m / I_d is based on its relevance for the three following reasons.

1) It is strongly related to the performances of analog.

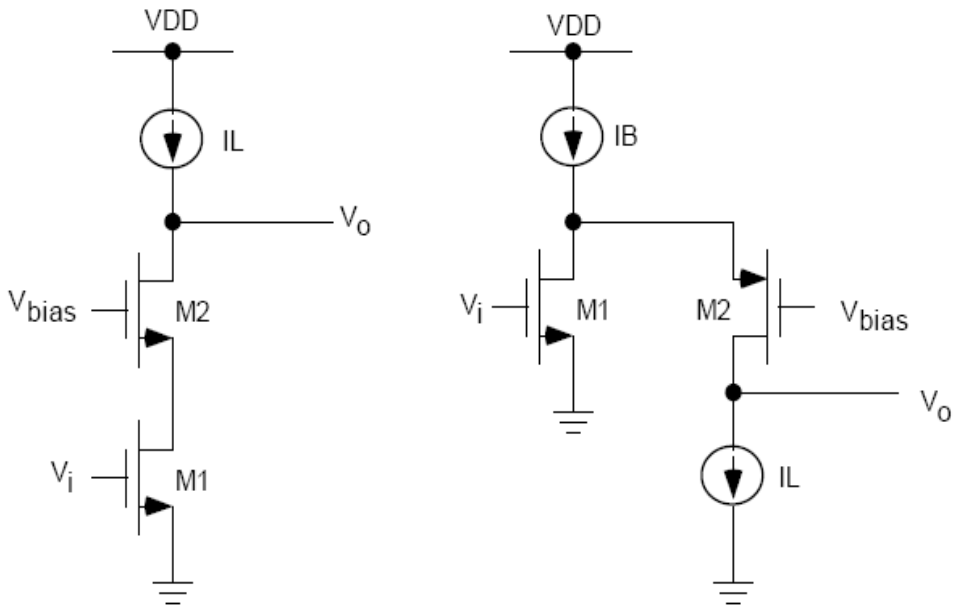
2) It gives an indication of the device operating region.

3) It provides a tool for calculating the transistors dimensions

3.8 Why Folded Cascode OTA?

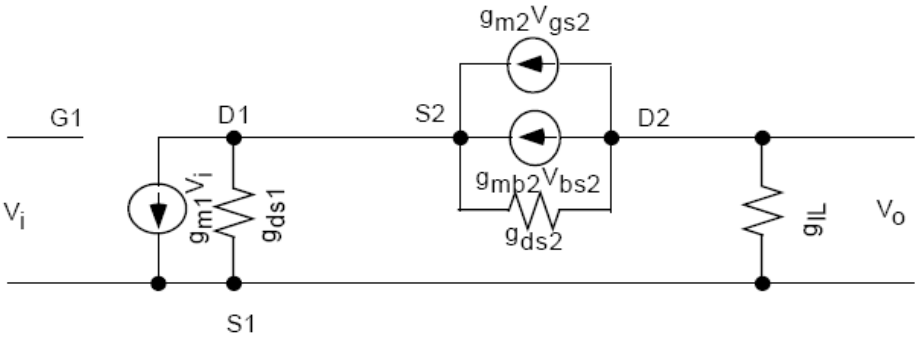
The gain that can be achieved by a single stage is around 30 dB. Thus, in order to achieve higher gain it is necessary to use a cascade of two stages. However, two stages bring about two poles one close to the other and this requires compensation network, besides increasing the complexity, reduces the design flexibility. A cascade with cascode load permits us to achieve high gain without the disadvantage of having two poles one close to each other.

Therefore the use of cascode based OTA is an interesting solution alternative to the two stages OTA. Thus two options have been left; one is "Telescopic configuration" and the other one is "folded cascode" configuration. The primary advantage of folded structure lies in the choice of voltage levels because it does not "stack" the cascode transistor on the top of the input device. Further Telescopic OTA suffers with limited output swing and hence the dynamic range. It is smaller than that of Folded Cascode because the tail transistor directly cuts into output swing from both side of op-amp.

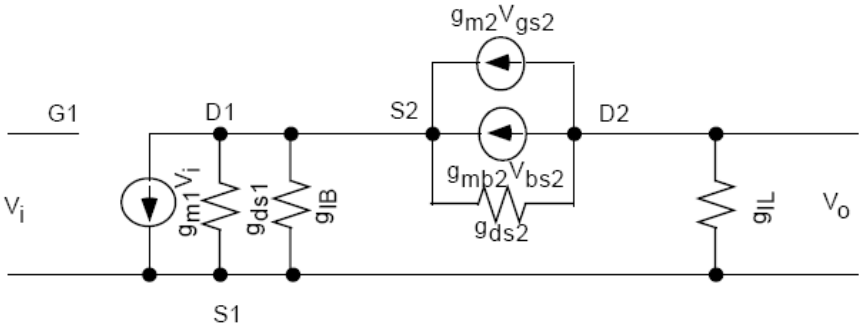


(a) (b)

Figure 3.20 (a) TelescopicCascode (b) Folded Cascode



(a)



(b)

Figure 3.21 Equivalent Circuit of (a) Telescopic Cascode and (b) Folded Cascode

3.8.1 Basic Configuration of CMOS Folded cascode OTA

The folded-cascode OTA is shown in Figure 3.22. The name "folded-cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the MOSFETs to n-channels. This OTA, like all OTAs, has good PSRR compared to the two-stage op-amp since the OTA is compensated with the load capacitance.

To understand the operation of the folded-cascode OTA, consider Figure 3.22 without the diff-amp M1/M2 in the circuit. Without the diff-amp present in the circuit, tail current flows in all MOSFETs. MOSFETs M3and M4 provide the DC bias voltages toM5-M8. Note that the cascoded MOSFETs (M9-M12) are not biased for wide-swing operation.

A wide-swing biasing circuit could replace M3/M4, and M9-M12 could be replaced with a wide-swing current mirror. Biasing for wide-swing operation increases the output

voltage swing. When the diff-amp is added back into the circuit, it steals half current from M7-M12, reducing their drain currents to divide by 2.

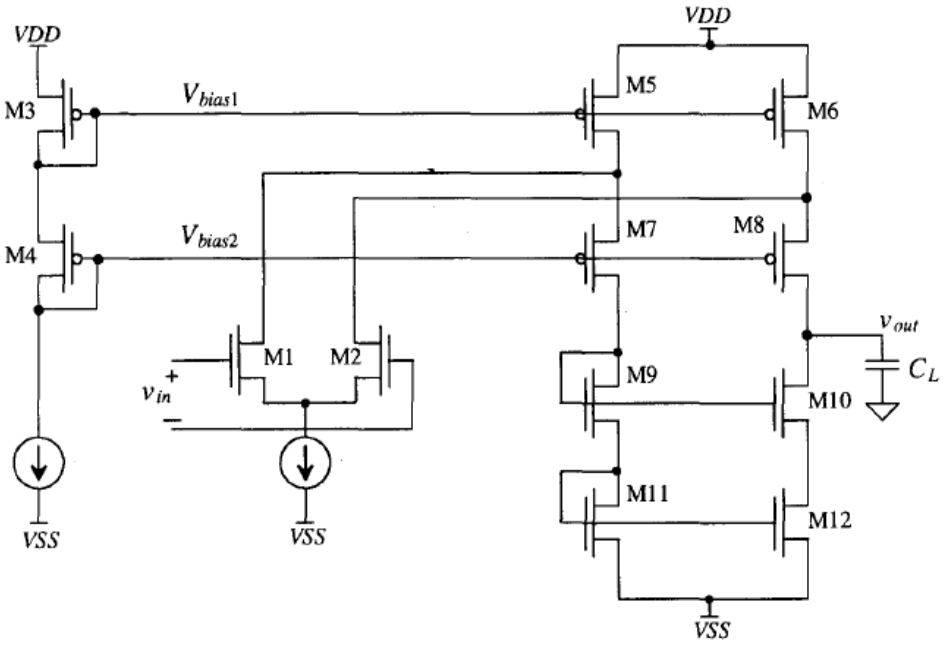


Figure 3.22 Folded Cascode OTA

Applying an AC input voltage, V_{in} causes the diff-amp differential drain current to become $g_m V_{in}$ (g_m is the transconductance of the diff-amp). This AC differential drain current is mirrored in the cascoded MOSFETs M7 through M12. The output voltage of the OTA is then

$$V_{out} = g_m V_{in} R_0$$

----------(3.17)

where

R_0 =(R looking in to drain of M10)□(R looking in to drain of M8)

$$=[r_{010}(1+g_{m10}r_{012})]\square[r_{08}(1+g_{m08}r_{06})]$$

The gain of the folded-cascode OTA is given by

$$\frac{V_{out}}{V_{in}} = g_m R_0$$

The dominant pole of the OTA is located at $1/2\pi R_0 C_L$ • Parasitic poles exist at the sources of M7/M8 and M9/M1O. These parasitic poles should be larger than the unity gain frequency $f_u = \frac{g_m}{2\pi C_L}$ of the OTA.

3.8.2 CMOS Differential Amplifier(N-Channel) with Current Mirror

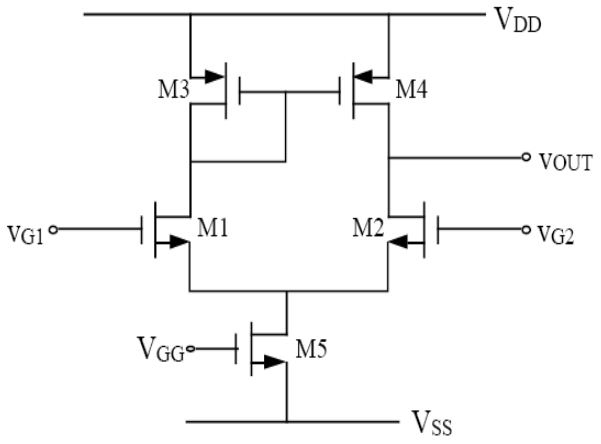
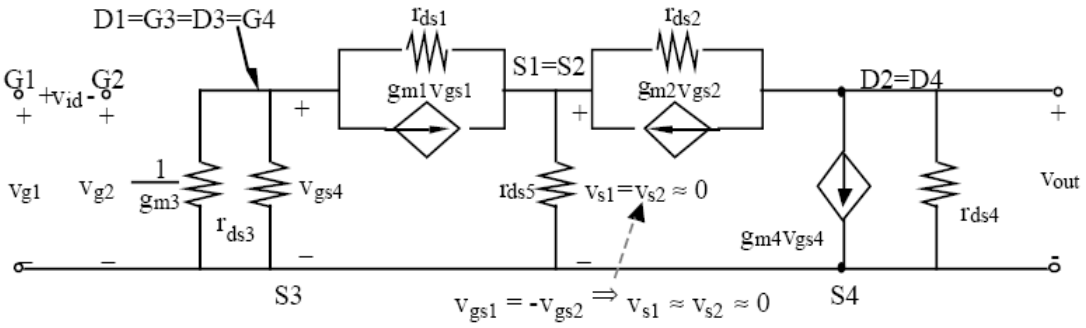
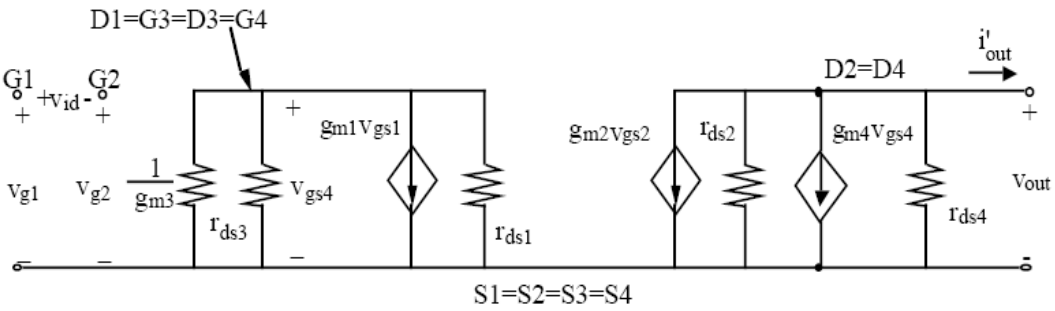


Figure 3.23 N-Channel Input Pair Differential Amplifier



(a)



(b)

Figure 3.24(a) Small Signal Model and (b) Simplified Small Signal Model using symmetry

Unloaded Differential Transconductance Gain:

$$i_{out}' = -V_{gs4}g_{m4} - g_{m2}V_{gs2} = \frac{g_{m1}g_{m4}(r_{ds1} \parallel r_{ds3})}{1+g_{m3}(r_{ds1} \parallel r_{ds3})}V_{s1} - g_{m2}V_{gs2}$$

If $g_{m3}(r_{ds1} \parallel r_{ds3}) >> 1, g_{m3} = g_{m4},\ g_{m1} = g_{m2} = g_{md}$ then

$$i_{out}' \approx g_{m1}V_{gs1} - g_{m2}V_{gs2} = g_{md}(V_{gs1} - v_{gs2}) = g_{md}V_{id}$$

$$i_{out}' \approx g_{md}V_{id} = \sqrt{\frac{K_N' W I_{SS}}{L}}V_{id}$$

----------(3.18)

Thus we have a single output which is proportional to the difference of inputs. **The effective G_m is just the g_m of either of the diff-pair transistors.**

Unloaded Differential Voltage Gain:

$$V_{out} \approx \frac{g_{md}}{g_{ds2}+g_{ds4}}V_{id} = \frac{2}{\lambda_N + \lambda_P}\sqrt{\frac{K_N' W}{L I_{SS}}}V_{id}$$

----------(3.19)

Parasitic Capacitances:

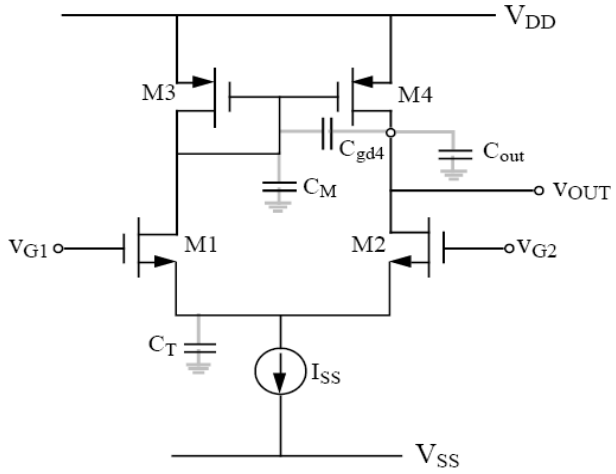


Figure 3.25 Parasitic Capacitances

C_T = Tail Capacitor (Common Mode only)

C_M = Mirror Capacitor = $C_{dg1} + C_{db1} + C_{gs3} + C_{gs4} + C_{db3}$

C_{OUT} = Output Capacitor = $C_{bd4} + C_{bd2} + C_{gd2} + C_L$

Small Signal Model:

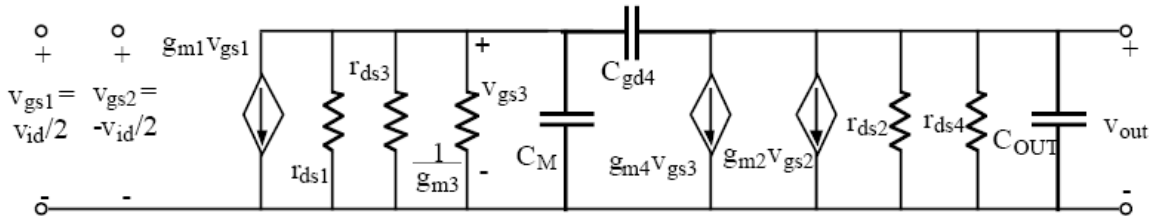


Figure 3.26 Parasitic Capacitance with Small Signal Model

3.8.3 CMOS Differential Amplifier(P-Channel) with Current Mirror

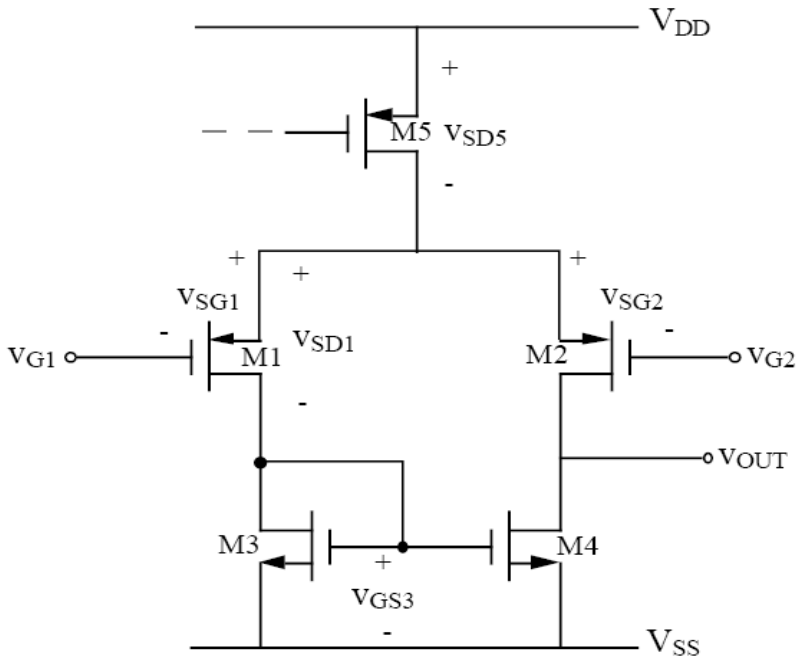


Figure 3.27 P-Channel Differential Amplifier with Current Mirror

Lowest common mode input voltage at gate of M1 (M2)

$$V_{G1(\min)} = V_{SS} + V_{GS3} + V_{SD1} - V_{SG1}$$

For saturation, the minimum value of:

$$V_{SD1} = V_{SG1} - V_{T1}$$

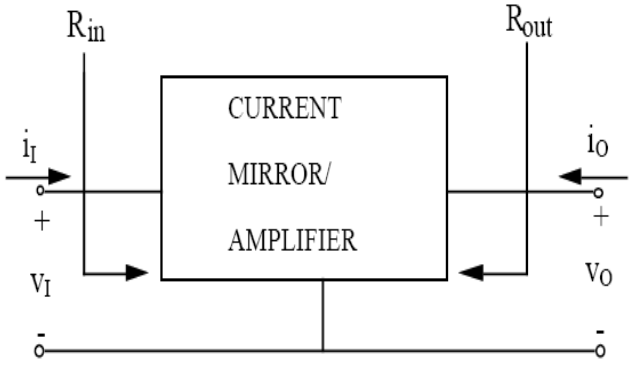
$$\text{Therefore } V_{G1(\min)} = V_{SS} + V_{GS3} - V_{T1}$$

$$\text{or } V_{G1(\min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta}} + V_{TO3} - V_{T1}$$

$$V_{G1(\max)} = V_{DD} - V_{SD5} - V_{SG1} = V_{DD} - V_{SD5} - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{T1}$$

----------(3.20)

3.8.4 What is Current Mirror?



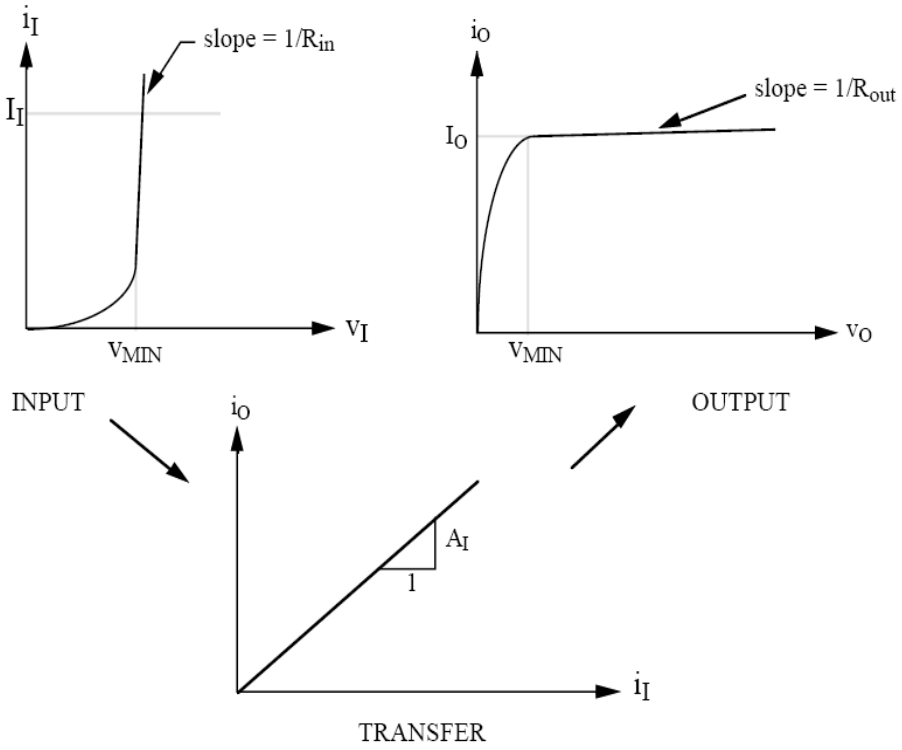


Figure 3.28 Graphical Characterization of current Mirror

Ideally: $i_0 = A_I i_I$

$R_{in} \approx 0$

$R_{out} \approx \infty$

3.8.5 Cascode Current Mirrors

This configuration is used to increase the output resistance of current source or sink. Increasing the outputresistance of a current source or sink is simply a matter of stacking up the MOSFETs until the desired output resistance is reached. The limitation of stacking a large number of cascode devices is the increase in the minimum voltage across the current source/sink needed to keep the entire device in saturation.

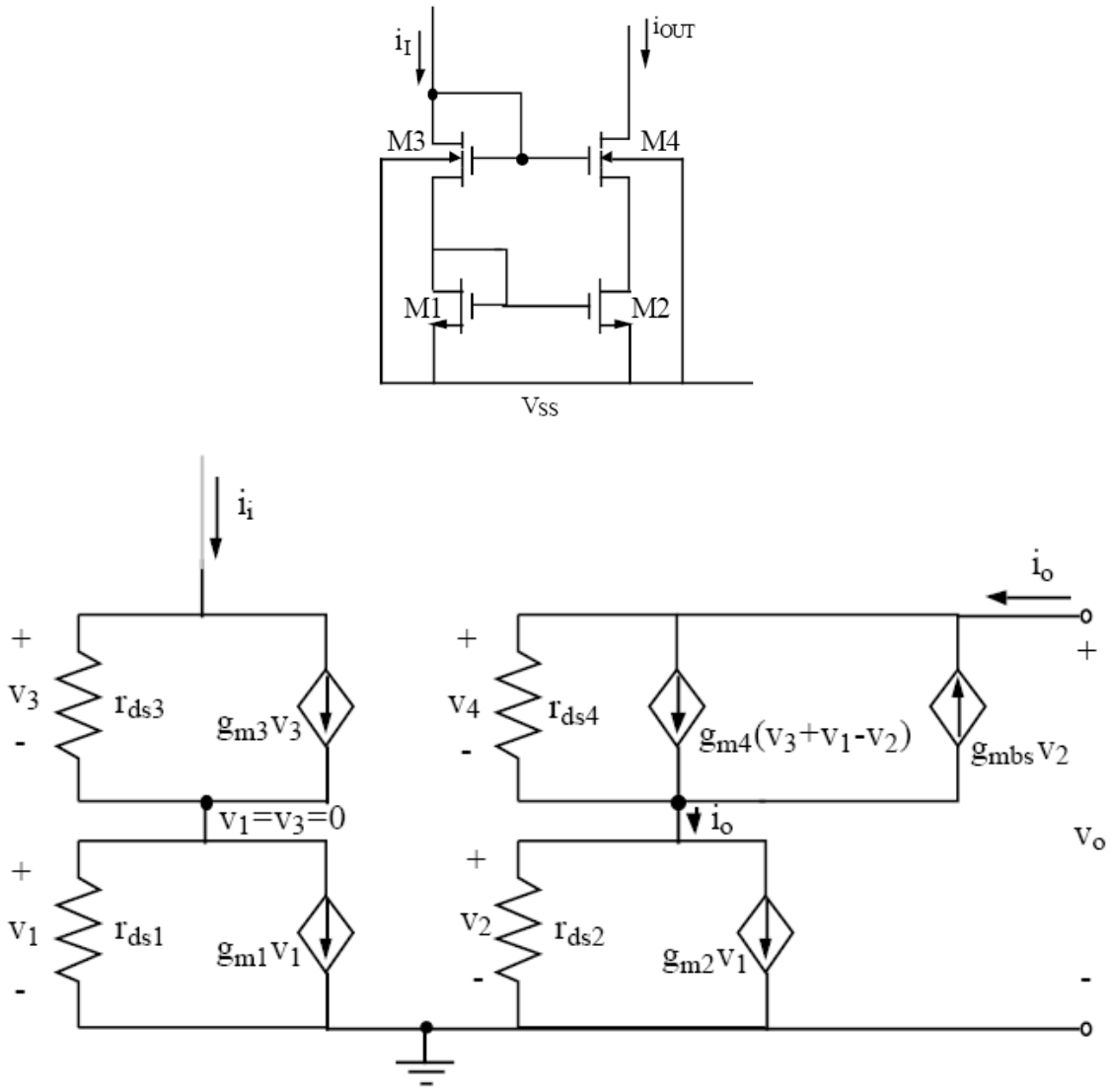


Figure 3.29 Cascode Current Mirror and its small signal Model

Calculation of Output Resistance:

$$V_0 = V_4 + V_2 = r_{ds4}[i_0 - g_{m4}(V_3 + V_1 - V_2) + g_{mbs4}V_2] + r_{ds2}(i_0 - g_{m2}V_1)$$

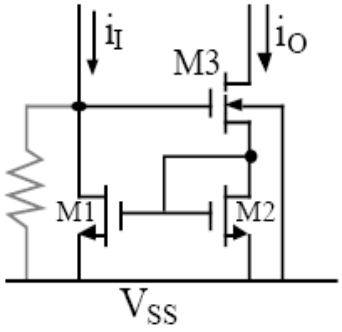
$$V_2 = r_{ds2}i_0$$

$$V_0 = i_0[r_{ds4} + (g_{m4}r_{ds2})r_{ds4} + (r_{ds2}g_{mbs4})r_{ds4} + r_{ds2}]$$

$$r_{out} = \frac{v_0}{i_0} = r_{ds4} + r_{ds2} + r_{ds2}r_{ds4}(g_{m4}g_{mbs4})$$

----------(3.21)

3.8.6 Wilson Current Mirror



Principle of Operation:

Series negative feedback increase output resistance

1. Assume input current is constant and that there is high resistance to ground from the gate of M3 or drain of M1.
2. A positive increase in output current causes an increase in V_{GS2}.
3. The increase in V_{GS2} causes an increase in V_{GS1}.
4. The increase in V_{GS1} causes an increase in i_{D1}.
5. If the input current is constant, then the current through the resistance to ground from the gate of M3 or the drain of M1 decreases resulting in a decrease in V_{GS3}.
6. A decrease in V_{GS3} causes a decrease in the output current opposing the assumed increase in step 2.

Output Impedance of the Wilson Current Source:

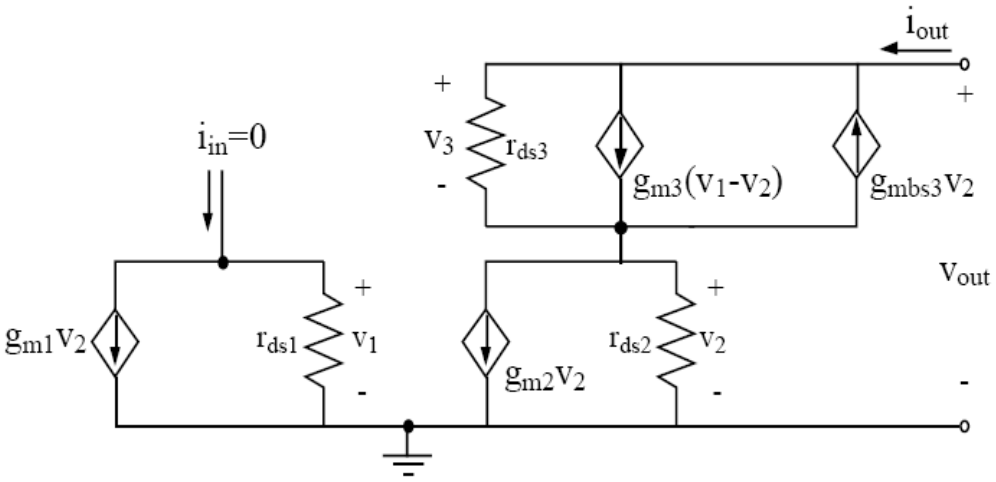


Figure 3.30 Small Signal Model of Wilson Current Mirror

$$V_{out} = r_{ds3}[i_{out} - g_{m3}V_1 + g_{m3}V_2 + g_{mbs3}V_2] + V_2$$

$$V_{out} = r_{ds3}i_{out} - g_{m3}r_{ds3}(-g_{m3}r_{ds1}V_2) + g_{m3}r_{ds3}V_2 + g_{mbs3}r_{ds3}V_2 + V_2$$

$$V_2 = i_{out}[\frac{r_{ds2}}{1 + r_{ds2}g_{m2}}]$$

$$V_{out} = r_{ds3}i_{out} + [g_{m3}r_{ds3} + g_{mbs3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3}]V_2 + V_2$$

$$r_{out} = r_{ds3} + r_{ds2}[\frac{1 + g_{m3}r_{ds3} + g_{mbs3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + r_{ds2}g_{m2}}]$$

$$r_{out} \approx \frac{r_{ds2}g_{m1}r_{ds1}g_{m3}r_{ds3}}{r_{ds2}g_{m2}} \approx r_{ds1}(g_{m3}r_{ds3}) \text{ if } g_{m1} = g_{m2}$$

----------(3.22)

Improved Wilson Current Mirror:

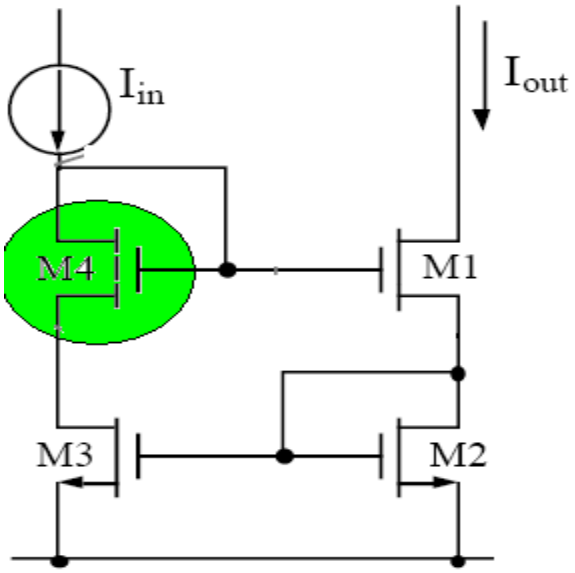


Figure 3.31 Improved Wilson Current Mirror

Additional diode-connected transistor equalizes the drain-source voltage drops of transistors M2 and M3.

Table 3.3: Summary of Current Mirrors

Current Mirror	Performance	Output Resistance	Minimum Voltage
Wilson Current Mirror	Excellent	$g_m r_{ds}^{\ 2}$	$2V_{ON}$
Cascode Current Mirror	Excellent	$g_m r_{ds}^{\ 2}$	$V_T + 2V_{ON}$

3.8.7 Designed Practical Folded cascode OTA

To understand the operation of the folded cascode OTA as shown in Figure 3.32, this last has a differential stage consisting of PMOS transistors M9 and M10 intend to charge Wilson mirror. MOSFETs M11 and M12 provide the DC bias voltages to M5-M6-M7-M8 transistors.The open-loop voltage gain is given by:

$$A_v = \frac{g_{m9} g_{m4} g_{m6}}{I_D{}^2 (g_{m4} \lambda_n{}^2 + g_{m6} \lambda_p{}^2)}$$

----------**(3.23)**

Where g_{m9}, g_{m4}, g_{m6} are the transconductance of Transistor M_9, M_4 and M_6. I_D is the bias current flowing in MOSFETs M_9, M_4 and M_6. C_L is the load capacitance at the output node. λ_n and λ_p are the parameter related to channel length modulation for NMOS and PMOS device. Taking the Complementarily between M_4 and M_6 so that:

$$g_{m4} = g_{m6}\,.$$

Gain Becomes

$$A_v = \frac{g_{m9} g_{m4}}{I_D{}^2 (\lambda_n{}^2 + \lambda_p{}^2)}$$

----------**(3.24)**

The unity gain frequency of the OTA is given by design strategy is given as:

$$f_u = \frac{g_{m9}}{2\pi C_L}$$

---------**(3.25)**

$$w_u \rightarrow \frac{g_{m9}}{I_D} \leftrightarrow \frac{I_D}{(\frac{W}{L})_9}$$

----------**(3.26)**

$$A_v \rightarrow \frac{g_{m4}}{I_D} \leftrightarrow \frac{I_D}{(\frac{W}{L})_4}$$

$$g_m = \sqrt{2k'(\frac{W}{L})I_d}$$

$$g_m = \frac{2I_d}{V_{gs} - V_{th}}$$

----------(3.27)

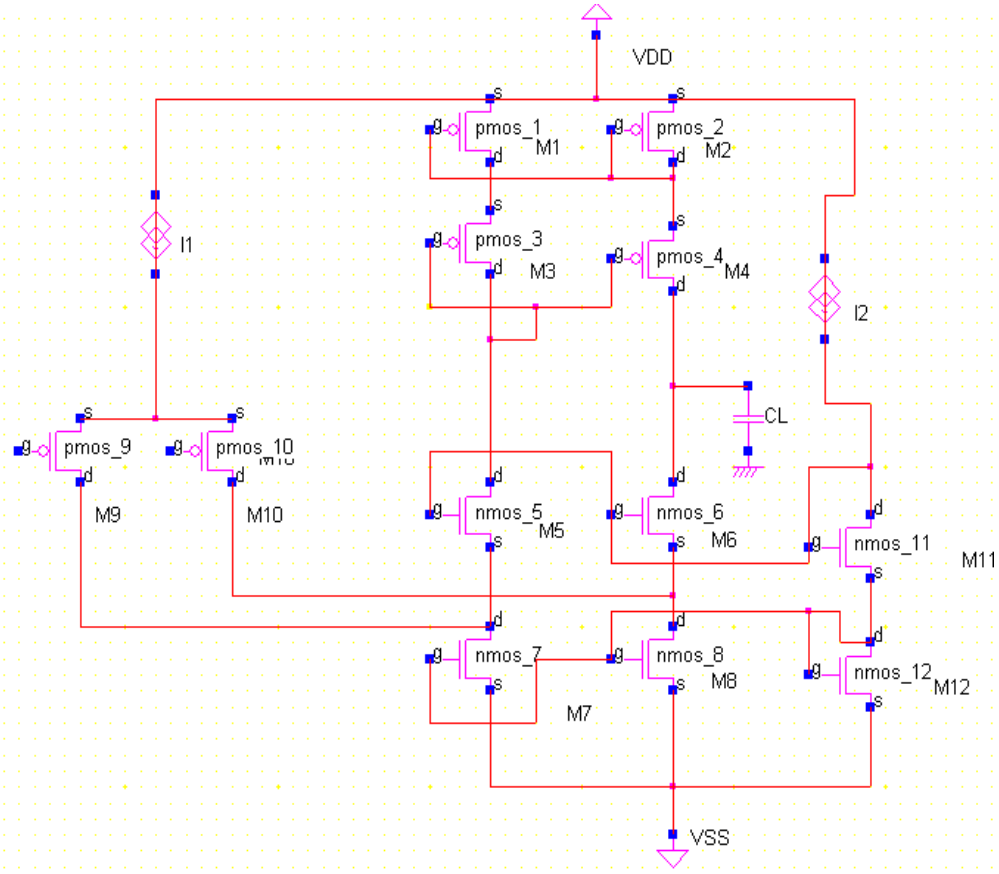


Figure 3.32 Designed Practical Folded Cascode OTA Schematic

Table 3.4: Specifications for Designed Practical Folded Cascode OTA

Specifications	Value
Gain(dB)	55
F_t (MHz)	400
Load Capacitor(pF)	0.1
Phase Margin(degree)	$>50^0$
Technology	$0.18\mu m$

Based on above specification and design equations **Sizing of Transistors** are as under.

Table 3.5 Calculated Design Parameter for Folded Cascode OTA

PARAMETER	VALUE
$g_{m9,10} / I_D(V^{-1})$	8.3
$I_D /(W / L)_{9,10}(\mu A)$	0.9
$g_{m4} / I_D(V^{-1})$	5.84
$I_D /(W / L)_4(\mu A)$	1.62

Table 3.6 Sizing of Transistor for Folded Cascode OTA

Transistor Width	Value(μm)
M_1, M_2, M_3, M_4	24.69
$M_5, M_6, M_7, M_8, M_{11}, M_{12}$	3.00
M_9, M_{10}	44.44

The designed **Folded Cascode OTA** was biased at **1.8V** power supply voltage using **CMOS technology of 0.18 µm with the BSIM3V3 (Level 49 Parameter) MOSFET model Parameter.**

3.9 Simulation Results of Wilson Current Mirror base Folded Cascode OTA

3.9.1 Gain and Unit Gain Band Width (UGBW) of Wilson Current Mirror base Folded Cascode OTA

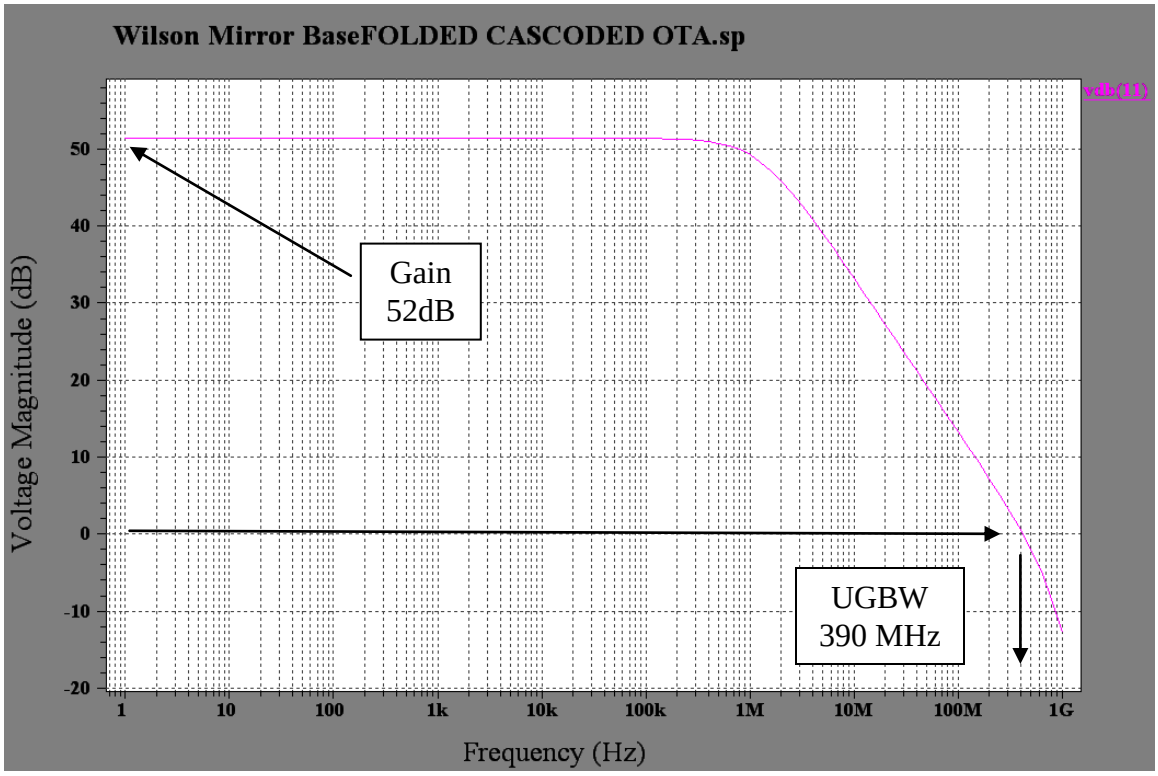


Figure 3.33 AC Analysis of Wilson Current Mirror base Folded Cascode OTA

3.9.2 Phase Margin of Wilson Current Mirror base Folded Cascode OTA

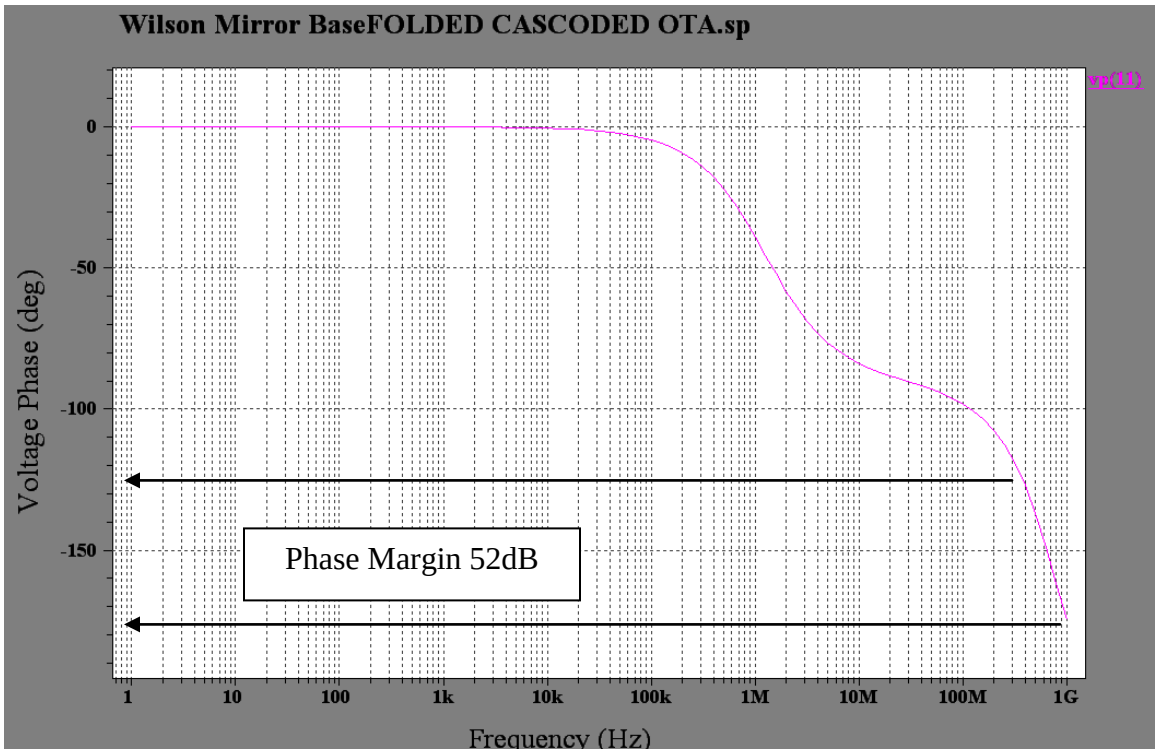


Figure 3.34 Phase Margin of Wilson Current Mirror base Folded Cascode OTA

3.9.3 Input/Output Swing and Offset of Wilson Current Mirror base Folded Cascode OTA

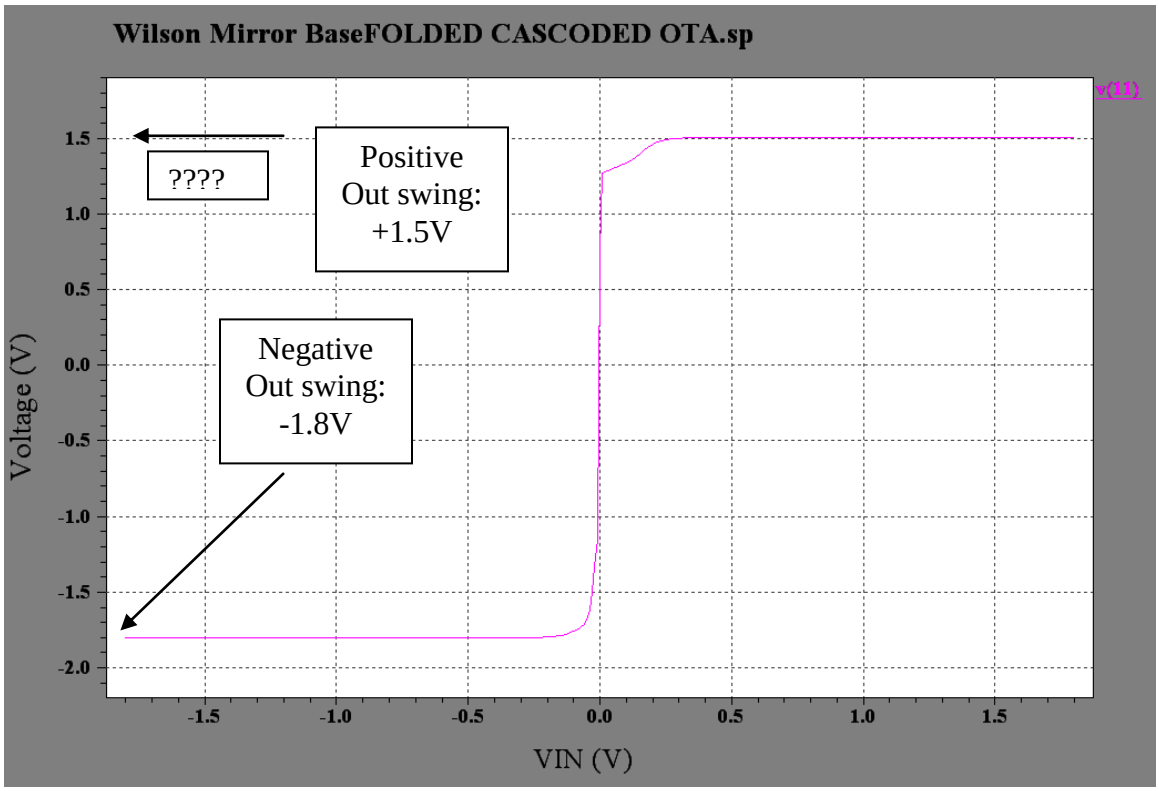


Figure 3.35 I/O Swing and Offset of Wilson Current Mirror base Folded Cascode OTA

3.9.4 Slew Rate of Wilson Current Mirror base Folded Cascode OTA

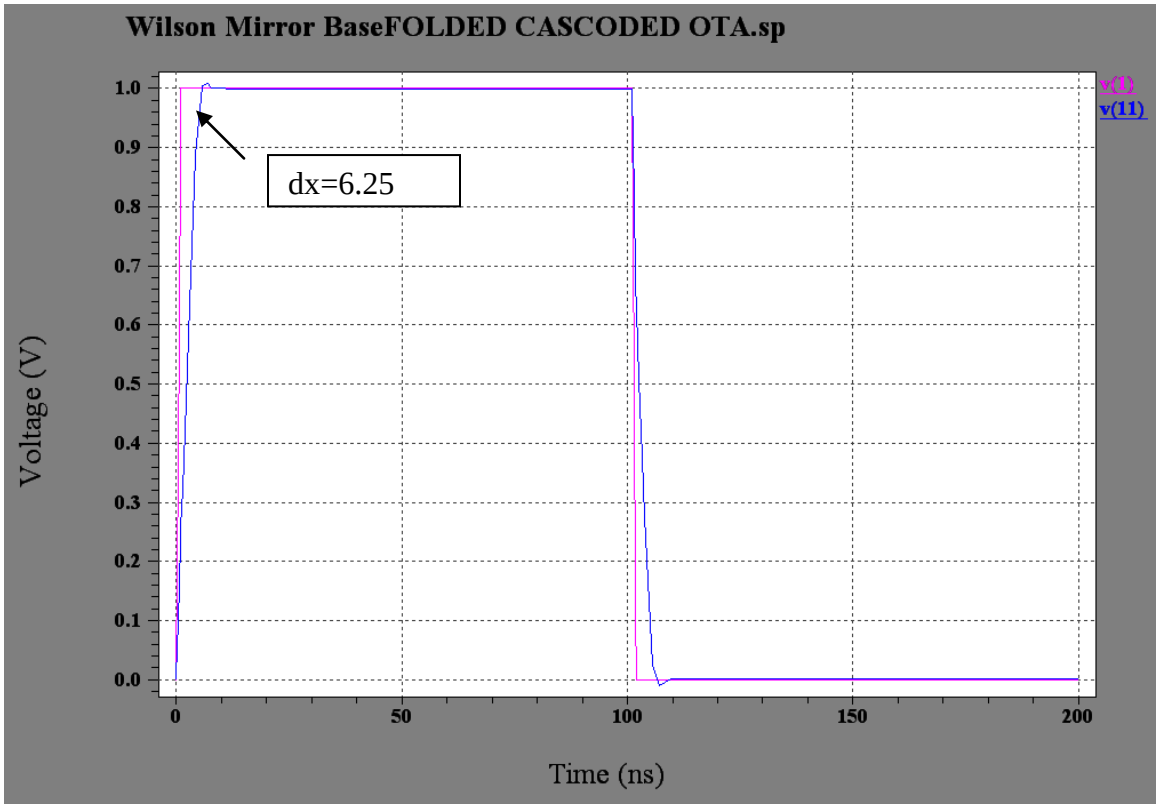


Figure 3.36 Slew Rate of Wilson Current Mirror base Folded Cascode OTA

3.9.5 Common Mode Gain of Wilson Current Mirror base Folded Cascode OTA

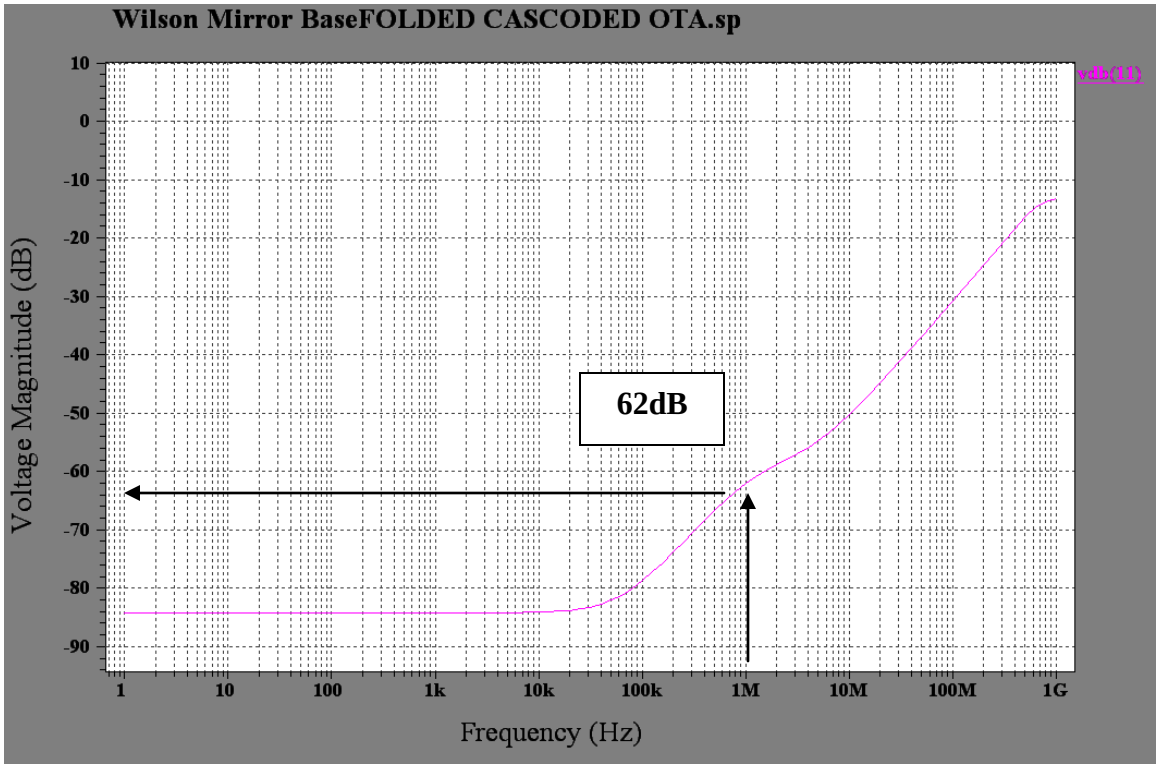


Figure 3.37 Common Mode Gain of Wilson Current Mirror base Folded Cascode OTA

3.9.6 Input Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

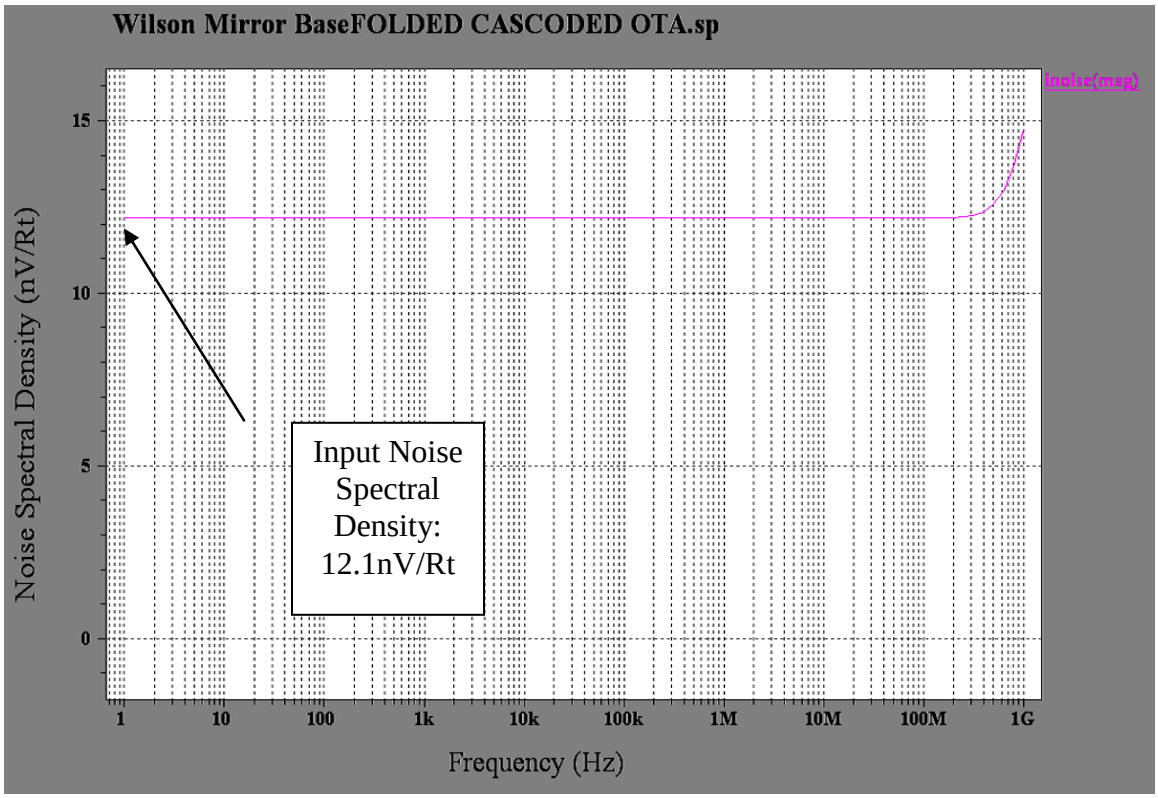


Figure 3.38 Input Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

3.9.7 Output Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

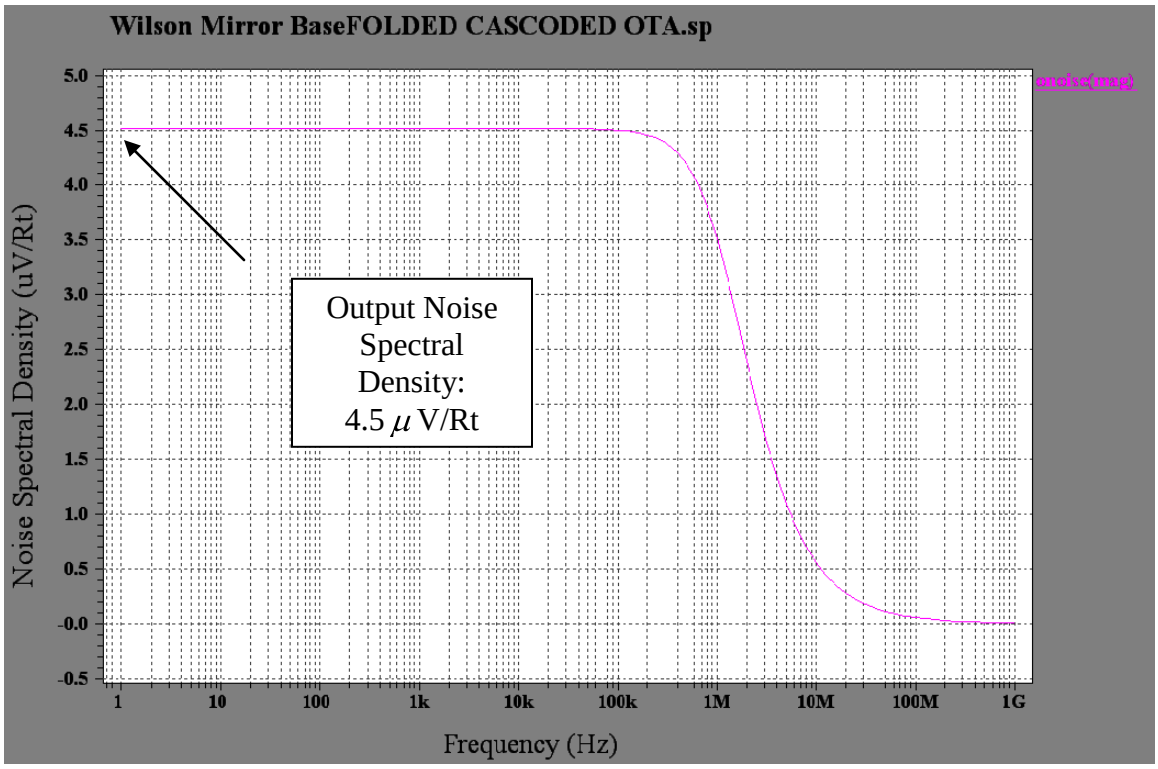


Figure 3.39 Output Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

3.9.8 Transient Analysis of of Wilson Current Mirror base Folded Cascode OTA

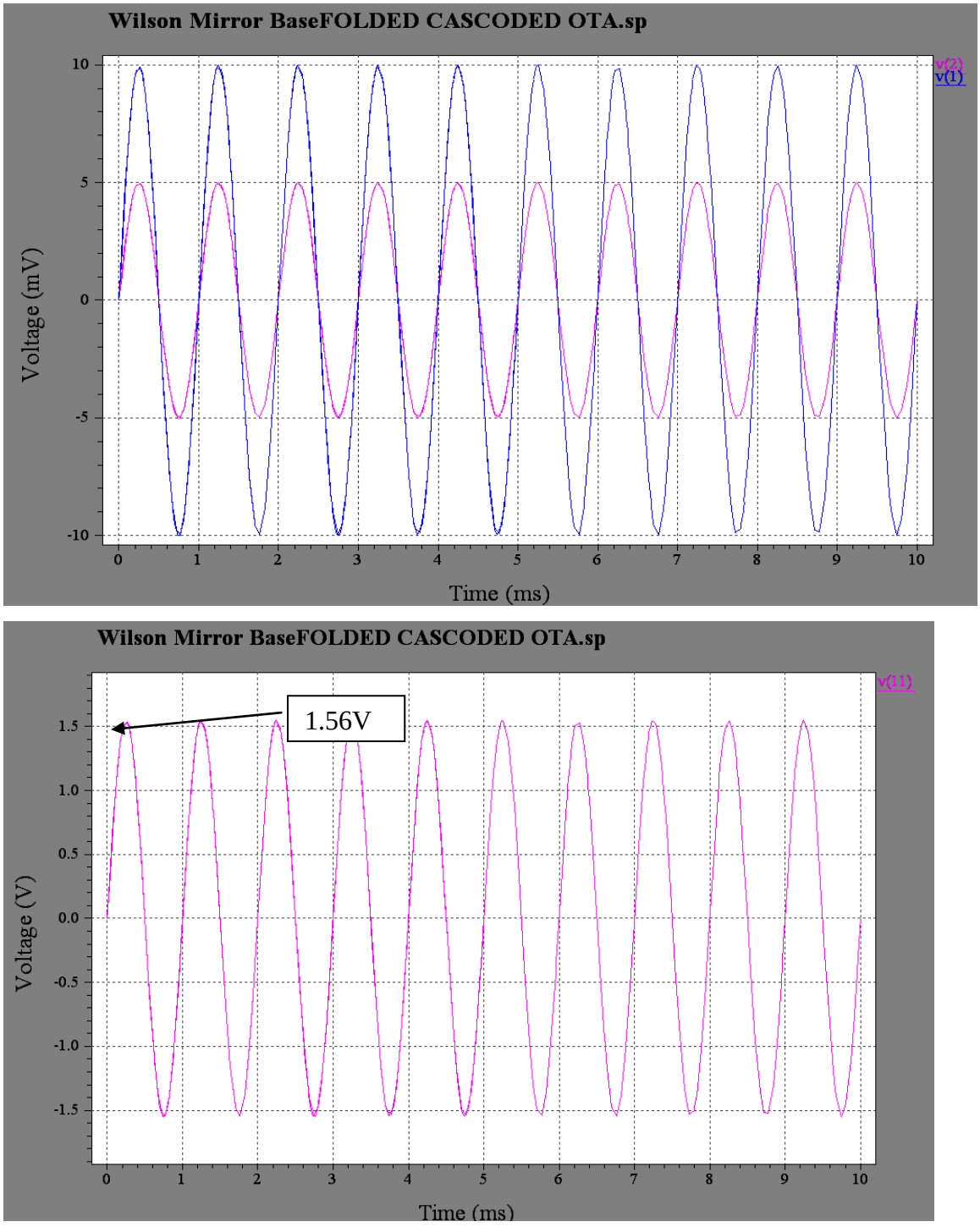


Fig 3.40 Differential Pair Inputs and Transient Analysis of Wilson Current Mirror base Folded Cascode OTA

3.9.9 ICMR of of Wilson Current Mirror base Folded Cascode OTA

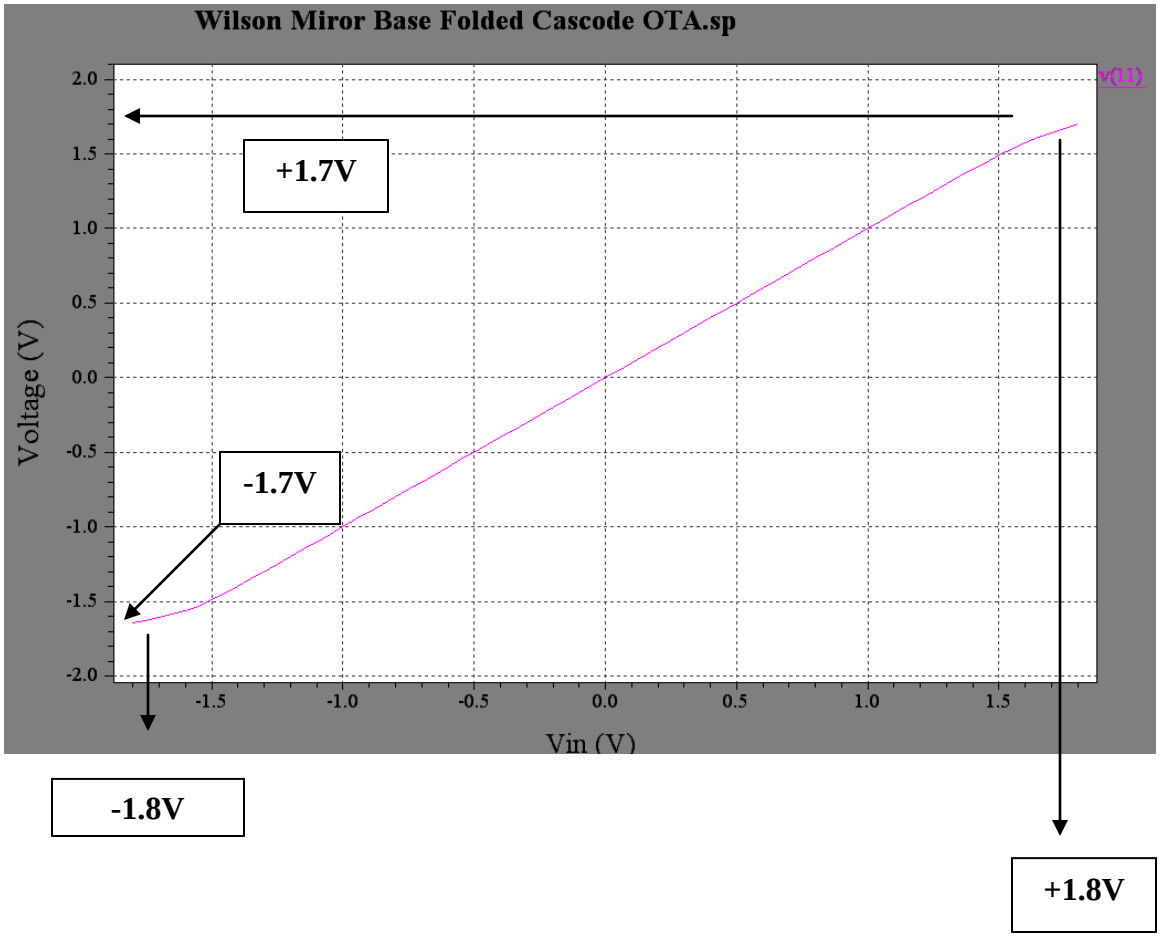


Fig 3.41 ICMR of Wilson Current Mirror base Folded Cascode OTA

3.10 Input-Output Noise per Device

Table 3.7: Input-Output Noise per device of Wilson Current Mirror base Folded Cascode OTA

Device	Input Noise per Device	Output Noise per Device
M1	1.92406E-04 V	3.24865E-03 V
M2	1.48551E-04 V	3.25518E-03 V
M3	4.83627E-05 V	9.85057E-05 V
M4	2.24518E-04 V	1.87938E-04 V
M5	8.04512E-05 V	2.33637E-04 V
M6	9.41097E-05 V	2.34209E-04 V
M7	2.05378E-04 V	3.64260E-03 V
M8	2.39759E-04 V	3.66058E-03 V
M9	2.18714E-04 V	3.44945E-03 V
M10	1.69629E-04 V	3.44791E-03 V
M11	4.91905E-05 V	2.11486E-05 V
M12	1.99607E-04 V	1.26429E-04 V

3.11 Summary of Simulated Results of Wilson Current Mirror base Folded Cascode OTA

Table 3.8: Summary of Simulated Results of Wilson Current Mirror base Folded Cascode OTA

Specifications	Simulated Results
Gain	52dB
UGBW	390MHz
Phase Margin	52 degree
CMRR@1Mhz	114dB
Offset Voltage	0.05V
Input/Output Swing	[-1.8V/ 1.5V]
Slew Rate	160V/μS
Input Noise spectral Density	12.1nV/Rt
Output Noise Spectral Density	4.5μV/ Rt
ICMR	-1.7V to 1.7V
Power Consumption	2.8885E-04 watts

3.12 Layouts and 3-D Process of Wilson Current Mirror base Folded Cascode OTA

Analog layout

In layout of digital circuits, the speed and the area are the two most important issues. In contrast, the layout for analog circuits, everything should be considered carefully. In analog layout more care has to be given as the circuit performance changes drastically due to noise, mismatch, crosstalk and shielding required to protect critical nodes from being disturbed. Without proper layout, the mismatches and coupled noise would be quite large and would significantly degrade the performance of the amplifier.

Analog layout issues

Device mismatch is often considered as part of main bottleneck of analog design. Random device mismatch plays important role in design of accurate analog circuits. The device mismatch is due to number of factor like local process variation, lithographic variations and process gradients. These factors affect all devices transistors, resistor and capacitor. During fabrication process mismatch in physical parameter like doping concentration(N_a), mobility(μ), oxide thickness and layout dimensions(W,L) gives origin to mismatch in electrical parameter like V_T ,β and thus mismatch in I_D.

Matching of all individual devices is of paramount concern in analog circuit design. Infact almost all of the ‘‘Analog Layout Techniques’’ are actually methods for improving matching between different devices on a chip. Matching is important because most of the analog circuit designs use a ratio base design technique. Some common techniques that help to improve device matching are MULTI-GATE FINGER LAYOUT and COMMON CENTROID LAYOUT.

Use of transistor fingering for large and critical transistor is always beneficial. In fingering, the transistor is ‘‘Fingered’’ into multiple transistors that are connected in

parallel. The folded transistor reduces the source/drain junction area and the gate resistance. The gate resistance can be reducing by decomposing the transistor into more parallel fingers. Random noise also dealt with circuit design level. However there are some layout techniques which can help to reduce random noise. The gate resistance of the poly-silicon and neutral body region, which are both random noise sources, is reduced by multi-gate finger layout.

Width: 33.2µm
Height: 41.2µm

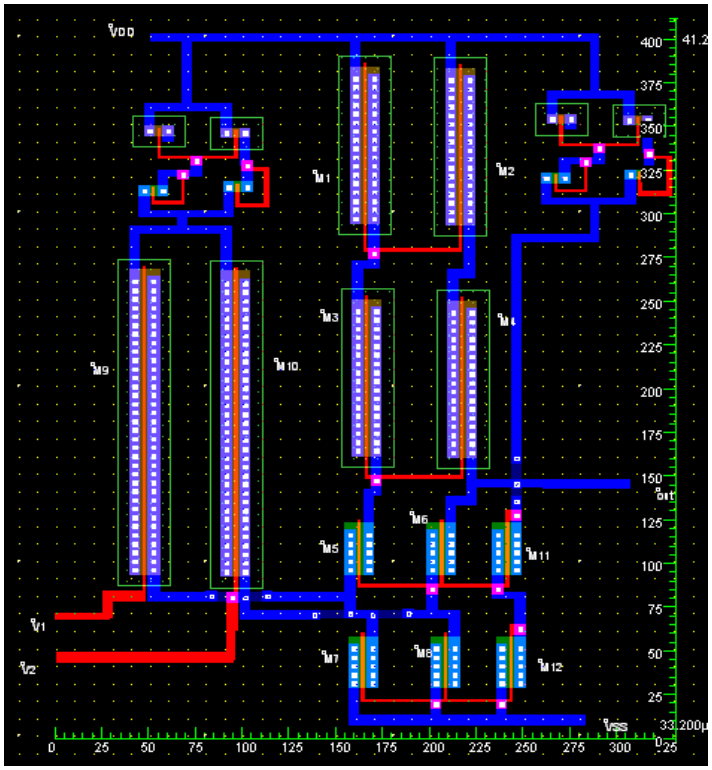


Figure 3.42: Layout of Wilson Current Mirror base Folded Cascode OTA

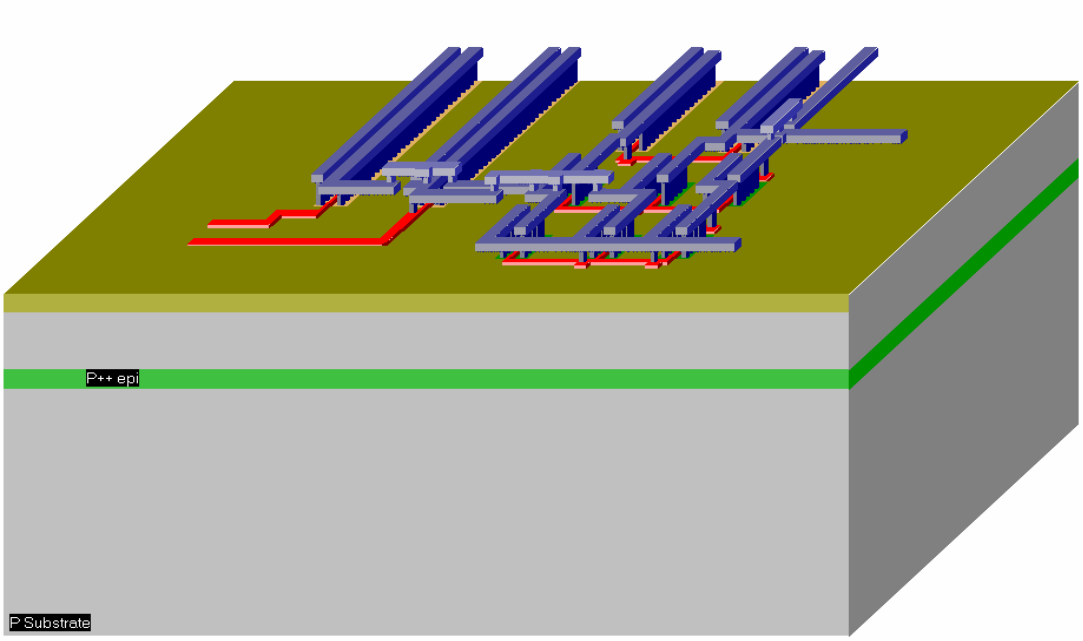


Figure 3.43: 3-D Process of Wilson Current Mirror base Folded Cascode OTA

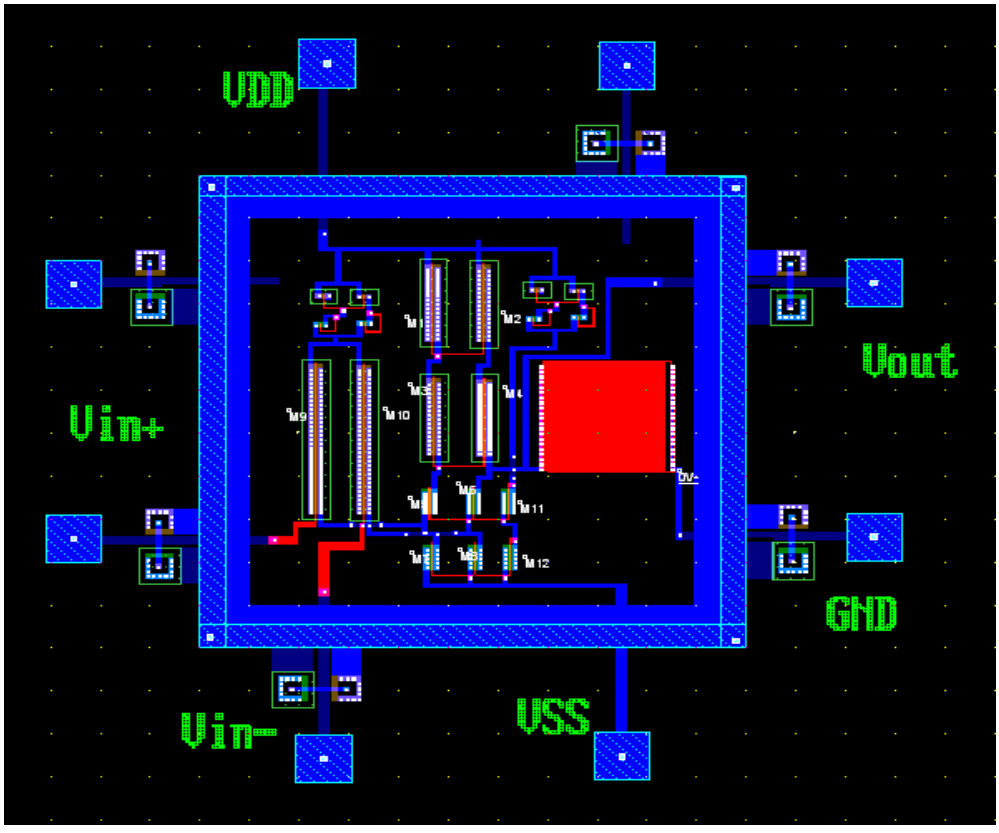


Figure 3.44: Layout of Wilson Current Mirror base Folded Cascode OTA with Bonding Pad

3.13 Post Simulation Results of Wilson Current Mirror base Folded Cascode OTA

3.13.1 Gain and Unit Gain Band Width (UGBW) of Wilson Crrent Mirror base Folded cascode OTA

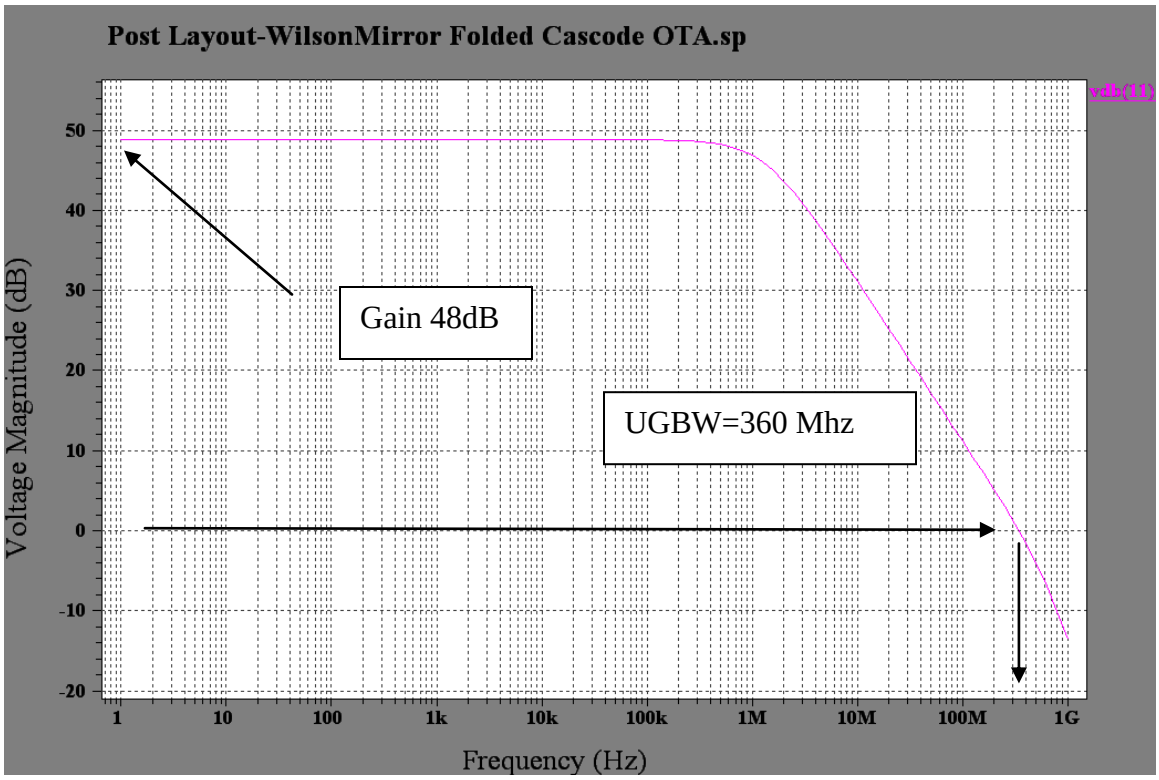


Figure 3.45 Post Layout AC Analysis of Wilson Current Mirror base Folded Cascode OTA

3.13.2 Phase Margin of Wilson Current Mirror base Folded Cascode OTA

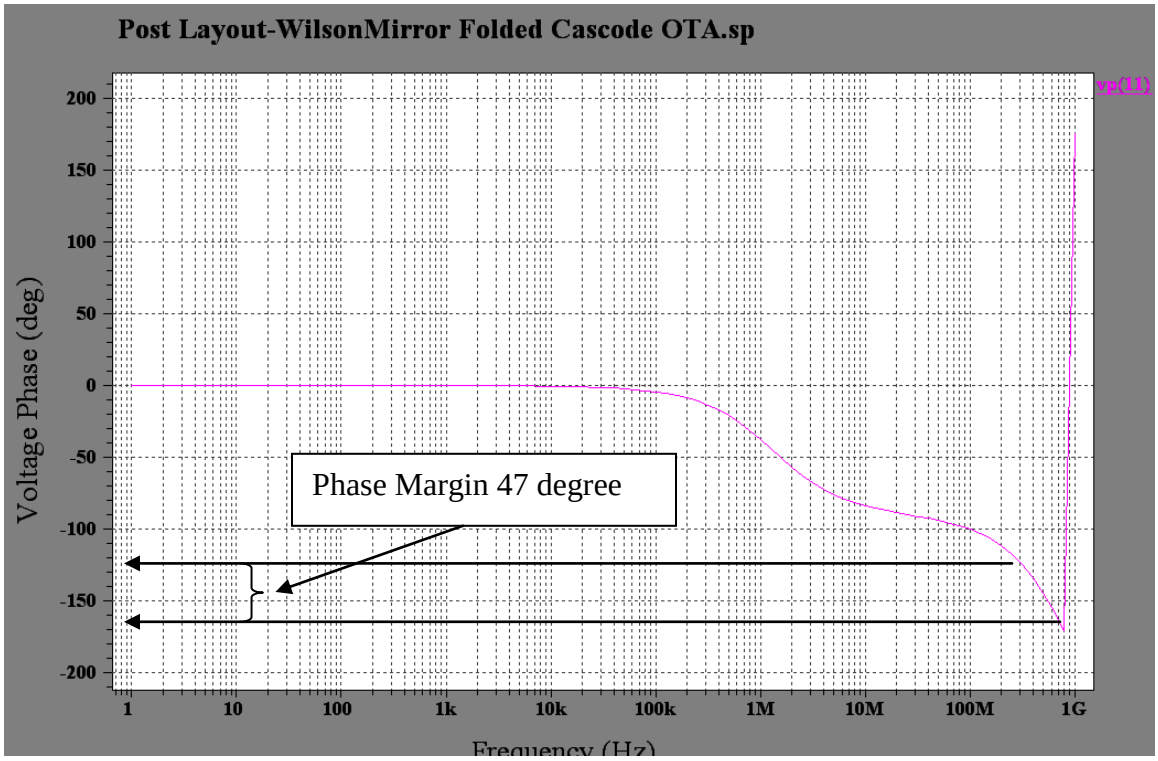


Figure 3.46 Post Layout of Phase Margin of Wilson Current Mirror base Folded Cascode OTA

3.13.3 Input-Output Swing and Offset of Wilson Current Mirror base Folded Cascode OTA

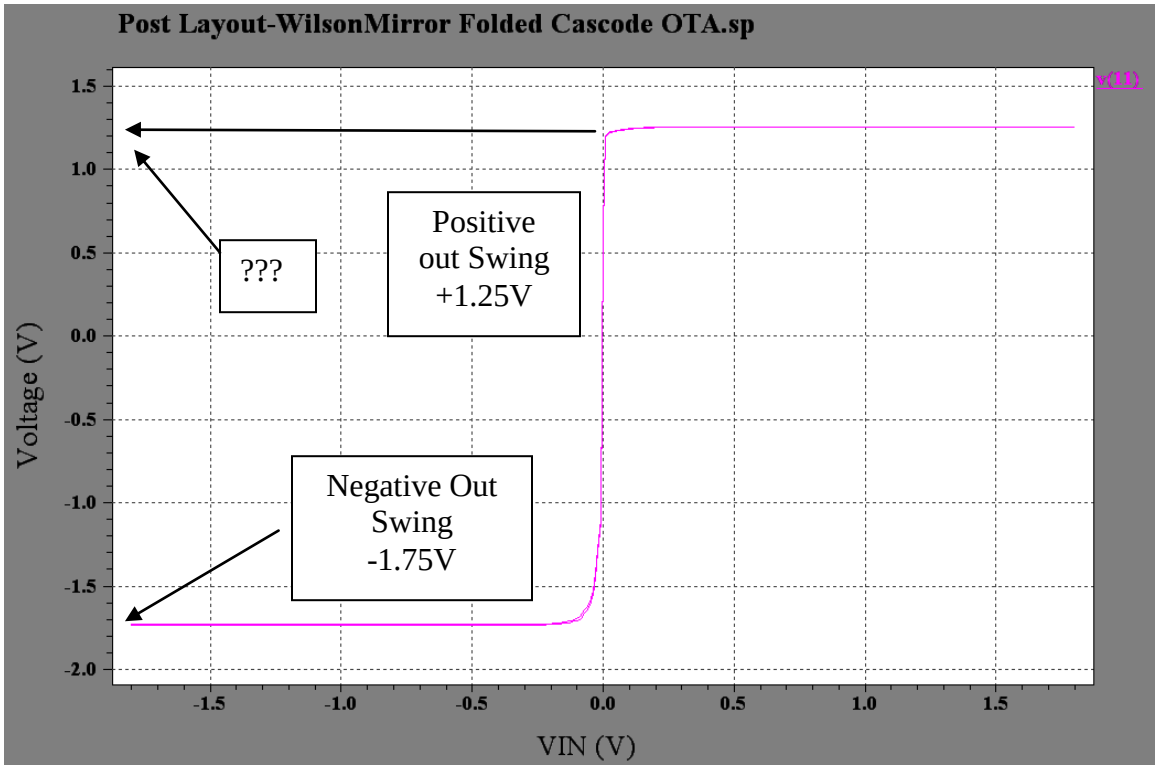


Figure 3.47 Post Layout Input-Output Swing and offset of Wilson Current Mirror base Folded Cascode OTA

3.13.4 Slew Rate of Wilson Current Mirror base Folded Cascode OTA

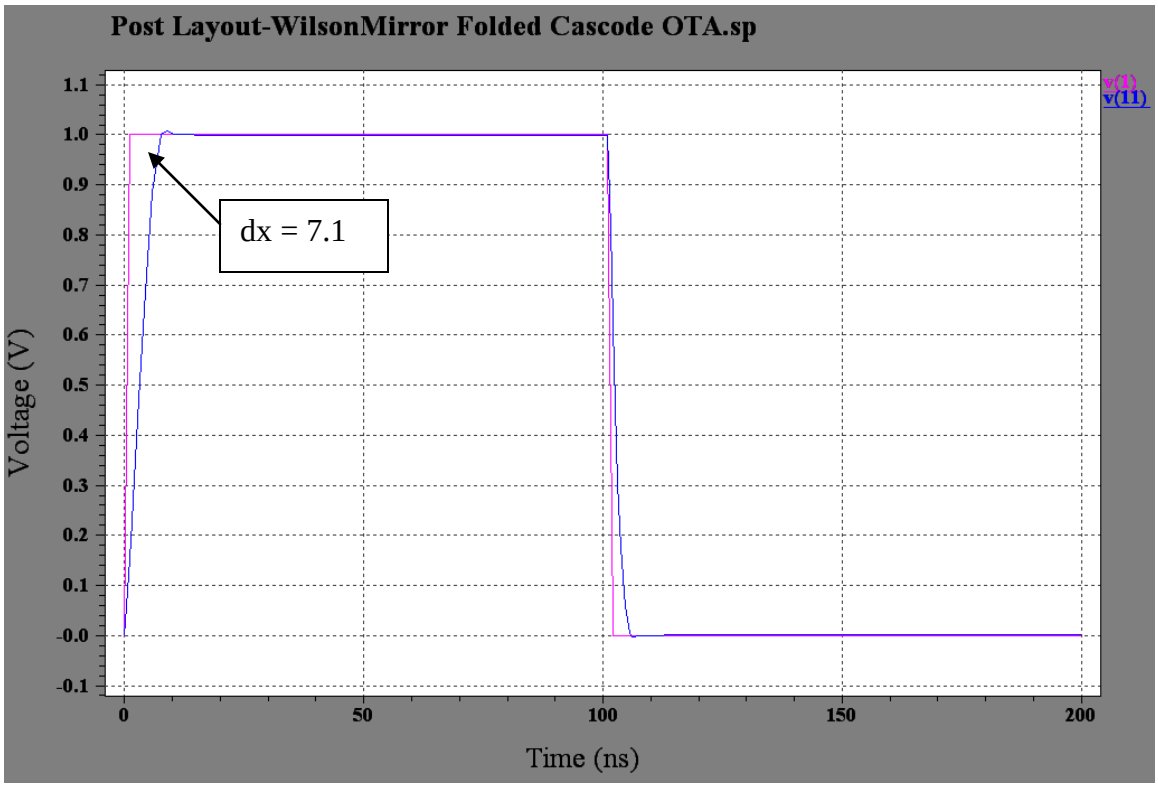


Figure 3.48 Post Layout Slew Rate of Wilson Mirror base Folded Cascode OTA

3.13.5 Common Mode Gain of Wilson Current Mirror base Folded Cascode OTA

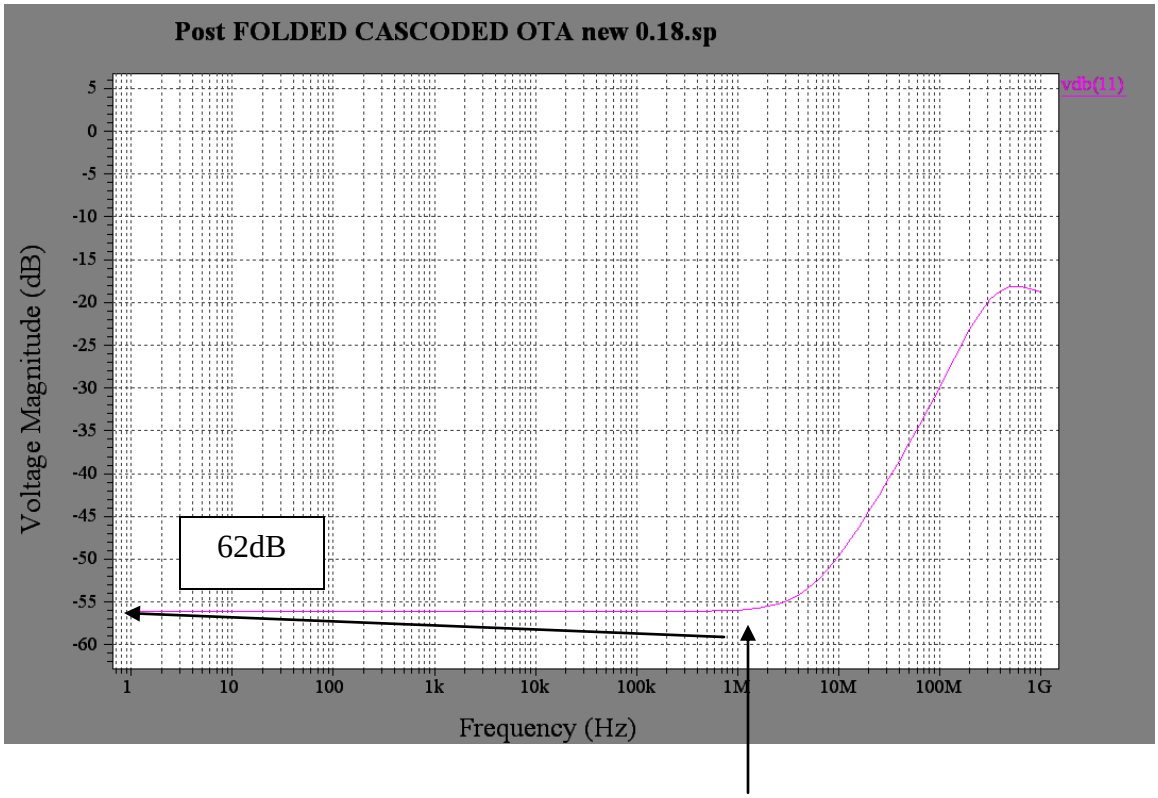


Figure 3.49 Post Layout CMRR of Wilson Mirror base Folded Cascode OTA

3.13.6 Input Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

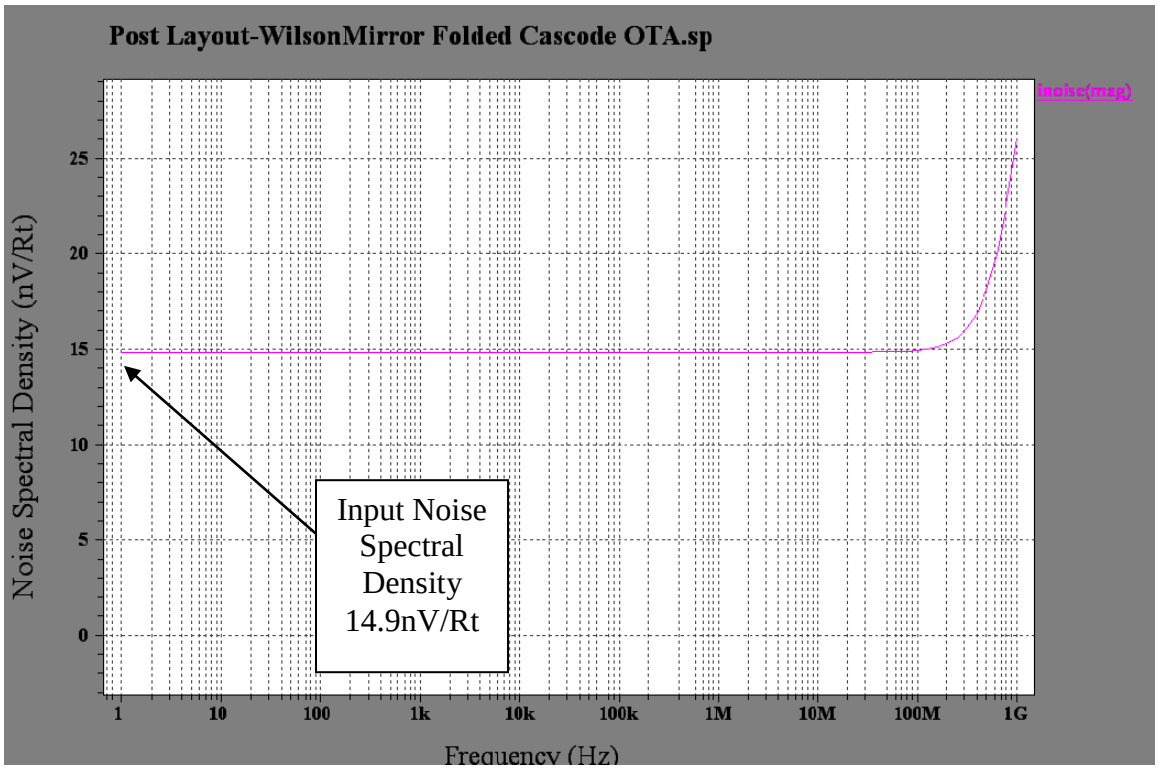


Figure 3.50 Post Layout Input Noise Spectral Density of Wilson Mirror base Folded Cascode OTA

3.13.7 Output Noise Spectral Density of Wilson Current Mirror base Folded Cascode OTA

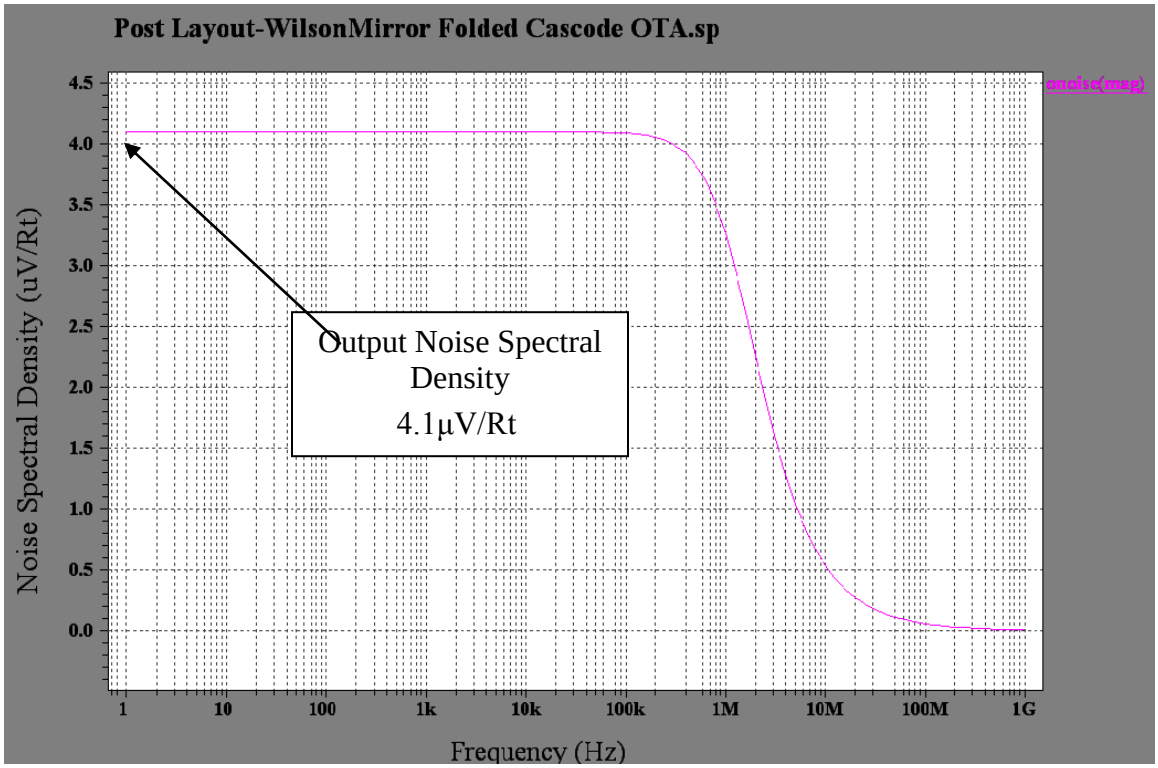


Figure 3.51 Post Layout Output Noise Spectral Density of Wilson Mirror base Folded Cascode OTA

3.13.8 Transient Analysis of of Wilson Current Mirror base Folded Cascode OTA

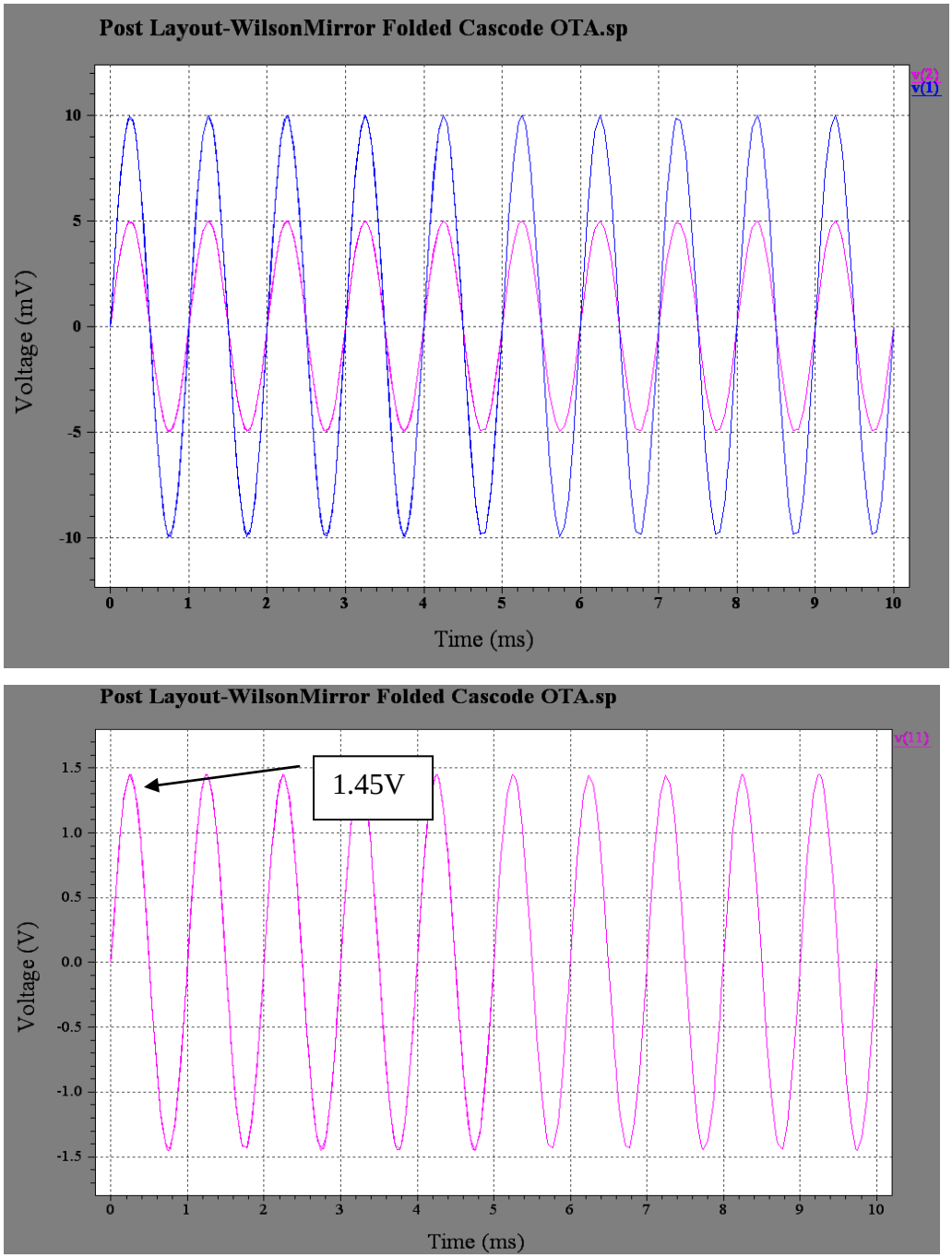


Figure 3.52 Post Layout Differential Pair Input and Transient Analysis of Wilson Current Mirror base Folded Cascode OTA

3.18.9 ICMR of Wilson Current Mirror base Folded Cascode OTA

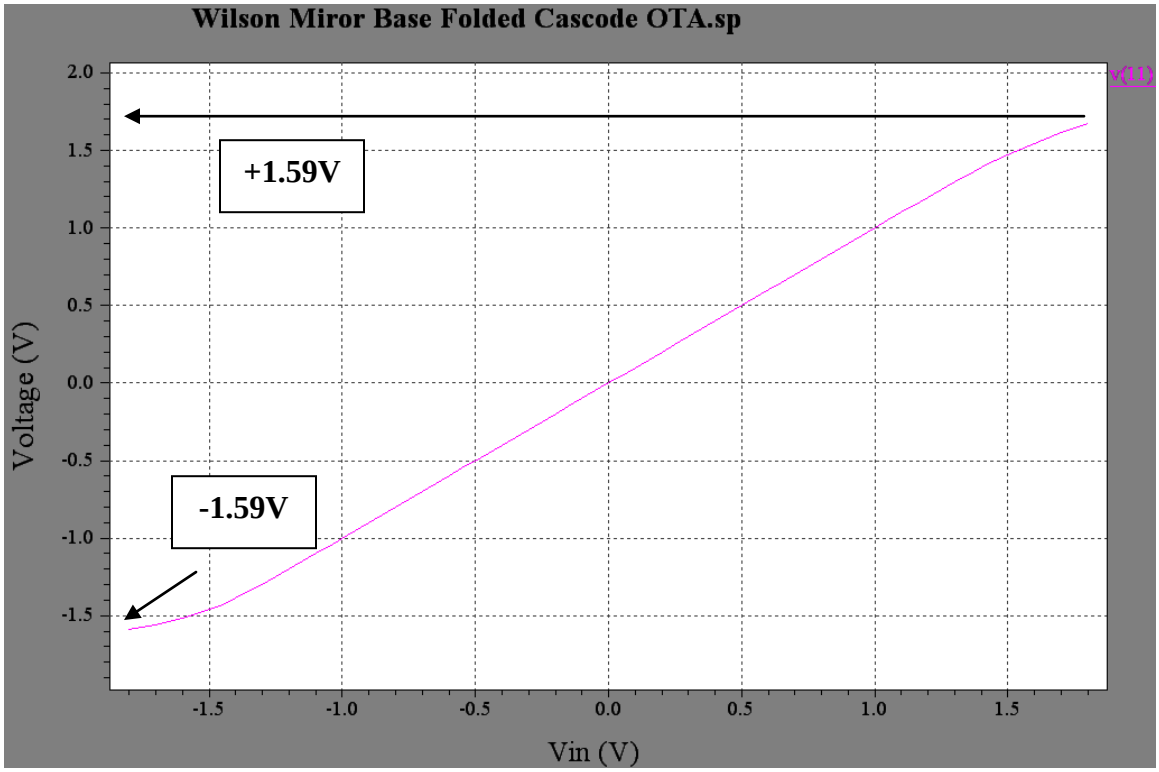


Figure 3.53 Post Layout ICMR of Wilson Current Mirror base Folded Cascode OTA

3.13 Pre and Post Layout Simulated Result Comparison of Wilson Mirror base Folded cascode OTA

Table 3.9 Pre and Post Layout Simulated Result Comparison of Wilson Mirror base Folded cascode OTA

Simulated Results	Pre-Layout Simulation	Post Layout Simulation
Gain	52dB	48dB
UGBW	390MHz	360MHz
Phase Margin	50 degree	47 degree
CMRR	114dB	104dB
Offset Voltage	0.05V	0.05V
I/O Swing (Wilson Mirror)	[-1.8V/ 1.5V]	[-1.75V/ 1.25V]
Slew Rate	160V/μS	142V/μS
Input Noise spectral Density	12.1nV/Rt	14.9nV/Rt
Output Noise Spectral Density	4.4μV/ Rt	4.2μV/ Rt
ICMR	-1.7V to 1.7V	-1.59V to 1.59V
Power Consumption	2.8885E-04 watts	3.1473E-04watts

3.15 Monte Carlo Analysis of Wilson Mirror base Folded cascode OTA

3.15.1 AC Analysis with Change NMOS Threshold Voltage(Absolute Variation)

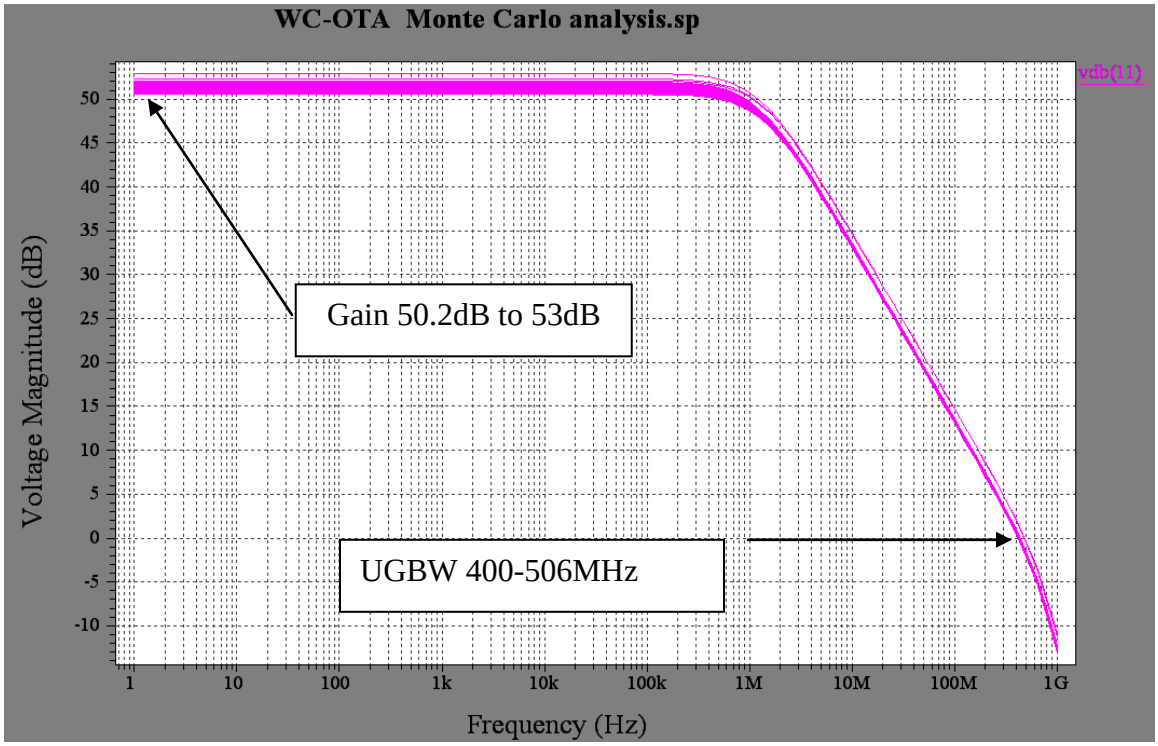


Figure 3.54 Monte Carlo AC Analysis with Change NMOS Threshold Voltage (Absolute Variation)

3.15.2 AC Analysis with Change PMOS Thresold Voltage(Absolute Variation)

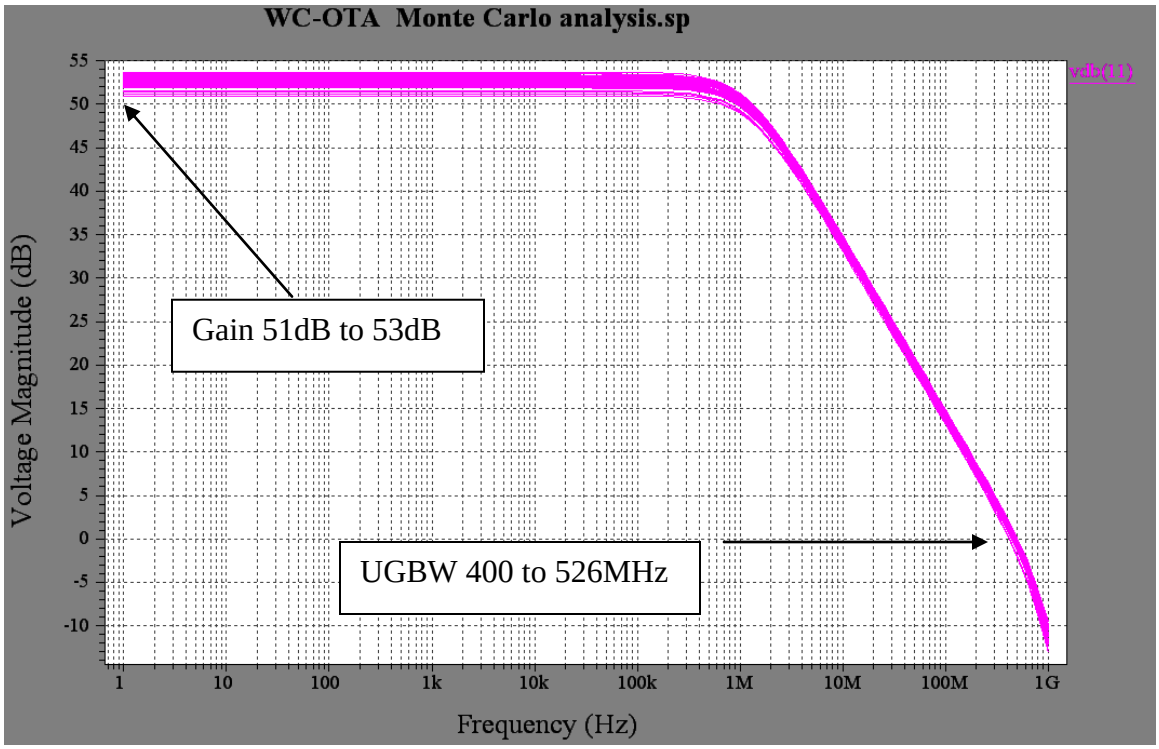


Figure 3.55 Monte Carlo AC Analysis with Change PMOS Threshold Voltage (Absolute Variation)

3.15.3 AC Analysis with Change both NMOS and PMOS Thresold Voltage (Absolute Variation)

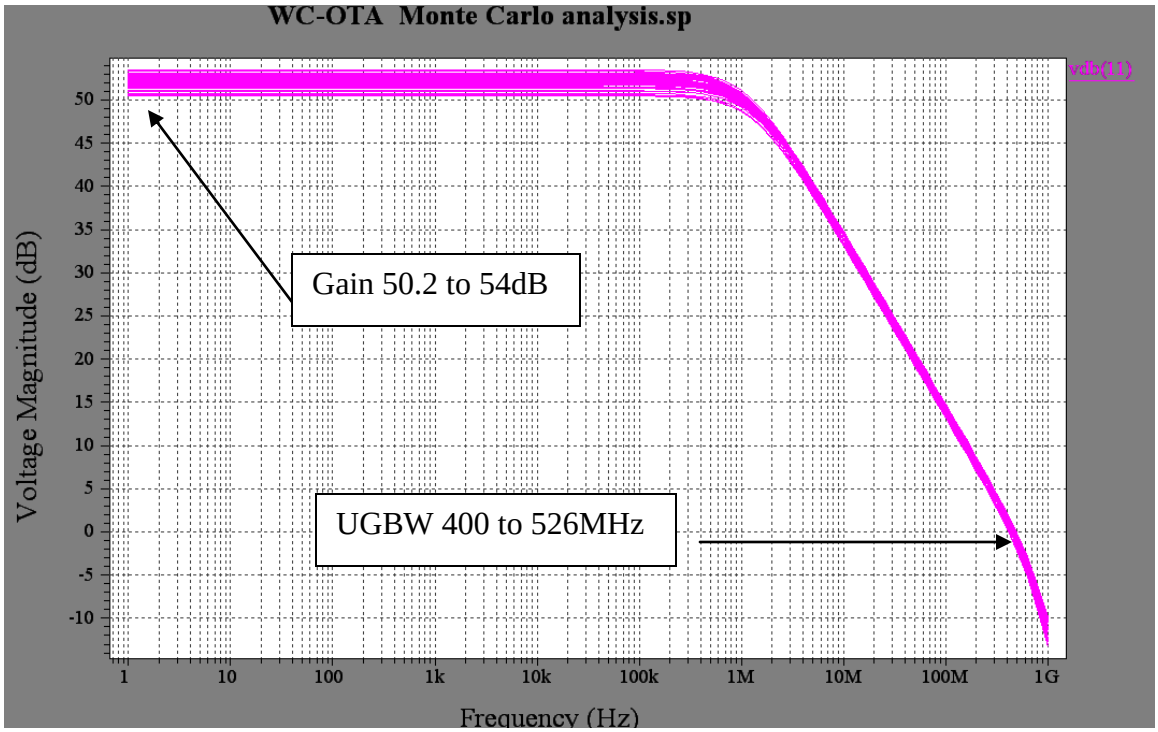
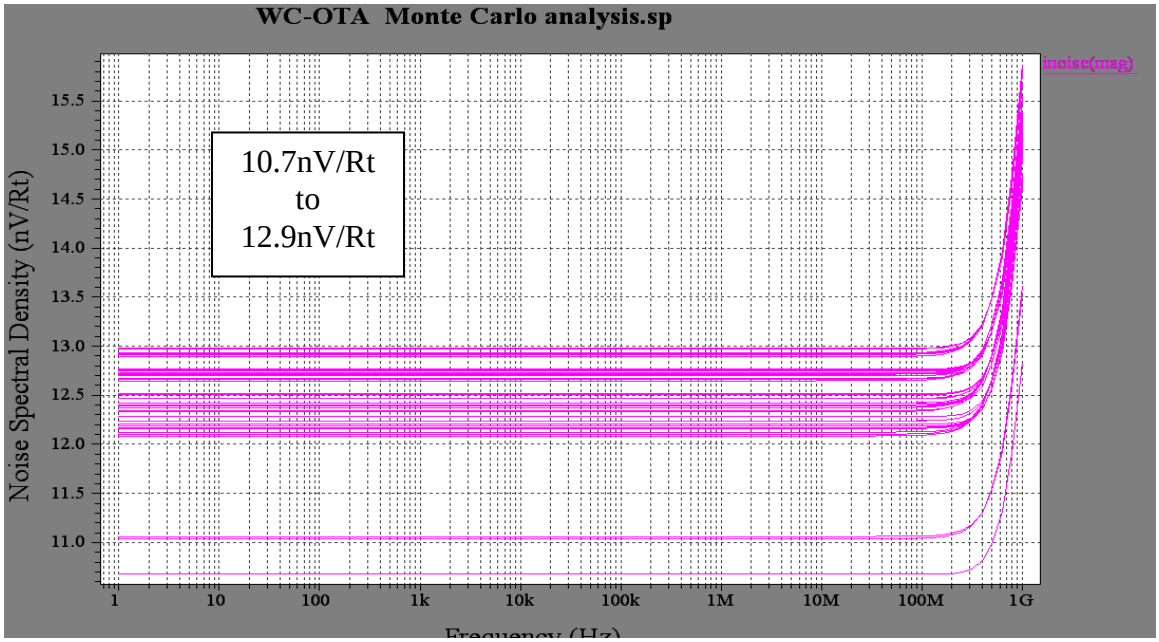
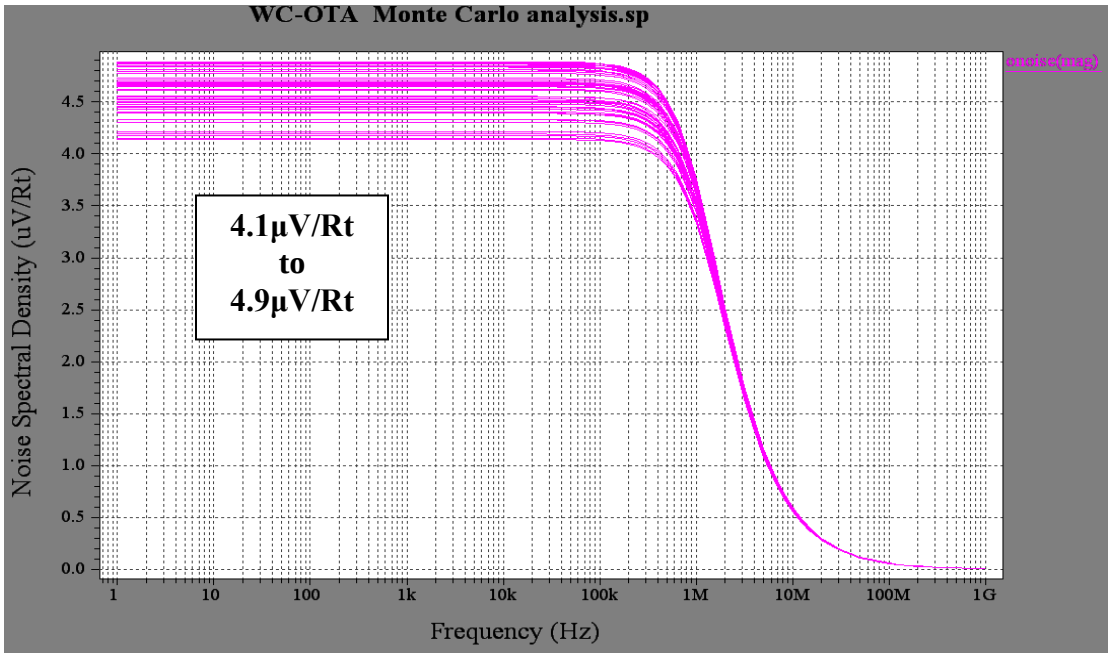


Figure 3.56 Monte Carlo AC Analysis with Change both PMOS and NMOS Threshold Voltage (Absolute Variation)

3.15.4 Input-Output Noise Spectral density Analysis with Change both NMOS and PMOS Threshold Voltage (Absolute Variation)



(a)



(b)

Figure 3.57 Monte Carlo (a) Input and (b) Ouput Noise Spectral Density Analysis

3.15.5 AC Analysis with Change Oxide Thickness (Absolute Variation)

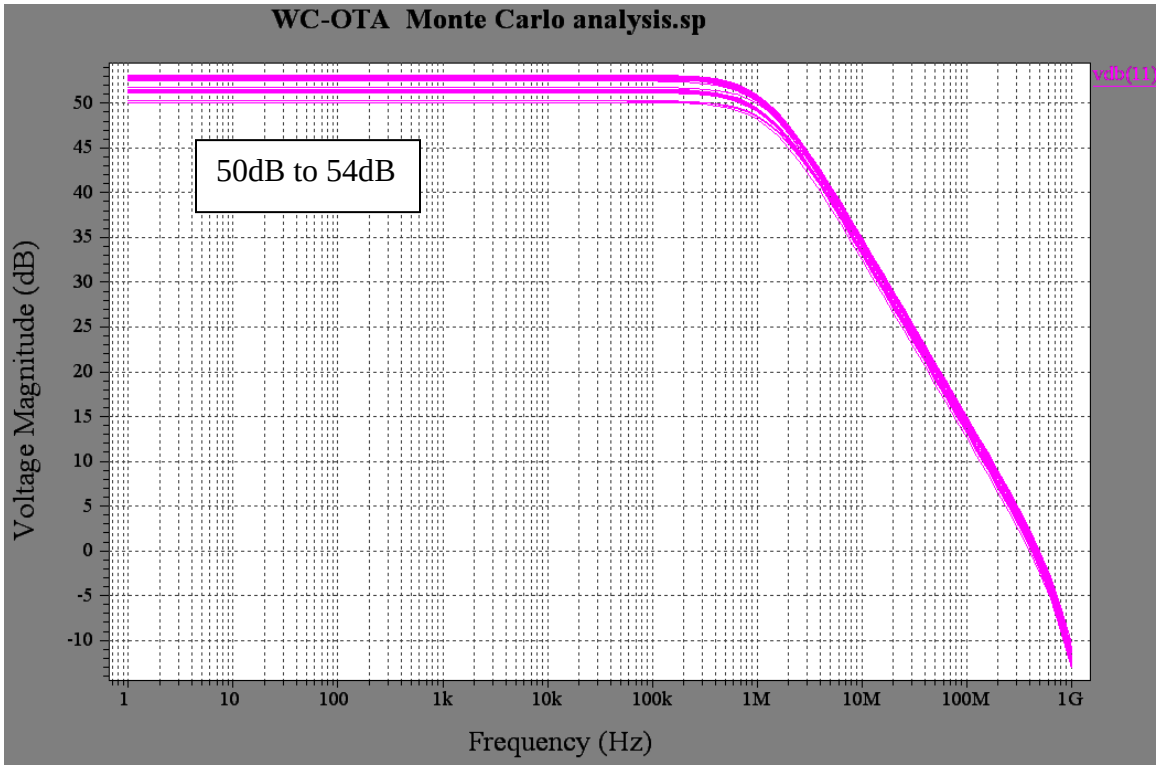


Figure 3.58 Monte Carlo AC Analysis with Change Oxide Thickness (Absolute Variation)

3.16 Cascode Current Mirror Improved Folded cascode OTA Design

Since the folded cascode OTA based on Wilson mirror has a limited output swing, So, we propose to improve the current mirror. For the folded cascode OTA using a Wilson mirror, the maximum output voltage is set lower than: $V_{dd} + V_T + 2V_{ds,sat}$ so, we use cascode mirror in order to restore this fall to $2V_{ds,sat}$. The improved circuit yield to specifications schedule presented by table 3.4 follows the same design strategy explained previously; we obtain the same transistors sizes of the last circuit.

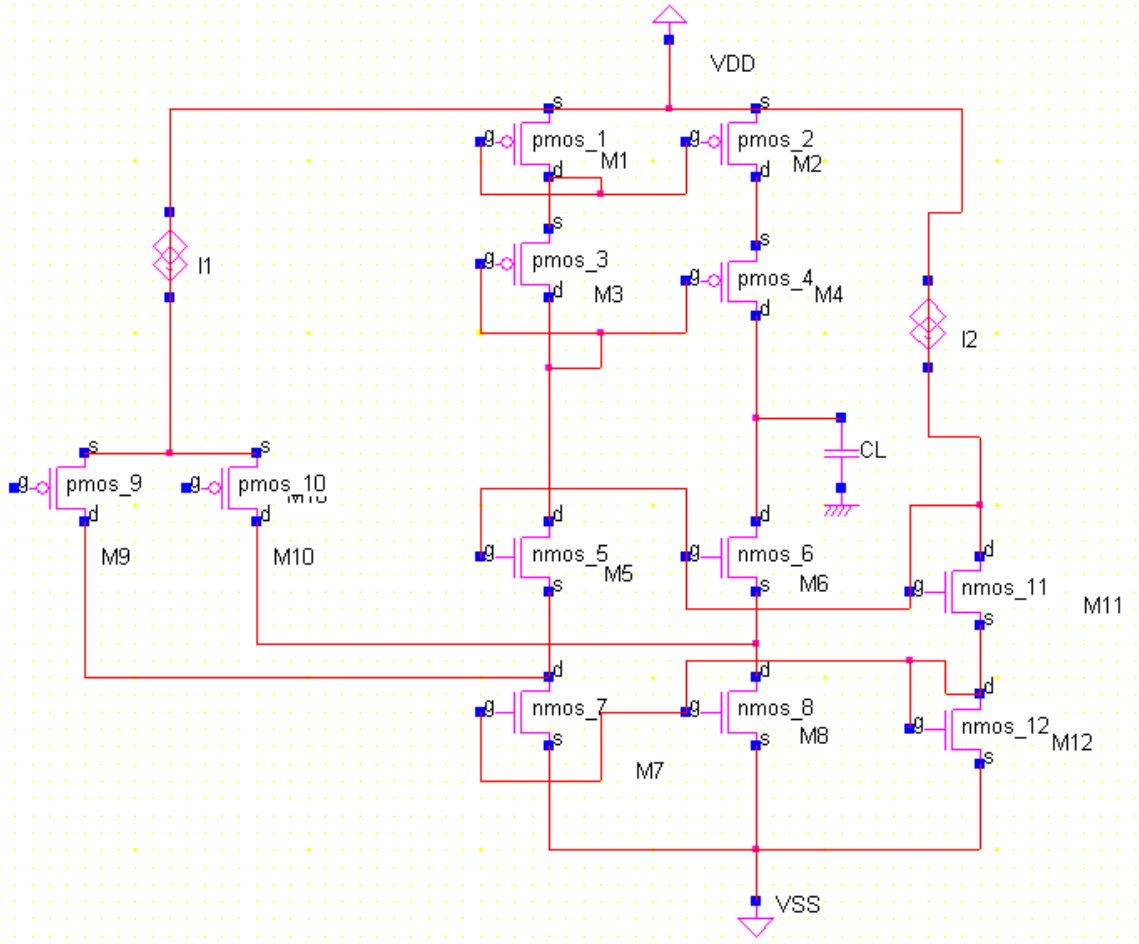
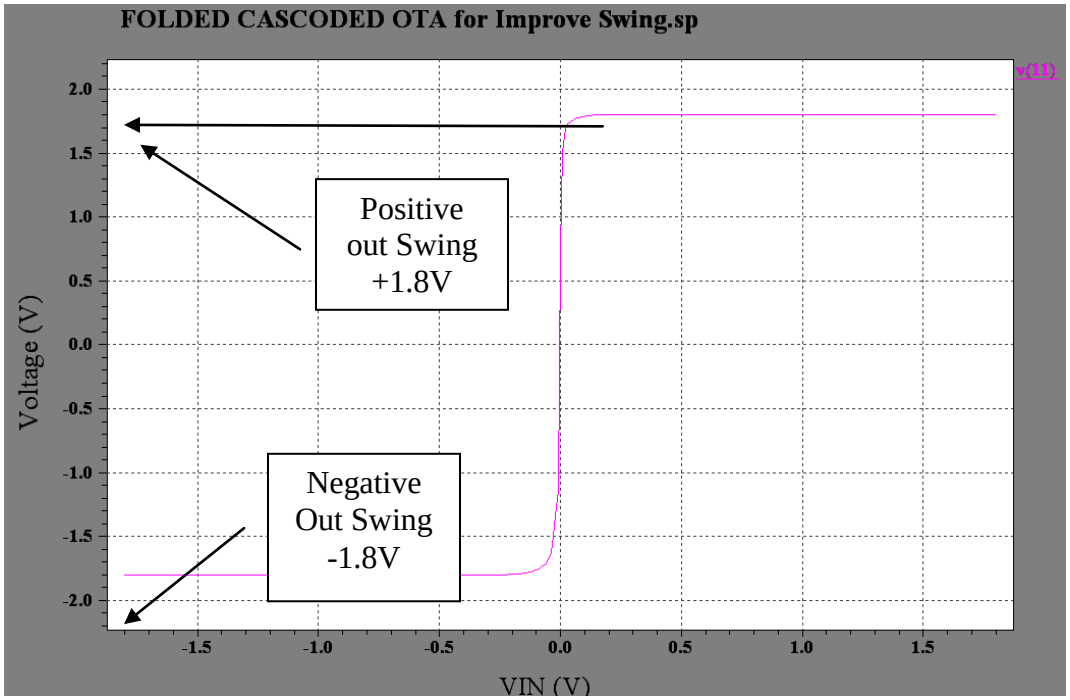
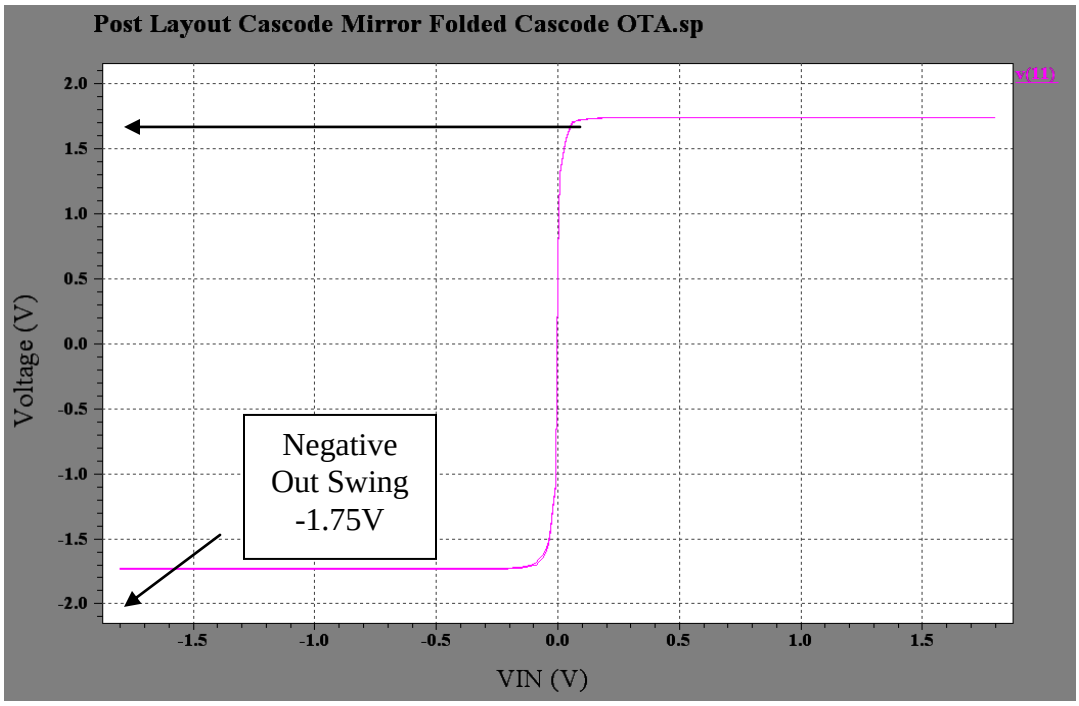


Figure 3.59 Designed Practical Cascode Current Mirror Folded Cascode OTA Schemetic



(a)



(b)

Figure 3.60 (a) Pre and (b) Post Layout of Cascode Current base Folded Cascode OTA

Table 3.10: Input and Output Swing Comparison of Wilson Current Mirror and Cascode Current Mirror

Current Mirror	Pre-Layout Simulation Input and Output Swing	Post Layout Simulation Input and Output Swing
Wilson Mirror	**[-1.8V/ 1.5V]**	**[-1.75V/ 1.25V]**
Cascode Mirror	**[-1.8V/ 1.8V]**	**[-1.75V/ 1.75V]**

3.17 Noise and its analysis

Unwanted disturbance that interferes with a desired signal

- External: power supply & substrate coupling, crosstalk, EMI, etc.
- Internal: random fluctuations that result from the physics of the devices or materials
- Smallest detectable signal, signal-to-noise ratio (SNR), and dynamic range are Determined by noise

$$SNR = \frac{p_{Signal}}{P_{Noise}} = \frac{V^2_{rms,signal}}{V^2_{rms,noise}}$$

----------(3.28)

Types of Noise:

Thermal Noise: Thermal excitation of charge carriers

$$\frac{\overline{V^2_{rms}}}{\Delta f} = 4KTR,\ V^2/H_z$$

----------(3.29)

Shot Noise: Fluctuations in dc current flow through junctions.

$$\frac{\overline{I^2_{rms}}}{\Delta f} = 2qI_{DC},\ A^2/H_z$$

----------(3.30)

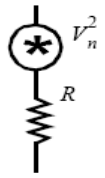
Flicker Noise: Traps in Semiconductor.

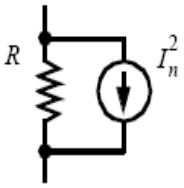
$$\frac{\overline{V^2_{rms}}}{\Delta f} = \frac{K_f V^2_{DC}}{f},\ V^2/H_z$$

----------(3.31)

T=Temperature
K=1.38 x 10^{-23}J/K
q=1.6x10^{-19}C
K_f=Flicker Coefficient

Resistor Noise Source





Noise Density: $\frac{\overline{V^2_n}}{\Delta f} = 4KTR,\ V^2/H_z$ $\qquad$ $\frac{\overline{I^2_n}}{\Delta f} = \frac{4KT}{R},\ A^2/H_z$

Noise Power: $\overline{V^2_n} = 4KTR\ \Delta fn,\ V^2$ $\qquad$ $\overline{I^2_n} = \frac{4KT}{R}\Delta fn,\ A^2$

----------(3.32)

Δfn = Noise Bandwidth

Noise Bandwidth is not same as 3dB Bandwidth

KT/C limit:

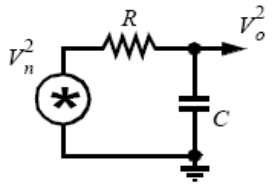


Figure 3.61 Noise in Low Pass Filter

$$\overline{V_0^2} = 4KTR\Delta fn, V^2$$

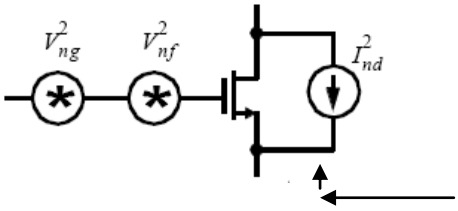
$$\overline{V_0^2} = 4KTR(\frac{1}{4RC})$$

$$\overline{V_0^2} = \frac{KT}{C}, V^2$$

----------(3.33)

- Total noise power is independent of R
- Capacitor is noiseless, but accumulates noise from resistor

Noise Sources in CMOS



$$R_{ds} = \frac{1}{g_m}$$

Long Channel Saturation

Figure3.62 Noise Source in CMOS

Drain Thermal Noise

$$\frac{\overline{I_{nd}^2}}{\Delta f} = 4KT\gamma g_m, A^2 / H_z$$

----------(3.34)

γ = 2/3 for Long Channel
2 for Short Channel

Gate Thermal Noise

$$\frac{\overline{V_{ng}^2}}{\Delta f} = 4KTR_G / 3, V^2 / H_z$$

----------**(3.35)**

Can be neglected with good layout

Flicker Noise

$$\frac{\overline{V_{nf}^2}}{\Delta f} = \frac{K_f}{WLC_{ox} f}, V^2 / H_z$$

----------**(3.36)**

Input Referred Noise

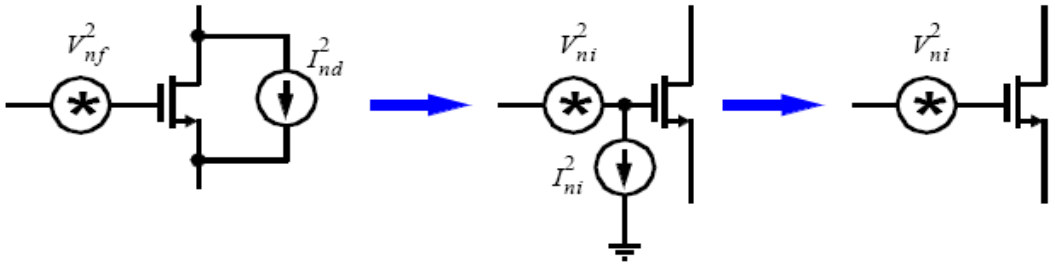


Figure 3.63 Input Referred Noise

MOSFET input current noise source can be neglected at low frequencies.

Input Referred Drain Noise

$$\frac{\overline{V_{nd}^2}}{\Delta f} = \frac{\overline{I_{nd}^2}}{\Delta f} / g_m^2 = \frac{4KT\gamma}{g_m}, V^2 / H_z$$

----------**(3.37)**

Total Input Referred Noise

$$\frac{\overline{V_{ni}^2}}{\Delta f} = \frac{4KT\gamma}{g_m} + \frac{K_f}{WLC_{ox} f}, V^2 / H_z$$

----------**(3.38)**

1/f Corner Frequency defines where flicker noise is equal to thermal noise and to reduce flicker noise need to increase transistor area

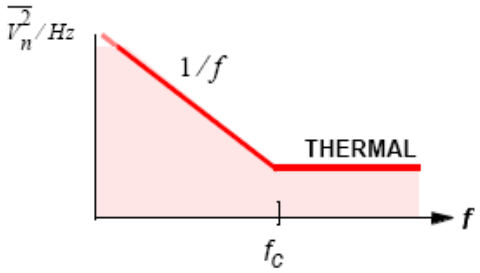


Figure 3.64: 1/f Corner Frequency

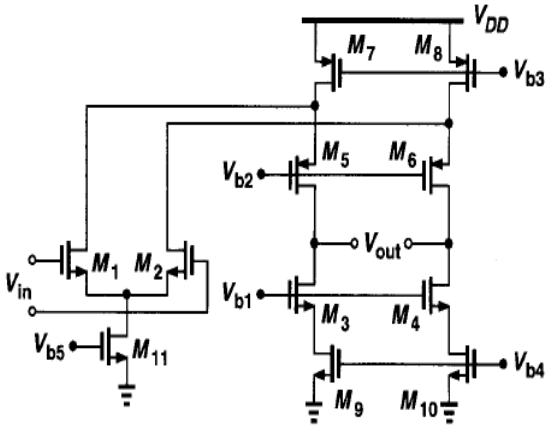
$$\frac{4KT\gamma}{g_m} = \frac{K_f}{WLC_{ox}f}$$

$$f_c = \frac{K_f g_m}{4KT\gamma WLC_{ox}}$$

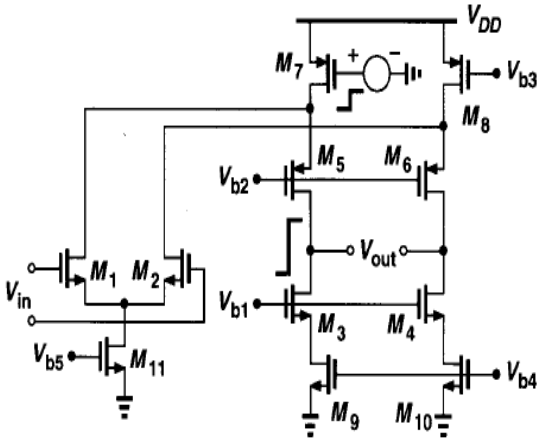
----------(3.39)

With many transistors in an OTA, it may seem difficult to intuitively identify the dominant sources of noise. A simple rule for inspection is to change the gate voltage of each transistor by a small amount and predict the effect at the output.

Let us consider Folded Cascode OTA as shown in Figure3.58. The noise of the cascode devices is negligible at low frequencies, leaving $M_1 - M_2, M_7 - M_8$ and $M_9 - M_{10}$ as potentially significant sources. By changing gate voltage of M_7 by small amount, output is considerable chage.



(a)



(b)

Figure 3.65 Noise in Folded Cascode OTA

Thermal Noise:

For input referred thermal noise, first refer noise of $M_7 - M_8$ and $M_9 - M_{10}$ to the output.

$$\overline{V_{n,out,M_{7,8}}^2} = 2(4KT\frac{2}{3g_{m7,8}}g_{m7,8}^2R_{out}^2)$$

----------(3.40)

Where factor 2 for noise of M_7 and M_8. R_{out} denotes the open loop output resistance. Similarly

$$\overline{V_{n,out,M_{9,10}}^2} = 2(4KT\frac{2}{3g_{m9,10}}g_{m9,10}^2R_{out}^2)$$

----------(3.41)

Dividing this by $g_{m1,2}^2R_{out}^2$ and adding the contribution of $M_1 - M_2$, we found the overall noise.

$$\overline{V_{n,\text{int}}^2} = 8KT(\frac{2}{3g_{m1,2}} + \frac{2g_{m7,8}}{3g_{m1,2}^2} + \frac{2g_{m9,10}}{3g_{m1,2}^2})$$

----------(3.42)

Flicker Noise:

$$\overline{V_{n,out,M_{7,8}}^2} = 2(\frac{K_P}{C_{ox}(WL)_{7,8}}\frac{1}{f}g_{m7,8}^2R_{out}^2)$$

$$\overline{V_{n,out,M_{9,10}}^2} = 2(\frac{K_P}{C_{ox}(WL)_{9,10}}\frac{1}{f}g_{m9,10}^2R_{out}^2)$$

$$\overline{V_{n,out,M_{1,2}}^2} = 2(\frac{K_P}{C_{ox}(WL)_{1,2}} \frac{1}{f} g_{m1,2}^2 R_{out}^2)$$

----------(3.43)

And $A_V = g_{m1,2} R_{out}$

Total Input Referred Flicker Noise:

$$\overline{V_{n,\text{in}}^2} = \frac{\overline{V_{n,out,total}^2}}{A_V^{\ 2}} = \frac{2K_N}{C_{ox} f}(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{9,10}} \frac{g_{m9,10}^2}{g_{m1,2}^2}) + \frac{2K_P}{C_{ox} f} \frac{1}{(WL)_{7,8}} \frac{g_{m7,8}^2}{g_{m1,2}^2}$$

----------(3.44)

The Overall Noise:

$$\overline{V_{n,\text{in}}^2} = 8KT(\frac{2}{3g_{m1,2}} + \frac{2g_{m7,8}}{3g_{m1,2}^2} + \frac{2g_{m9,10}}{3g_{m1,2}^2}) + \frac{2K_N}{C_{ox} f}(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{9,10}} \frac{g_{m9,10}^2}{g_{m1,2}^2}) + \frac{2K_P}{C_{ox} f} \frac{1}{(WL)_{7,8}} \frac{g_{m7,8}^2}{g_{m1,2}^2}$$

----------(3.45)

The noise contribution of the PMOS and NMOS current sources *increases* in proportion to their transconductance. This trend results in a trade-off between output voltage swings and input-referred noise: for a given current, as implied by $g_m = \frac{2I_D}{V_{GS} - V_{TH}}$, if the verdrive voltage of the current sources is minimized to allow large swings, then their transconductance is maximized.

Chapter 4

Design and Implementation of Dual-Band CMOS Gm-C IF Filter for GSM and FM Band

4.1 Introduction

Active RC filters using the operational amplifier (opamp) have been widely used in various low frequency applications in telecommunication networks, signal processing circuits, communication systems, control, and instrumentation systems for a long time. However, active RC filters cannot work at higher frequencies (over 200kHz) due to opamp frequency limitations and are not suitable for full integration. They are also not electronically tunable and usually have complex structures. Many researches have been made to overcome these drawbacks [104]–[111]. The most successful approach is to use the operational transconductance amplifier (OTA) to replace the conventional opamp in active RC filters [112]–[146]. In recent years OTA-based high frequency integrated circuits, filters and systems have been widely investigated.

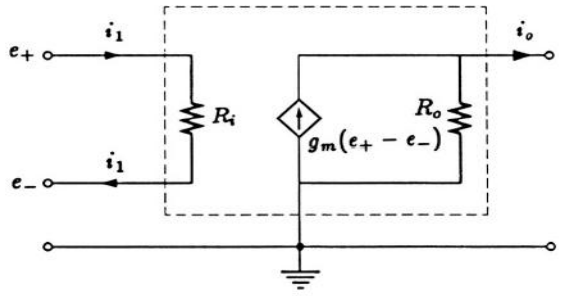
An ideal operational transconductance amplifier is a voltage-controlled current source, with infinite input and output impedances and constant transconductance. The OTA has two attractive features: its tranconductance can be controlled by changing the external dc bias current or voltage, and it can work at high frequencies. The OTA has been implemented widely in CMOS and bipolar and also in BiCMOS and GaAs technologies. The typical values of transconductances are in the range of tens to hundreds of μS in CMOS and up to mS in bipolar technology. The CMOS OTA,can work in the frequency range of several hundred of KHz to more than 100MHz. Linearization techniques make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent [105-108].

Programmable high-frequency active filters can design by incorporating the OTA. These OTA filters also have simple structures and low sensitivity with advantages such as low power consumption, noise, parasitic effects, and cost. Active filters which use only OTAs and capacitors have been widely studied [115]–[126], [129–146], are intuitively called OTA-C filters.

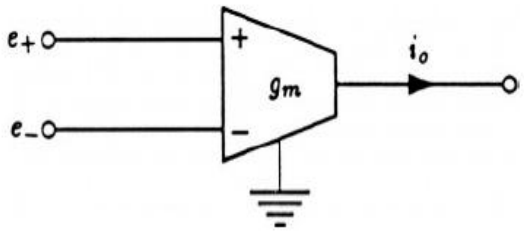
It should be noted that practical OTAs will have finite input and output impedances. For the CMOS OTA, for example, the input resistance is usually very large, but the output resistance is in the range of $50\text{k}\Omega$ to $1\text{M}\Omega$, and the input and output capacitances are typically of the order of 0.05pF [110]. Also, at very high frequencies, the OTA transconductance will be frequency dependent due to its limited bandwidth. These nonideal impedance and transconductance characteristics will influence the stability and frequency performances of OTA filters. Practical OTAs will also exhibit nonlinearity for large signals and have noise, which will affect the dynamic range of OTA filters.

4.2 The Operational Transconductance Amplifier and Simple Circuits

OTA as a differential-input, grounded output two-port, as shown in Figure 4.1 In an ideal OTA, assume that the input resistance, R_i approaches infinity. Thus, $i_1 = 0$ and the output resistance R_0 approaches infinity.



(a)



(b)

Figure 4.1 (a) Small Signal equivalent circuit and (b) Symbol of OTA

4.2.1 Grounded Resistor

Consider the circuit in Figure 4.2(a). It is clear that

$$I_1 = -I_0 = g_m E_1$$

$$Z_{in} = \frac{E_1}{I_1} = \frac{1}{g_m}$$

----------(4.1)

and this circuit simulates a grounded resistor as shown in Figure 4.2(b). Although mathematically the input terminals of the OTA could just as well be inverted, it is important to note that the output of the OTA is fed back to the negative terminal of its input to prevent instability.

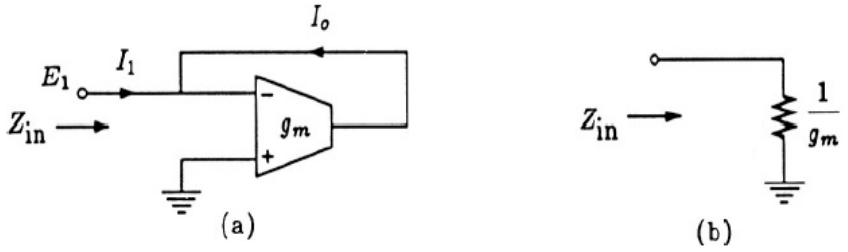


Figure 4.2 OTA Simulation of grounded Resistor

4.2.2 Floating Resistor

To simulate a floating resistor, two OTAs are required. From the circuit of Figure 4.3(a)

$$I_1 = g_m(E_1 - E_2)$$

$$I_2 = -g_m(E_1 - E_2)$$

----------(4.2)

$$I_1 = -I_2 \frac{(E_1 - E_2)}{\frac{1}{g_m}}$$

----------(4.3)

Which is exactly the voltage-current relationship required by the circuit of Figure 4.2(b).

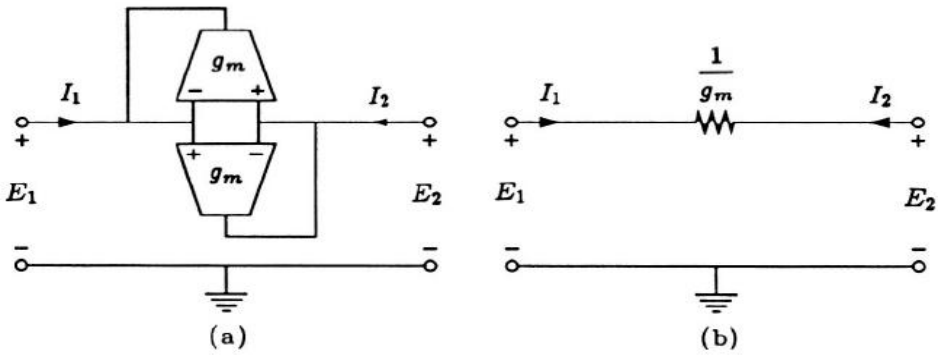


Figure4.3 OTA Simulation of floating Resistor

4.2.3 Integrator

The circuit of Figure 4.4 realizes a lossless integrator. Since the output current of the OTA, I_0 is $g_m(E_1 - E_2)$ the output voltage, E_0 is that current times the impedance of the capacitor.

$$E_0 = \frac{g_m}{sC}(E_1 - E_2) \text{ or}$$

$$\frac{E_0}{(E_1 - E_2)} = \frac{g_m}{sC}$$

----------(4.4)

Thus, the circuit of Figure 4.4 realizes a differential-input integrator. By grounding one of the two input terminals, it can be either an inverting or non-inverting integrator.

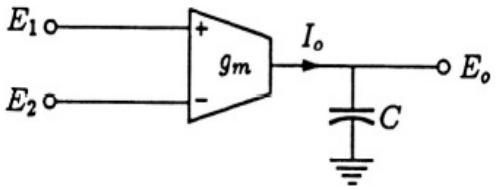


Figure 4.4 OTA Simulation of Integrator

4.2.4 Lossy Integrator

In constructing active filters, sometimes it is necessary to use lossy integrators. This can easily be accomplished by connecting a resistor in parallel with the capacitor of Figure 4.5. Since resistors are not practical in IC technology used to form OTA-C filters, the grounded resistor simulation of Figure 4.2 can be employed. Such circuit is shown in Figure 4.5.

$$\frac{E_0}{(E_1 - E_2)} = \frac{g_{m1}}{sC + g_{m2}}$$

----------(4.5)

By grounding one of the input terminals, either an inverting or a non inverting lossy integrator can be realized.

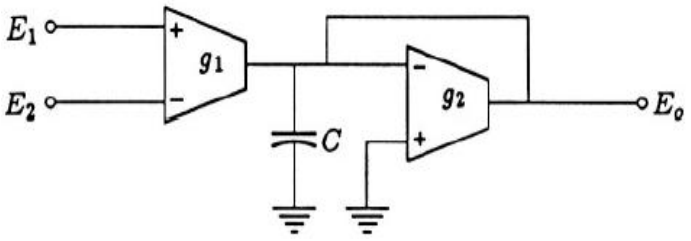


Figure 4.5 OTA Simulation of Lossy Integrator

4.2.5 Amplifier

If the capacitance in Figure4.5 is removed, then equation 4.5 become

$$\frac{E_0}{(E_1 - E_2)} = \frac{g_{m1}}{g_{m2}}$$

----------(4.6)

which is the input-output relationship of an amplifier. The configuration of Figure 4.6 thus realizes an amplifier with a differential input. Again, by grounding one of the input terminals, it can serve as a grounded amplifier with either a positive or a negative gain. The gain is determined simply by the ratio of the transconductances of the two OTAs.

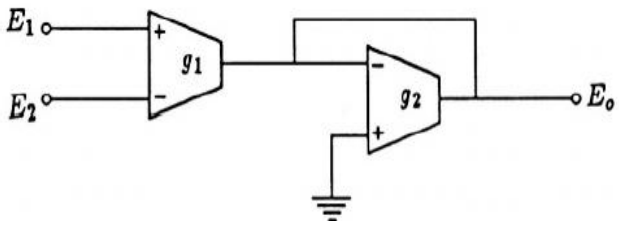


Figure 4.6 OTA Simulation of Amplifier

4.2.6 Weighted Summer

In the arrangement of Figure 4.7, the output currents of three OTAs(g_{m1}, g_{m2} and g_{m3}) are summed and the total current flows through the resistor realized by OTA(g_{m4}).

$$E_0 = \frac{1}{g_{m4}}(g_{m1}E_1 + g_{m2}E_2 + g_{m3}E_3)$$

----------(4.7)

Thus, the output voltage of this circuit is equal to the weighted sum of the three input voltages.

The different weighting factors are determined by the relative values of transconductances of the OTAs in comparison with the value of the transconductance

g_{m4} obviously, there can be as many input voltages as desired. Further, the sign of any term in equation 4.7 can be reversed by grounding the other input terminal.

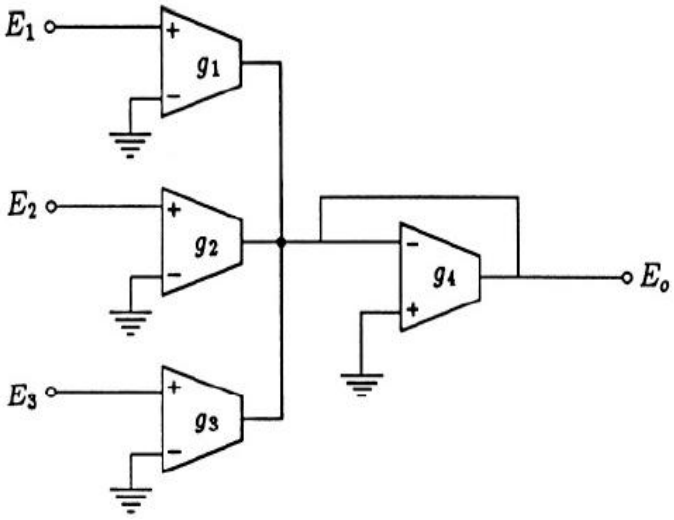


Figure 4.7 OTA Simulation of Weighted Summer

4.2.7 Positive Impedance Inverter

The three-terminal two-port (excluding the load impedance Z_L), of Figure 4.8 must satisfy the following relationships.

$$I_1 = g_{m2}E_2$$

$$I_2 = -g_{m1}E_1$$

----------(4.7)

Equation 4.7 satisfies condition of a positive impedance inverter. Hence, the input impedance at one port is proportional to the reciprocal of the terminating impedance at the other port.

$$Z_{in} = \frac{E_1}{I_1} = \frac{I_2}{-g_{m1}}\left(\frac{1}{g_{m2}E_2}\right) = \frac{1}{g_{m1}g_{m2}Z_L}$$

----------(4.8)

If Z_L is impedance of capacitance C then

$$Z_{in} = \frac{sC}{g_{m1}g_{m2}}$$

----------(4.9)

which is the impedance of an equivalent inductance $L_{eq} = \frac{C}{g_{m1}g_{m2}}$ The circuit in Figure 4.8 thus simulates a grounded inductance.

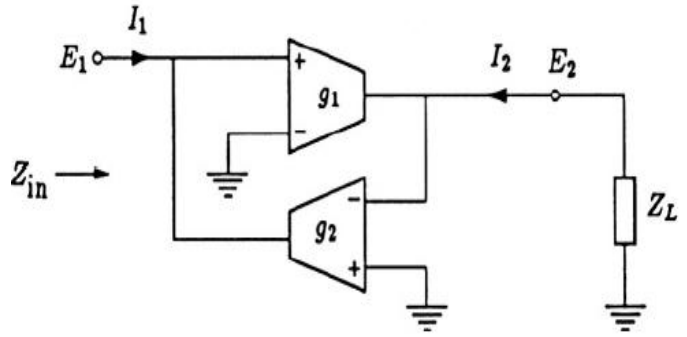


Figure 4.8 OTA Simulation of grounded inductance

If a floating inductance is required, use two inverters and a grounded capacitor, as shown in Figure 4.9.

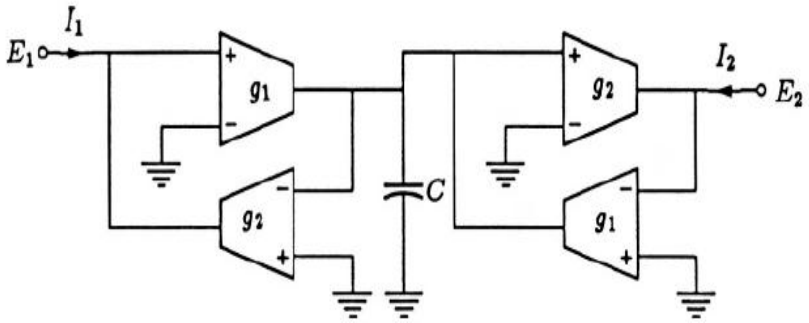


Figure 4.9 OTA Simulation of floating inductance

4.3 Filter Fundamentals

Filters as linear systems can be easily analyzed and synthesized with network transfer functions in frequency domain. In Continuous-time domain, Laplace transform can be

used to model the transfer functions, while in discrete-time domain, Z-Transform is applied. Referring to Figure 4.10, the schematic representation of a filter system, in continuous-time domain, the filter transfer function can be defined in terms of Laplace-transformed excitation X(s) and zero state response Y(s).

$$H(s) = \frac{L[y(t)]}{L[(x(t)]} = \frac{Y(s)}{X(s)}$$

$$\frac{a_m s^m + a_{m-1} s^{m-1} + ... + a_0}{a_n s^n + a_{n-1} s^{n-1} + ... + b_0} = \frac{N(s)}{D(s)}$$

----------(4.10)

Where $m \leq n$ for any realizable practical network. N and D are the numerator and denominator polynomials. n is the order of the filter.

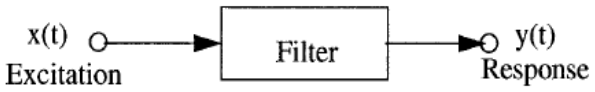


Figure 4.10 Schematic representation of filter system

If the numerator and denominator polynomial of Eq. (4.10) are factored, H(s) can be written in the following alternative representation

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_m (s - z_1)(s - z_2).....(s - z_m)}{b_n (s - p_1)(s - p_2).....(s - p_n)}$$

----------(4.11)

In Eq. (4.11), $z_1, z_2, ...z_m$ are referred to as the zeros of H(s) and $p_1, p_2, ...p_m$ are referred as the poles of H(s).

Under steady state conditions, the transfer functions of Eq.(4.10) can be written as

$$H(s) = H(j\omega) = H(j\omega)e^{j\Phi(\omega)}$$

----------(4.12)

Where $H(j\omega)$ is the magnitude response and $\Phi(\omega)$ is the phase response of the filter. Normally the filter magnitude response requirements are specified as gain in decibels [dB] which is defined as

$$G(\omega) = 20\log H(j\omega) \qquad \text{[dB]}$$

----------(4.13)

While $\Phi(\omega)$, in radians, is the phase response of the filter. Sometimes it is prescribed via the group delay $\tau(\omega)$, defined as

$$\tau(\omega) = -\frac{d\phi(\omega)}{d\omega}$$

----------(4.14)

$\tau(\omega)$ represents the delay experience by a component of frequency ω of the input spectrum.

The order of denominator of a filter transfer function is called the order of the filter. The filter order decides the frequency selectivity of the filter. A higher order means high frequency selectivity. Some of the other specifications of the filter which are not directly involved in choosing the filter transfer function, but are very critical factors are, Noise performance related to signal to noise ratio (SNR), Linearity performance defined using a term called “Total Harmonic Distortion (THD)” and dynamic range, power consumption etc.

4.4 Filter Architecture

There are mainly three methods to realize high order analog filters, namely the cascade approach, the multiple-loop feedback and the ladder simulations approach. For boh

cascade and multiple-loop feedback techniques, high order filter are realized by constructing first and second-order filter sub-networks. The ladder simulations technique has excellent low sensitivity properties.

4.4.1 Sensitivity

Analog filter are realized by interconnecting electrical components. These components may deviate from their nominal design value due to fabrication tolerances, environmental effects such as temperature and humidity variations, and chemical changes that occur during the circuit life. Consequently, the filters performances will deviate from the desired design value. Presumably, these deviations may differ due to different filter architecture adopted. Selectivity is one of the most important criteria for the comparing different architecture.

Given a component x, then in general any performance criteria P, such as the quality factor, a pole or zero frequency, or the magnitude response, will depend on x; such that $P = P(x)$. The sensitivity is defined as the deviation in P called by an error Δx. As expressed as

$$S_x^P = \frac{dP/P}{dx/x} = \frac{d(\ln P)}{d(\ln x)}$$

----------(4.15)

The Eq.(4.15) indicate that the relative change of a performance measure P, is S_x^P times as large as relative change of the circuit parameter x on which P depends.

Thus

$$\frac{\Delta P}{P} = S_x^P(\frac{\Delta x}{x})$$

----------(4.16)

Therefore, good circuits should have low sensitivities to variations of their components. The deviation in performance P caused by tolerance of one single component x is measured by single-parameter sensitivity. Actually a filter consists of many components which will all impact to the performance P variation.

4.4.2 Cascade Realizations

The voltage transfer functions of a high order filter can be expressed as

$$H(s)=\frac{V_o}{V_i}=\frac{N(s)}{D(s)}=\frac{a_m s^m+a_{m-1}s^{m-1}+.....+a_1 s+a_0}{s^n+b_{n-1}s^{n-1}+.....+b_1 s+b_0}$$

----------(4.17)

With $n \geq m$ and n>2. Here assumptions is that both m and n are even, so that N(s) and D(s) can be factored into the product of second order pole-zero pairs.If N(s) and D(s) are odd functions, it can factored into product of even functions and first order functions.

So, Eq. (4.17) can be written as product of second order functions

$$H_k(s)=\frac{a_{2k}s^2+a_{1k}s+a_{0k}}{s^2+s(w_{pk}/Q_{pk})+{w_{pk}}^2}$$

----------(4.18)

Such that

$$H(s)=\prod_{k=1}^{n/2}H_k(s)=\prod_{k=1}^{n/2}\frac{a_{2k}s^2+a_{1k}s+a_{0k}}{s^2+s(w_{pk}/Q_{pk})+{w_{pk}}^2}$$

----------(4.19)

The transfer functions of the individual biquads are labeled $H_k(s)$. If it is assumed that the output impedances of the biquads are sufficiently small, each second order block will produce a voltage transfer function of order 2. Several second-order blocks can be connected in cascade to realize a high order voltage mode filter as in Figure 4.11. Therefore overall transfer function can be expressed as

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{V_{01}V_{02}}{V_{in}V_{01}} \ldots\ldots\ldots \frac{V_{n/2-1}V_{out}}{V_{n/2-2}V_{n/2-1}}$$

$$H(s) = H_1 H_2 \ldots\ldots\ldots H_{n/2-1} H_n$$

----------(4.20)

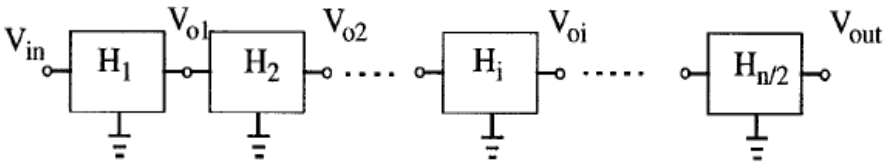


Figure 4.11 Cascaded realization of nth-order transfer functions

Here component x exists in biquadratic section H_j and n/2 biquad sections have no interaction with each other, so the performance impact on H(s) cased by the variations Δx can be derived as [1]

$$S_x^{H(s)} = S_{H_j(s)}^{H(s)} S_x^{H_j(s)} = S_x^{H_j(s)}$$

----------(4.21)

Eq 4.21 indicates that in cascade connection the sensitivity of high order transfer function to the element x and its variations in relation to x are as large as those of the second order block which contains the element

4.4.3 The Multiple-loop Feedback Realization

In the cascade realizations approach, there is no feedback between the biquadratic sections. However the second class of cascading techniques involves feedback across the biquadratic sections. In this approach multiple feedbacks is applied in a cascade

connection of biquadratic sections. This leads to a better sensitivity performance of the overall circuit compared to the corresponding circuit obtained using the Cascade approach. This approach has two general topologies: the leapfrog topology [147], and the summed-feedback topology [148].

4.4.3.1 Leapfrog Topology

The leapfrog (LF) configuration is shown in Figure 4.12. Each of the boxes named Ti realizes a second order lossless filter transfer function (biquad) except for the terminations at the input and output. The feedback loop always comprises of two sections; thus, inverting and non-inverting sections must alternate to keep the loop gains negative and the loops stable [147]. If the circuit is derived from a resistively terminated lossless ladder filter, as is normally the case, T_1 and T_n are lossy and all the internal sections are lossless.

A lossless block implies a function T_i with infinite Q, which may not be stable by itself, but the overall feedback connection guarantees stability. This topology is useful in the functional simulation of LC ladder filter.

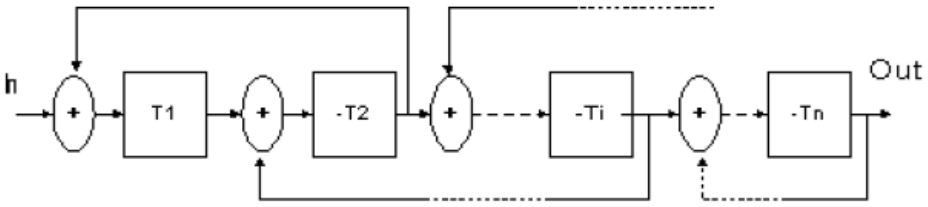


Figure 4.12 Leapfrog Topology

4.4.3.2 Summed-feedback topology

The summed-feedback topology [148], as shown in Figure 4.13, is not suitable for realizing any finite transmission zeros. To overcome this problem, one of two techniques can be used: (1) the multiple-or distributed-input technique, in which the input signal is

also fed to the input of all cascading sections, or (2) the summation of the input signal and the output signals from all cascaded sections.

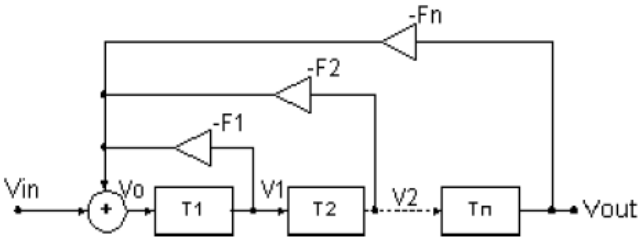


Figure 4.13 Summed-feedback topology

There are three other design methods based on that topology: the primary resonator block (PRB) [149] where all the used T_i stages are identical, the follow-the leader feedback (FLF) [150], and the shifted-companion form (SCF) [151]. Both the FLF and SCF methods are generalizations of the PRB method. The general block diagram of FLF [150] method is shown in Figure 4.14. In this case, T_i can be first order low pass or high pass functions or alternatively second order biquadratic sections. The summation of the feedback voltages is responsible for the realization of the poles of the function, while the second summation is required for the realization of any finite transmission zeros.

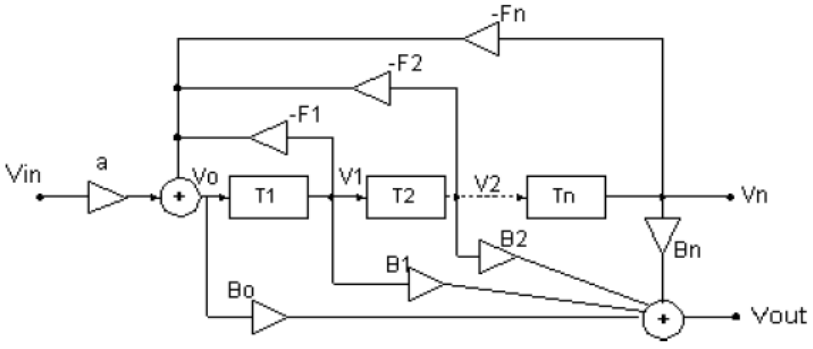


Figure 4.14 Follow-the-leader feedback (FLF) topology

4.4.3.3 LC Ladder Simulation

Another approach to realize a high-order OTA-C filter is to take a passive LC filter with known element values and replace its elements or groups of elements with OTA circuits. This approach enables us to take advantage of the wealth of information generated for

passive filters. The LC ladder arrangement shown in Figure 4.15(a) is example of third-order high pass filter.

We first convert the series arrangement of E_1 and R_1 into its Norton's equivalent, as shown in Figure 4.15(b). Then, the resistances and inductance in this circuit can be replaced by the OTA modules mentioned section 4.2

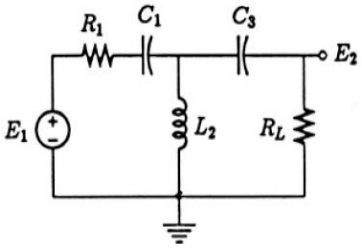
Starting from the left, OTA g_1 convert voltage E_1 into a current equal to $E_1 g_1$. OTA g_2 simulates a grounded resistor. OTAs g_3, g_4 and capacitor C_2 form a circuit that simulates a grounded inductor, as given in Figure 4.8. Finally OTA g_5 Simulates the grounded resistor R_L.

$$g_1 = g_2 = \frac{1}{R_1}$$

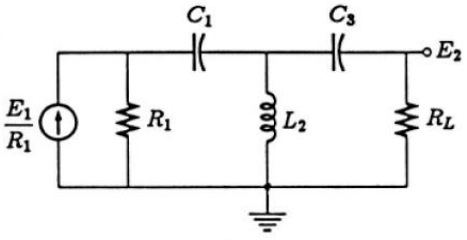
$$\frac{C_2}{g_3 g_4} = L_2$$

$$g_5 = \frac{1}{R_L}$$

----------(4.22)



(a)



(b)

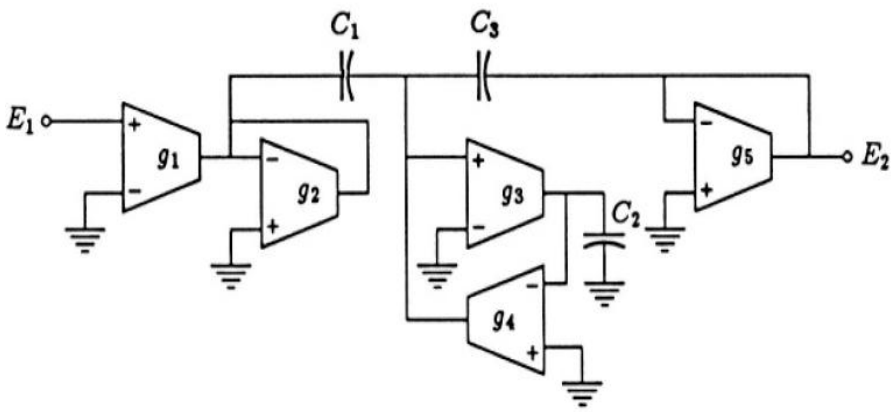


Figure 4.15 LC Ladder Methodology

4.4.3.4 Performance Comparison of the three different architecture

The cascade method is widely used in industry because it is very easy to implement, and efficient in its use of active devices. It used a modular approach and results in filters that show satisfactory performance in practice. The main advantage of cascade filter is that it is very easy to tune because each biquad is responsible for the realization of only one pole pair (and zero pair), the realizations of the individual critical frequencies of the filter are decoupled from each other. The main disadvantage of this decoupling is that for the filters of high order with stringent requirement and tight tolerances, cascade designs are often found to be too sensitive to component variations in the pass band.

Compared with cascade approach, the multiple-loop feedback shows superior sensitivity performance in high order filter realizations due to the nature of coupling between biquad sections. The main disadvantage is the multiple-loop feedback is normally quite complicated to synthesize.

Active filters simulating the behavior of LC ladders have been found to have the lowest sensitivity and consequently to be the most appropriate for filters with stringent requirement. The main disadvantage of this design method is that passive LC prototype must exist before as active simulation can be attempted. Also, usually a relatively large number of active devices are required for this approach.

In summary, among high order active filter realizations, those that simulate the behavior of LC ladders have been found to have lowest sensitivity component variations. Cascade realizations often have transfer function variability that are quite unacceptable in practice, while multiple-loop feedback method is in between for the sensitivity performance. On the other hand, ladder simulation filters consume maximum active devices among th three methods. The cascade realized filters take minimum active devices while multiple-loop feedback realized filters are also in between.

Table.4.1 Comparison of Filter Topologies

Type	**Approach**	**Sensitivity performance**	**Design**
Cascade	Biquadratic sections are cascaded	Bad	Simple and easily tunable
Multiple-Loop Feedback	Multiple feedback is applied in cascade of biquadratic sections	Good	Complex More critical nodes due to feedback
LC Ladder Simulation	Simulation of passive lossless ladder networks	Best	Simple

4.5 Active CMOS Gm-C Filters

4.5.1 Introduction

Filters are used in any electronic system where it is necessary to control the bandwidth of the signal path. Filters are frequency-selective electronic circuits designed to pass a band of wanted signals and stop or reject unwanted signals, noise or interference outside the pass band [1-25]. Filters played an essential role in many fields. In recent years, the rapid advances in computer hard disk drive (HDD) [152-157] and wireless communication systems [158-164], considerable demand for higher performance filtering circuits.

In general, filters are classified according to the function they perform. Over the frequency range of interest of a filter, we define passband and stopband. Ideally, the passband of a filter is the range of frequencies over which signals are transmitted from input to output without attenuation or gain. Note that in practice, active devices may be used to achieve gain or amplification. In the stopband, the transmitted signal is highly attenuated. The disposition of passbands and stopbands lead to the four most common types of filter classification. These are lowpass, highpass, bandpass, and bandstop (or also referred to as notch) filters.

Active-RC filters have been widely used in low-frequency applications for a long time [165-169]. Discrete active-RC filters were successful substitutes for passive-RLC filters at low audio frequencies for reasons of size and economy. However, they were found less suitable for high-frequency applications and fully integrated implementations due to the high frequency limitations of op-amps and the large chip area requirements of resistors. Consequently, many alternative active filter circuit topologies have been developed to overcome these drawbacks, for example the popular switched-capacitor filter. In switched-capacitor filter structures, MOS switches and capacitors effectively replace the resistors (unsuitable for full integration) in active-RC filter structures.

Nowadays, switched-capacitor filters can be fully integrated using all available IC technologies especially CMOS. In addition, precision frequency response is achievable without on-chip tuning, and high dynamic range can be achieved. However, they are still not suitable for very high frequency applications due to the sampling mode of their operation, which would require very high clock speeds, along with the use of extra continuous-time (CT) input anti-aliasing filters and output smoothing filters.

CT filters based on the operational transconductance amplifier (OTA) (also referred to as V-I converter, transconductor, or transconductance amplifier) and capacitors, the so-called OTA-C, or gm-C, filters have received the greatest interest and attention in recent research [170-173, 152-169]. OTA-C filters offer advantages over traditional active-RC filters in terms of design simplicity, high frequency capability, electronic tunability, suitability for monolithic integration, reduced component count, and potential for design automation. Although OTA-C filters are primarily aimed at high frequency operation. OTA-C filters have been widely used in communication systems [152-169].

The performance of a filter relies strongly on the circuit components, filter structure, design methods, and IC technology used. In particular, different circuit components and IC technology can result in very different performances for the chosen filter topology. The design of a high performance OTA-C filter is a complex task. It must simultaneously optimize different requirements, such as operating frequency range, power consumption, noise and dynamic range, sensitivity to device variations and fabrication tolerances, chip area, and cost. A number of IC technologies such as Bipolar [174-175], BiCMOS [176-180], CMOS [152-169], GaAs, etc have been used for integrated filter design.

CMOS has now become the preferred technology for analogue design. Practical analogue filters are typically designed in CMOS technologies requiring supply voltages at or below 3.3V. Most analogue or mixed-signal systems are power critical, and power consumption is limited to a few milliwatts.

Motivated by the rapidly growing mobile and wireless communication market, fully integrated filters for very high frequency and low power consumption applications have received considerable worldwide attention. The most important filters for fully integrated high frequency applications are perhaps the OTA-C filters, which have been extensively investigated and widely utilized. Structure generation, design methods, performance analysis and comparison of OTA-C filters have been extensively investigated.

The operational transconductance amplifier (OTA) is the main building block in the filter topology [181-191].The key function of the OTA is to convert the input voltage into the output current while accuracy and linearity are both maintained. However, the nonidealties of the OTA dominate the filter performance. The parasitic capacitors produce deviation of 3 dB cutoff frequency of filters, the finite output impedance affects the quality factor, and the voltage-to-current conversion affects the filter linearity. When designing a wireless receiver, one of the most important tasks is to design IF filter to separate the desired signal from the unwanted ones. Traditionally multi-standard terminals emerge based on maximum hardware reuse from end to end coupled with a full CMOS implementation with the ultimate goal of a single chip solution. It is found the down conversion architecture, as shown in Fig: 4.16 is well suited for these terminals and has been attracting world-wide attention in recent years.

With down-conversion architectures, several standards such as FM, Bluetooth, GSM, WCDMA, Wi-Fi can be accommodated using a single receiver. This has obvious advantages in terms of reduction in power consumption and silicon area. Although there are a number of high-performance filters designs in the literature [192-198] with different tuning range it is still challenge to achieve high Q and accuracy of filter tuning [193,197-200]. The accuracy of the Gm-C filters can be further improved by employing automatic tuning scheme.

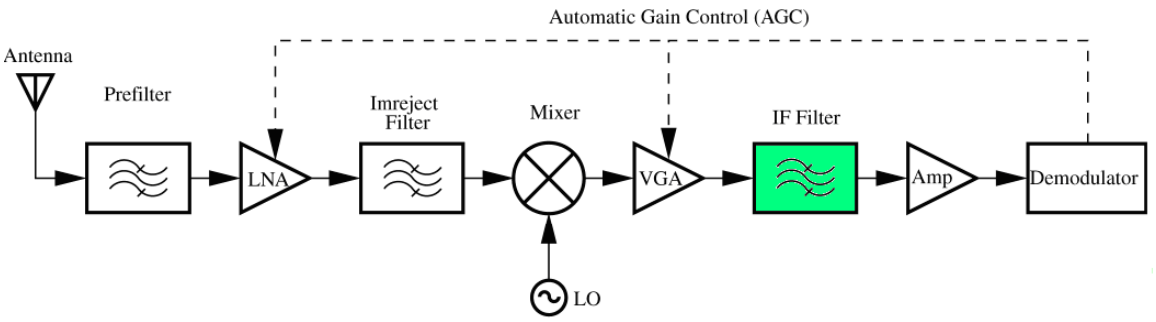


Figure 4.16 Basic Down conversion Receiver

The OTA-C technique offers the advantage that the transconductance can be tuned This is accomplished either by controlling the bias current of the input transistors, or their drain-source voltage in the case of triode-region MOS transconductors. A transconductor design with a very wide tuning range is needed to realize the required cut-off frequency tuning range [201].

The main limitation of using the transconductance control is that the linearity of the transconductor is dependent on the tuning bias. The larger bias current, the better linearity is achieved. Moreover, the linearity is not constant [202-203].

Transconductance tuning can be either the capacitors, as shown in Figure 4.17(a) [204], or the transconductors, as depicted in Figure 4.17(b) [204-205] can be switched to make a large step in the cut-off frequency. Analogue circuits based on the operational transconductance amplifier (OTA) and capacitor (OTA-C) technique is promising for high-frequency operation [206]. Having an OTA of programmable transconductance and a programmable capacitor, it is possible to design filters for a wide frequency tuning range. For most CMOS processes, it is not possible to create a capacitor with a wide range of programmability which can operate at high frequencies. Therefore, the transconductor must have a wide tuning range.The OTA-C technique is offer such advantages as high speed and low power [207, 201, and 206] but also has limited applicability because of low dynamic range and poor linearity compared with the active-

RC technique [208]. In order to increase the dynamic range of OTA-C filters, transistor level design is most important, because the linearity of the filter is directly related to the linearity of the OTA. Therefore, a wide range of techniques have been proposed in literature to improve the linearity of transconductors. Using current conveyors [96] and resistors as building blocks, it is possible to design highly linear transconductors.

There is a trade-off between linearity and power consumption. Source degeneration OTA circuit topologies are used in order to optimize the linearity and power consumption. In [205, 209], low power consumption and large dynamic range is achieved. The drawback is relatively small tuning range. To avoid this problem, a so-called negative source degeneration resistor (NSDR) OTA circuit topology is proposed in [201]. In addition, a new adaptive DC-blocking, triode-biased MOSFET transconductor is proposed in [203], which enables wide and continuous frequency tuning with low power consumption. A single OTA integrator-based OTA-C filter may be needed to further reduce power consumption and chip area [210].

The OTA-C technique is vulnerable to all parasitic components; this includes the effect of switches in series with capacitors or elsewhere in the signal path. The filter circuit structure plays an important role in determination of filter performance. The cascade structure can be implemented with lower power consumption and smaller silicon area than ladder simulation methods, but sensitivity is relatively high. On the other hand, ladder simulation structures have low sensitivity, but cost more power consumption and chip area due to the need for extra OTA convert floating capacitors

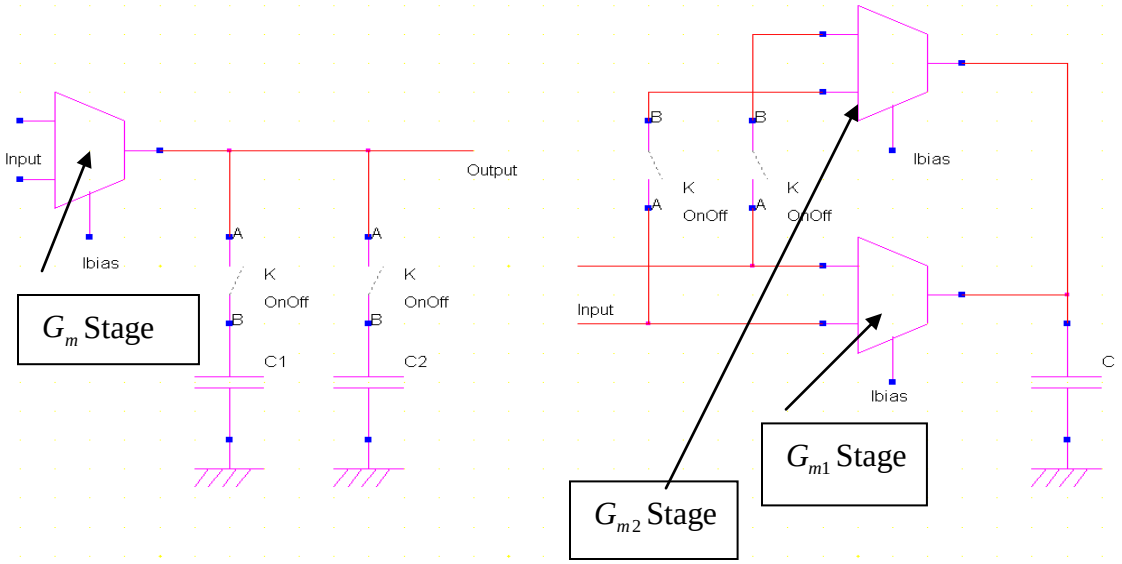
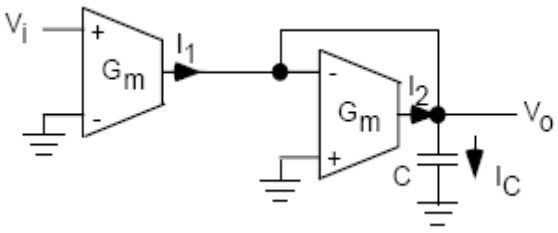


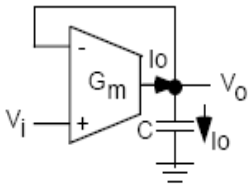
Figure 4.17(a) Tuning using Switched Capacitance (b) Tuning using Switching OTA

4.5.2 Design of First Order Gm-C Filter

Figure 4.18 shows the first order Gm-C filter building blocks.



(a)



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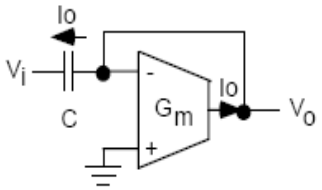

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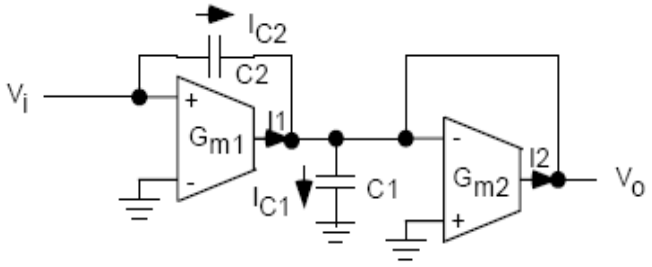


(d)

Figure 4.18 First Order Single-Ended Gm-C Filter

In Figure 4.18(a)

$$I_1 = G_m V_i$$

$$I_2 = -G_m V_0$$

$$I_c = sCV_0 = I_1 + I_2 = G_m V_i - G_m V_0$$

$$(sC + G_m)V_0 = G_m V_i$$

$$\frac{V_0}{V_i} = \frac{G_m}{sC + G_m} = \frac{G_m / C}{S + G_m / C} = \frac{w_0}{s + w_0}$$

----------(4.23)

In Figure 4.18(b)

$$I_0 = G_m(V_i - V_0) = sCV_0$$

$$\frac{V_0}{V_i} = \frac{G_m}{sC + G_m} = \frac{G_m / C}{S + G_m / C}$$

----------(4.24)

That is Figure 4.18(a) and 4.18(b) implements the same transfer function.

In Figure 4.18(c)

$$I_0 = -G_m V_0 = sC(V_0 - V_i)$$

$$\frac{V_0}{V_i} = \frac{G_m}{sC + G_m} = \frac{s}{s + G_m / C} = \frac{s}{s + w_0}$$

----------(4.25)

In Figure 4.18(d)

$$I_1 = G_{m1}V_i$$

$$I_2 = -G_{m2}V_0$$

$$I_{c2} = sC_2(V_i - V_0)$$

$$I_{c1} = sC_1V_0 = I_1 + I_2 + I_{c2} = G_{m1}V_i - G_{m2}V_0 + sC_2(V_i - V_0)$$

$$\frac{V_0}{V_i} = \frac{sC_2 + G_{m1}}{s(C_1 + C_2) + G_{m2}} = \frac{s[C_2/(C_1 + C_2)] + [G_{m1}/(C_1 + C_2)]}{s + [G_{m2}/(C_1 + C_2)]} = \frac{a_1 s + a_0}{s + w_0}$$

----------(4.26)

Table 4.2 Gm-C First Order Filter Transfer Function

Circuit Type	Transfer Function	w_0
First order Low pass Figure 4.18(a) and (b)	$\frac{G_m/C}{S + G_m/C}$	G_m/C
First order Low pass Figure 4.18(c)	$\frac{s}{s + G_m/C}$	G_m/C
General First order Figure 4.18(d)	$\frac{s[C_2/(C_1 + C_2)] + [G_{m1}/(C_1 + C_2)]}{s + [G_{m2}/(C_1 + C_2)]}$	$G_{m2}/(C_1 + C_2)$

From Eq. (4.26)

$$TF(s) = \frac{s[C_2/(C_1 + C_2)] + [G_{m1}/(C_1 + C_2)]}{s + [G_{m2}/(C_1 + C_2)]} = \frac{a_1 s + a_0}{s + w_0}$$

$$\frac{C_2}{C_1 + C_2} = a_1$$

$$C_2 = (\frac{a_1}{1 - a_1})C_1$$

$$\frac{G_{m1}}{(C_1 + C_2)} = a_0$$

$$\frac{G_{m2}}{(C_1 + C_2)} = w_0$$

$$C_1 + C_2 = C_1 + (\frac{a_1}{1 - a_1})C_1 = \frac{C_1}{1 - a_1} = \frac{G_{m2}}{w_0}$$

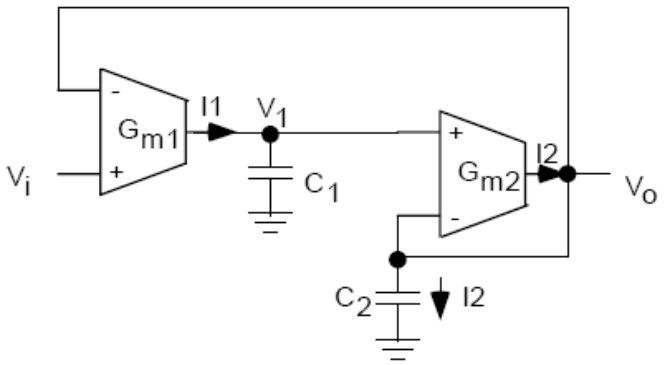
----------(4.27)

4.5.3 Design of Second Order Gm-C Filter

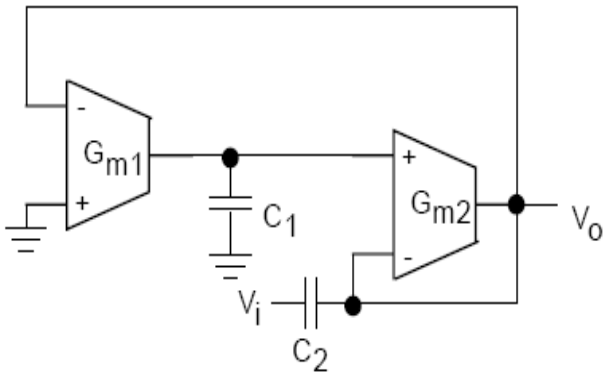
There are two different design for second order Gm-C filter building blocks. One requires two OTAs while other three OTAs. The selection depends on whether an adjustable Q is required or not.

Figure 4.19 shows the second order filter implementation using 2 OTAs. The implementation has non-adjustable Q, once the capacitive component had been determined.

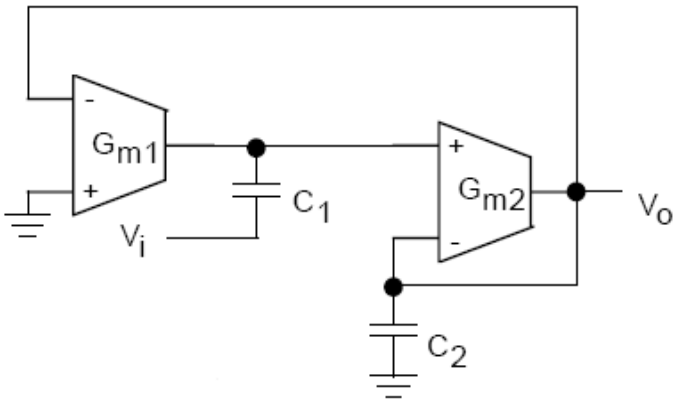
Fixed Q Implementation



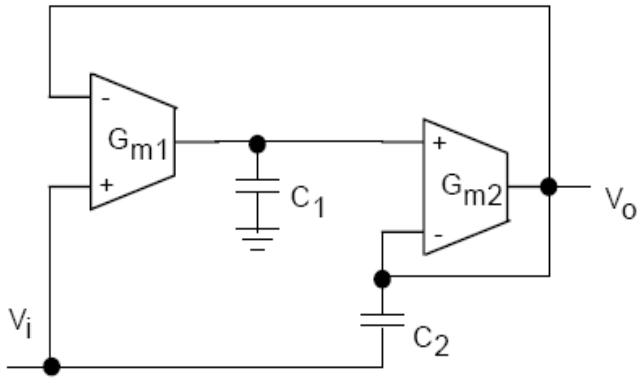
(a) Low Pass Filter



(b) High Pass Filter



(c) Band Pass Filter



(d) Band Stop Filter

Figure 4.19 Second Order Single-Ended Gm-C Filter

The transfer function for low pass circuit in Figure 4.19(a)

$$I_1 = G_{m1}(V_i - V_0)$$

$$I_2 = G_{m2}(V_i - V_0)$$

$$V_1 = \frac{I_1}{sC_1} = \frac{G_{m1}}{sC_1}(V_i - V_0)$$

$$V_0 = \frac{I_2}{sC_2} = \frac{G_{m2}}{sC_2}[\frac{G_{m1}}{sC_1}(V_i - V_0) - V_0]$$

$$\frac{V_0}{V_i} = \frac{G_{m1}G_{m2}}{s^2C_1C_2 + sC_1G_{m2} + G_{m1}G_{m2}} = \frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s(\frac{G_{m2}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$$

----------(4.28)

Comparing the transfer function of Eq.(4.28) with standard low pass transfer function as shown in Table 4.3. The w_0 and Q are obtained as follows:

Table 4.3 Gm-C Second Order Filter (Fixed Q) Transfer Function

Circuit Type	Transfer Function
Low Pass	$\frac{w_0^2}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$
High Pass	$\frac{s^2}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$
Band Pass	$\frac{s(\frac{w_0}{Q})}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$
Band Stop	$\frac{s^2 + w_0^2}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$

$$w_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} = \frac{G_m}{\sqrt{C_1C_2}}; \text{ if } G_m = G_{m1} = G_{m2}$$

$$\frac{w_0}{Q} = \frac{G_{m2}}{C_2}$$

$$Q = \frac{w_0 C_2}{G_m} = \sqrt{\frac{C_2}{C_1}}$$

----------(4.29)

For a given value of C_1 and C_2, Q is fixed but w_0 can be adjusted by changing G_m. The expressions for the High pass, Band pass and Band stop can be derived in a similar way. The results are summarized in Table. 4.4.

Table: 4.4 Gm-C Second Order 2 OTAs Implementation Filter Parameter

Circuit Type	**Transfer Function**	w_0^*	Q
Low Pass w_0 **adjustable** **Q Fixed** **Fig 4.19(a)**	$\frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s(\frac{G_{m2}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C_2}{C_1}}$
High Pass w_0 **adjustable** **Q Fixed** **Fig 4.19(b)**	$\frac{s^2}{s^2 + s(\frac{G_{m2}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C_2}{C_1}}$
Band Pass w_0 **adjustable** **Q Fixed** **Fig 4.19(c)**	$\frac{s(\frac{G_{m2}}{C_2})}{s^2 + s(\frac{G_{m2}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C_2}{C_1}}$
Band Stop w_0 **adjustable** **Q Fixed** **Fig 4.19(d)**	$\frac{s^2 + \frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s(\frac{G_{m2}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C_2}{C_1}}$

* Assume $G_m = G_{m1} = G_{m2}$

The capacitance can be computed from any of the four transfer functions.

$$w_0 = w = \frac{G_m}{\sqrt{C_1 C_2}}$$

$$C_1 C_2 = (\frac{G_m}{w})^2$$

$$Q = \sqrt{\frac{C_2}{C_1}}$$

$$C_2 = Q^2 C_1$$

$$Q^2 C_1^2 = (\frac{G_m}{w})^2 = C^2$$

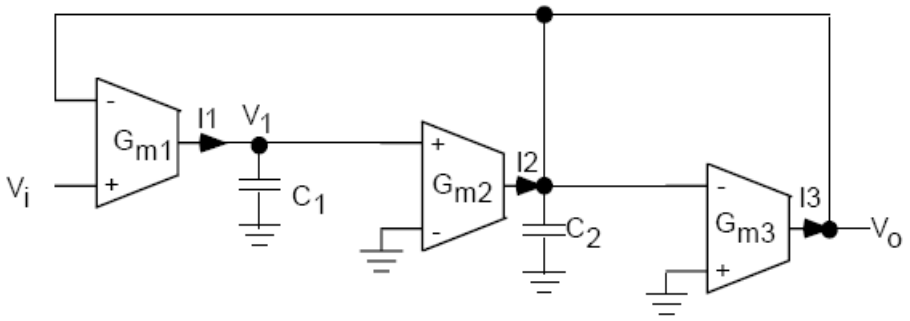
$$C = \frac{G_m}{w}$$

$$C_1 = \frac{C}{Q}$$

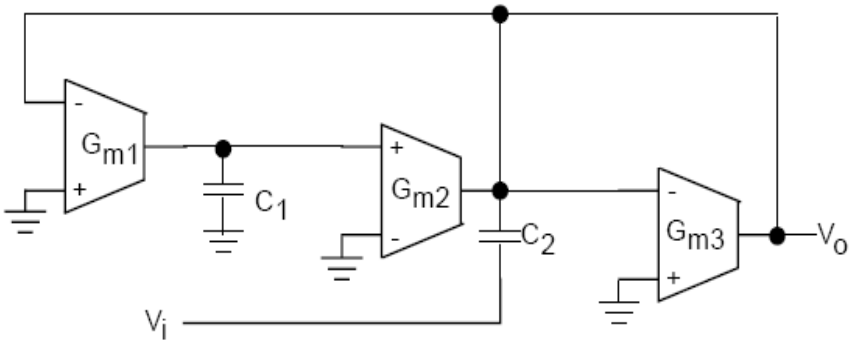
$$C_2 = Q^2 C_1$$

----------(4.30)

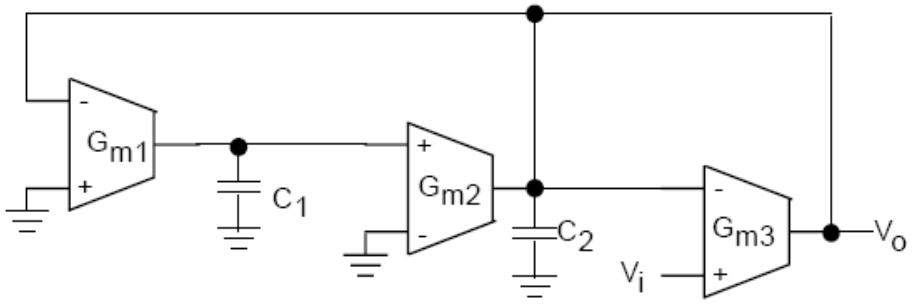
Adjustable Q Implementation



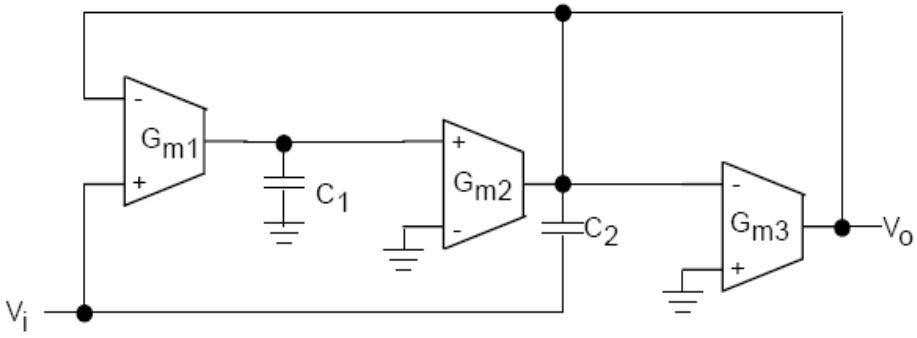
(a) Low Pass Filter



(b) High Pass Filter



(c) Band Pass Filter



(d) Band Stop Filter

Figure 4.20 Gm-C Second Order Filter Implementation with adjustable Q

Figure 4.20 shows the second order filter implementation using 3OTAs.The implementation has adjustable Q, its value is determined by third OTA. The transfer function derivation for low pass circuit 4.20(a) is as follows.

$$I_1 = G_{m1}(V_i - V_0)$$

$$I_2 = G_{m2}V_1$$

$$V_1 = \frac{I_1}{sC_1} = \frac{G_{m1}}{sC_1}(V_i - V_0)$$

$$I_2 = \frac{G_{m2}G_{m1}}{sC_1}(V_i - V_0)$$

$$V_0 = \frac{1}{sC_2}[I_2 + I_3] = \frac{1}{sC_2}[\frac{G_{m2}G_{m1}}{sC_1}(V_i - V_0) - G_{m3}V_0]$$

$$\frac{V_0}{V_i} = \frac{G_{m1}G_{m2}}{s^2C_1C_2 + sC_1G_{m3} + G_{m1}G_{m2}} = \frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s(\frac{G_{m3}}{C_2}) + \frac{G_{m1}G_{m2}}{C_1C_2}}$$

----------(4.31)

Comparing the transfer function of Eq.(4.31) with standard low pass transfer function as shown in Table 4.3. The w_0 and Q are obtained as follows:

$$w_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} = \frac{G_m}{C}; \text{ if } G_m = G_{m1} = G_{m2} \text{ and } C = C_1 = C_2$$

$$\frac{w_0}{Q} = \frac{G_{m3}}{C_2}$$

$$Q = \frac{w_0C}{G_{m3}} = \frac{G_m}{G_{m3}}$$

----------(4.32)

For a given capacitor value, Q and w_0 can be adjusted independently of each other. Q can be adjusted by G_{m3} and w_0 by G_m .The expressions for the High pass, Band pass and Band stop can be derived in a similar way. The results are summarized in Table. 4.5.

Table 4.5 Gm-C Second Order 3 OTAs Implementation Filter Parameter

Circuit Type	Transfer Function	w_0^*	Q
Low Pass w_0 **adjustable** **Q adjustable** **Fig 4.20(a)**	$\frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2+s(\frac{G_{m3}}{C_2})+\frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{C}$	$\frac{G_m}{G_{m3}}$
High Pass w_0 **adjustable** **Q adjustable** **Fig 4.20(b)**	$\frac{s^2}{s^2+s(\frac{G_{m3}}{C_2})+\frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{C}$	$\frac{G_m}{G_{m3}}$
Band Pass w_0 **adjustable** **Q adjustable** **Fig 4.20(c)**	$\frac{s(\frac{G_{m3}}{C_2})}{s^2+s(\frac{G_{m3}}{C_2})+\frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{C}$	$\frac{G_m}{G_{m3}}$
Band Stop w_0 **adjustable** **Q adjustable** **Fig 4.20(d)**	$\frac{s^2+\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2+s(\frac{G_{m3}}{C_2})+\frac{G_{m1}G_{m2}}{C_1C_2}}$	$\frac{G_m}{C}$	$\frac{G_m}{G_{m3}}$

* Assume $G_m = G_{m1} = G_{m2}$ and $C = C_1 = C_2$

$$C = \frac{G_m}{w_0}$$

$$G_{m3} = \frac{G_m}{Q}$$

----------(4.33)

4.6 Implementation of Active CMOS Gm-C Band Pass Filters

4.6.1 Introduction

The market of wireless communications had a tremendous growth over the past few years. Wireless technology is now capable of reaching virtually every location on earth. Hundreds of millions of users exchange information every day using cellular phones and other wireless communication products. There has been also a vast growth, over the last decades, of very large scale integration (VLSI) electronic devices like desktop and laptop computers, personal digital assistants (PDA), cellular phones, tablets, printers, scanners, digital cameras and even home appliances.

The purpose of receiver is to translate RF signals to base-band, which requires the process of shifting incoming frequency, amplify, filtering and finally demodulate. Such process comes across with so many interference like selectivity, Image problem and distortion. Superhetrodyne receiver allows the designer to optimize the receiver performance through choice of Intermediate Frequency and Filtering, followed by mixer. Mixer doesn't "Mix" the two signals but it multiplies the two input sinusoidal signals.

$$(A\sin\omega_1 t)(B\sin\omega_2 t) = \frac{AB}{2}[\cos(\omega_1-\omega_2)t - \cos(\omega_1+\omega_2)t]$$

Down Convert Up-Convert

A mixer can be used to either down-convert or up-convert the RF input signal. Designer must remove the undesired output by filtering. A band-pass pre-selection filter is usually used ahead of the mixer to suppress the image signal. Noise present in the image would also be translated to IF band, degrading signal-to-noise ratio.

There are two cases that apply with down conversion as shown below:

Case 1: Local Oscillator (LO) frequency is higher than RF frequency. This places the image frequency 2 x F_{IF} above the RF frequency. A sharp cutoff Low Pass Filter (LPF) or Band Pass Filter (BPF) could be used to attenuate the image.

$$F_{IF} = F_{RF} - F_{LO}$$

Case 2: RF is frequency higher than Local Oscillator (LO) frequency. This places the image frequency 2 x F_{IF} below the RF frequency. A sharp cutoff Band Pass Filter (BPF) could be used to attenuate the image.

$$F_{IF} = F_{LO} - F_{RF}$$

Band Pass Filters (BPFs) are used in the transmitter and receiver circuits of many wireless systems for channel selection and filtering in the Radio Frequency (RF) and Intermediate Frequency (IF) ranges. The BPFs are designed either as external filters or on-chip filters. External filters provide very high Quality factor (Q) but require buffers to drive the off-chip components. These buffers consume more power and in order to reduce the power consumption, on-chip filters are preferred in wireless systems. On-chip filters are designed with active circuits and offer very low power consumption and good efficiency. Most of the on-chip filters are designed with Operational Transconductance Amplifier (OTA) and capacitors and are generally called as Gm-C filters. The Gm-C filter offers many advantages in terms of low-power and works well at high frequencies. The Gm-C circuits represent a popular technique of integrated realization of high frequency continuous time filters. Gm-C filters can operate in a wide range of frequencies from several hundred of KHz to more than 100MHz.The Q of Gm-C filters can be adjusted by controlling the output impedance even at lower frequencies.

The second order BPFs are designed and simulated with CMOS 0.18μm technology (BSIM3V3 Level 49 parameter) with a supply voltage of 1.8V. The performances of the

filters are analyzed using various parameters like center frequency, gain, bandwidth, Q, S-parameters, power consumption, tuning ratio and noise.

OTAs are used for large gain and large bandwidth performances in filters. As discussed in chapter 3, Wilson Current Mirror OTA (WCM-OTA) has a differential stage consisting of PMOS transistors to charge Wilson mirror. Another two MOSFETs are used to provide the DC bias voltages. But the WCM-OTA has low output voltage swing. Cascode Current Mirror OTA (CCM-OTA) overcomes the draw back of WCM-OTA and has large output voltage swing. The OTA used in designing the band pass filter are shown in Figure 4.21. BPF with a Biquad structure consisting of two OTAs is considered.

A useful feature of OTA is that its transconductance can be adjusted by the bias current. Filters made using the OTA can be tuned by changing the bias current I_{bias} . Two practical concerns when designing an OTA for filter applications are the input signal amplitude and the parasitic input/output capacitances. The external capacitance should be large compared to the input or output parasitic capacitance of the OTA. Large signals cause the OTA gain to become non-linear. This limits the maximum frequency of a filter built with an OTA and causes amplitude or phase errors. These errors can be minimized with proper selection of I_{bias} .

In this section, the design, implementation and performance of the Second order active Gm-C CMOS BPFs operating at IF range with center frequencies 70MHz for GSM receiver and 10.6MHz for FM systems respectively are proposed. If the system is to support more number of carriers then there is need for bandwidth of 3MHz for GSM receiver and 1MHz for FM receiver. The filters that will support this bandwidth have to be designed. Hence BPFs operating at center frequency 70MHz (bandwidth: 3MHz) and 10.6MHz (Bandwidth: 1MHz) are proposed.

This section presents the design of a dual-band Band-pass IF channel selection filter to be used in a Dual-Band conversion receiver for GSM and FM. An automatic tuning system is also implemented.

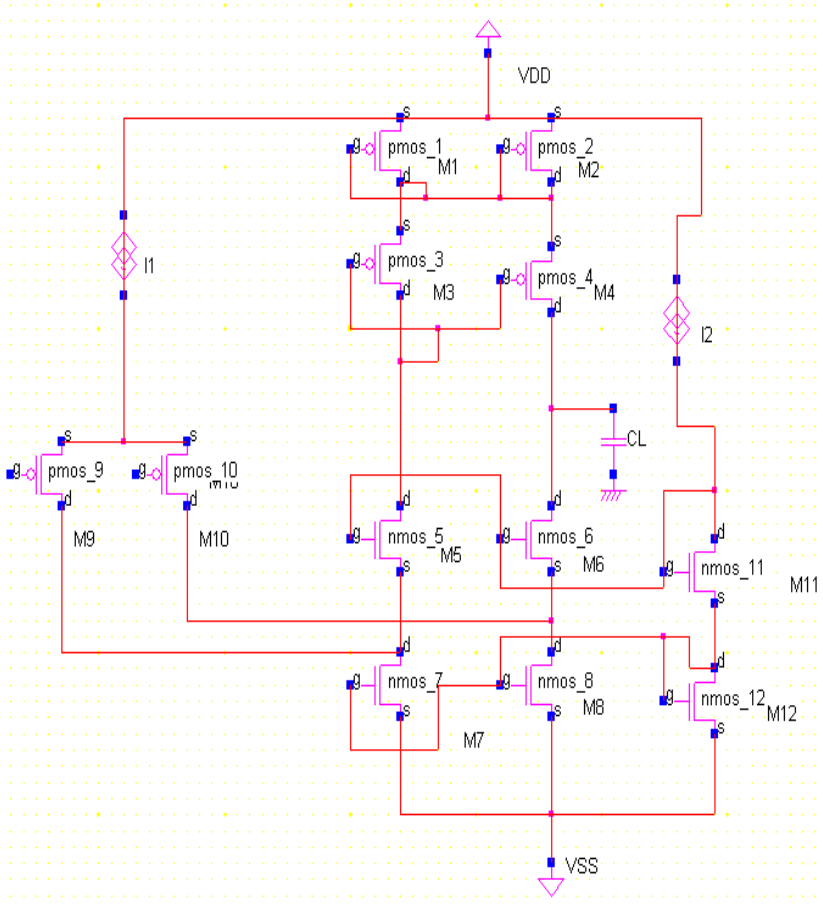


Figure 4.21 Designed Practical Cascode Current Mirror OTA (CCM-OTA)

4.6.2 Filter Specifications

The dual-band filter can be implemented as shown in Figure 4.17, either switching the capacitor or switching the OTAs. Here the problem of nonlinearity of the switches since they are in the signal path. It is challenging to share the same filter structure for both standards.

Table 4.6 Dual Band Filter Specifications

Technology	**0.18µm CMOS**	
Supply Voltage	**1.8V**	
Filter Order	**2**	
Type	**Gm-C**	
Gain	**>0 dB**	
Center Frequency	**GSM:70MHz**	**FM:10.6MHz**
Bandwidth	**3MHz**	**1MHz**
Q Factor	**23**	**10.6**
Power Consumption	**<500µW**	
Tuning Range	**10.6MHz IF to 70MHz IF**	
Tuning Ratio	**6.6**	
S_{21}	**Max at center Frequency**	
S_{11}	**Min. at Center Frequency**	

4.6.3 General Biquad Implementations for Second order CMOS Gm-C Band Pass Filter

A biquad has two poles and two zeros. Poles are complex and always in the LHP (Left Half Plane) and the zeros may or may no be complex and may be in the LHP or the RHP (Right Half Plane).Transfer function for biquad is:

$$H(s) = \frac{V_{out(s)}}{V_{in(s)}} = K\frac{(s-z_1)(s-z_2)}{(s-p_1)(s-p_2)}$$

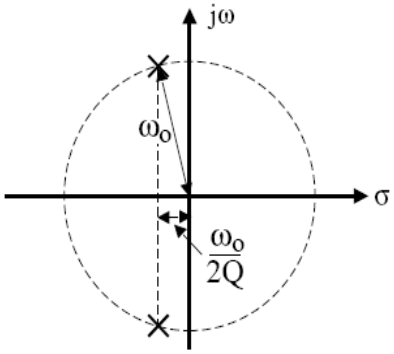
Low pass: zeros at ∞

High pass: zeros at 0

Band pass: one zero at 0 and other at ∞

Band stop: zeros at $\pm j\omega_0$

All pass: Poles and zeros are complex conjugates



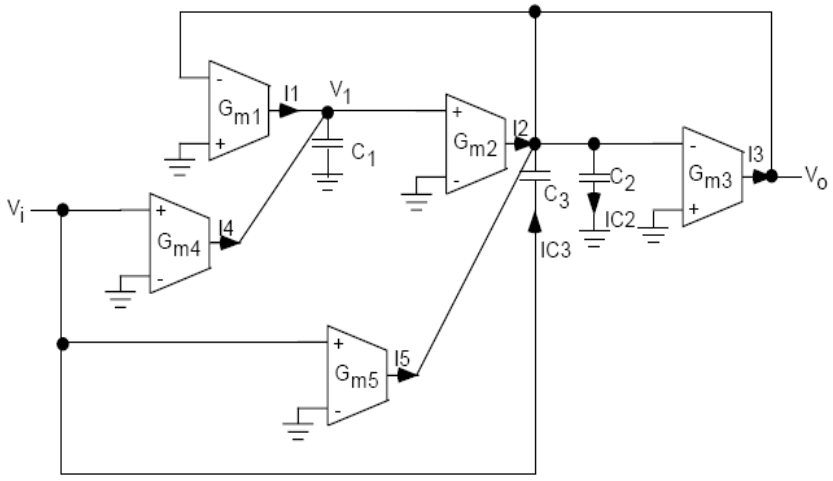


Figure 4.22 General Second Order Biquad Filter Implementation

Figure 4.22 shows the single-ended OTA implementation of general second order biquad filter. The transfer function is derived as follows:

$$I_1 = -G_{m1}V_0$$

$$I_2 = G_{m2}V_1$$

$$I_3 = -G_{m3}V_0$$

$$I_4 = G_{m4}V_i$$

$$I_5 = G_{m5}V_i$$

$$I_{C3} = sC_3(V_i - V_0)$$

$$I_{C1} = I_1 + I_4 = -G_{m1}V_0 + G_{m4}V_i$$

$$V_1 = \frac{1}{sC_1} I_{C1} = \frac{1}{sC_1}(-G_{m1}V_0 + G_{m4}V_i)$$

$$I_{C2} = I_2 + I_3 + I_5 + I_{C3} = G_{m2}V_1 - G_{m3}V_0 + G_{m5}V_i + sC_3(V_i - V_0)$$

$$\frac{V_0}{V_i} = \frac{s^2C_1C_3 + sC_1G_{m5} + G_{m2}G_{m4}}{s^2C_1(C_2 + C_3) + sC_1G_{m3} + G_{m1}G_{m4}}$$

$$\frac{V_0}{V_i} = \frac{s^2(\frac{C_3}{C_2 + C_3}) + s(\frac{G_{m5}}{C_2 + C_3}) + (\frac{G_{m2}G_{m4}}{C_1(C_2 + C_3)})}{s^2 + s(\frac{G_{m3}}{C_2 + C_3}) + (\frac{G_{m1}G_{m4}}{C_1(C_2 + C_3)})} = \frac{a_2s^2 + a_1s + a_0}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$$

----------(4.34)

General Implementation of 5 OTAs reduces to 3 or 2 OTAs for the standard filters such as low pass filter. Comparing the two transfer functions,

$$\frac{V_0}{V_i} = \frac{s^2(\frac{C_3}{C_2 + C_3}) + s(\frac{G_{m5}}{C_2 + C_3}) + (\frac{G_{m2}G_{m4}}{C_1(C_2 + C_3)})}{s^2 + s(\frac{G_{m3}}{C_2 + C_3}) + (\frac{G_{m1}G_{m4}}{C_1(C_2 + C_3)})} = \frac{a_2s^2 + a_1s + a_0}{s^2 + s(\frac{w_0}{Q}) + w_0^2}$$

$$\frac{C_3}{C_2 + C_3} = 0 \Rightarrow C_3 = 0 \Rightarrow open$$

$$\frac{G_{m5}}{C_2 + C_3} = 0 \Rightarrow G_{m5} = 0$$

That means both capacitor C_3 and C_4 cab be deleted, resulting in the circuit shown in Figure4.23 (a).

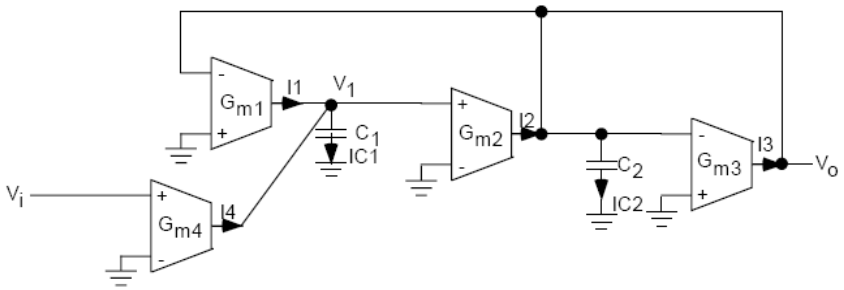


Figure4.23 (a) General Biquad reduces to 4 OTAs

The 4 OTAs implementation can be reduced to 3 OTAs if $G_{m1} = G_{m4}$.

$$I_1 = -G_{m1}V_0$$

$$I_4 = G_{m4}V_i$$

$$I_{C1} = I_1 + I_4 = -G_{m1}V_0 + G_{m4}V_i = G_{m1}(V_i - V_0); G_{m1} = G_{m4}$$

That is, G_{m1} and G_{m4} can be combined as shown in Fig 4.23(b)

$$I_{C1} = I_1 = G_{m1}(V_i - V_0)$$

----------(4.35)

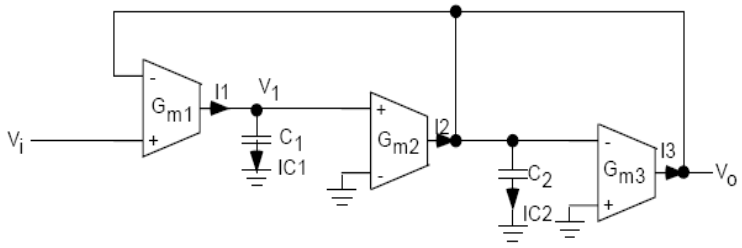


Figure4.23 (b) General Biquad reduces to 3 OTAs

The 3 OTAs implementation can be reduced to 2 OTAs if $G_{m2} = G_{m3}$.

$$I_2 = G_{m2}V_1$$

$$I_3 = -G_{m3}V$$

$$I_{C2} = I_2 + I_3 = G_{m2}V_1 - G_{m3} = G_{m2}(V_i - V_0); G_{m2} = G_{m3}$$

That is G_{m2} and G_{m3} can be combined as shown in Figure 4.23(c)

$$I_{C2} = I_2 = G_{m2}(V_i - V_0)$$

----------(4.36)

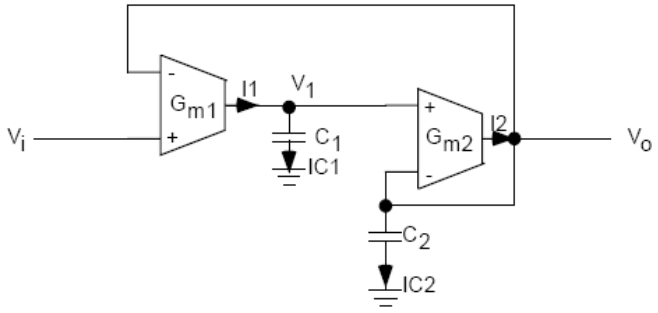
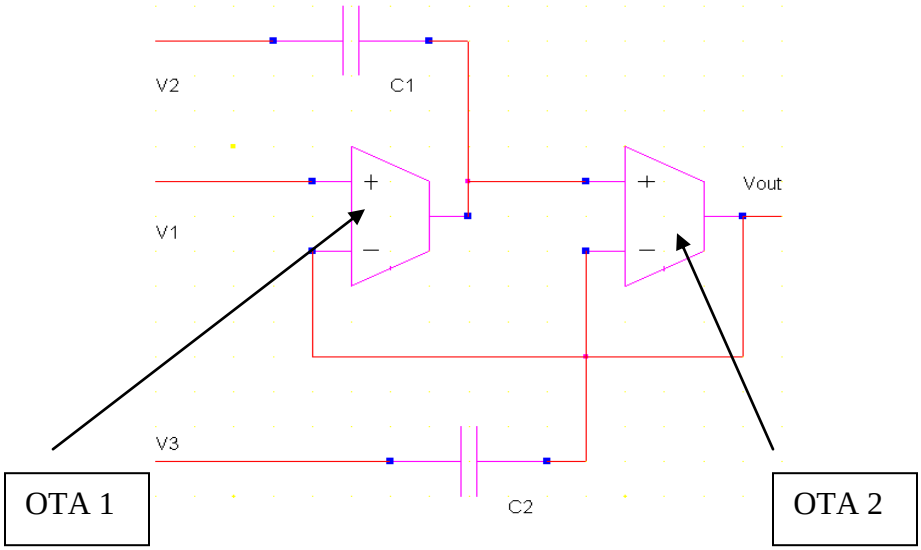


Figure4.23 (c) General Biquad reduces to 2 OTAs

Figure 4.24 shows a schematic of 2nd order Biquad Filter implementation using Cascode Current Mirror OTA (CCM-OTA@Figure4.21), which is operating at Intermediate Frequency (IF) 10.6MHz for FM band and 70MHz for GSM band. The Input conditions and filter type are given in Table 4.7.



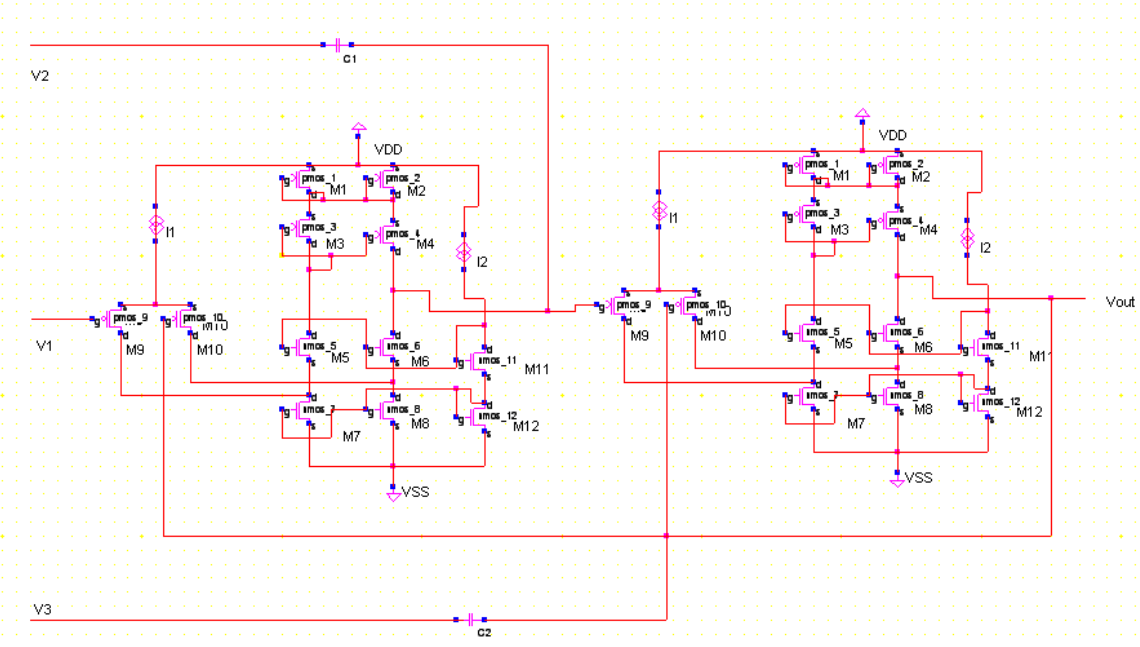


Figure 4.24 Schematic and Circuit of 2nd order Biquad Filter using 2 OTAs

If we assume that the transconductance of each stage are equal, then center frequency and Q of the filter is given as:

$$w_0 = \frac{G_m}{\sqrt{C_1 C_2}}$$

$$Q = \sqrt{\frac{C_2}{C_1}}$$

----------(4.37)

Table 4.7 Design equation for Proposed Biquad filter

Filter Type	Input Conditions	Transfer Functions
Low-pass	$V_{in} = V_1$, **with** V_2 **and** V_3 **grounded**	$\frac{G_m^2}{s^2 C_1 C_2 + s C_1 G_m + G_m^2}$
High-pass	$V_{in} = V_3$, **with** V_1 **and** V_2 **grounded**	$\frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_1 G_m + G_m^2}$
Band-pass	$V_{in} = V_2$, **with** V_1 **and** V_3 **grounded**	$\frac{s C_1 G_m}{s^2 C_1 C_2 + s C_1 G_m + G_m^2}$
Band-stop	$V_{in} = V_1 = V_3$ **with** V_2 **grounded**	$\frac{s^2 C_1 C_2 + G_m^2}{s^2 C_1 C_2 + s C_1 G_m + G_m^2}$

The value of the capacitors C1 and C2 for Intermediate Frequency (IF) 10.6MHz for FM band and 70MHz for GSM band are given in Table 4.8.

Table 4.8 Capacitor Value for GSM and FM IF

Capacitor Value	GSM IF(70MHz)	FM IF(10.6MHz)
C1	**38.34fF**	**0.54pF**
C2	**20.68pF**	**60.1pF**

4.7 Simulation Results of GSM 70MHz IF Biquad Second order CMOS Gm-C Filter

4.7.1 70MHz IF Second order CMOS Gm-C Low Pass Filter Response

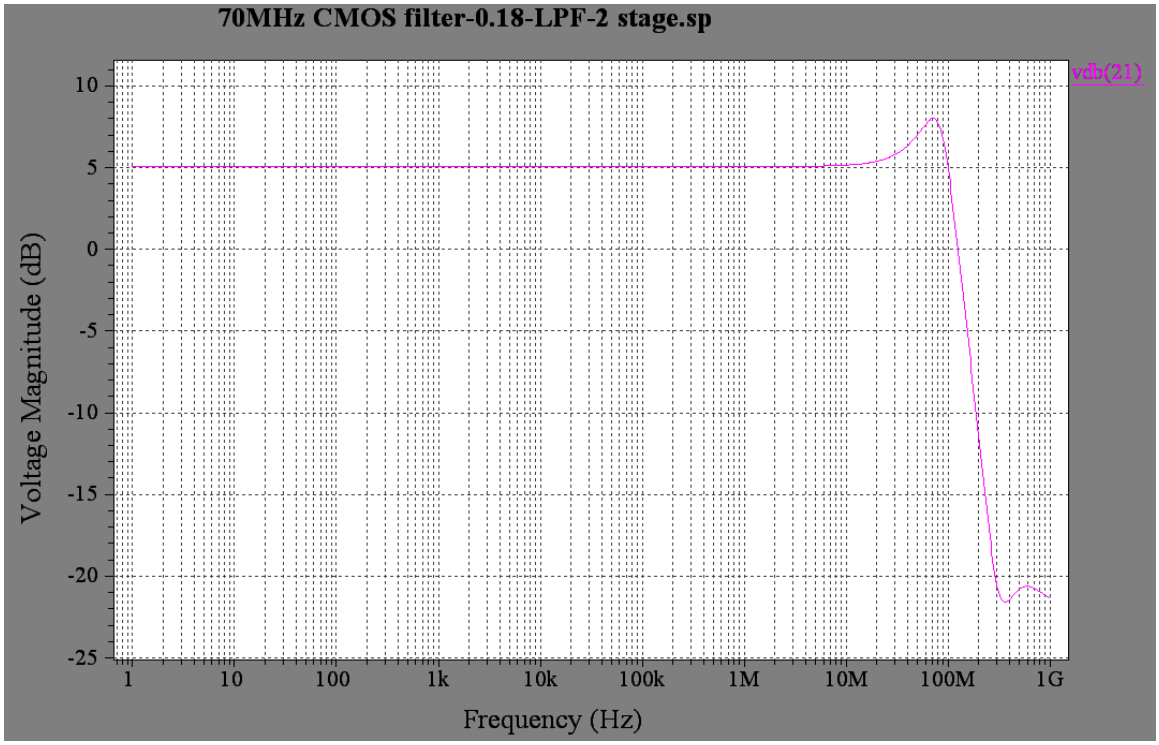


Figure 4.25 70MHz IF Second order CMOS Gm-C Low Pass Filter Response

4.7.2 70MHz IF Second order CMOS Gm-C High Pass Filter Response

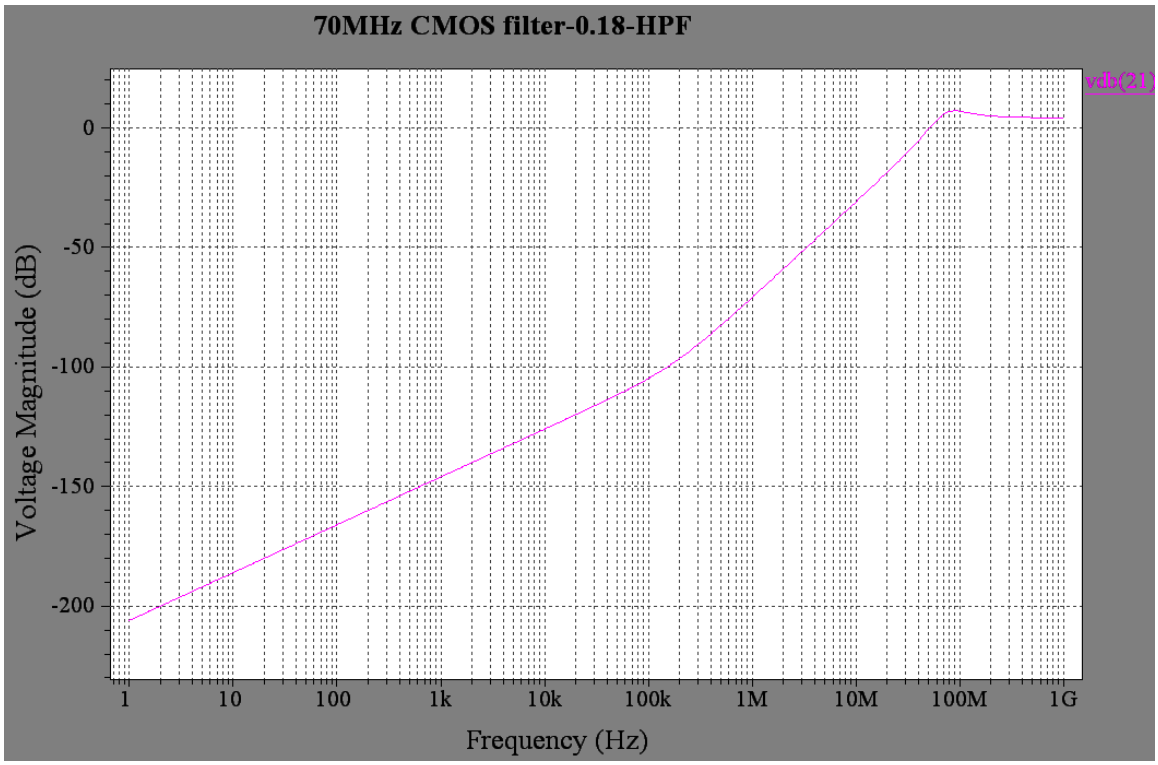


Figure 4.26 70MHz IF Second order CMOS Gm-C High Pass Filter Response

4.7.3 70MHz IF Second order CMOS Gm-C Band Pass Filter Response

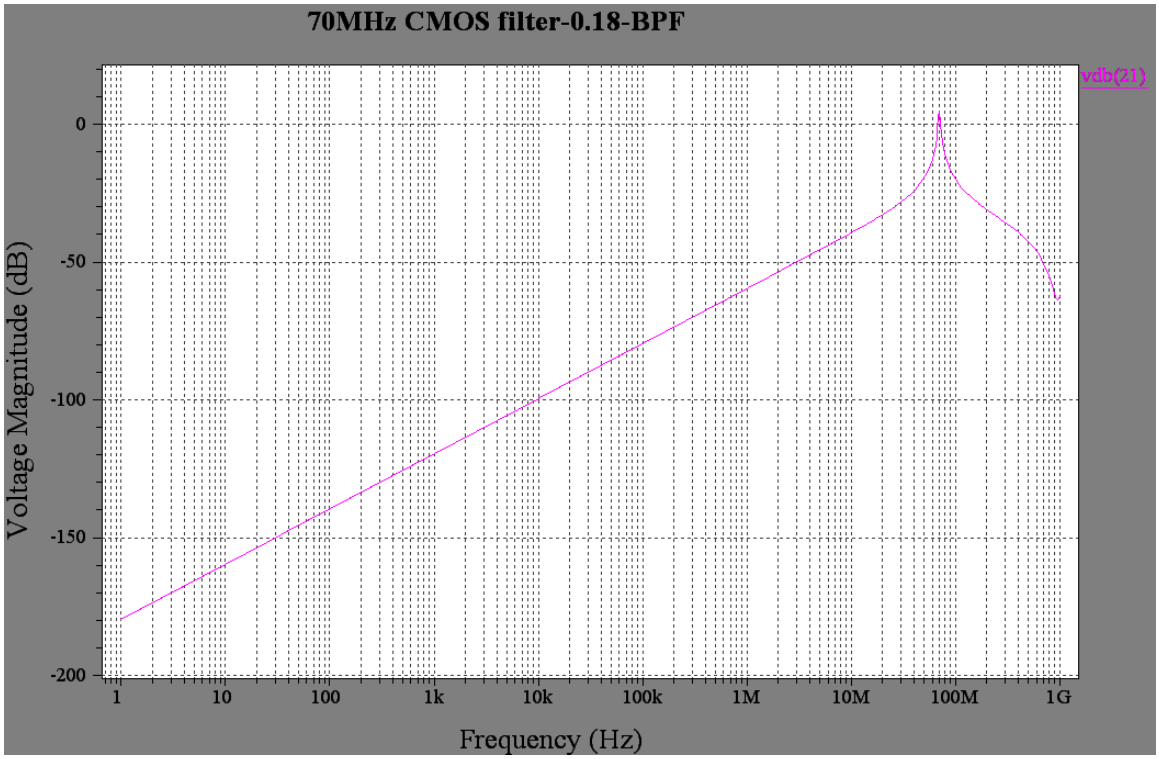


Figure 4.27 70MHz IF Second order CMOS Gm-C Band Pass Filter Response

4.7.4 70MHz IF Second order CMOS Gm-C Band Stop Filter Response

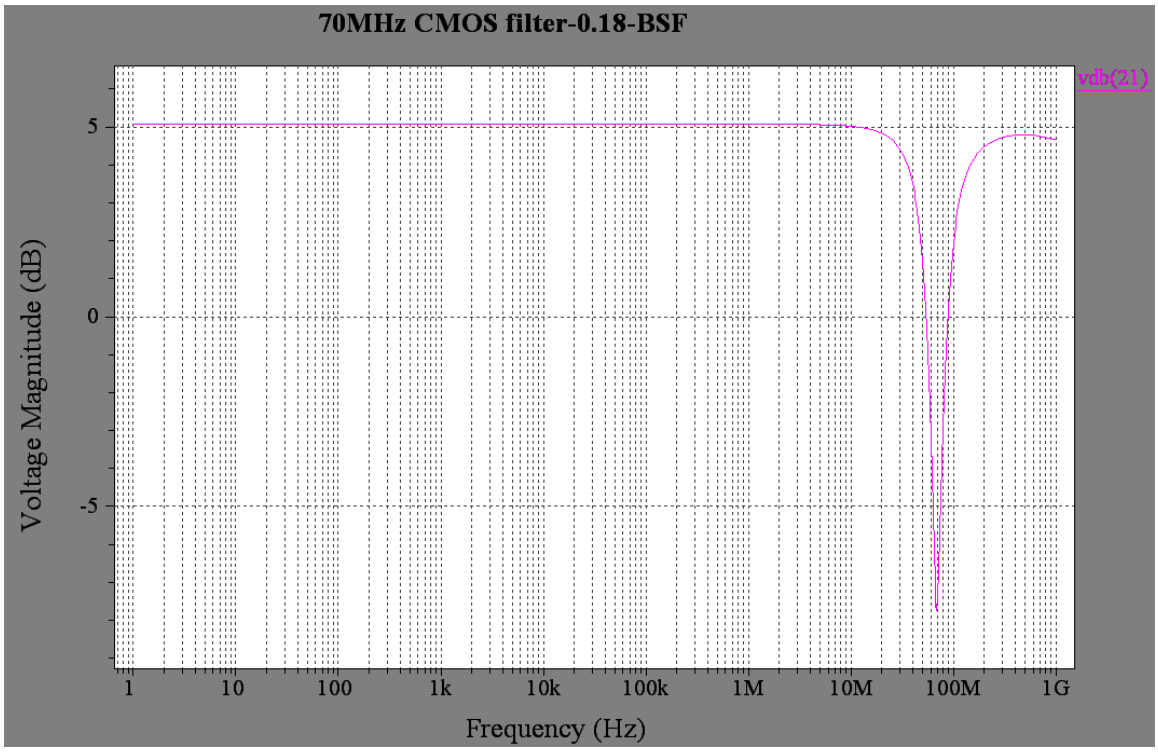


Figure 4.28 70MHz IF Second order CMOS Gm-C Band Stop Filter Response

4.8 Layout of GSM 70MHz IF Biquad Second order CMOS Gm-C Filter

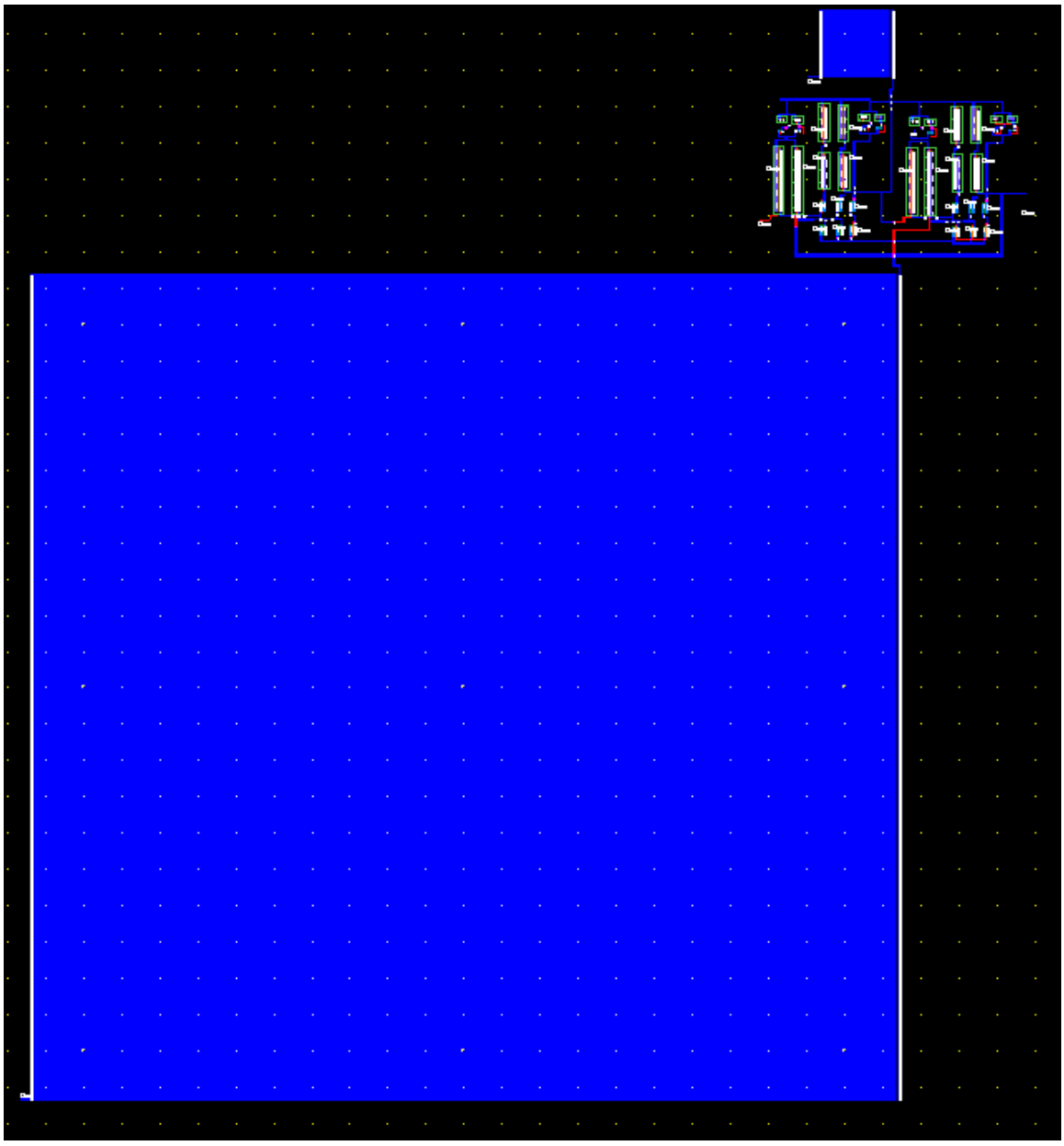


Figure 4.29 Layout of GSM 70MHz IF Biquad Second order CMOS Gm-C Filter

4.9 Post Layout Simulation Results of GSM 70MHz IF Biquad Second order CMOS Gm-C Filter

4.9.1 70MHz IF Second order CMOS Gm-C Low Pass Filter Post Layout Response

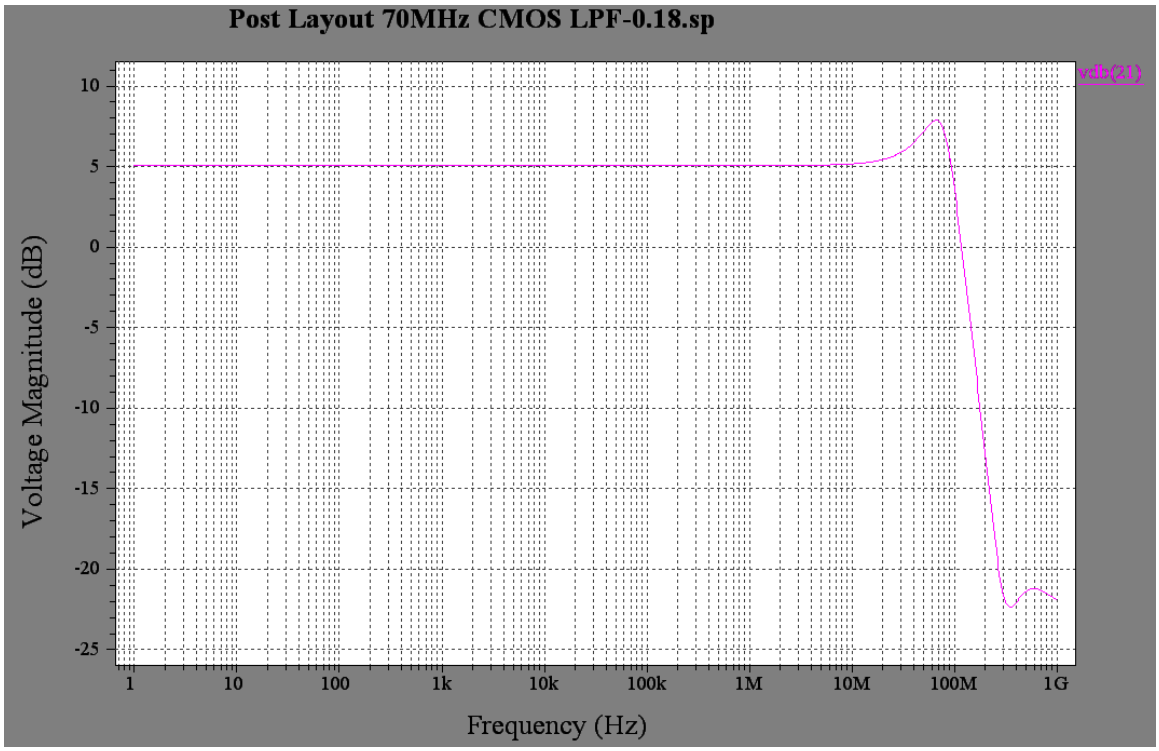


Fig 4.30 70MHz IF Second order CMOS Gm-C Low Pass Filter Post Layout Response

4.9.2 70MHz IF Second order CMOS Gm-C High Pass Filter Post Layout Response

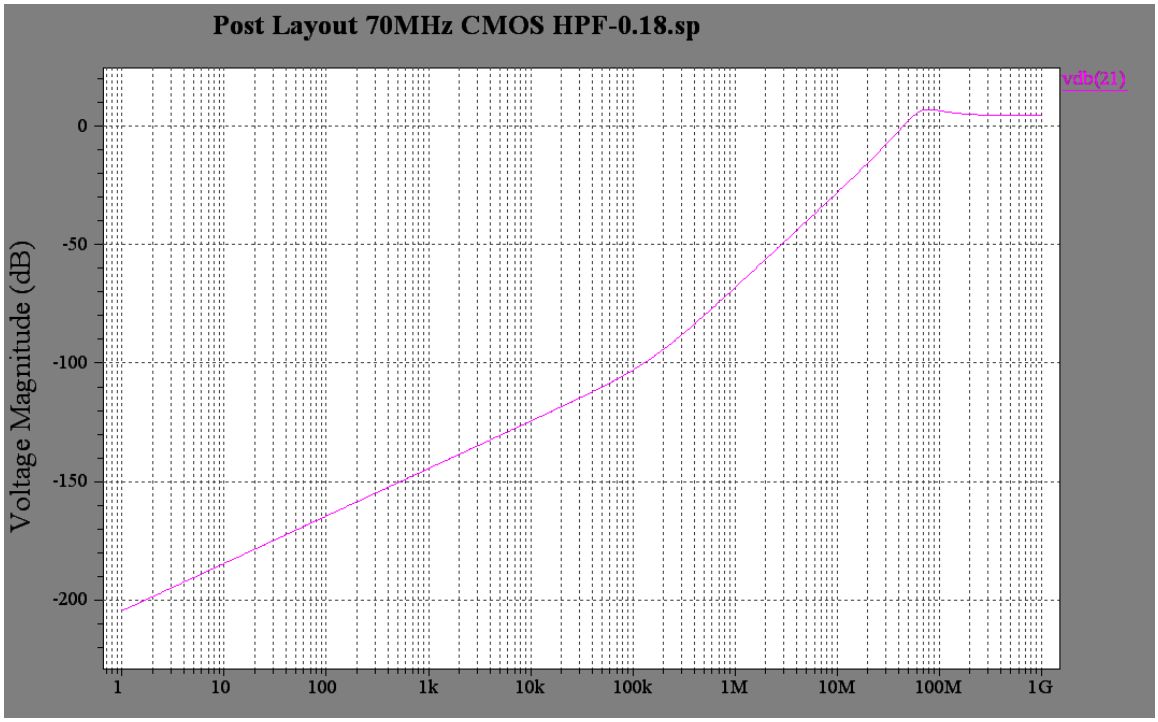


Fig 4.31 70MHz IF Second order CMOS Gm-C High Pass Filter Post Layout Response

4.9.3 70MHz IF Second order CMOS Gm-C Band Pass Filter Post Layout Response

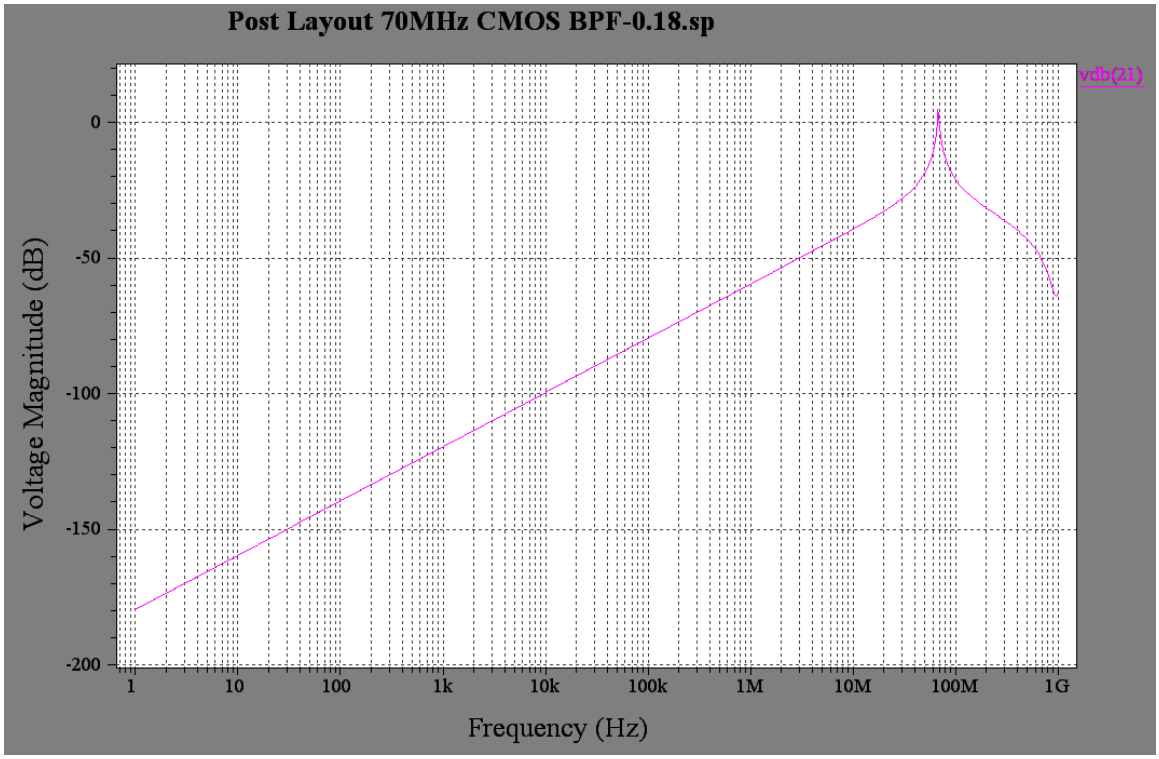


Fig 4.32 70MHz IF Second order CMOS Gm-C Band Pass Filter Post Layout Response

4.9.4 70MHz IF Second order CMOS Gm-C Band Stop Filter Post Layout Response

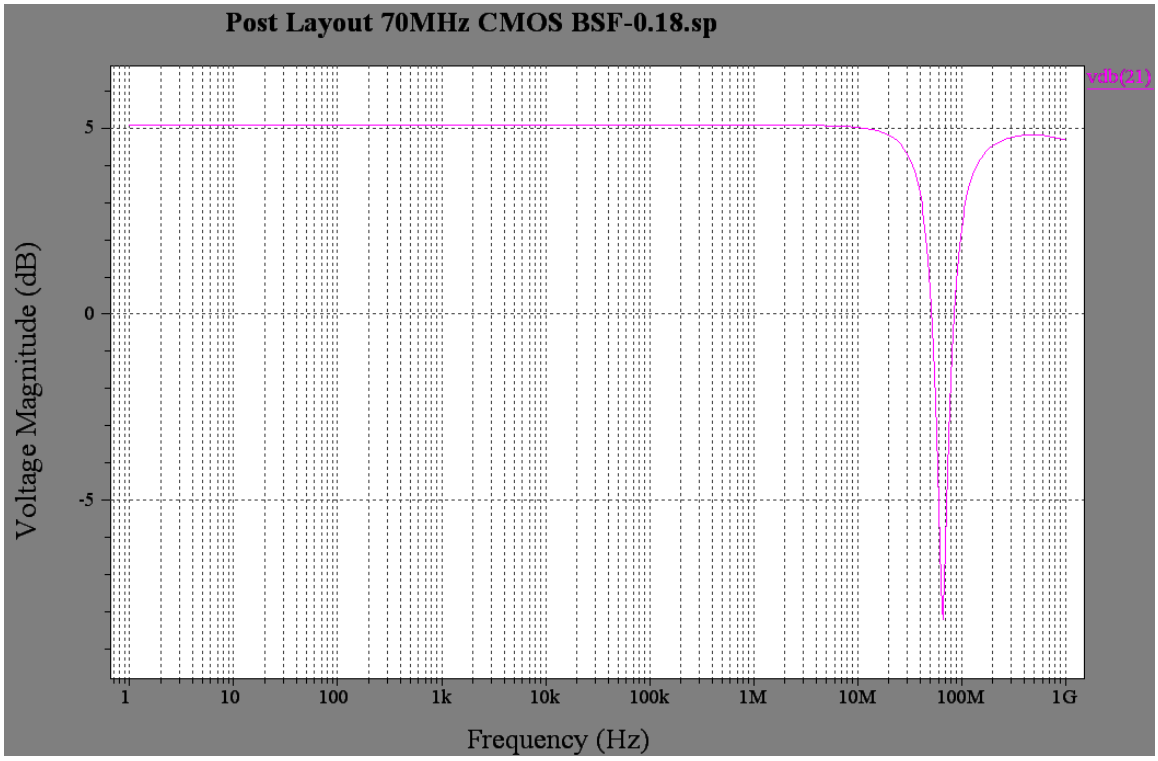


Fig 4.33 70MHz IF Second order CMOS Gm-C Band Stop Filter Post Layout Response

4.10 Pre and Post Layout Simulated Result comparison of 70MHz IF Second order CMOS Gm-C Filter

Table 4.9 Pre and Post Layout Simulated Result comparison For 70MHz IF Second order CMOS Gm-C Filter

Filter Type	Pre-Layout	Post-Layout
Low Pass	70MHz	69.3MHz
High Pass	70MHz	69.1MHz
Band Pass	70MHz	69.2MHz
Band Stop	70MHz	69.4MHz

4.11 Monte Carlo Simulations for 70MHz IF CMOS Gm-C Band Pass Filter with NMOS Threshold Voltage (Absolute Variation)

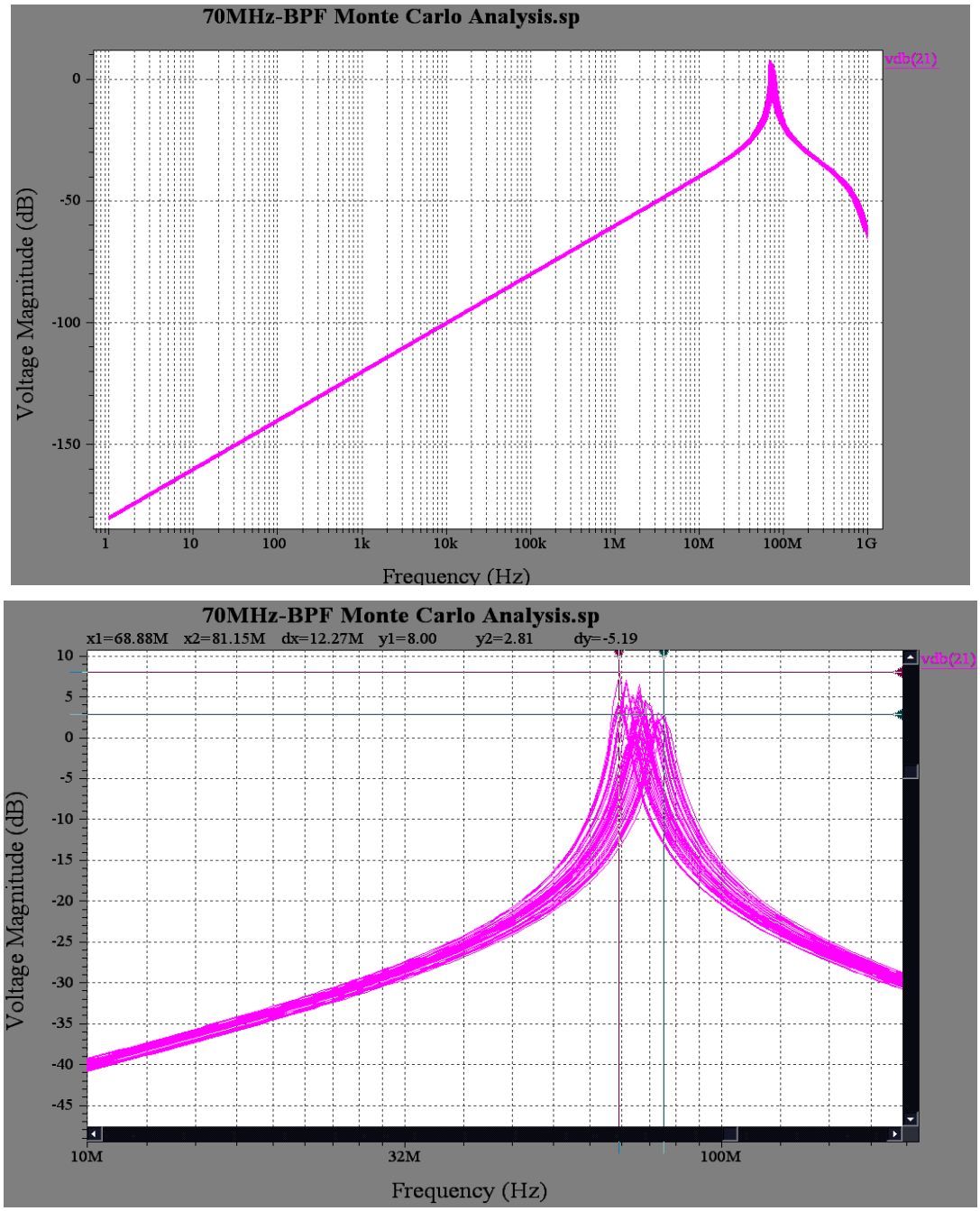


Fig 4.34 Monte Carlo Simulation of 70MHz IF Second order CMOS Gm-C Band Pass Filter with NMOS Threshold Voltage (Absolute Variation)

4.12 Temperature Variations (± 10%) in 70MHz IF CMOS Gm-C Band Pass Filter

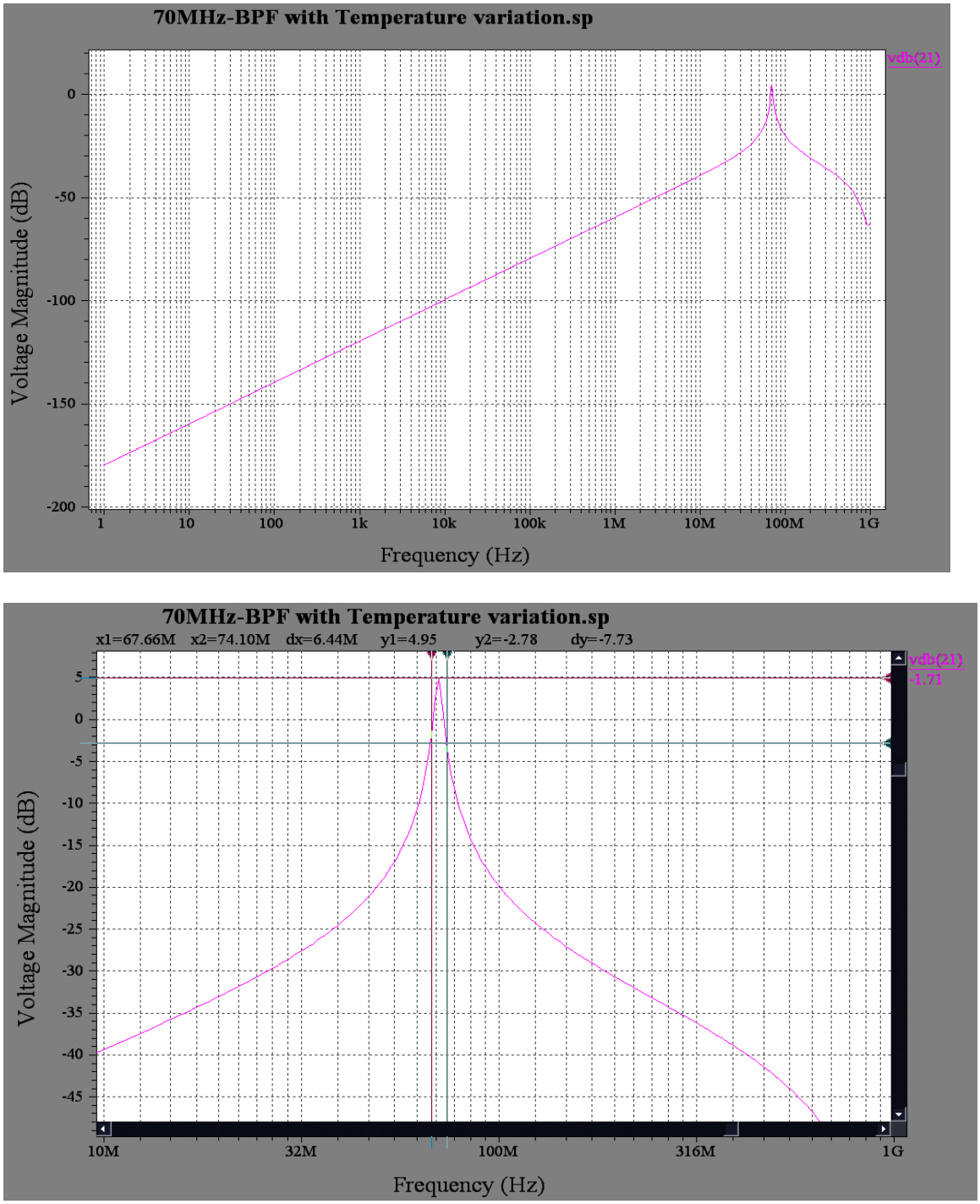


Figure 4.35 70MHz IF Second order CMOS Gm-C Band Pass Filter Response@24.3^{0}C

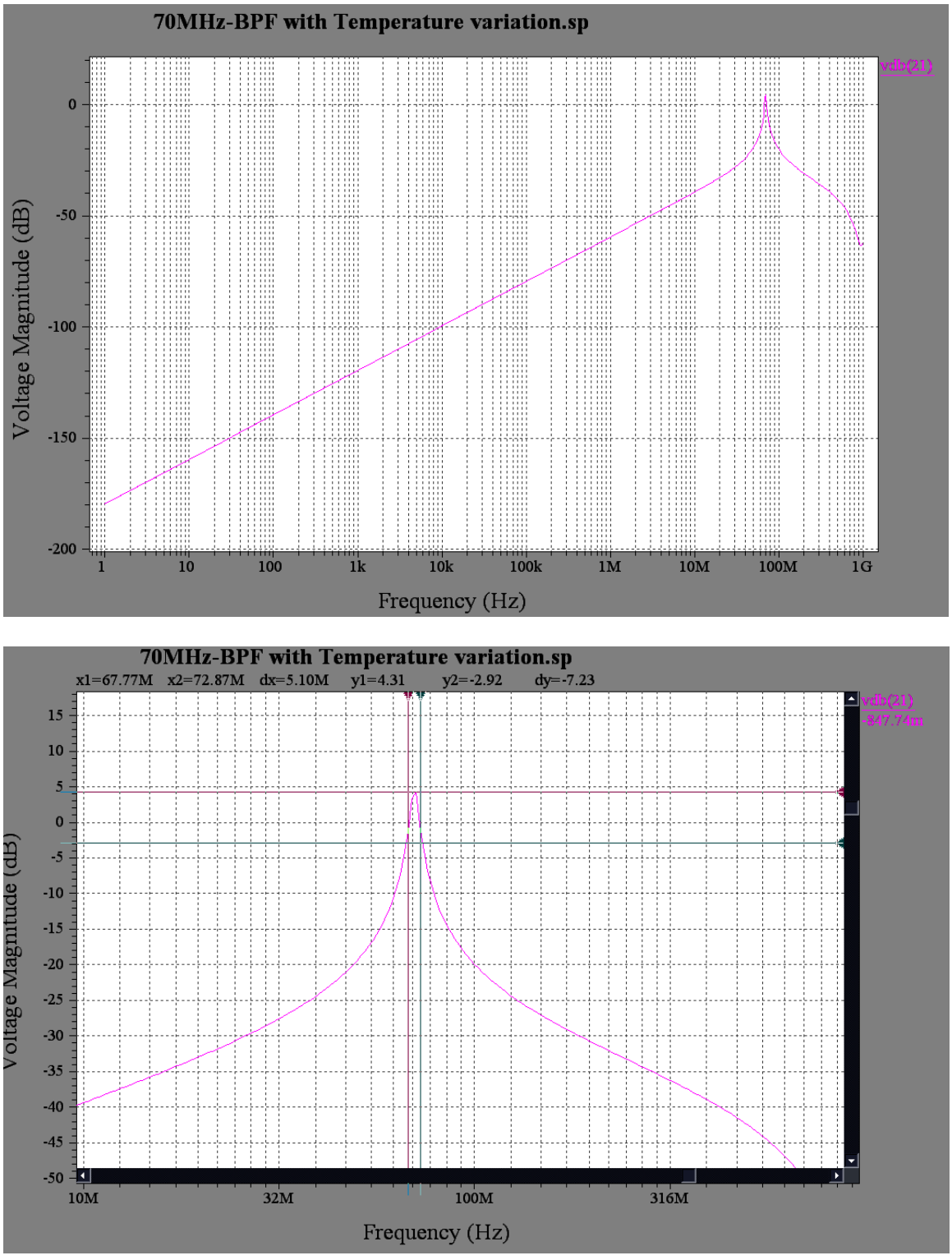


Figure 4.36 70MHz IF Second order CMOS Gm-C Band Pass Filter Response@27^{0}C

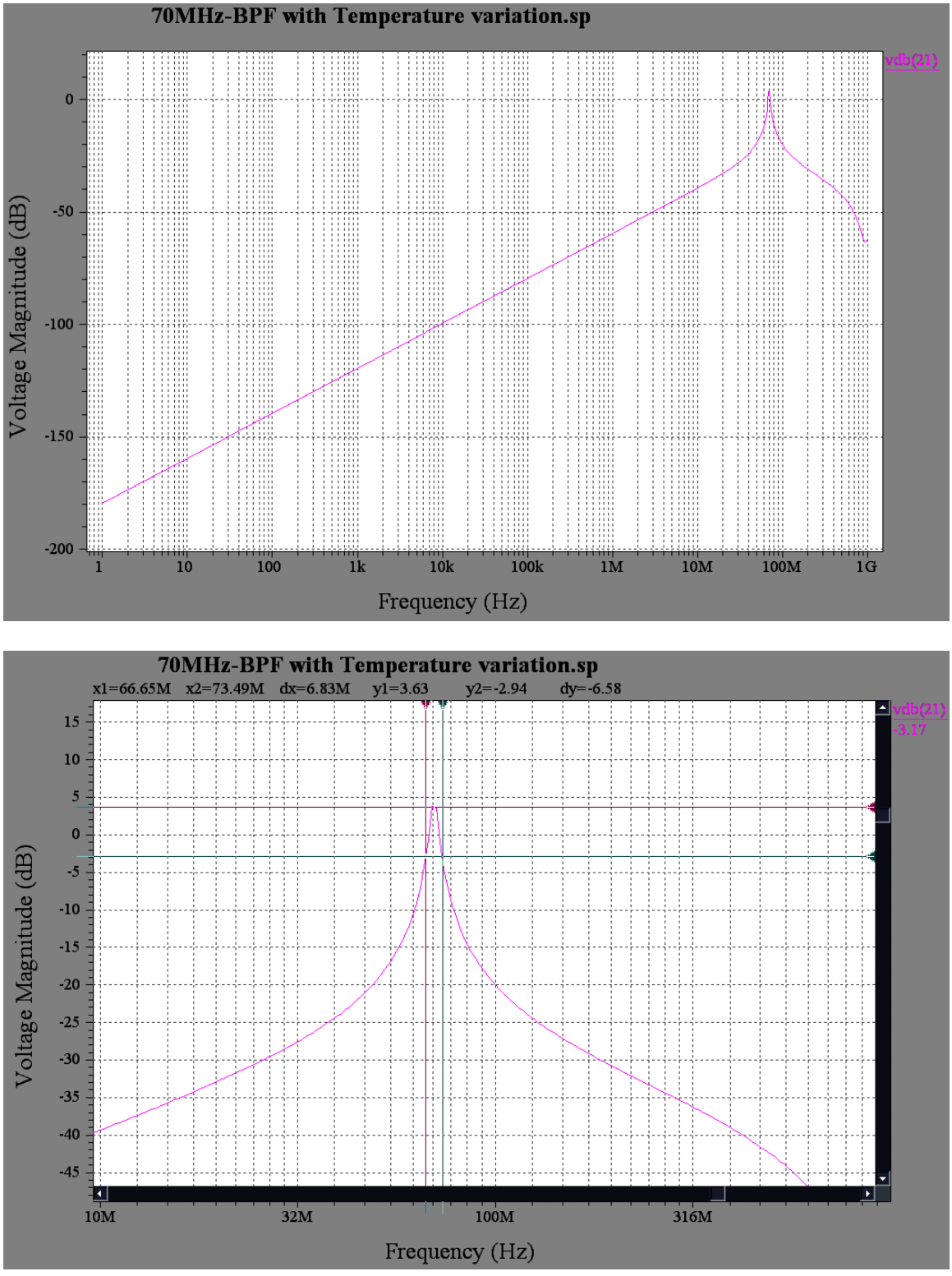


Figure 4.37 70MHz IF Second order CMOS Gm-C Band Pass Filter Response@29^{0}C

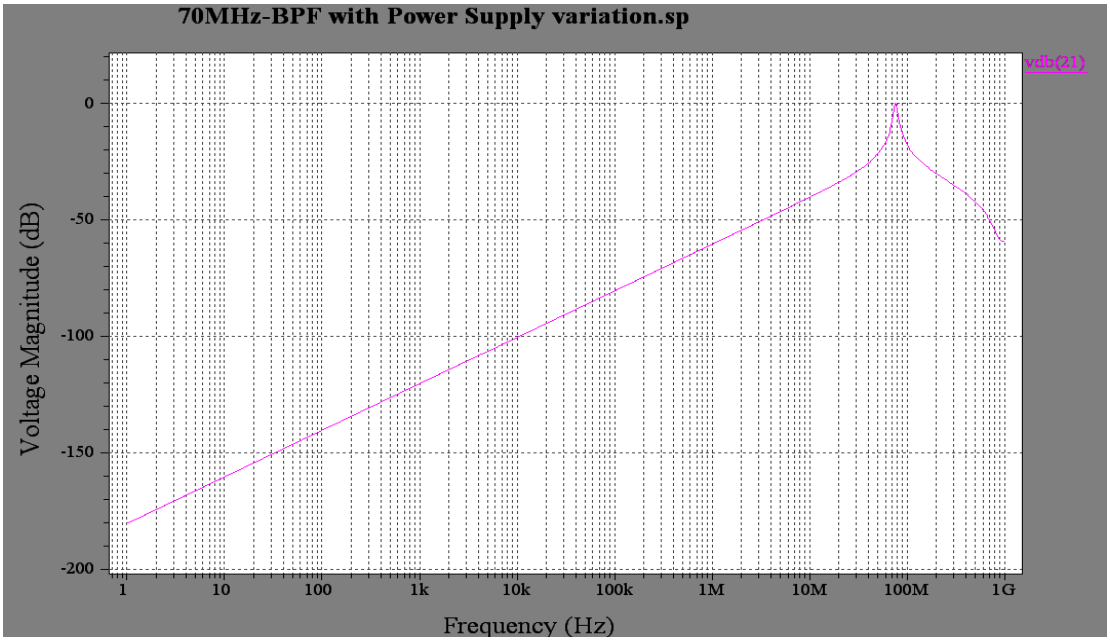
Table: 4.10 Temperature variations on 70MHz IF CMOS Gm-C Band Pass Filter

Parameter	$T = 24.3^0$ C	$T = 27^0$ C	$T = 29.7^0$ C
Center frequency	71.10 MHz	69.99 MHz	70.56 MHz
Gain at Center Frequency	4.95dB	4.31dB	3.63dB
3dB Bandwidth	6.44 MHz	5.10 MHz	6.83 MHz
Quality Factor(Q)	11.04	13.72	10.33

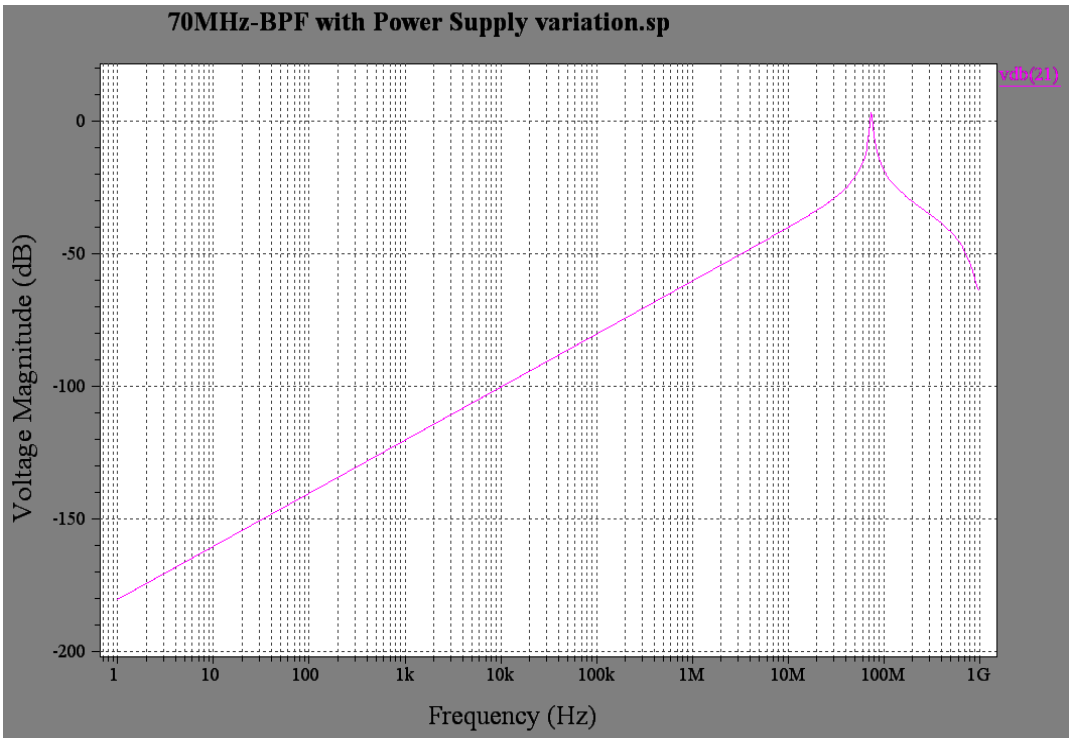
Table: 4.11 Supply Voltage variations on 70MHz IF CMOS Gm-C Band Pass Filter

Parameter	1.62V Supply	1.8V Supply	1.98V Supply
Center frequency	76.54 MHz	69.99 MHz	74.76 MHz
Gain at Center Frequency	3.56dB	4.31dB	3.24dB
3dB Bandwidth	5.62 MHz	5.10 MHz	6.45 MHz
Quality Factor(Q)	13.61	13.72	11.59

4.13 Supply Voltage Variations (±10%) in 70MHz IF CMOS Gm-C Band Pass Filter



(a)



(b)

Figure 4.38 70MHz IF Second order CMOS Gm-C Band Pass Filter Response at (a) 1.62V Supply and (b) 1.98V Supply

4.14 Simulation Results of FM 10.6 MHz IF Biquad Second order CMOS Gm-C Filter

4.14.1 10.6MHz IF Second order CMOS Gm-C Low Pass Filter Response

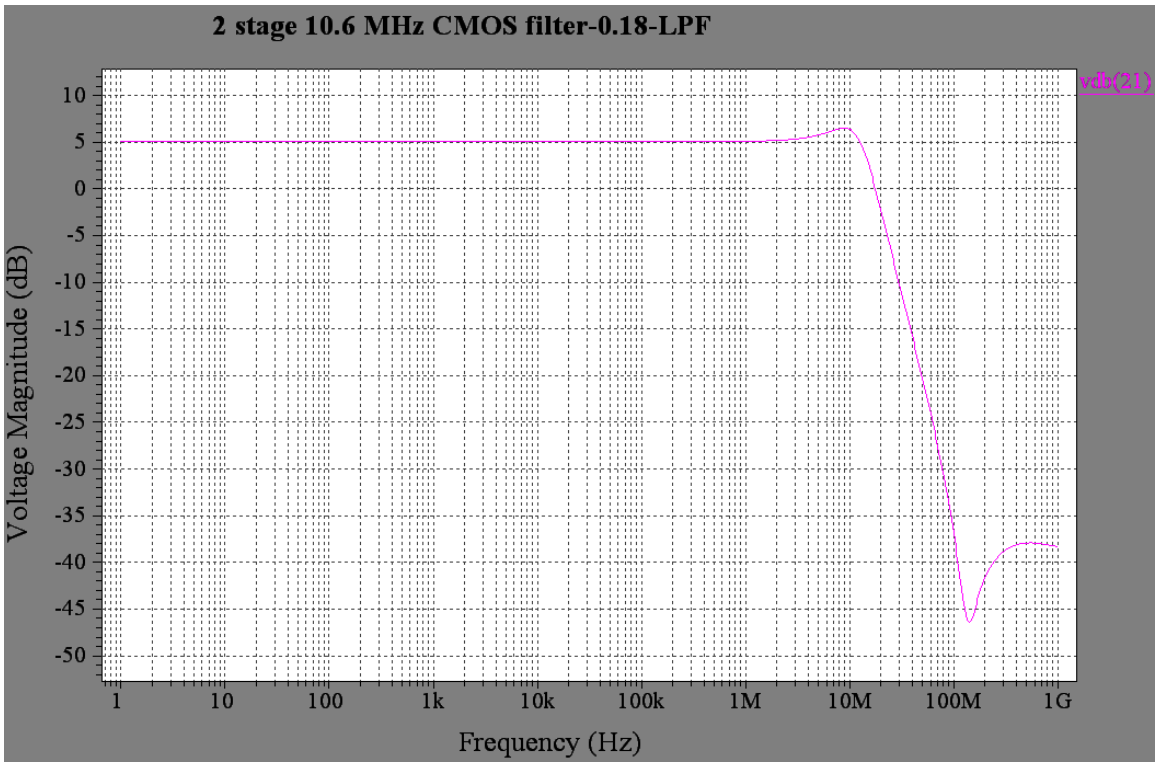


Figure 4.39 10.6MHz IF Second order CMOS Gm-C Low Pass Filter Response

4.14.2 10.6MHz IF Second order CMOS Gm-C High Pass Filter Response

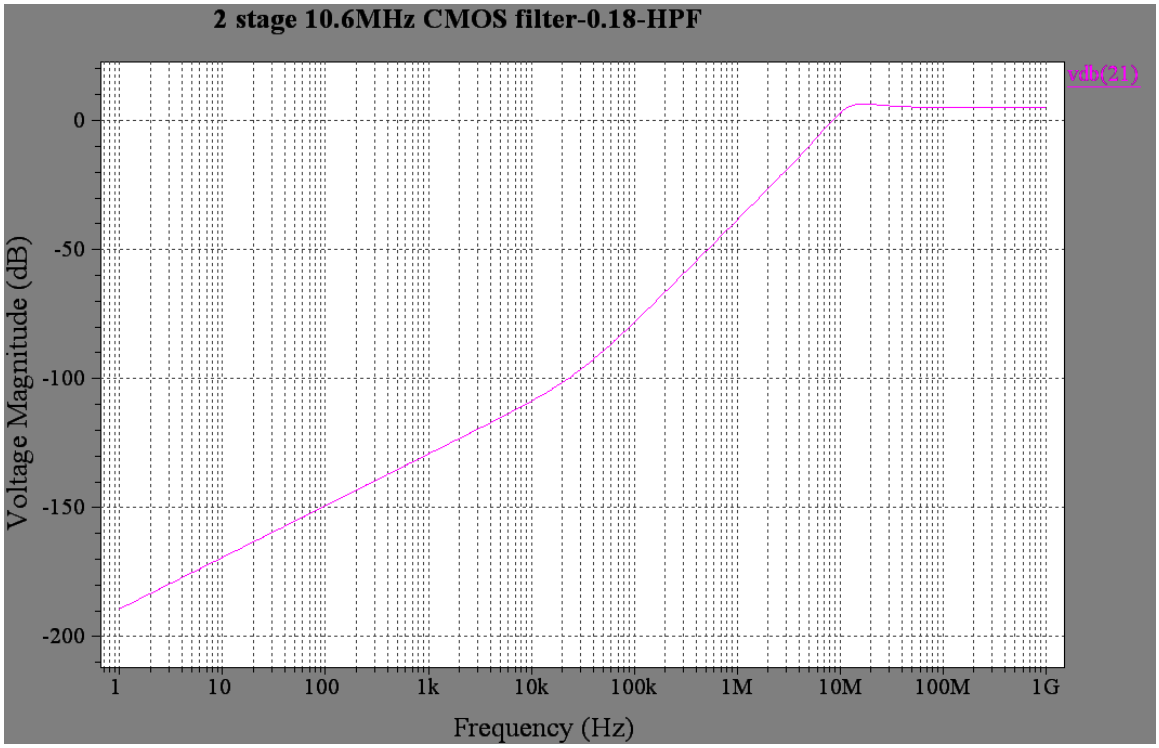


Figure 4.40 10.6MHz IF Second order CMOS Gm-C High Pass Filter Response

4.14.3 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response

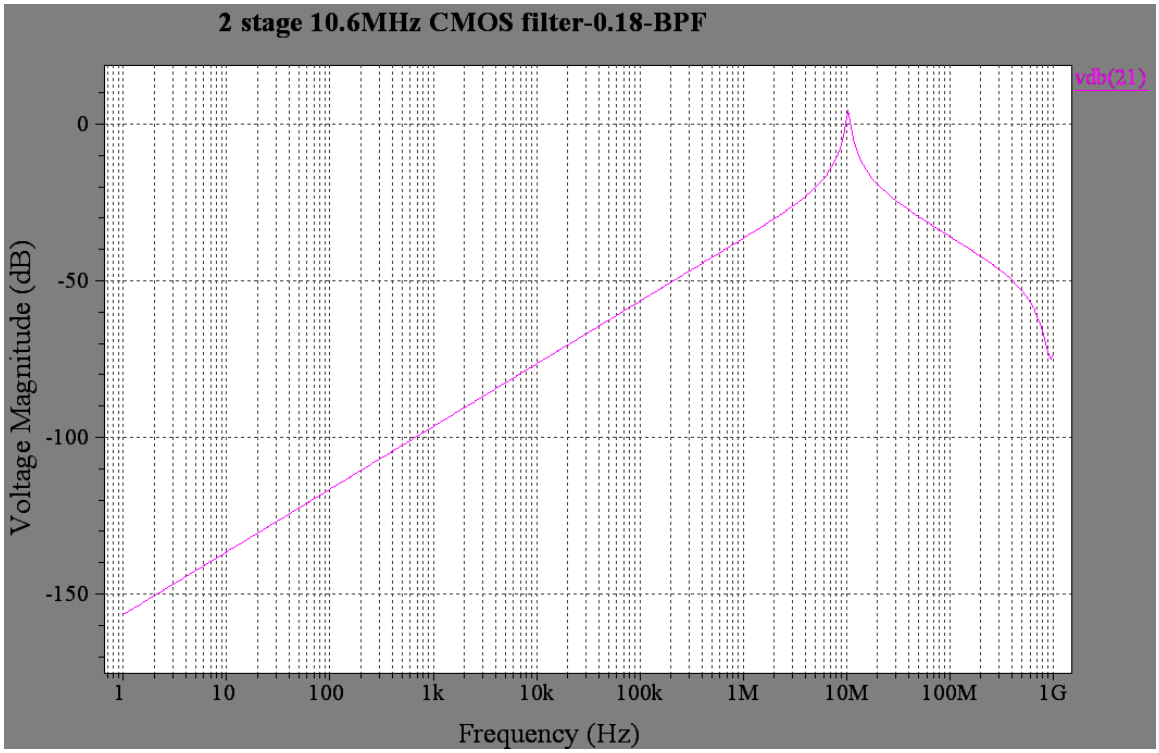


Figure 4.41 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response

4.14.4 10.6MHz IF Second order CMOS Gm-C Band Stop Filter Response

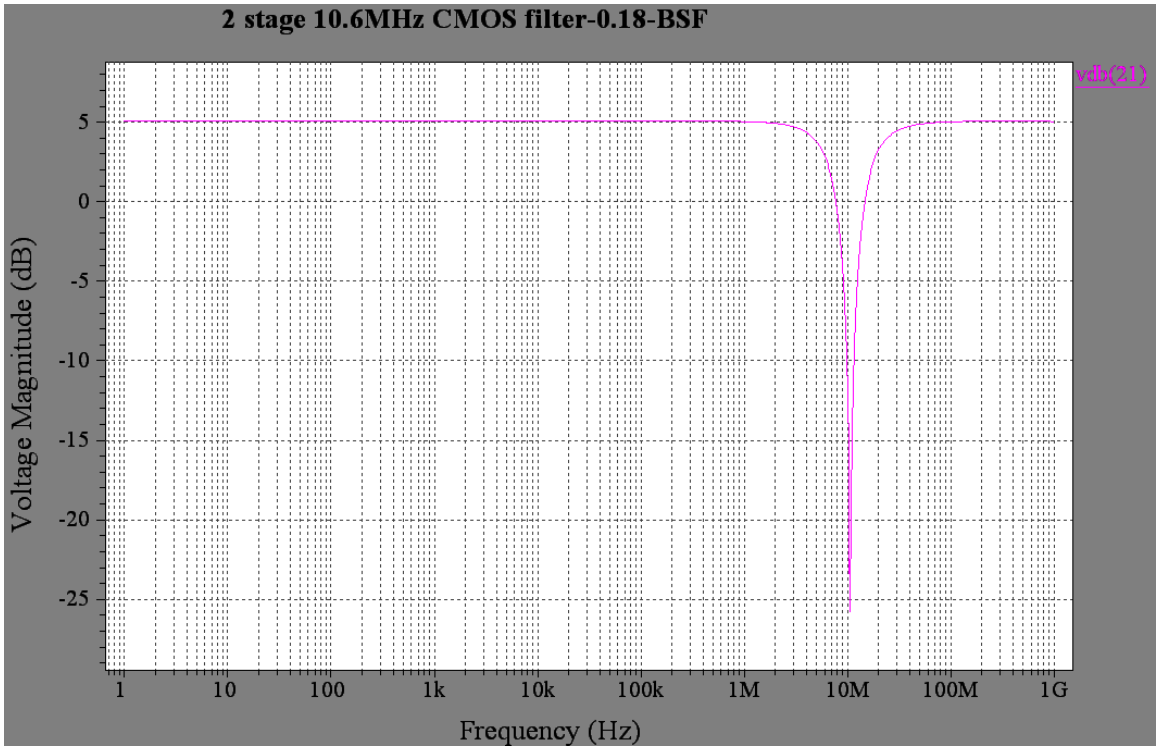


Figure 4.42 10.6MHz IF Second order CMOS Gm-C Band Stop Filter Response

4.15 Layout of FM 10.6MHz IF Biquad Second order CMOS Gm-C Filter

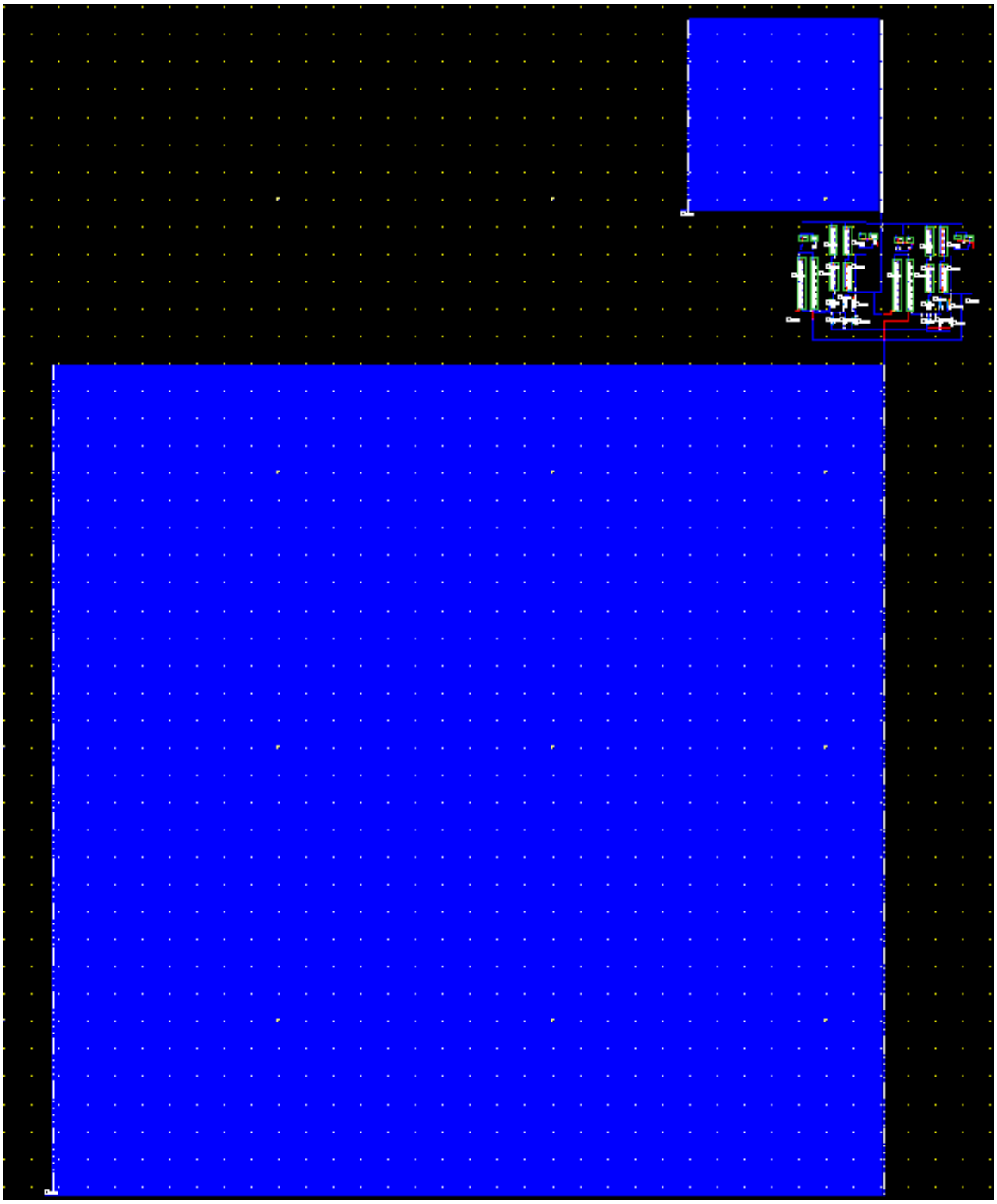


Figure 4.43 Layout of FM 10.6MHz IF Biquad Second order CMOS Gm-C Filter

4.16 Post Layout Simulation Results of FM 10.6MHz IF Biquad Second order CMOS Gm-C Filter

4.16.1 10.6MHz IF Second order CMOS Gm-C Low Pass Filter Post Layout Response

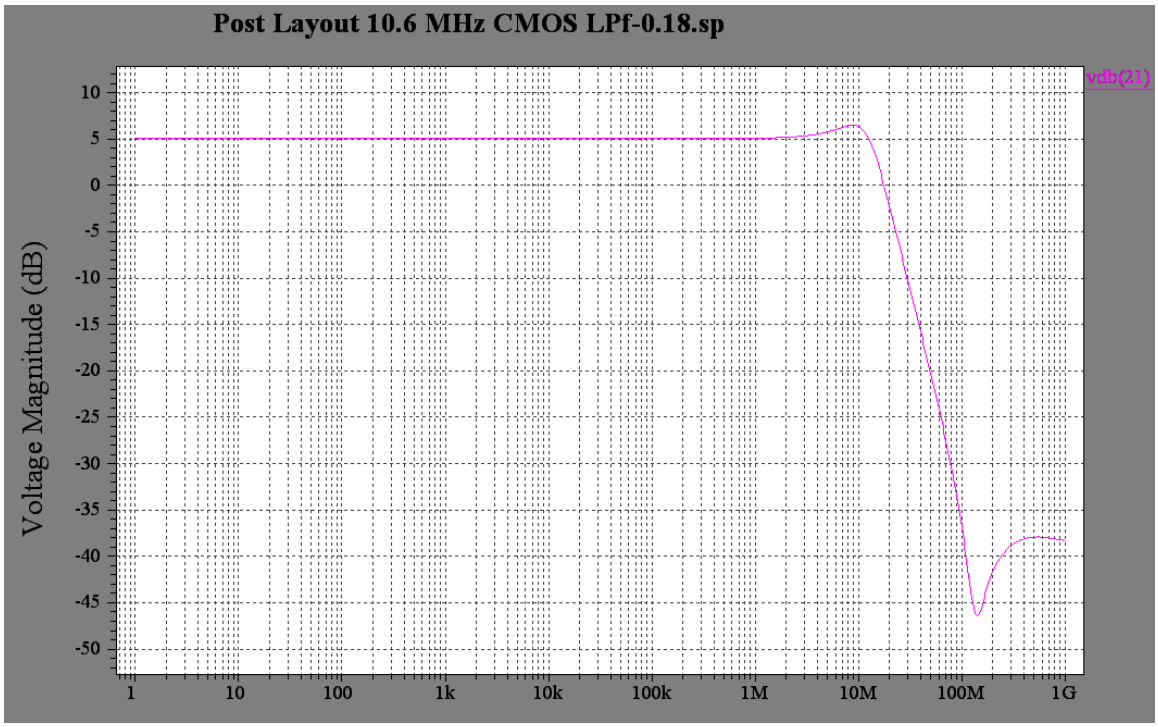


Fig 4.44 10.6MHz IF Second order CMOS Gm-C Low Pass Filter Post Layout Response

4.16.2 10.6MHz IF Second order CMOS Gm-C High Pass Filter Post Layout Response

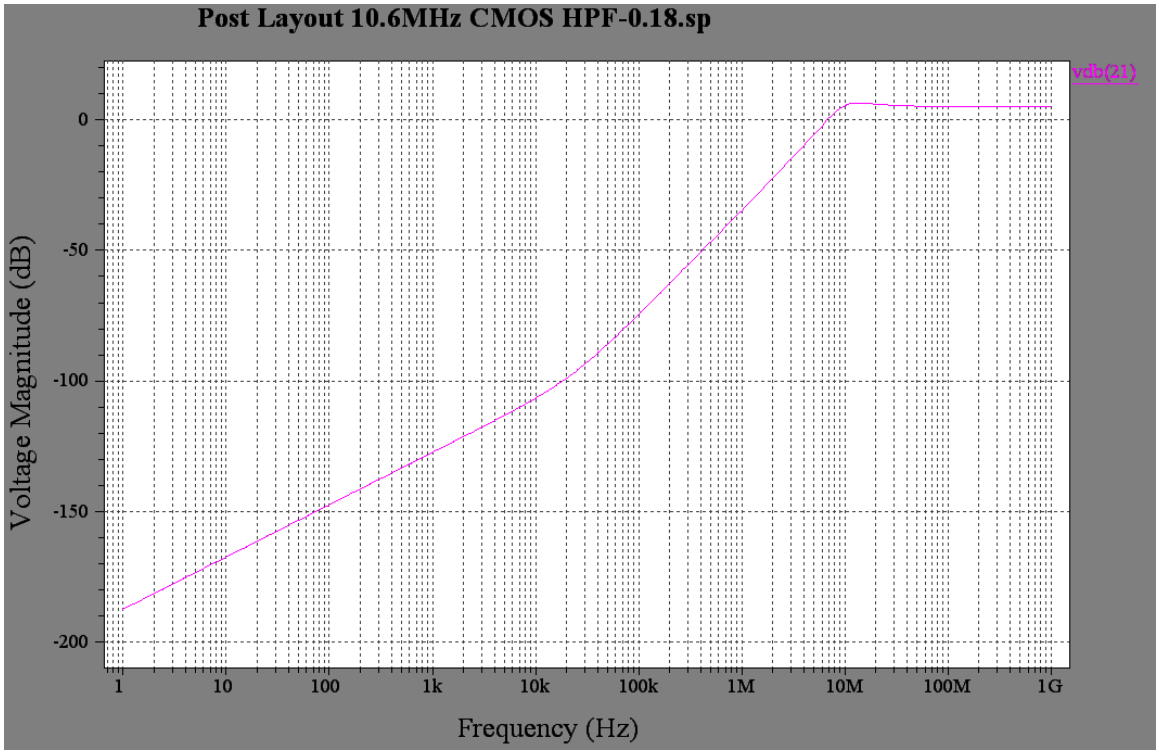


Fig 4.45 10.6MHz IF Second order CMOS Gm-C High Pass Filter Post Layout Response

4.16.3 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Post Layout Response

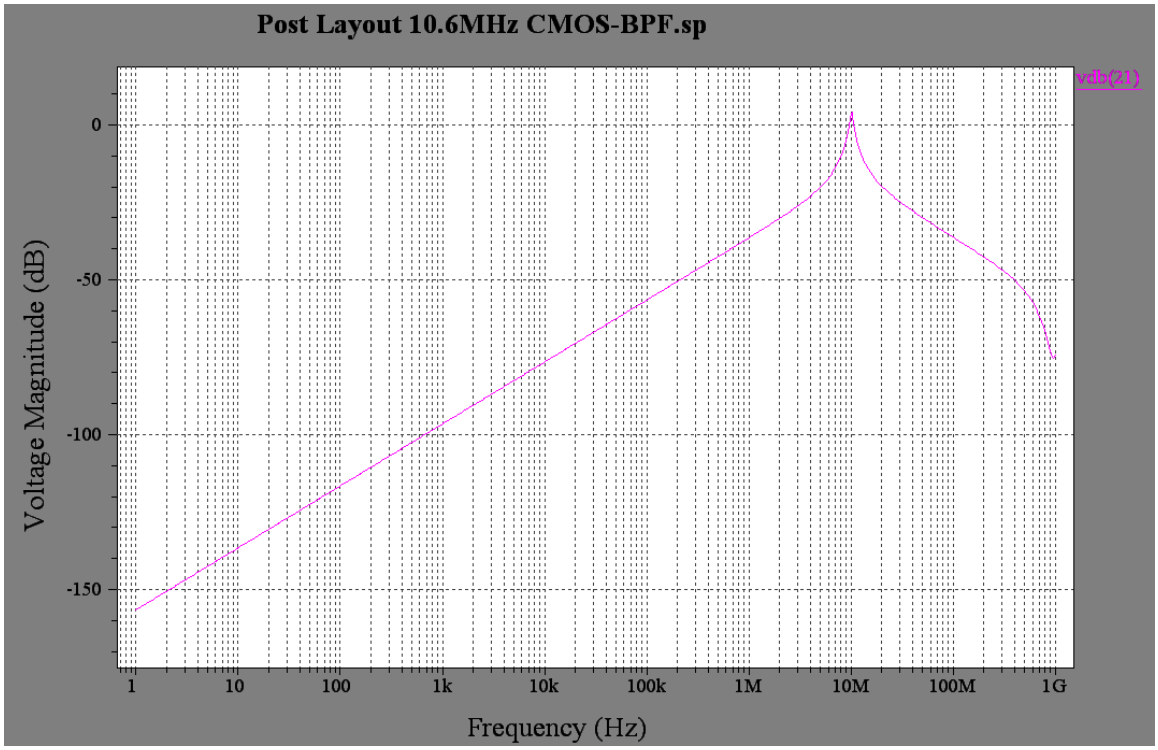


Fig 4.46 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Post Layout Response

4.16.4 10.6MHz IF Second order CMOS Gm-C Band Stop Filter Post Layout Response

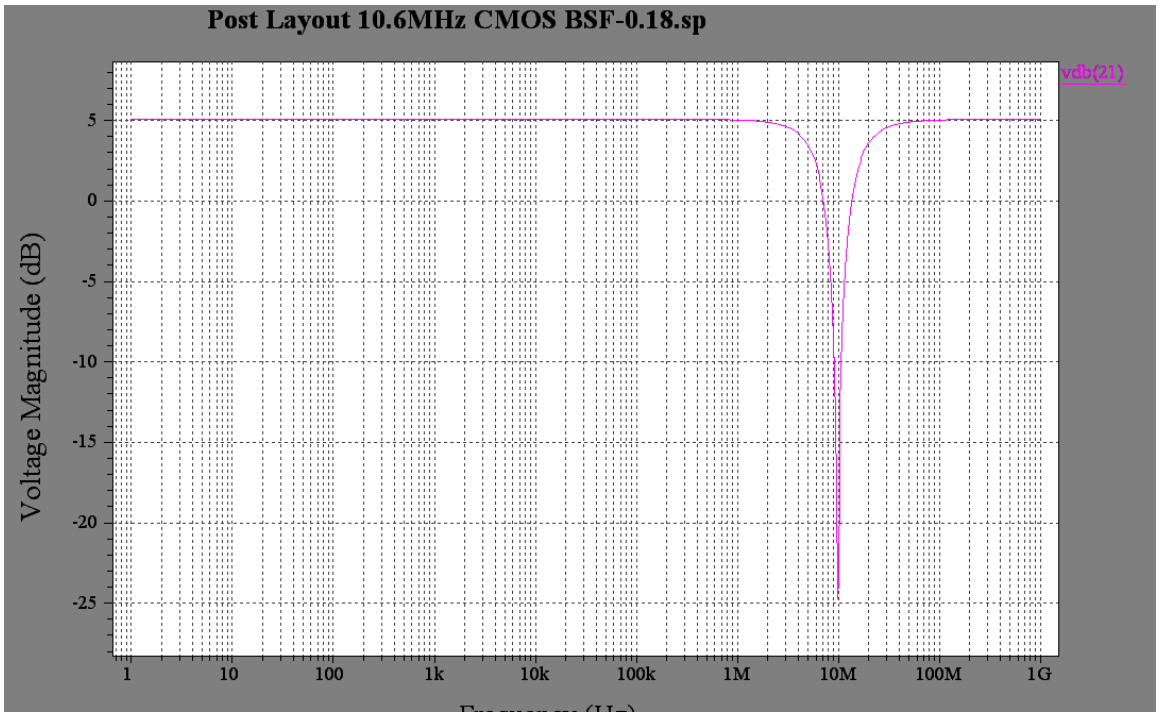


Fig 4.47 10.6MHz IF Second order CMOS Gm-C Band Stop Filter Post Layout Response

4.17 Pre and Post Layout Simulated Result comparison of 10.6MHz IF Second order CMOS Gm-C Filter

Table 4.12 Pre and Post Layout Simulated Result comparison 10.6MHz IF Second order CMOS Gm-C Filter

Filter Type	Pre-Layout	Post-Layout
Low Pass	10.6MHz	10.1MHz
High Pass	10.6MHz	9.9MHz
Band Pass	10.6MHz	10.2MHz
Band Stop	10.6MHz	10.0MHz

4.18 Monte Carlo Simulations for 10.6MHz IF CMOS Gm-C Band Pass Filter with NMOS Threshold Voltage (Absolute Variation)

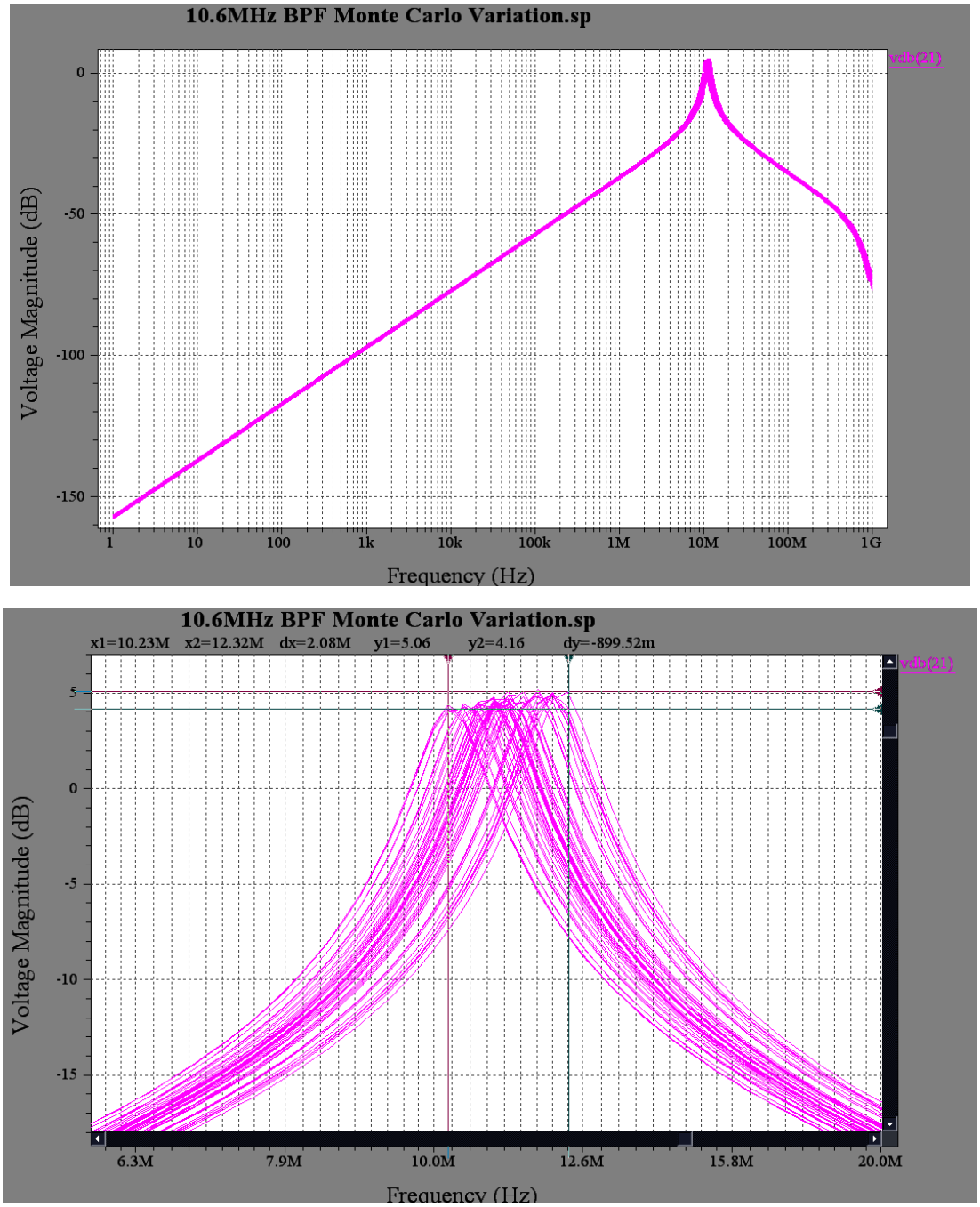


Fig 4.48 Monte Carlo Simulation of 10.6MHz IF Second order CMOS Gm-C Band Pass Filter with NMOS Threshold Voltage (Absolute Variation)

4.19 Temperature Variations (±10%) in 10.6MHz IF CMOS Gm-C Band Pass Filter

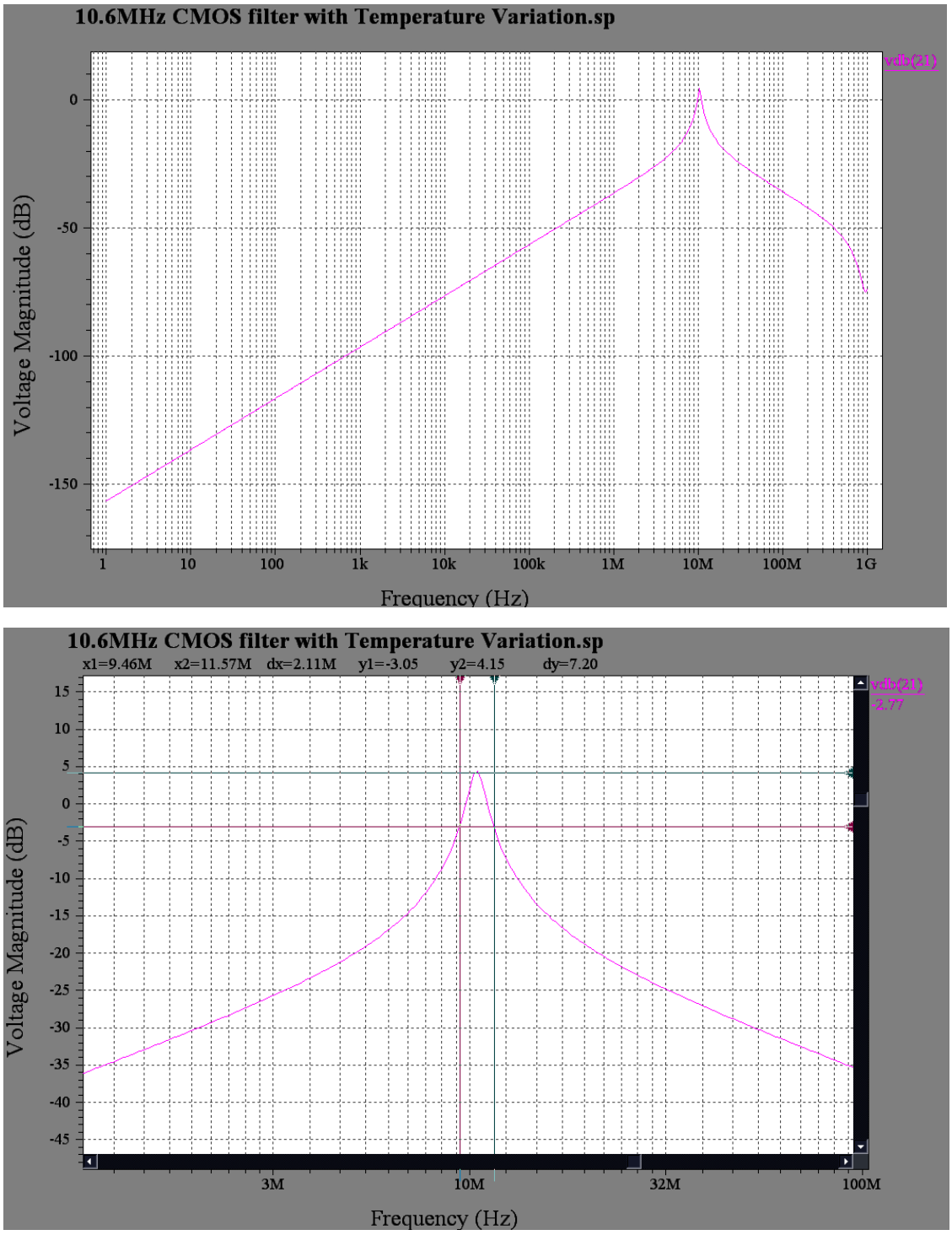
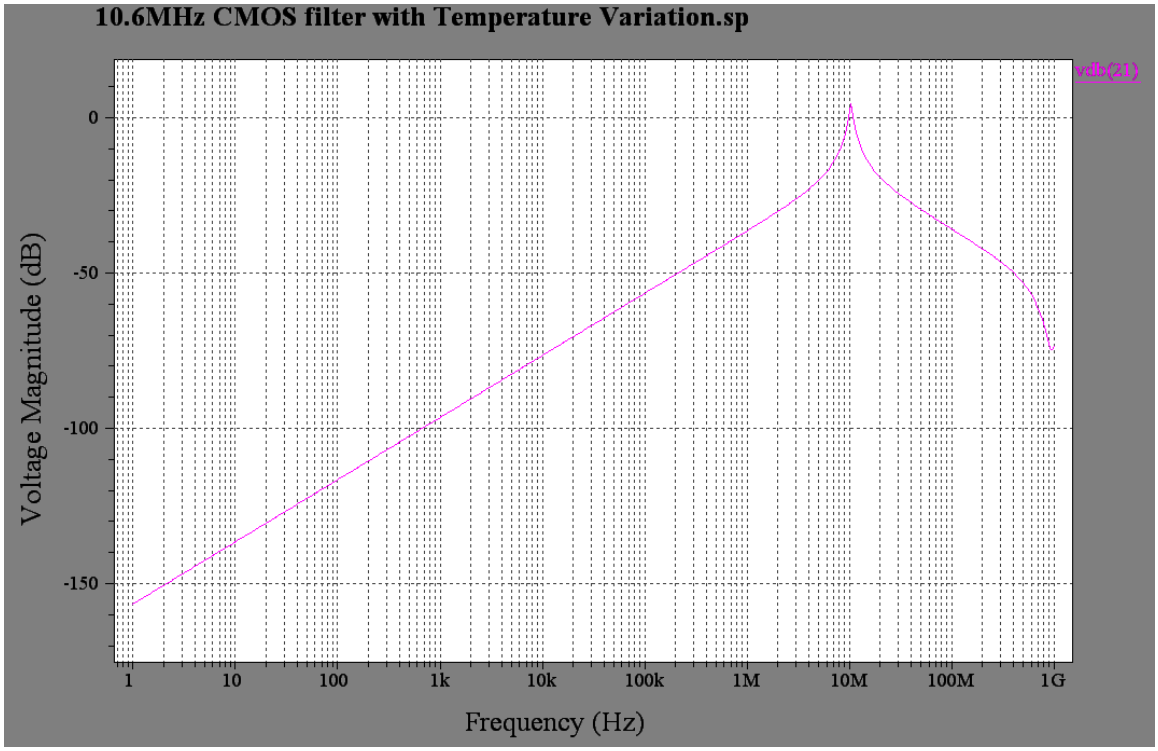


Figure 4.49 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response@24.3^{0}C



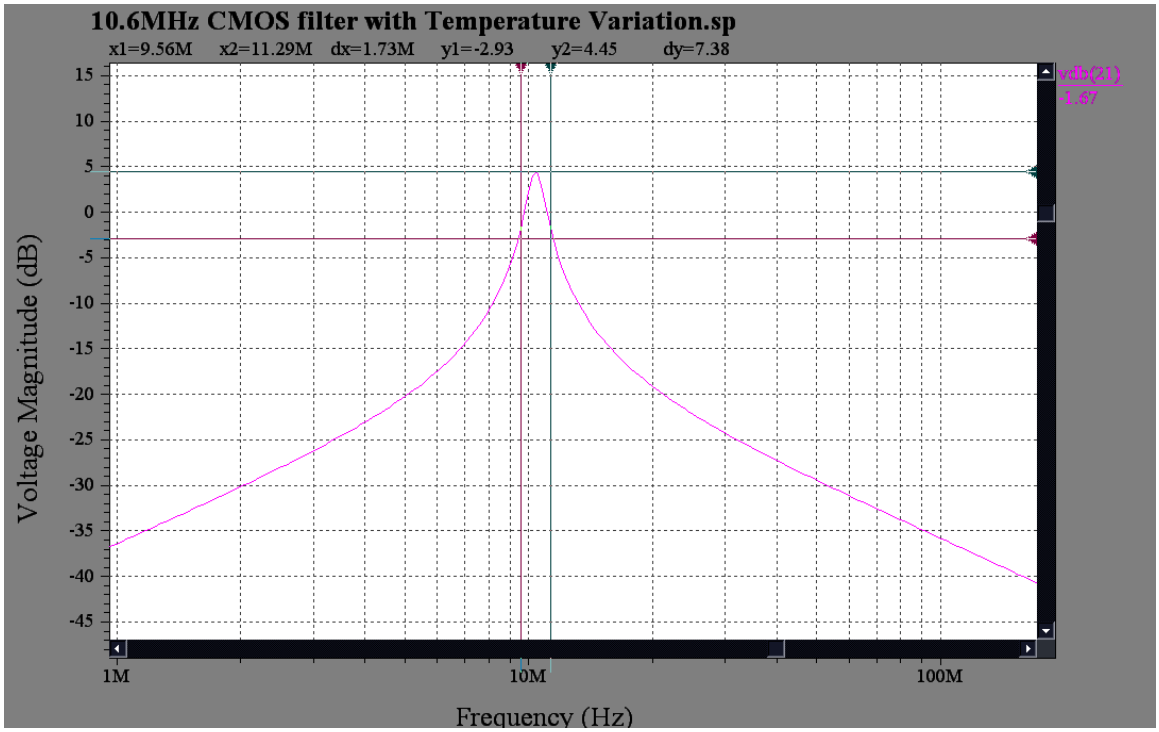


Figure 4.50 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response@27^{0}C

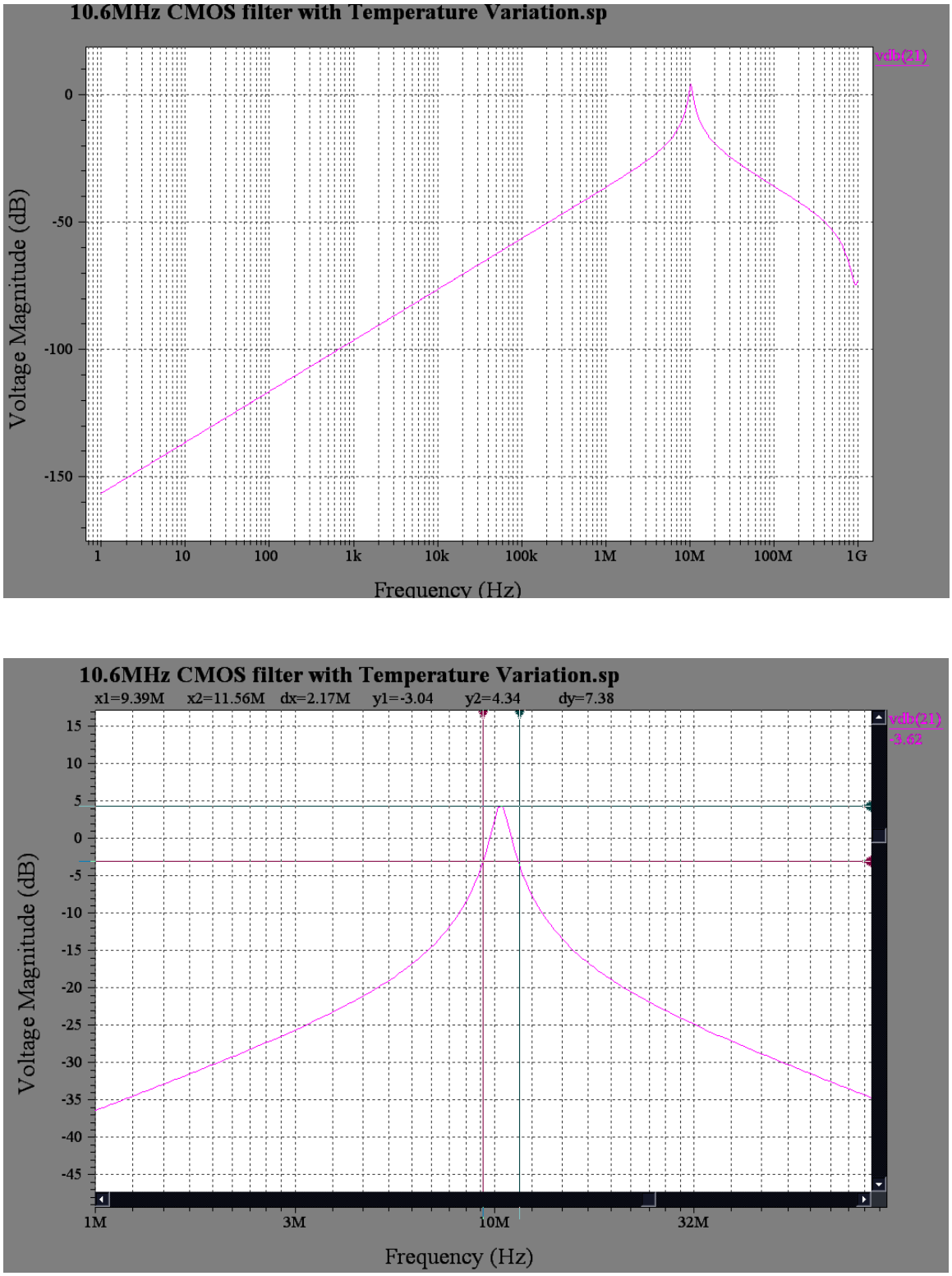


Figure 4.51 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response@29.7^{0}C

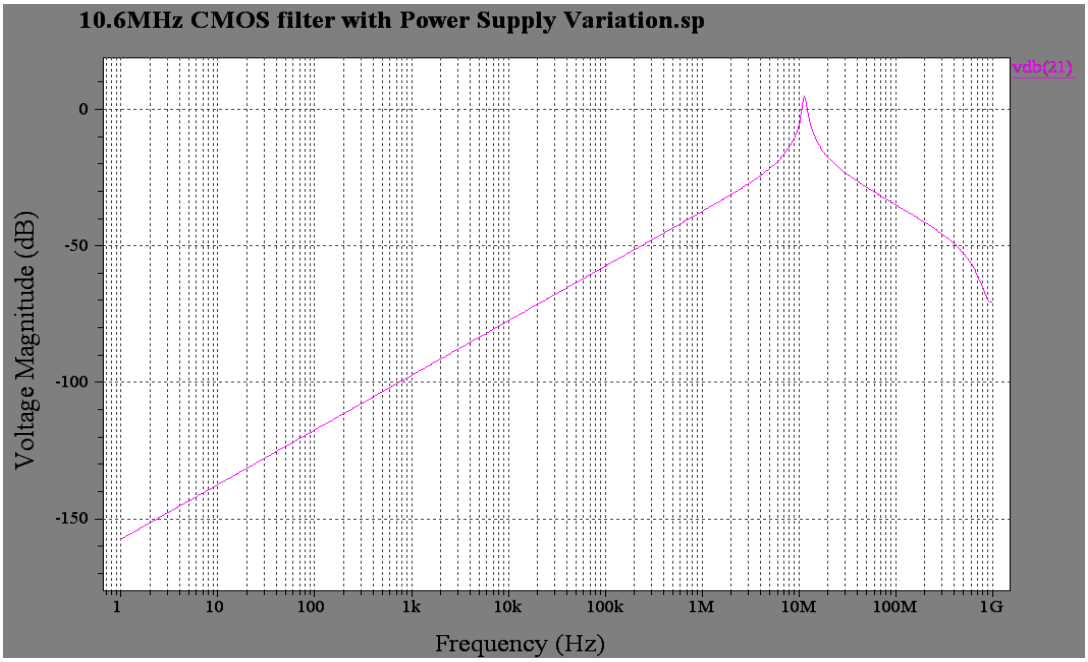
Table: 4.13 Temperature variations on 10.6MHz IF CMOS Gm-C Band Pass Filter

Parameter	$T=24.3^0$ C	$T=27^0$ C	$T=29.7^0$ C
Center frequency	10.34MHz	10.6MHz	10.42MHz
Gain at Center Frequency	4.15	4.45	4.34
3dB Bandwidth	2.11	1.73	2.17
Quality Factor(Q)	4.90	6.12	4.80

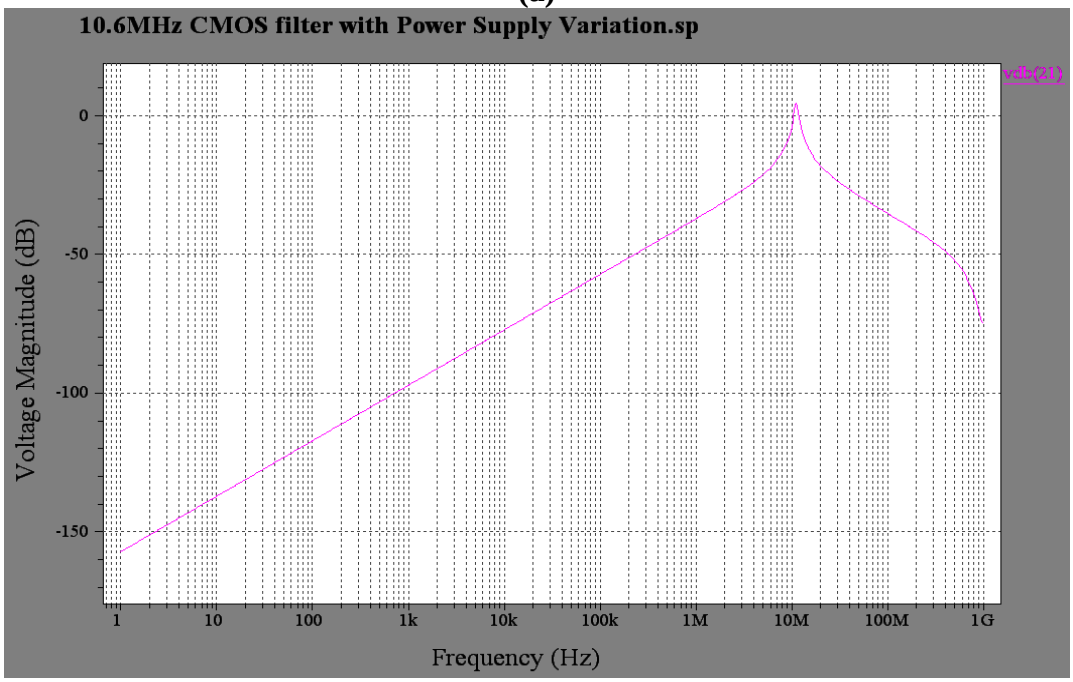
Table: 4.14 Supply Voltage variations on 10.6MHz IF CMOS Gm-C Band Pass Filter

Parameter	1.62V Supply	1.8V Supply	1.98V Supply
Center frequency	11.60	10.6MHz	11.31
Gain at Center Frequency	4.81	4.45dB	4.68
3dB Bandwidth	2.35	1.73MHz	2.29
Quality Factor(Q)	4.93	6.12	4.93

4.20 Supply Voltage Variations (±10%) in 10.6MHz IF CMOS Gm-C Band Pass Filter



(a)



(b)

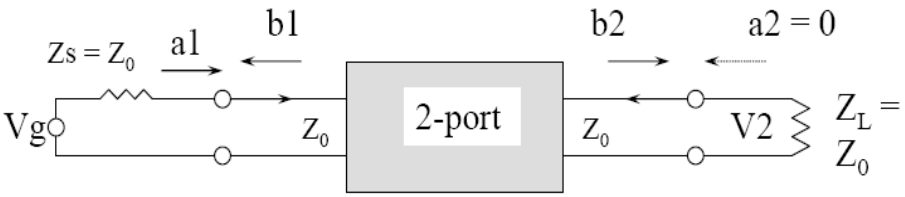
Figure 4.52 10.6MHz IF Second order CMOS Gm-C Band Pass Filter Response at (a) 1.62V Supply and (b) 1.98V Supply

4.21 S-Parameters

The S-parameter simulation is performed for the Band Pass Filter for impedance matching of 50 ohms on input and output of the filter. The S parameters are found by considering the filter structures as two port network. For a two-port network there are four S parameters S_{11}, S_{21}, S_{12} and S_{22}. S_{11} and S_{22} are simply the forward and reverse reflection coefficients, with the opposite port terminated in Z_0 (usually 50 ohms.). S_{21} and S_{12} are simply the forward and reverse gains assuming a Z_0 source and load (again usually 50 ohms).

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$



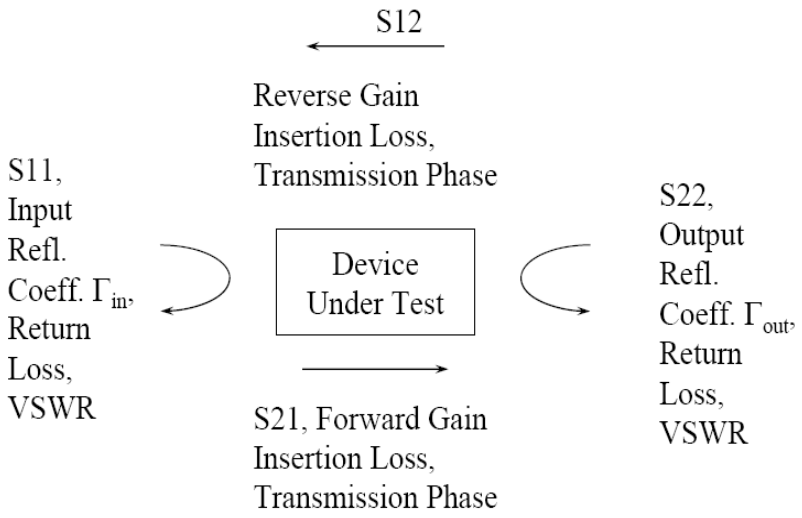
Here a1 and a2 are incident wave and b1 and b2 are reflected waves.

$S_{11} = \frac{b_1}{a_1}$ (With $a_2 = 0$) = Input Reflection Coefficient Γin for the case of $Z_L = Z_0$.

$S_{21} = \frac{b_2}{a_1}$ (With $a_2 = 0$) = Forward Transmission (Insertion) Gain for the case of $Z_L = Z_0$.

$S_{12} = \frac{b_1}{a_2}$ (With $a_1 = 0$) = Reverse Transmission (Insertion) Gain for the case of $Z_S = Z_0$.

$S_{22} = \frac{b_2}{a_2}$ (With $a_1 = 0$) = Output Reflection Coefficient Γout for the case of $Z_S = Z_0$.



Smith Chart:

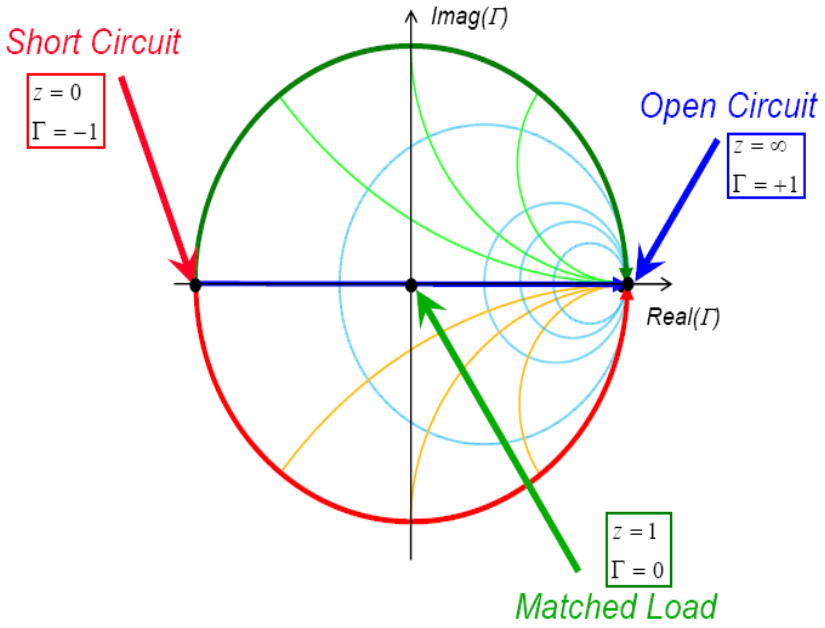


Figure 4.53 Basic Smith Chart

4.21.1 S-Parameter Simulation Results for 70MHz GSM IF

4.21.1.1 S-Parameter S_{21} Simulation Result

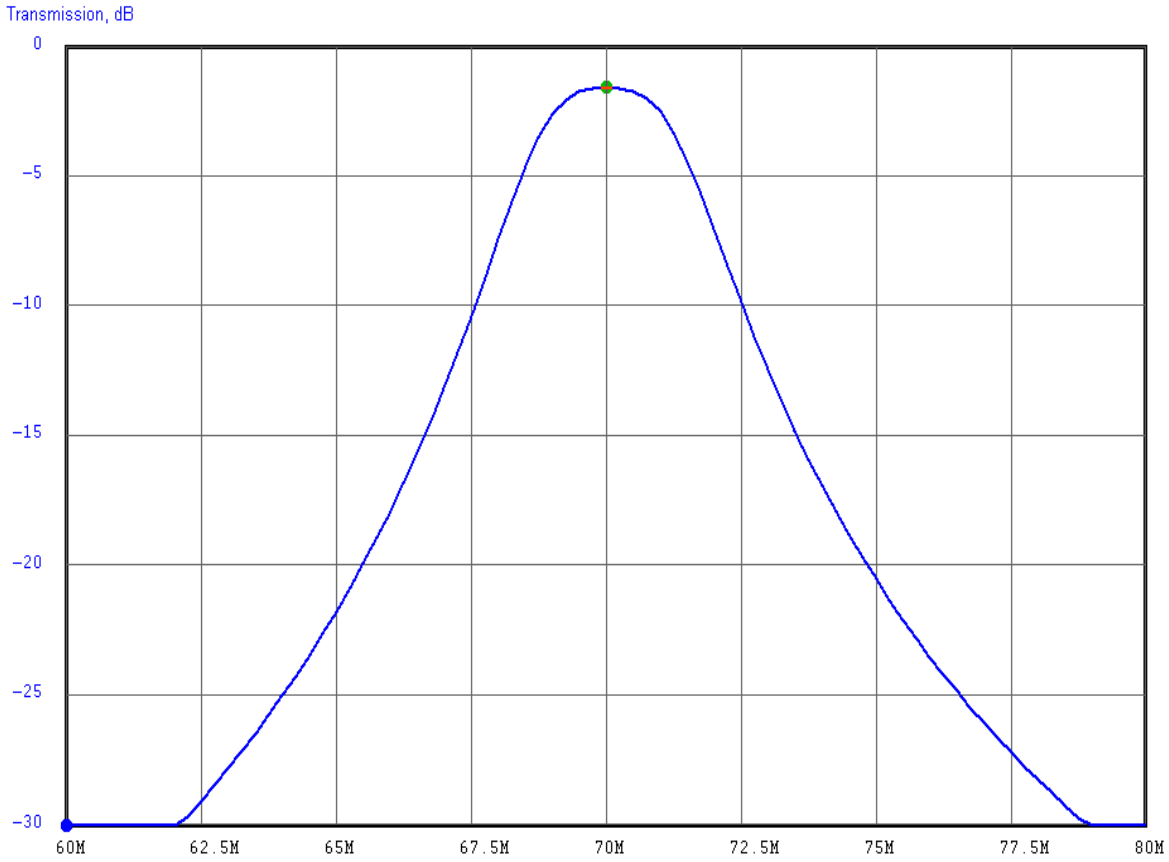


Figure 4.54 Transmission S_{21} for 70MHz GSM IF

4.21.1.2 S-Parameter S_{21} and S_{11} Simulation Result

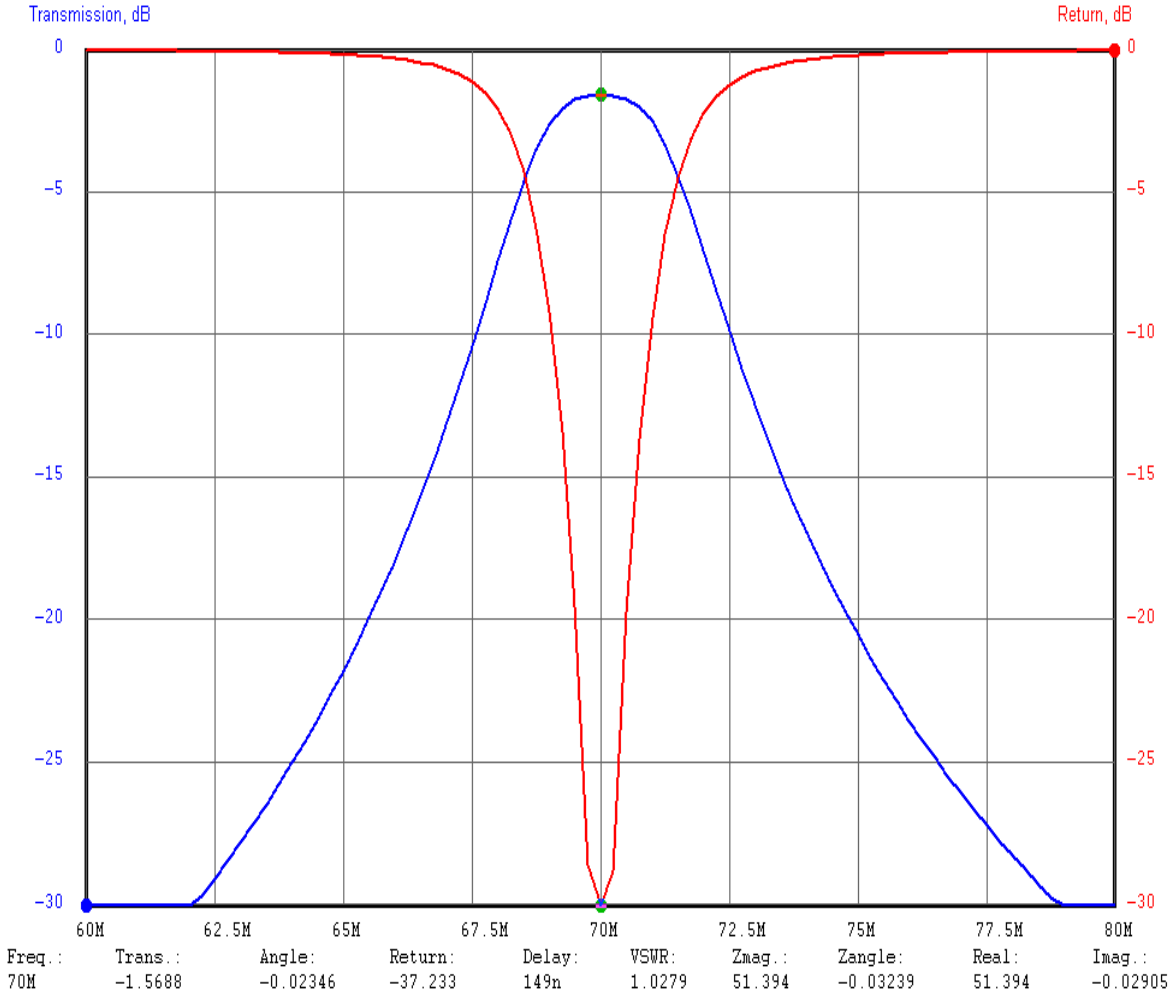


Figure 4.55 Transmission S_{21} and Return S_{11} for 70MHz GSM IF

4.21.1.3 S-Parameter S_{21} and Angle of Transmission Simulation Result

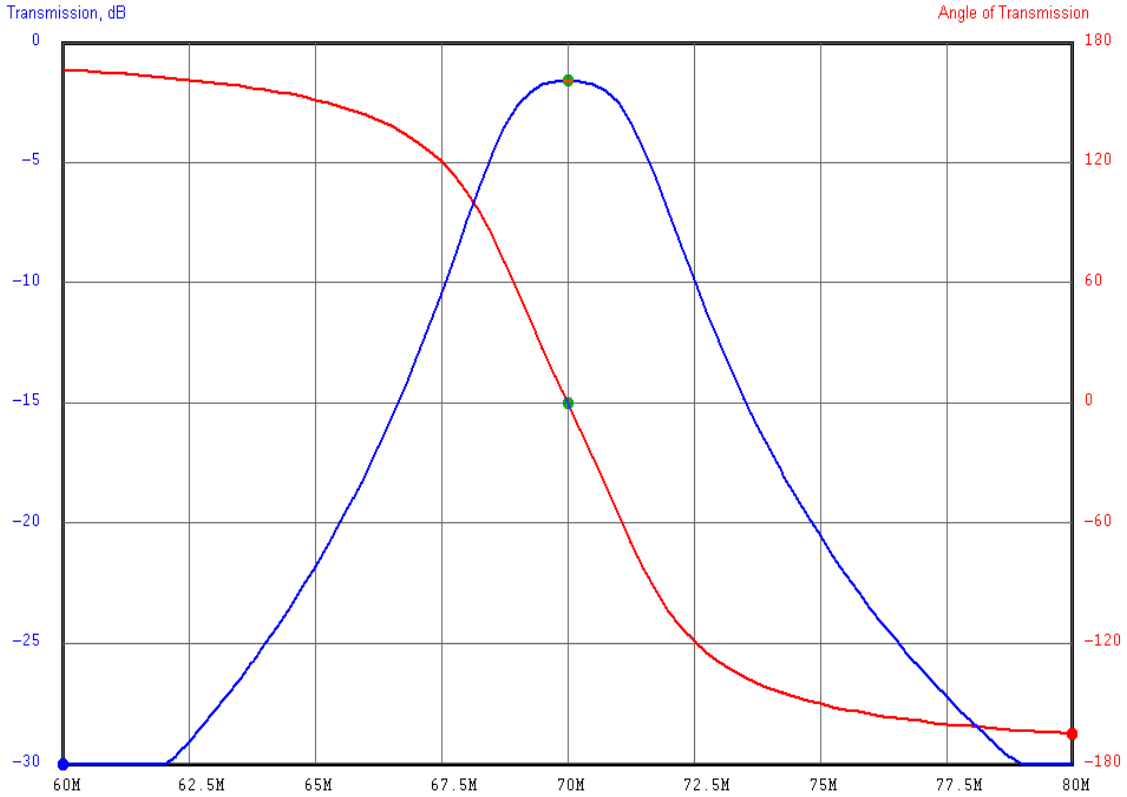


Figure 4.56 Transmission S_{21} and Angle of Transmission for 70MHz GSM IF

4.21.1.4 Simulation Result of Smith Chart for S_{11}

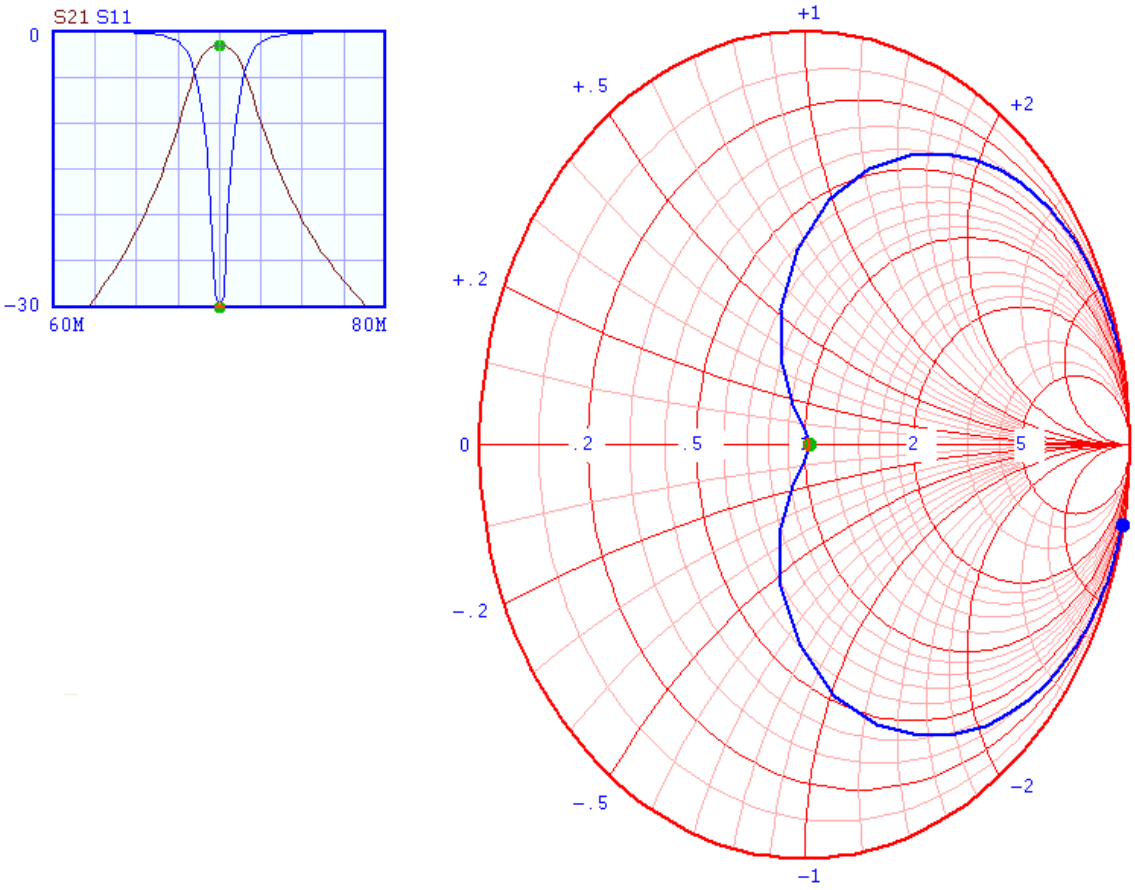


Figure 4.57 Smith Chart S_{11} for 70MHz GSM IF

4.21.1.5 Simulation Result of Smith polar plot for S_{21}

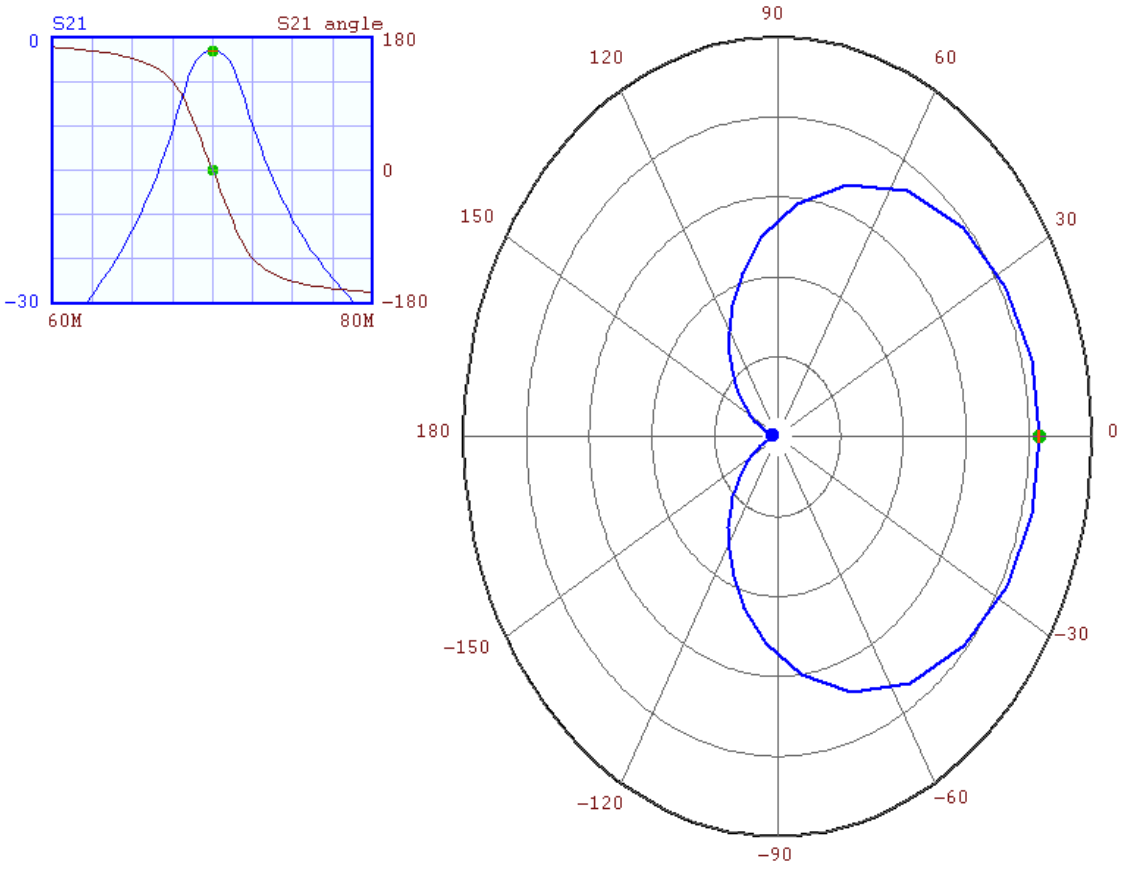


Figure 4.58 Smith Polar Plot S_{21} for 70MHz GSM IF

4.21.2 S-Parameter Simulation Results for 10.6 MHz FM IF

4.21.2.1 S-Parameter S_{21} Simulation Result

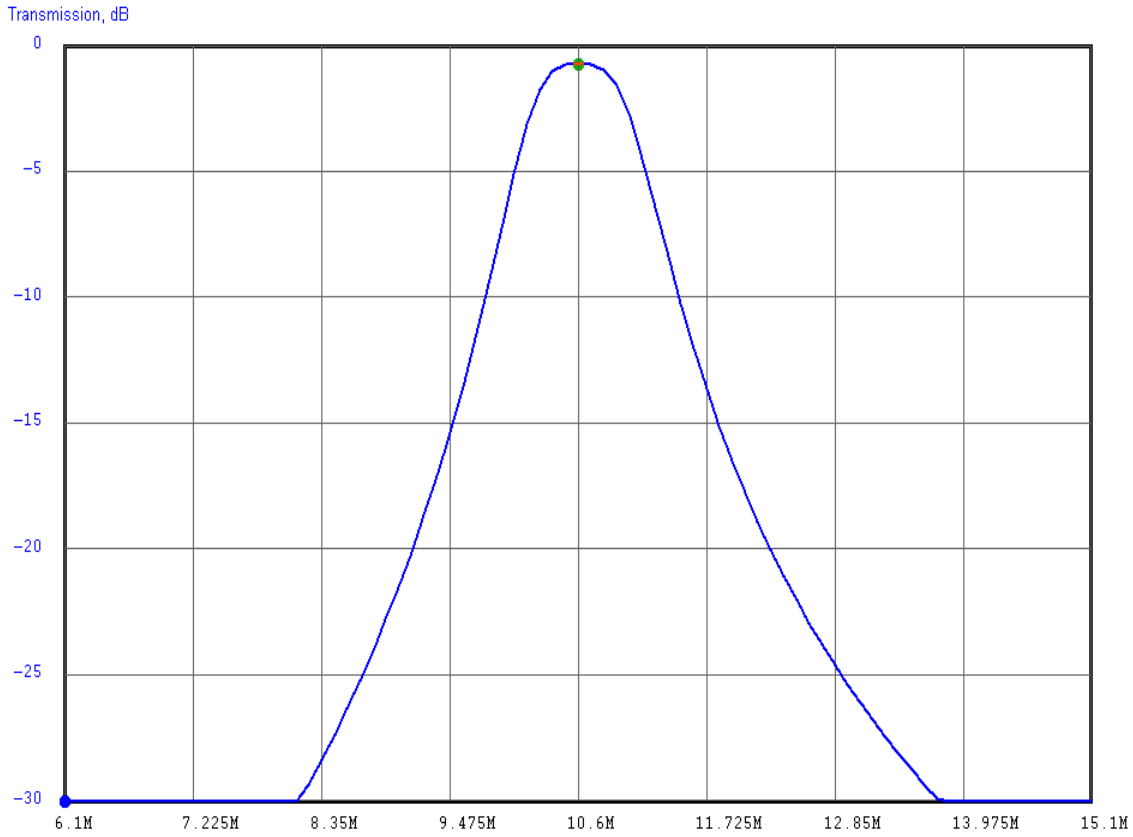


Figure 4.59 Transmission S_{21} for 10.6MHz FM IF

4.21.2.2 S-Parameter S_{21} and S_{11} Simulation Result

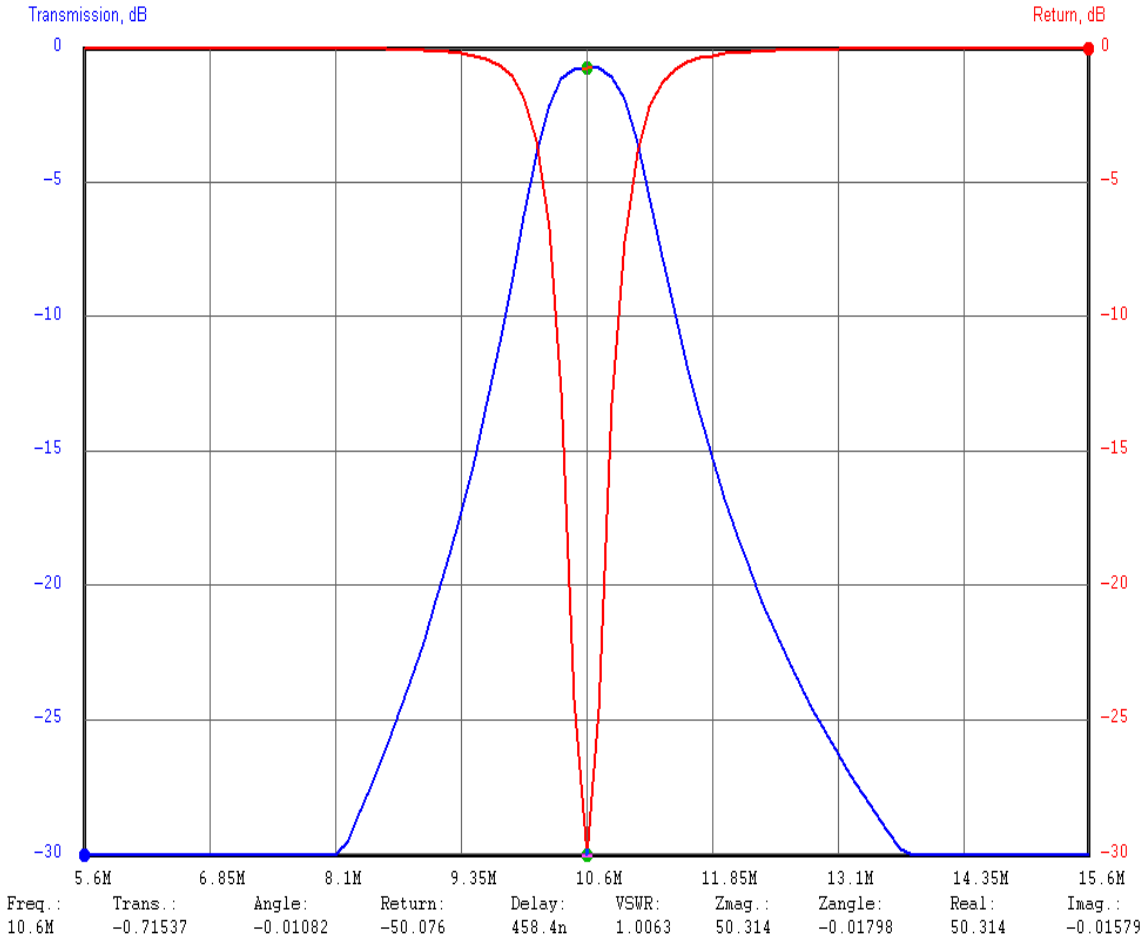


Figure 4.60 Transmission S_{21} and Return S_{11} for 10.6MHz FM IF

4.21.2.3 S-Parameter S_{21} and Angle of Transmission Simulation Result

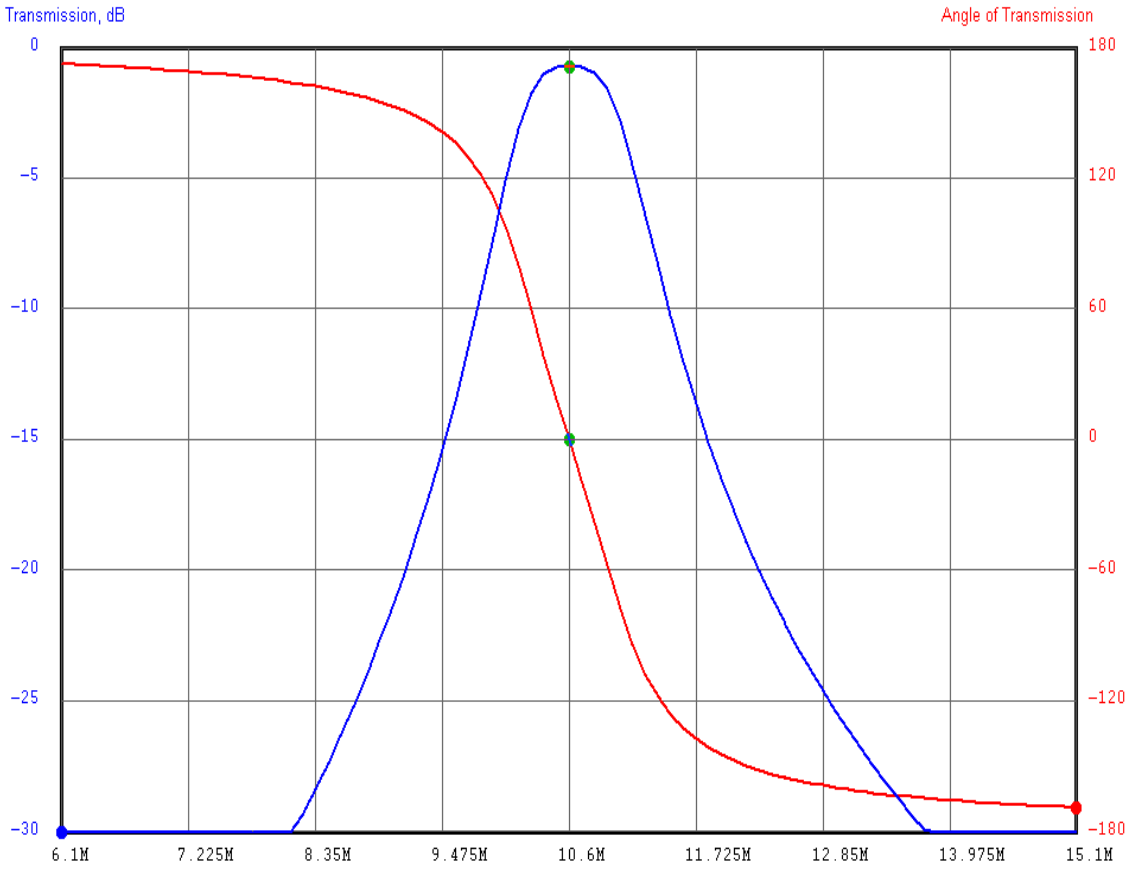


Figure 4.61 Transmission S_{21} and Angle of Transmission for 10.6MHz FM IF

4.21.2.4 Simulation Result of Smith Chart for S_{11}

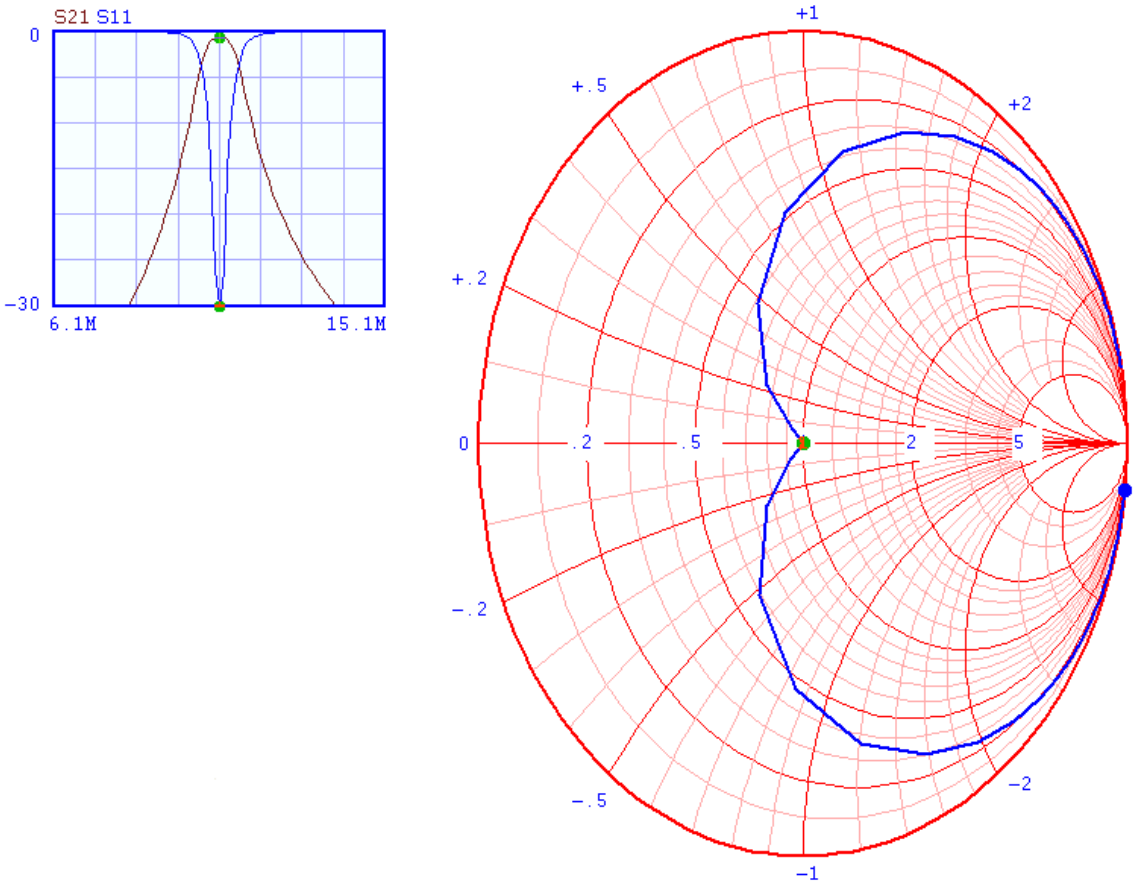


Figure 4.62 Smith Chart S_{11} for 10.6MHz FM IF

4.21.2.5 Simulation Result of Smith polar plot for S_{21}

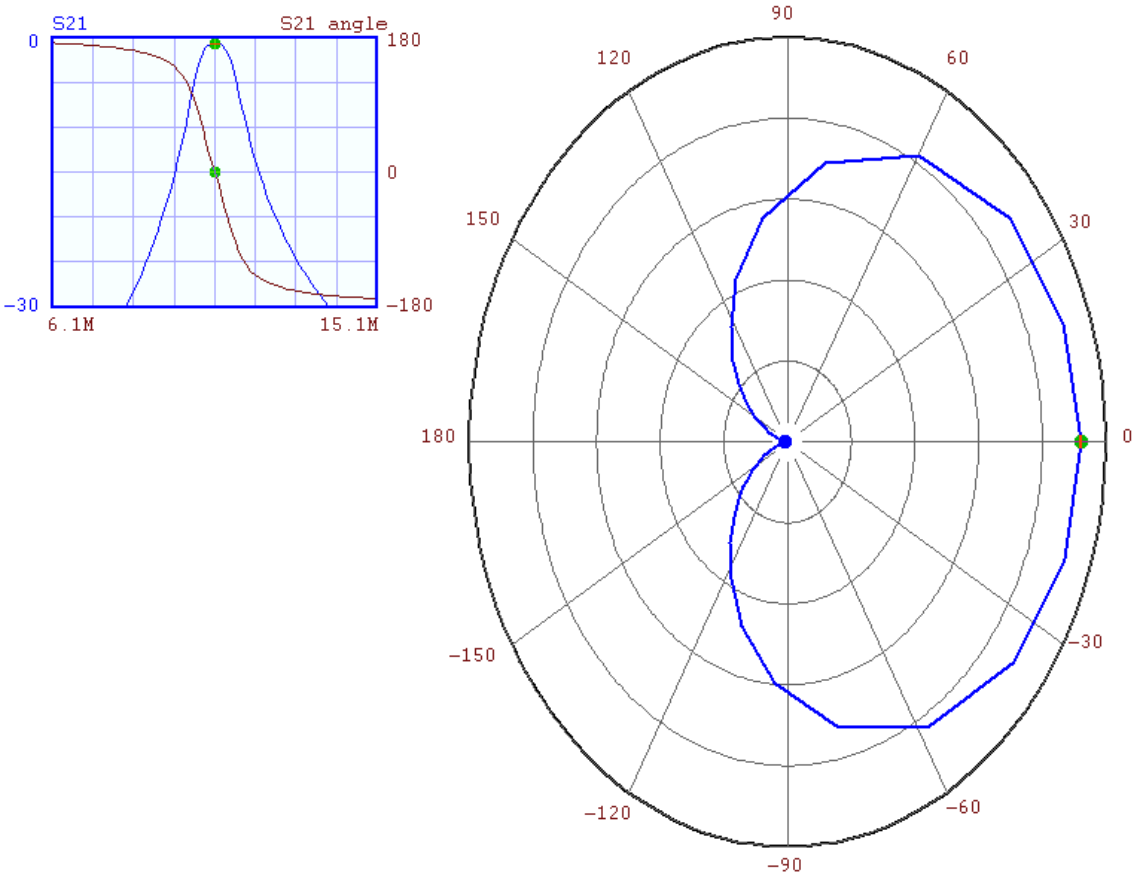


Figure 4.63 Smith Polar Plot S_{21} for 10.6MHz FM IF

4.22 Dual Band Filter Measurement Results

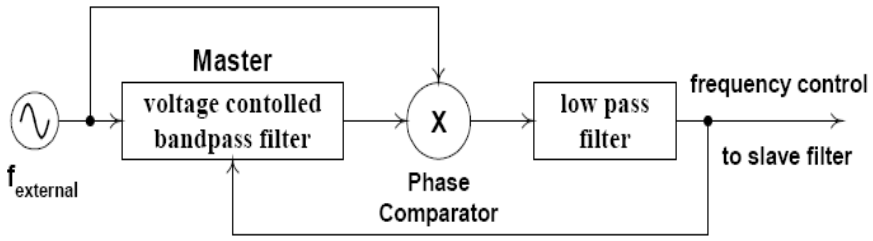
Table 4.15 Dual Band Filter measurement results

Technology	**0.18µm CMOS**	
Supply Voltage	**1.8V**	
Filter Order	**2**	
Type	**Gm-C**	
Gain	**4.31**	**4.8**
Center Frequency	**GSM:70MHz**	**FM:10.6MHz**
Bandwidth	**5.10MHz**	**1.73MHz**
Q Factor	**13.72**	**8.83**
Power Consumption	**574µW**	
Tuning Range	**10.6MHz IF to 70MHz IF**	
Tuning Ratio	**6.6**	
S_{21}	**-1.5688dB**	**-0.71dB**
S_{11}	**-37.23dB**	**-50.076**
Sensitivity@-5MHz	**-21.73dB**	**-46dB**
Sensitivity@+5MHz	**-20.53dB**	**-36.5dB**

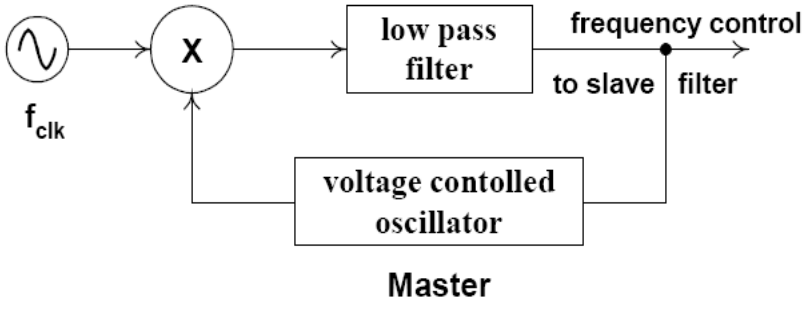
4.23 Automatic Tuning Scheme

4.23.1 Existing Tuning Method

Automatic tuning is used to control the frequency response of continuous-time filters. A tuning is required in a continuous-time filter to compensate the drift of element values due to process and temperature variations which will affect the accuracy of filter. The center frequency can be improved to a few percent or even to a fraction of 1% by using tuning techniques based on the master slave tuning principle, implemented by means of a phase locked loop (PLL) using either a voltage controlled filter (VCF) or voltage controlled oscillator (VCO), as shown in Fig. 4.61[211].



(a)



(b)

Figure 4.64 (a) Master-slave frequency tuning scheme based on a VCF
(b) Master-slave frequency tuning scheme based on a VCO

In the voltage controlled filter (VCF), an external reference signal $f_{external}$ is applied to the master filter which is similar to a second-order filter section which is similar to those used in the filter to be tuned. The frequency-dependent input-output phase characteristics

of this reference are then exploited to tune the circuit. Any offset in the phase comparator will result in a frequency tuning error.

Disadvantage of VCF configuration is that harmonic distortion in the reference signal will introduce additional tuning errors. This is because the harmonics will not come out from the reference filter with the same phase shift as the fundamental frequency. When multiplied with the incoming signal, these residual out-of-phase harmonics will alter the result of phase comparison. Some of those distortions are dc components. This dc component can be considered as noise, which will produce error on the dc output of the phase comparator.

In the VCO approach, the multiplier or the phase comparator has to compare the frequency of the signal coming out from the VCO with that of the reference signal. The error voltage is filtered out by the low pass filter and feedback to the voltage-controlled oscillator. As compared to the VCF approach, only the phase variations that mean frequency, of one signal with respect to the other must be detected. So, for the requirement of phase comparator a simple XOR gate can be used. For the precision of the tuning system, the important parameter is the oscillating frequency of the VCO.

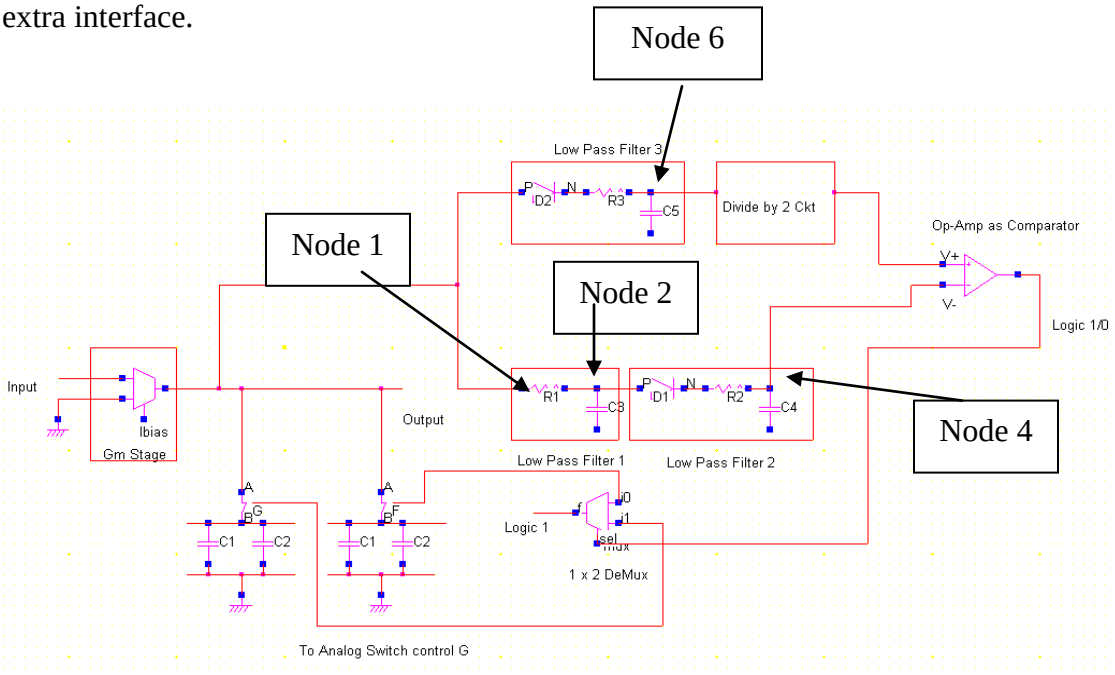
The main problem is the implementation of a voltage-controlled oscillator that is well matched to the filter to be tuned. The best candidate is usually a second-order harmonic oscillator, which must be carefully considered since harmonic distortion and nonlinearities in the transconductors would shift the effective oscillation frequency, thus introducing a tuning error.

Another design consideration of the VCO technique is the feed through from the oscillator to the filter, which should be minimized. Master-slave techniques are ultimately limited by the mismatches of the main filter elements. This problem is more prominent in high frequency where the filter becomes more sensitive to parasitic which are extremely difficult to match in the master and the slave.

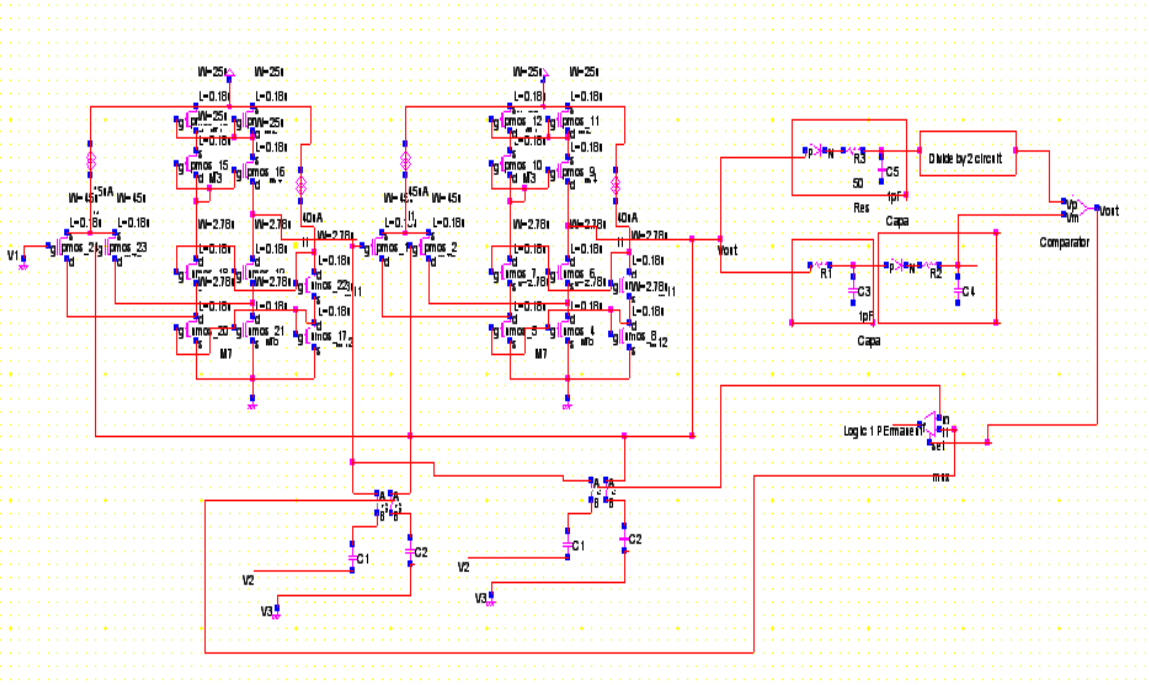
4.23.2 Proposed Tuning Method

A digital frequency tuning technique is shown in Figure 4.61. The tuning circuit consists of an LPF, Comparator, De-Multiplexer, and Switch. In an OTA-C filter, frequency tuning can be achieved by tuning the transconductors using a control voltage or by tuning the capacitors using a capacitor array (CA). The first solution implies changing the dynamic range of the filter since the bias conditions of the OTA and thus linearity of the filter is changed. The second solution using CA is preferable to optimize the dynamic range of the filter during tuning at the expense of area since the CA and associated switches require more area.

Digital frequency tuning scheme shown in Figure 4.61 is very well suited with those type of applications where the frequency tuning is implemented using CAs. The output of the de-multiplexer is directly connected to the switches of the CA without the need of an extra interface.



(a)



(b)

Figure 4.65 Automatic Tuning Circuit (a) without Gm stage circuit

(b) With Gm Stage circuit

Here the Intermediate frequency is tuned between FM 10.6 MHz IF to 70 MHz IF for GSM using capacitor array. Consider two cases:

I-Case:

Suppose FM band is selected then 10.6MHz FM IF signal is passed from 10.06MHz Low pass filter, followed by Low pass filter2 and the same signal passed from 70MHz Low pass Filter3. Output of low pass filter2 is compared with reference voltage in comparator. Simulation results are shown below.

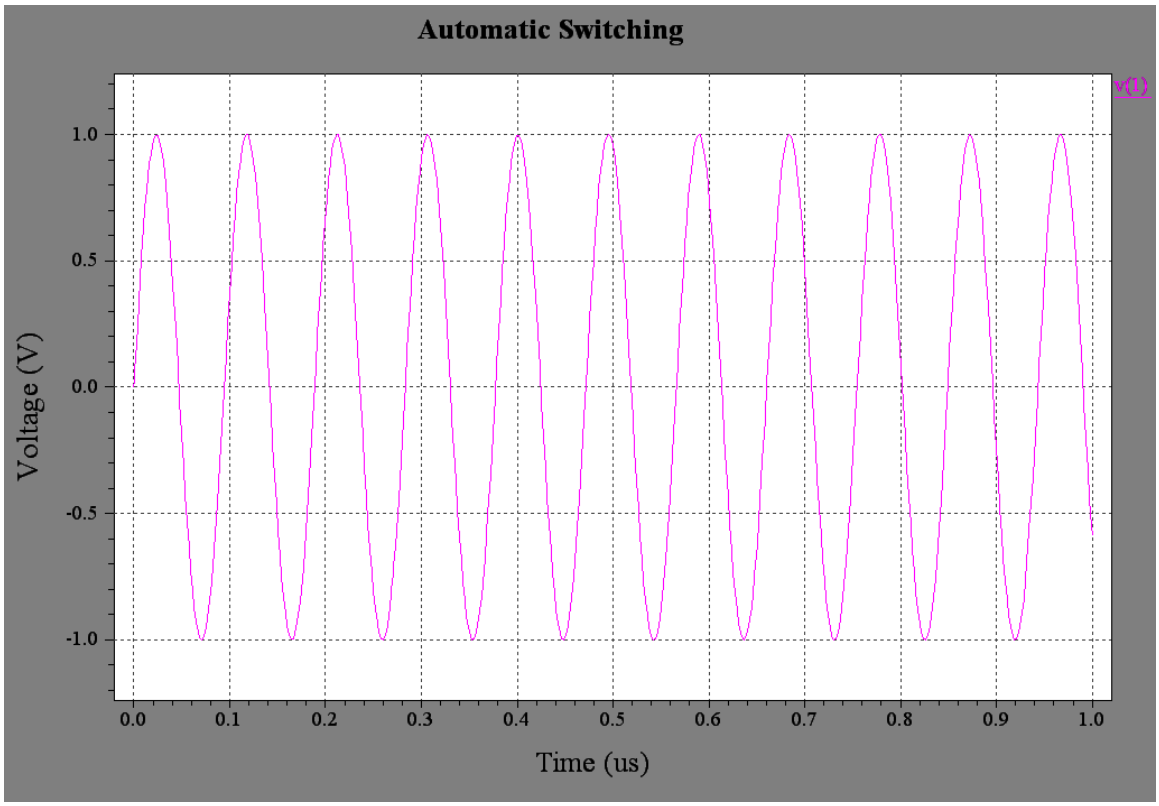


Figure 4.66 (a) I-Case Waveform at Node 1 in Automatic Tuning Circuit

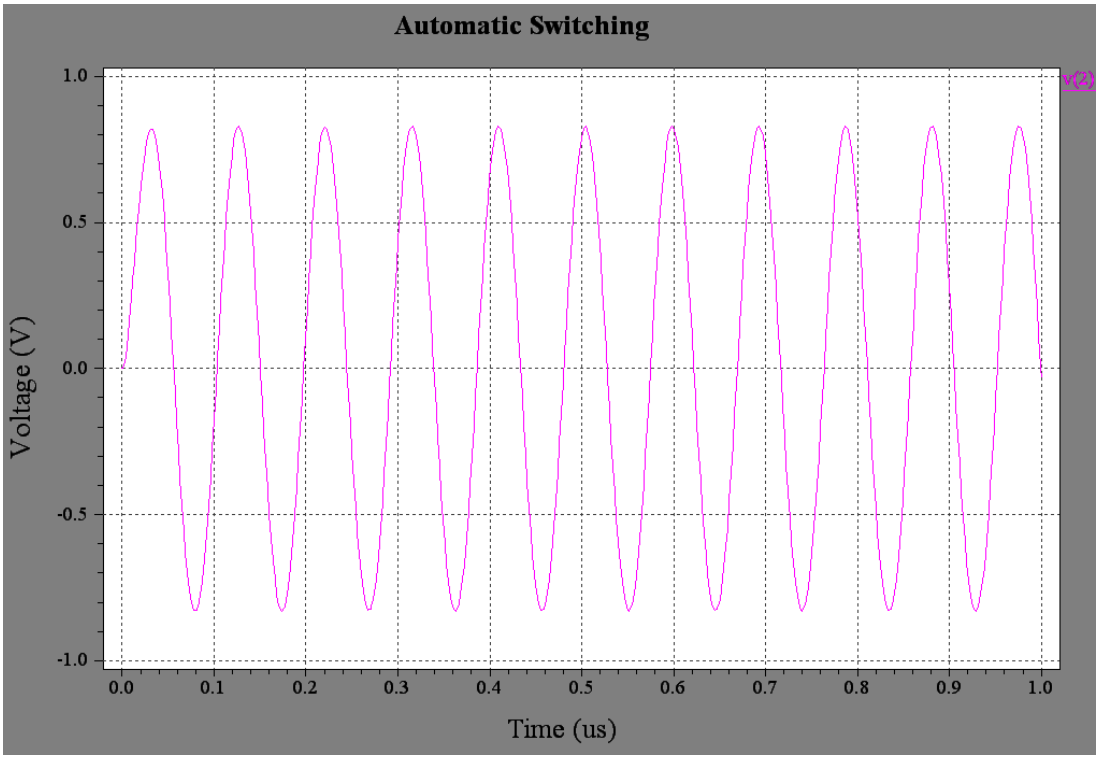


Figure 4.66(b) I-CaseWaveform at Node 2 in Automatic Tuning Circuit

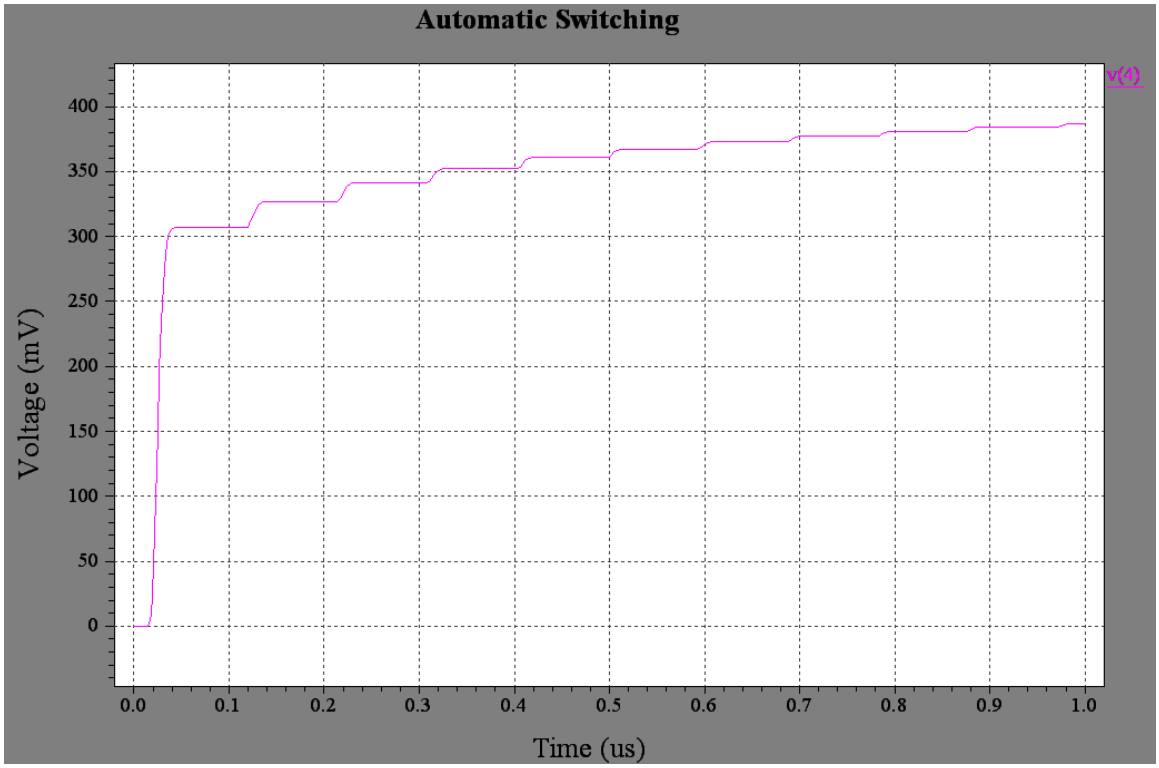


Figure 4.66(C) I-Case Waveform at Node 4 in Automatic Tuning Circuit

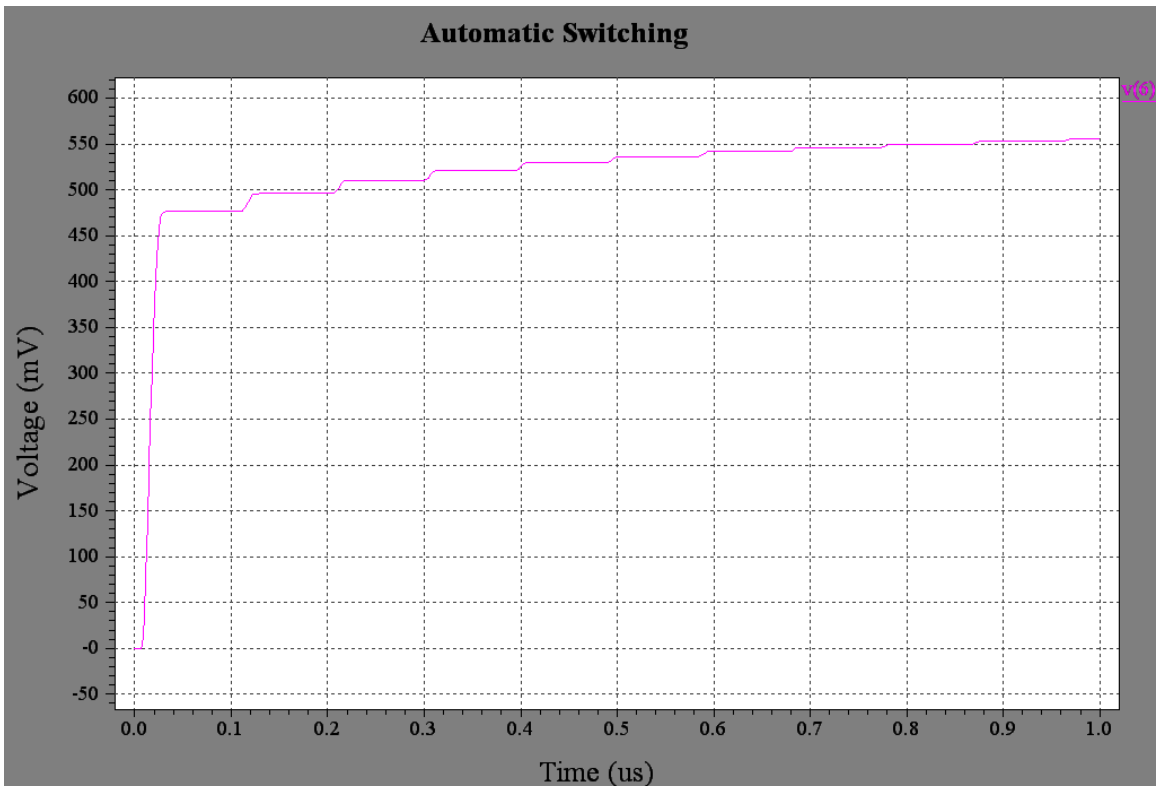


Figure 4.66(d) I-Case Waveform at Node 6 in Automatic Tuning Circuit

Output of Low pass filter2 at node 4 is 380mV is given to V- terminal of comparator and 250mV output of divide by 2 circuit, which is voltage divider circuit, is given to V+ terminal of Comparator. Comparator compares the two input voltages and based on that, output is logic 0, which is given to selection line of line of 1x2 de-multiplexer. Based on logic 0 at selection line of 1x2 de-multiplexer, input I0 is selected with Switch F is closed and particular Capacitor Array(CA) is activated.

II-Case:

IF GSM band is selected then 70MHz IF signal is passed from 10.6MHz Low pass filter and that 70MHz IF signal is highly attenuated because it is going to pass from 10.6MHz low pass filter. Highly attenuated output of 10.6MHz low pass filter is going to pass low pass filter2. Output of low pass filter2 is compared with reference voltage in comparator. Simulation results are shown below.

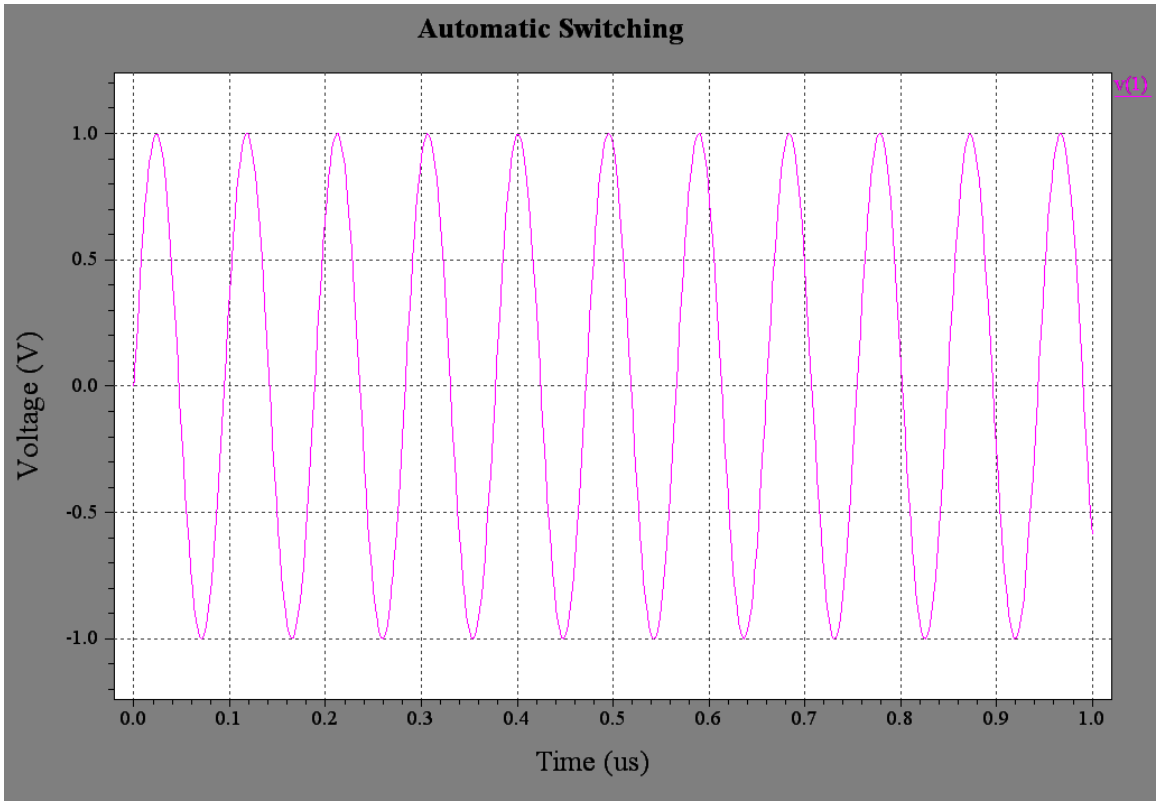


Figure 4.67(a) II-CaseWaveform at Node 1in Automatic Tuning Circuit

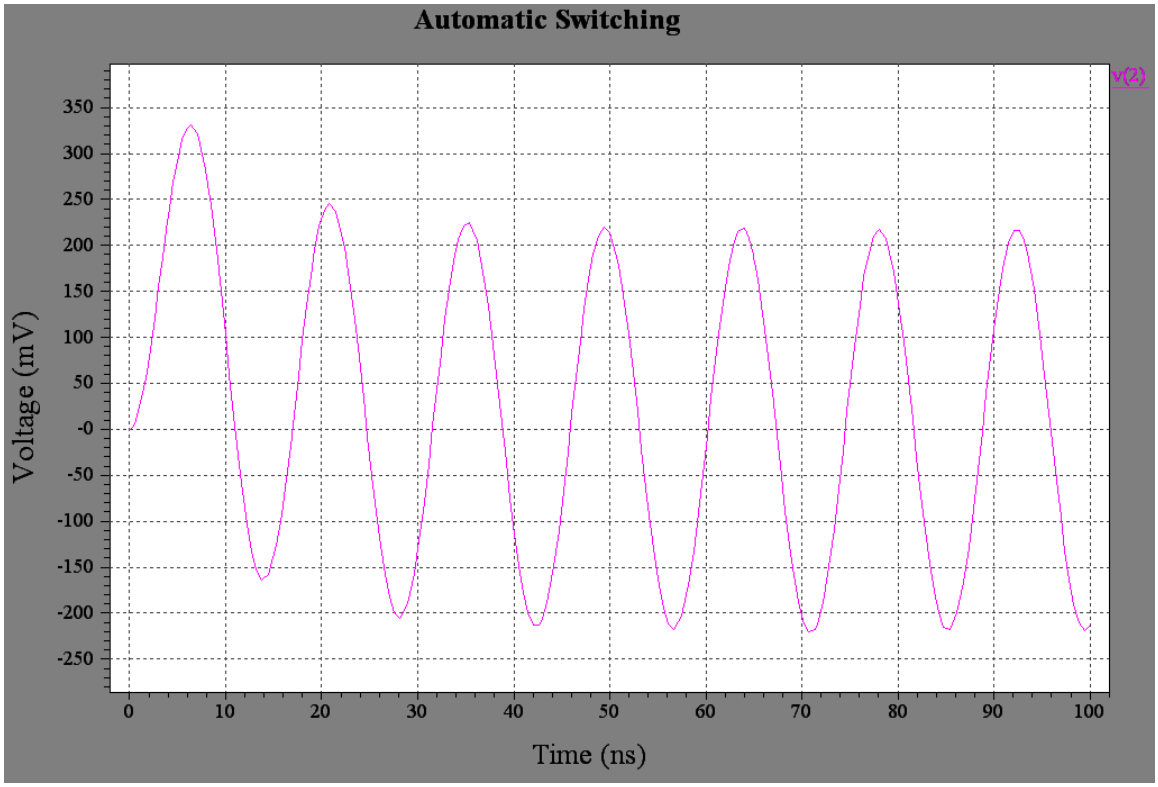


Figure 4.67(b) II-Case Waveform at Node 2 in Automatic Tuning Circuit

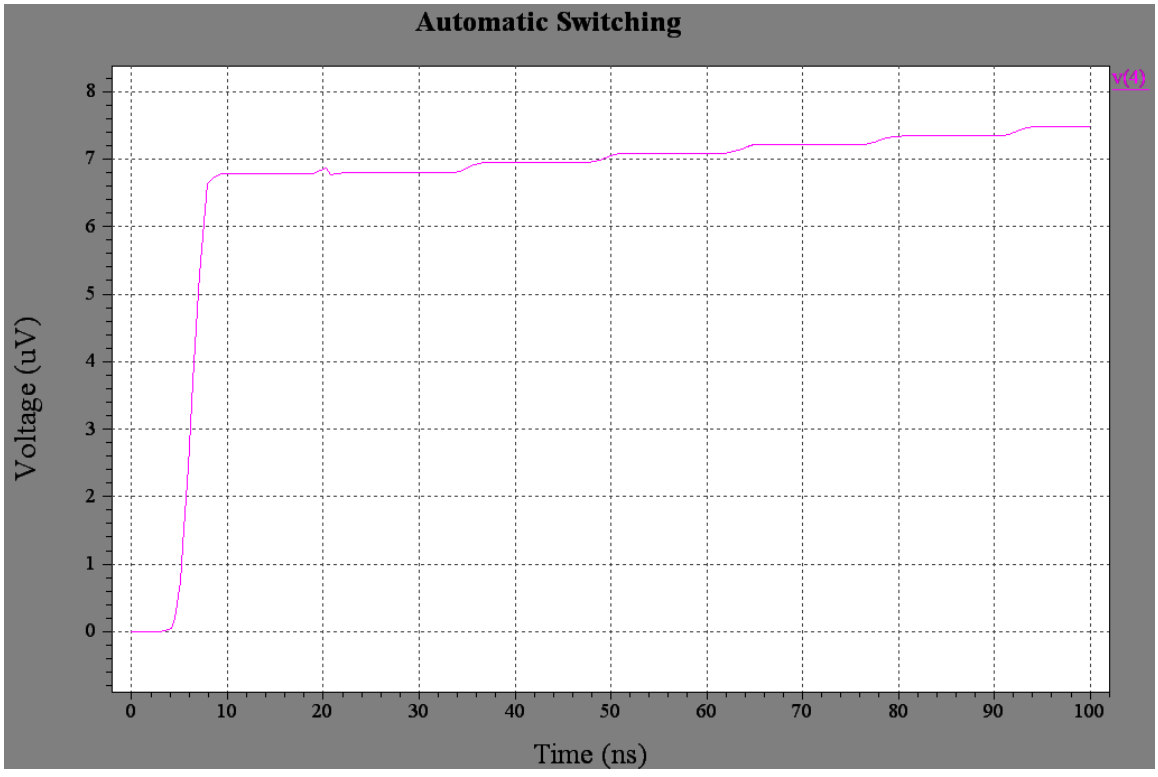


Figure 4.67(c) II-Case Waveform at Node 4 in Automatic Tuning Circuit

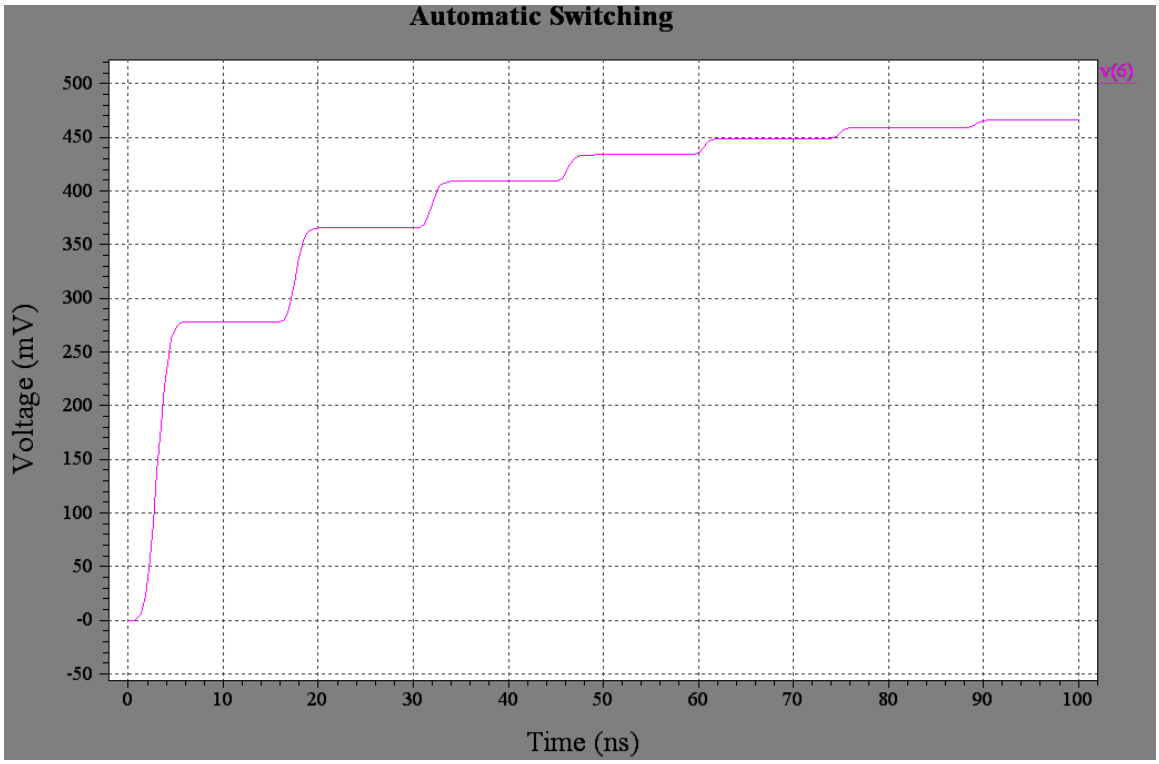


Figure 4.67(d) II-Case Waveform at Node 6 in Automatic Tuning Circuit

Output of Low pass filter2 is 7.5µV is given to V- terminal of comparator and 250mV output of divide by 2 circuit, which is voltage divider circuit, is given to V+ terminal of Comparator. Comparator compares the two input voltages and based on that, output is logic 1, which is given to selection line of line of 1x2 de-multiplexer. Based on logic 1 at selection line of 1x2 de-multiplexer, input I1 is selected with Switch G is closed and particular Capacitor Array (CA) is activated.

4.23.3 Comparator and Analog Switch Layouts

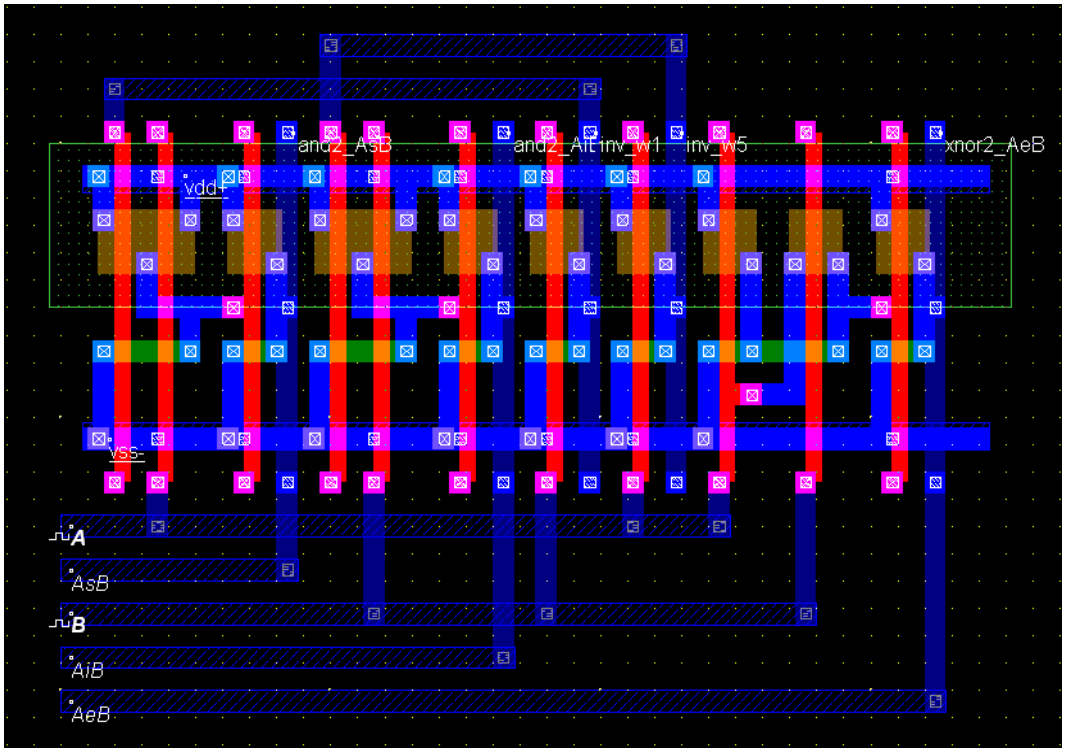


Figure 4.68 Comparator Layout

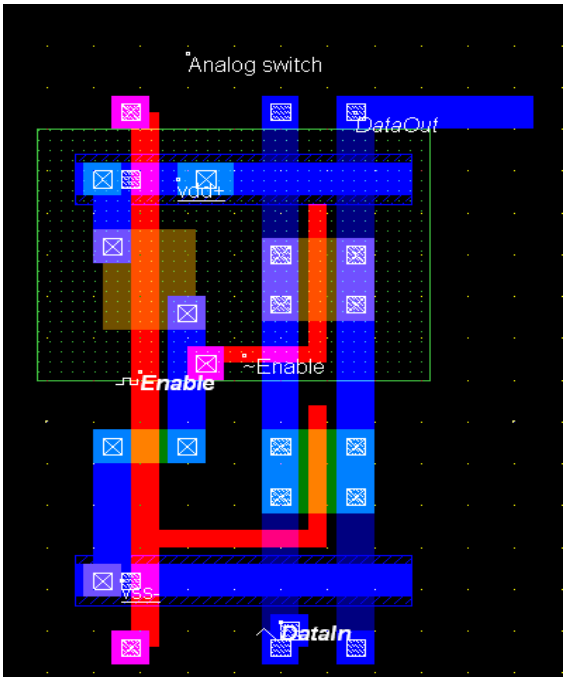


Figure 4.69 Analog Switch Layout

4.24 Comparison with Previously Reported works

Table 4.16 Comparison with Previously Reported works

Specification	[185]	[187]	[189]	[190]	[193]	[198]
Technology	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.35µm CMOS	0.18µm CMOS
Type	Gm-C	Gm-C	Gm-C	Gm-C	Gm-C	Gm-C
Supply Voltage	0.5V	1.8V	1.2V	1.8V	1.3V	1V
Filter Order	3	5	3	2	2	3
Tuning Range	1.4MHz to 6MHz	150KHz to 23MHz	-3dB cutoff: 9.8MHz	Cutoff Freq: 24MHz	200KHz to 3.1 MHz	135KHz-2.2 MHz
Power Consumption	60µW	10.8mW	3.8mA X 1.2V	384µW	0.2mW	<2mW

Specification	[212]	[213]	[214]	[215]	[216]	This Work
Technology	0.18µm CMOS	0.18µm CMOS	0.25µm Bi-CMOS	0.13µm CMOS	0.13µm CMOS	0.18µm CMOS
Type	Gm-C	Gm-C	Gm-C	Active Gm-RC	Active Gm-RC	Gm-C
Supply Voltage	1.8V	1.8V	2.5V	1.2V	1.2V	1.8V
Filter Order	6	4	3	4	2-6	2
Tuning Range	1.5MHz to 12MHz	0.5MHz to 12MHz	50KHz to 2.2MHz	2.11MHz to 11MHz	350KHz To 23.5 MHz	10.6MHz To 70MHz
Power Consumption	15mW	4.5mW	7.3mW	14.2mW	21.6mW	574 µW

Conclusion

Vast attention has been paid to active continuous-time filters over the years. Thus as the cheap, readily available integrated circuit OpAmps replaced their discrete circuit versions, it became feasible to consider active-RC filter circuits using large numbers of OpAmps. Similarly the development of integrated operational transconductance amplifier (OTA) led to new filter configurations. This gave rise to OTA-C filters, using only active devices and capacitors, making it more suitable for integration. The demands on filter circuits have become ever more stringent as the world of electronics and communications has advanced. In addition, the continuing increase in the operating frequencies of modern circuits and systems increases the need for active filters that can perform at these higher frequencies; an area where the LC active filter emerges. This research concentrates on the design of high frequency continuous-time Gm-C integrated filters.

In general, the bandwidth of the OTA used in the filter must be much larger than the filter cut-off frequency. The OTA must also have with linearity in order to achieve acceptable low distortion levels. For high frequency filters, single stage OTAs are preferred, because the internal nodes of multi-stage designs result in additional excess phase shift, as well as increased power consumption.

The designed Wilson Current Mirror base folded cascode OTA works for frequencies that lead to a base band circuit design for RF application, is based on transistor sizing methodology. Simulation results are performed using SPICE software and BSIM3V3 model for CMOS 0.18um process, show that the designed folded cascode OTA has a 52dB DC gain, a unity gain bandwidth around 390MHz, phase margin of 50degrees with power consumption 288μw. The circuit denotes an offset voltage of 0.05V, a Slew Rate of 160V/μs, and Input Common Mode Range (ICMR) close to Supply Rails (± 1.8V)

Mobile telephony together with mobile phones has revolutionized the world and the way people communicate. While the first mobile phones were simple devices whose main and only features were the voice communication and the messaging capability, today’s mobile phones are innovative devices that provide a wide variety of services to users.

Among such wide variety of services, one of the most attractive mobile phone services are the entertainment services, and specially the functionality that allows users to listen to FM radios through their mobile phones.

This thesis concentrates on the design and implementation of analog continuous- time Gm-C IF filter for Dual Band (FM and GSM) receivers. The main reason for using an intermediate frequency is to improve frequency selectivity. In communication circuits, a very common task is to separate out or extract signals or components of a signal that are close together in frequency. This is called filtering. With all known filtering techniques the filter's bandwidth increases proportionately with the frequency. So a narrower bandwidth and more selectivity can be achieved by converting the signal to a lower IF and performing the filtering at that frequency.

CMOS Gm-C IF filter is used in wireless systems for channel selection and filtering in Intermediate Frequency (IF) ranges. The Filter is designed either as external filters or on-chip filters. External filters provide very high Quality factor (Q) but require buffers to drive the off-chip components. These buffers consume more power and in order to reduce the power consumption, on-chip filters are preferred in wireless systems. On-chip filters are designed with active circuits and offer very low power consumption and good efficiency. Most of the on-chip filters are designed with Operational Transconductance Amplifier (OTA) and capacitors and are generally called as Gm-C filters. The Gm-C filter offers many advantages in terms of low-power and works well at high frequencies. The Gm-C circuits represent a popular technique of integrated realization of high frequency continuous time filters. Gm-C filters can operate in a wide range of frequencies from several hundred of KHz to more than 100MHz. The Q of Gm-C filters can be adjusted by controlling the output impedance even at lower frequencies.

The objective of this work is to design an integrated second order active Gm-C CMOS IF band pass filter for Dual Band Receiver; operating at center Frequency (10.6MHz IF for FM Band and 70MHz IF for GSM Band IF) range with tunability, Linearity, silicon area and Low power consumption

Designed of a 2^{nd} order Gm-C dual-band IF filter to be used in a dual-band down conversion receiver for FM band and GSM band, as design is carried out in the TSMC 0.18μm CMOS technology with the BSIM3V3 Level 49 MOSFET model and the filter operates form 1.8V single supply. The performances of the filters designed are analyzed using various parameters like center frequency, gain, bandwidth, Q, and S-parameters.

The ac responses of the 2nd order Gm-C dual-band IF Band Pass filter provides high Q (13.72 for GSM Band and 6.12 for FM Band) with bandwidth (5.10MHz for GSM Band and 1.73MHz for FM Band) and good gain (4.31 for GSM Band and 4.45 for FM Band)

The S-parameter simulation is performed for the 2nd order Gm-C dual-band IF Band Pass filter for impedance matching of 50 ohms on input and output of the filter. The S-parameters are found by considering the filter structures as two port network. S-parameters found are input return loss in dB (S_{11}) and forward voltage gain in dB (S_{21}). The S-parameter simulation of the 2nd order Gm-C dual-band IF Band Pass filter shows that the forward voltage gain (S_{21}) are at maximum (-1.56dB for GSM Band and -0.71dB for FM Band) at the center frequency of the filters and the losses (S_{11}) are at minimum (-37.23dB for GSM Band and -50.07dB for FM Band) at the center frequency of the filters.

The designed filter has tuning ratio 6.6 and suitable for IF channel selection of Wireless System with power consumption 575μw. Designed of a 2^{nd} order Gm-C dual-band IF filter is based on capacitor array (CA) and a digital automatic tuning system is implemented for tuning the Intermediate Frequency (IF) for GSM band and FM band.

Summary:

The designed Wilson current mirror based folded Cascode OTA was biased at 1.8V power supply voltage using CMOS technology of 0.18μm with the BSIM3V3 level 49 MOSFET model.

The circuit denotes an offset voltage of 0.05V, an input-output swing -1.8V/+1.5V,a Slew Rate of 160V/μS, and an input common-mode range close to supply rail ±1.8V. Designed Wilson Mirror base Folded Cascode OTA achieves a gain of 52dB and a wide bandwidth of 390 MHz with phase margin of 50 degrees.

Folded cascode OTA based on Wilson mirror has a limited output swing, because the maximum output voltage is set lower than: $V_{DD} + V_T + 2V_{ds,sat}$ so, we use cascode current mirror in order to restore this fall to $+2V_{ds,sat}$ and finally we achieved input-output swing -1.8V/+1.8V.

Based on Folded Cascode OTA, designed an integrated second order active Gm-C CMOS IF band pass filter for Dual Band Receiver, operating at center Frequency(10.6MHz IF for FM Band and 70MHz IF for GSM Band IF) range. The performances of the filters designed are analyzed using various parameters like center frequency, gain, bandwidth, Q, and S-parameters.

The ac responses of the 2nd order Gm-C dual-band IF Band Pass filter provides high Q (13.72 for GSM Band and 6.12 for FM Band) with bandwidth (5.10MHz for GSM Band and 1.73MHz for FM Band) and good gain (4.31 for GSM Band and 4.45 for FM Band).

The performances of the filters designed are also analyzed with 10% supply voltage and Temperature variations.

Layout represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout level, the

component parameters are totally different from schematic level. So it provides the facility to the user to analyze the response of the circuit before forwarding it to the time consuming & costly process of fabrication. There are rules for designing layout of a schematic circuit using which user can compare the output response with the expected one.

Extract creates SPICE (Simulation Programme with IC Emphasis) compatible circuit net lists from layouts. It can recognize devices, sub circuits, and the most common device parameters, including resistance, capacitance, device length, width, and area.

Monte Carlo analysis provides an accurate and powerful method for parametric yield estimation. The principle of Monte Carlo analysis can be defined as the generation of circuit figure-of-merit distributions as a function of statistically varying device model parameters that accurately reflect manufacturing process variations. Variations of physical parameters (e.g. oxide thickness or doping concentration) lead to variations of electrical parameters, like threshold voltage or gate capacitance. In turn, this affects the performance of circuits as it changes gate delays or leakage currents. By performing Monte-Carlo (MC) simulations on transistor level, the effect of global variations on the circuit behavior can be explored. Probability distributions for the varying device parameters serve as input for Monte-Carlo simulations. The distributions are based on measured statistics of the manufactured transistors. Therefore, IC manufacturers add Process Control Monitoring (PCM) structures on the scribe-line of the wafers.

The S-parameter simulation is performed for the 2nd order Gm-C dual-band IF Band Pass filter for impedance matching of 50 ohms on input and output of the filter. The S-parameters are found by considering the filter structures as two port network.
S-parameters found are input return loss in dB (S_{11}) and forward voltage gain in dB (S_{21}).

The S-parameter simulation of the 2nd order Gm-C dual-band IF Band Pass filter shows that the forward voltage gain (S_{21}) are at maximum (-1.56dB for GSM Band and -

0.71dB for FM Band) at the center frequency of the filters and the losses (S_{11}) are at minimum (-37.23dB for GSM Band and -50.07dB for FM Band) at the center frequency of the filters. The designed filter has tuning ratio 6.6 and suitable for IF channel selection of Wireless System with power consumption 575 μw.

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