DSP BASED CONTROLLER FOR UNITY POWER FACTOR FRONT-END PWM REGENERATIVE CONVERTER

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

(POWER APPARATUS & SYSTEMS)

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CERTIFICATE

This is to certify that the Major Project Report entitled **"DSP Based Controller for Unity Power Factor Front-End PWM Regenerative Converter"** submitted by Mr. **Khanduja Gagandip Singh Narendra Singh (07MEE006)** towards the partial fulfillment of the requirements for the award of degree in **Master of Technology (Electrical Engineering)** in the field of **Power Apparatus & Systems** of **Nirma University of Science and Technology** is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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ABSTRACT

Solid state ac-dc conversion of electric power is widely used in adjustable-speed drives, switch-mode power supplies, uninterrupted power supplies, and utility interface with non conventional energy sources such as solar PV, etc., battery energy storage systems, in process technology such as electroplating, welding units, etc., battery charging for electric vehicles, and power supplies for telecommunication systems, measurement and test equipments. Conventionally, ac-dc converters, which are also called rectifiers, are developed using diodes and thyristors to provide controlled and uncontrolled dc power with unidirectional and bidirectional power flow. They have the demerits of poor power quality in terms of injected current harmonics, caused voltage distortion and poor power factor at input ac mains and slow varying rippled dc output at load end, low efficiency and large size of ac and dc filters. In light of their increased applications, a new breed of rectifiers has been developed using new solid state self commutating devices such as MOSFETs, insulated gate bipolar transistors, gate turn-off thyristors.

The report of major project is based on the performance comparison of single phase diode bridge rectifier and the proposed front-end converter in terms of the Total harmonic distortion (% THD) of the line current, power factor of the system and ability of energy saving of the converter by reverse power flow action. The parameters of the voltage control loop for proposed converter are derived by two methods named Unity Modulus (Magnitude Optimum) Method and Ziegler-Nichols method. The parameters obtained from both the methods are compared by the mathematical model for forward and reverse power flow mode of operation. The model is generated in simulink (MATLAB) and results are obtained for steady state, transient and dynamic conditions. It is observed that the unity power factor is maintained during all the conditions for various loads. Drastic reduction in %THD of input current waveform is obtained in proposed front-end converter with an added advantage of regenerative capability. For comparison of control loops results a programming file is also generated in MATLAB (M-file) and from the same step response and Nyquist plots are obtained for system control loops.

The fabrication of IGBT based gate driver circuit and dead band circuit is performed. The gate driver circuit results are obtained after the fabrication of the PCB. The results are obtained for the normal working condition and also for the fault condition. The obtained results show the required performance of the gate driver circuit and the dead band

circuit. To understand the circuit in proper manner all the components are tested and the results for the same are obtained as per requirement.

The PWM signals for the prototype front-end converter are generated with the help of the MICRO-2407 DSP trainer kit. The results for the generated signal show the PWM signals as per the requirement for the both converters.

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ABBREVIATION

ASD	Adjustable Speed Drives
ADC	Analog to Digital Converter
ARAU	Auxiliary Register Arithmetic Unit
CALU	Central Arithmetic and Logic
CAN	Control Area Network
DAC	Digital to Analog Converter
EV	Event Manager
FFC	Feed Forward Controller
GPIO	General Purpose Input Output
JTAG	Joint Test Action Group
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
SCI	Serial Communication Interface
SMPS	Switched Mode Power Supplies
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supplies
WD	Watch Dog

NOMENCLATURE

K_{cr}	Critical gain of the system
K_i	Current feedback loop gain
K_l	Current loop gain
ζ	Damping ratio
L_s	Input source inductance
G	Maximum peak converter input voltage
P_{cr}	Period of sustained oscillation
K_n, K_p	PI controller gain
T_n, T_i	Time parameter of PI controller
T_r	Triangular carrier period
K_v	Voltage feedback loop gain

CONTENTS

CHAPTER-1

INTRODUCTION

1.1 Introduction and Overview of the Project

There are several conventional methods by which the output dc voltage can be controlled, e.g. a diode bridge with a tap changing transformer or an auto-transformer, as shown in fig.1.1. Although this method is simple but suffers from the demerits due to size, weight and cost of transformer. This type of control scheme was used to control dc voltage hence speed of dc motors used in electric traction of Indian Railways [1].

In case of an ac-to-dc phase controlled switching, the phase controller works as an ordinary contactor switch. For a certain period of time, the switch is closed (on), thus the input supply reaches to load and the output voltage can be obtained. Similarly, for the certain period of time the switch is open (off), thus the input voltage does not reach the load. Thus, instead of the complete input voltage reaching the load, the switch (phase controlled converter) slices the input voltage and only its part reaches the load. In this arrangement no transformer is required. Thus, the size, weight and cost reduce and efficiency is high.

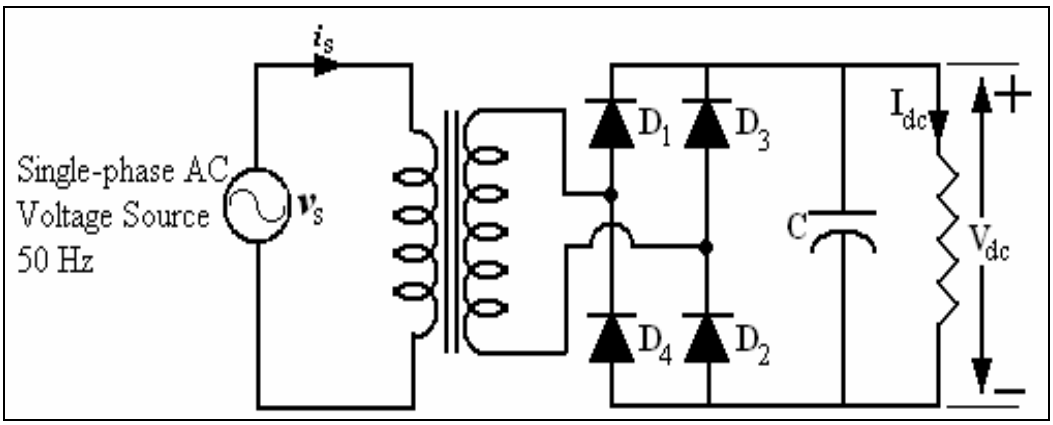

Fig.1.1 Diode bridge type ac-to-dc converter

1.2 Classification of Converters

The converters can be classified according to supply system, devices used in the circuits and as per application. The general classification of ac-to-dc converter is shown in fig.1.2. The simulation of the single phase diode bridge rectifier is performed by considering various parameters according to the parameters of proposed front-end converter. The simulink model, waveforms for dc link voltage, source voltage and line

current and the result for the THD of the line current for diode bridge type ac-to-dc converter are shown in fig.1.3, 1.4 and 1.5 respectively.

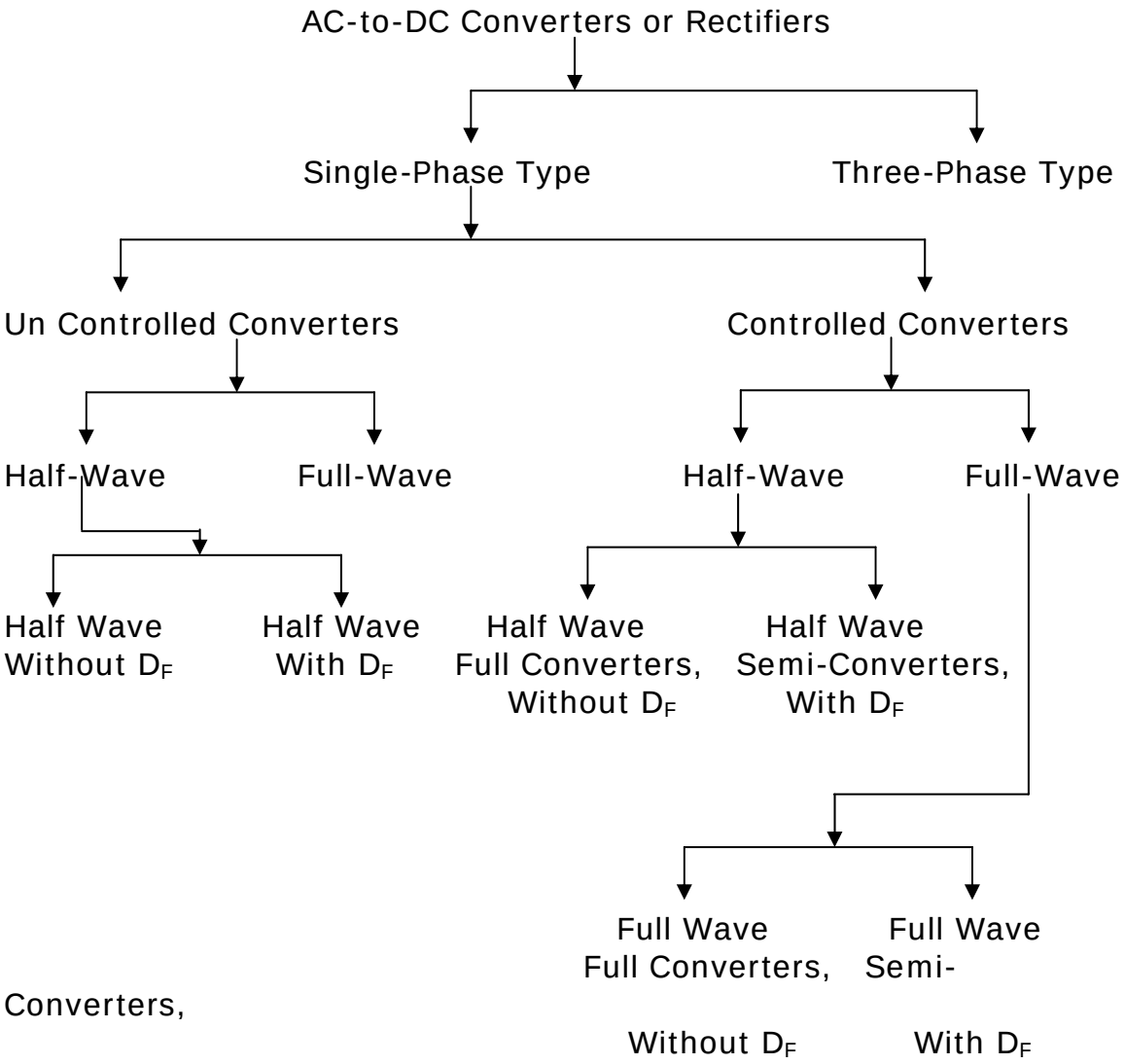

Fig.1.2 Classification of Converters

Specifications of single phase diode bridge rectifier are:

- Input Voltage = 1432 Volts
- Output Voltage = 2000 Volts
- Supply Frequency = 60 Hz
- DC Link Capacitor = 10000 μF
- Load Resistance = 40 Ω

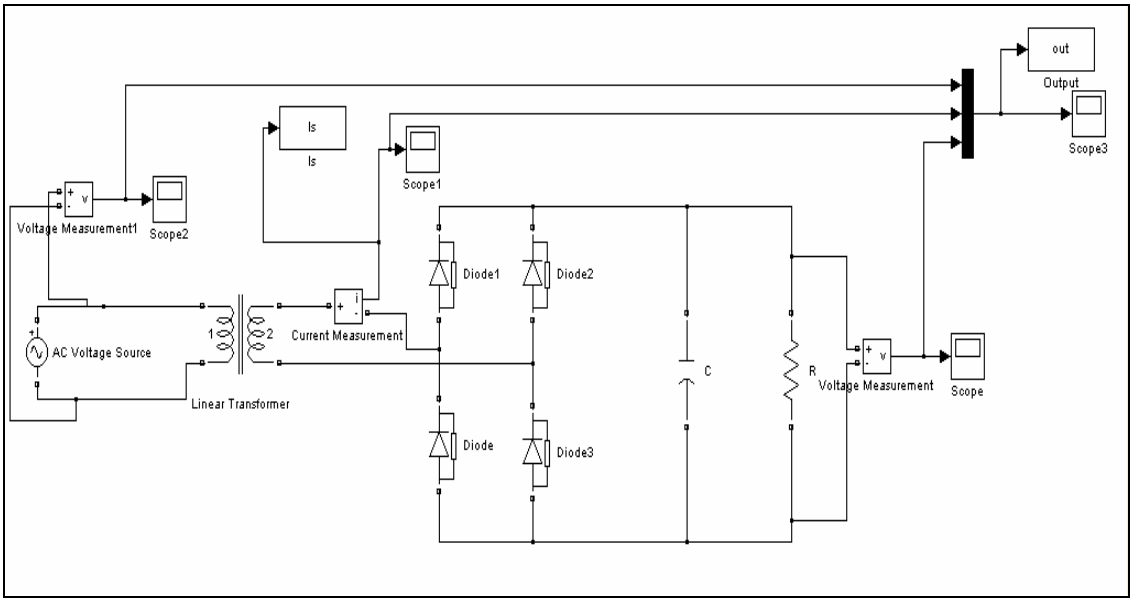

Fig.1.3 Simulink model of diode bridge rectifier

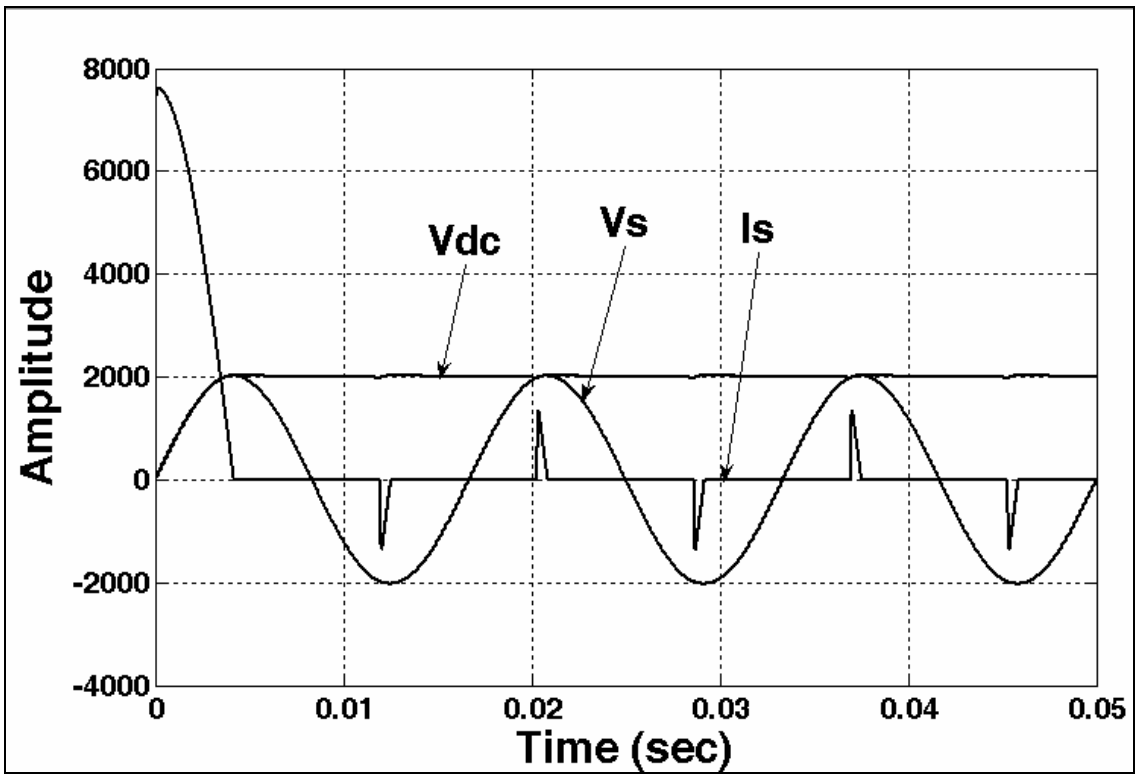

Fig.1.4 Waveforms for V_s, V_{dc} and I_s of single phase diode bridge rectifier
(scale: X-axis:1div. = 0.01 s, Y-axis: 1div. = 2000 V)

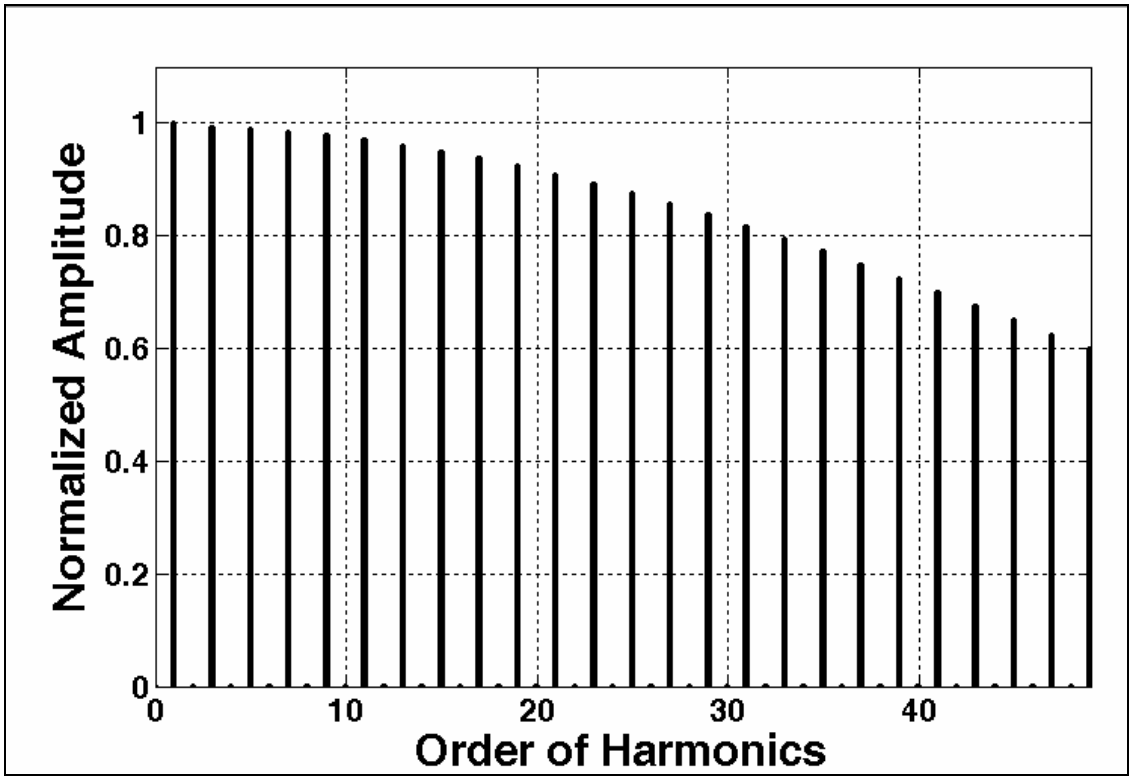

Fig.1.5 Normalized harmonic spectrum of line current for single phase diode bridge rectifier

Calculation of % THD:

$$\%\,THD\ (Up\ to\ 11th\ Order\ ) = \sqrt{\frac{(0.9929)^2 + (0.9897)^2 + (0.985)^2 + (0.9786)^2 + (0.9708)^2 + (0.9614)}{(0.9506)^2 + (0.9383)^2 + (0.9246)^2 + (0.9096)^2 + (0.8934)^2 + (0.8759)}{(1)^2}}$$

$$\%THD\,(Up\,to\,25^{th}\ Order) = 328.50\%$$

1.3 Literature Review

Solid state ac–dc conversion of electric power [2] is widely used in adjustable-speed drives (ASDs), switch-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and utility interface with non conventional energy sources such as solar PV, etc., battery energy storage systems (BESSs), in process technology such as electroplating, welding units, etc., battery charging for electric vehicles, and power supplies for telecommunication systems, measurement and test equipments. Conventionally, ac–dc converters, which are also called rectifiers, are developed using diodes and thyristors to provide controlled and uncontrolled dc power with unidirectional and bidirectional power

flow. They have the demerits of poor power quality in terms of injected current harmonics, caused voltage distortion and poor power factor at input ac mains and slow varying rippled dc output at load end, low efficiency and large size of ac and dc filters. In light of their increased applications, a new breed of rectifiers has been developed using new solid state self commutating devices such as MOSFETs, insulated gate bipolar transistors (IGBTs), gate turn-off thyristors (GTO), etc., even some of which have either not been thought or not possible to be developed earlier using diodes and thyristors. Such pieces of equipment are generally known as converters, but specifically named as switch-mode rectifiers (SMRs), power-factor correctors (PFCs), pulse width-modulation (PWM) rectifiers, multilevel rectifiers, etc. Because of strict requirement of power quality at input ac mains several standards have been developed and are being enforced on the consumers. Because of severity of power quality problems some other options such as passive filters, active filters (AFs), and hybrid filters along with conventional rectifiers, have been extensively developed especially in high power rating and already existing installations. However, these filters are quite costly, heavy, and bulky and have reasonable losses which reduce overall efficiency of the complete system. Even in some cases the rating of converter used in AF is almost close to the rating of the load. Under these observations, it is considered better option to include such converters as an inherent part of the system of ac–dc conversion, which provides reduced size, higher efficiency, and well controlled and regulated dc to provide comfortable and flexible operation of the system.

1. Frank Flinders, Wardina Oghanna

In the paper titled **“Simulation of a complex traction PWM rectifier using Simulink and the dynamic node technique” the authors describes** This paper describes the development of a simulation model for an actual PWM converter system being used in train recently introduced to the Suburban rail transport system in Brisbane, Australia. The simulation model was developed as a teaching aid in modern traction drive technology for railway technical staff. The model is constructed using the SIMULINK graphical simulation platform.

2. Thiyagarajah, K., Ranganathan, V.T., Iyengar, B.S.R.

In the paper titled **"A high switching frequency IGBT PWM rectifier/ inverter system for AC motor drives operating from single phase supply"** authors have explained a PWM rectifier/ inverter system using insulated gate- bipolar-transistors (IBGTs), capable of switching at 20 kHz is reported. The base drive circuit for the IGBT, incorporating short circuit protection is presented. The inverter uses Undeland snubber together with a simple energy recovery circuit, which ensures reliable and efficient operation even for 20 kHz switching. The front-end for the system is a regenerative single phase full-bridge IGBT inverter along with an ac reactor. Steady-state design considerations are explained and control techniques, for unity power factor operation and fast current control of the front-end converter, in a rotating as well as a stationary reference frame, are discussed.

3. P.N. Tekwani, Dhaval Patel

In the paper titled **"Design and Simulation of a PWM Regenerative Front-End Converter"** authors presented the simulation results of a new control scheme for a pulse width modulation (PWM) rectifier which provides unity power factor as well as very low percentage of total harmonic distortion (THD) in ac supply side current. The design considerations for the proposed control scheme and the method of obtaining the PI controller tuning parameters are discussed. For the proposed control scheme, simulation results are obtained for various levels of loading, observing the output dc voltage ripple, unity power factor condition and harmonic content in ac side supply current. Both motoring (forward power flow) as well as regenerative (reverse power flow) mode of operation of the rectifier have been considered.

4. Swami H.

In the paper titled **"Harmonic resistance emulator technique for single phase unity power factor correction"** author suggested a new technique (to be called as Harmonic Resistance Emulator) for single-phase power factor correction using the typical full-bridge active front-end converter is proposed. Unlike conventional single-phase power factor correction circuits, which make use of a single switch boost converter, this technique employs the full bridge converter to be operated in sine-triangle PWM (pulse

width modulation) mode. Two schemes of the proposed technique are discussed. One is the input-current sensor less scheme and the other is input-voltage-sensor less scheme.

5. Deur J., Peric N., stajic D.

In the paper titled **"Design of reduced-order feed forward controller"** authors presented the design of a linear, reduced-order, continuous or discrete-time feed forward controller (FFC) is presented. The FFC is located in the reference value branch of a linear feedback system of any order which is designed according to the damping optimum. The aim of the FFC is to decrease the control system reference response: time, while retaining a low overshoot and a well-damped form of the reference step response. This is achieved by locating the FFC zeros with the aid of the extended magnitude optimum, which is provided in the continuous or discrete-time variant. The influence of a sub optimally designed feedback system with a reduced-order feedback controller on feed forward control is analyzed.

6. Ya-Gang Wang, Hui-He Shao

In the paper titled "**Automatic tuning of optimal PI controllers**" authors explains that the PI controller is unquestionably the most commonly used control algorithm in the process control industry**.** PI controllers have traditionally been tuned empirically, e.g. by the method described in Ziegler and Nichols. This method has the great advantage of requiring very little information about the process. There is, however, a significant disadvantage because the method inherently gives very poor damping. Hang modified Ziegler-Nichols tuning formula, which improve the performance of PI controllers. A method for auto tuning optimal PI controllers is proposed. The PI auto tuner first introduce relay feedback experiments to identify a second-order plus dead time mode1, PI controller is then designed based on the proposed robustness specification and integrated error optimum. Simulation examples show that the proposed PI auto tuner gives satisfactory performance for different types of processes.

7. Hang, C.C. Astrom, K.J. Ho, W.K.

In the paper titled **"Refinements of the Ziegler-Nichols tuning formula"** authors reviewed the accuracy Ziegler-Nichols method in context of PID and PI auto tuning. For PID auto tuning, it will be shown that, for excessive overshoot in the set-point response, set-point weighting can be reduced the overshoot to the specific value, and the original

Ziegler-Nichols tuning formula can be retrained. It will be also shown that set-point weighting is superior to the conventional solution of reducing large overshoot by gain detuning or set-point filtering. However, for excessive set-point under shoot, the tuning formula will have to be modified. For PI tuning it will be shown that the Ziegler-Nichols tuning formula is inadequate and has to be completely revised. The application of set-point weighting and modification of the tuning formula can be based simply on the knowledge of the normalized gain or normalized dead time of the process. These heuristic refinements, when incorporated, will give appreciable improvement in the performance of auto tuners.

CHAPTER-2
PROPOSED FRONT-END CONVERTER

The proposed front-end converter [3] with 8 IGBT structure is shown in fig.2.1. Two single-phase converters are connected in parallel. This is to reduce the harmonic currents in the mains as well as to improve the ripple contents at the dc link. Sine-triangular PWM is used for the control of the converters. Same sine reference waveform is used for both the converters. For each converter, leg-B triangular waveform is 180° phase shifted compared to that of leg-A for the same converter. Resultant converter output voltage for each converter is the subtracted PWM voltage waveform from the two converter legs ($V_{AB} = V_{A0}-V_{B0}$). The outcome of that is fundamental gets added and the harmonics at the carrier frequency and its odd multiple get cancelled. Now the next higher harmonics are at the two times the carrier frequency.

For leg-A of converter-2 triangular wave is phase shifted by 90° compared to that of converter-1 so that harmonic frequencies around the second multiple of carrier wave gets cancelled. This is because harmonics at two times the carrier frequencies will be 180° phase shifted and hence flux produced by these cancel each other at the input transformer secondary side. So harmonic currents of two times the carrier frequency will not flow at the primary side and hence the higher order harmonic present at the primary side will be at the side bands of four times the carrier frequency (i.e., 4 x 11 x 60 Hz = 2640 Hz), with much reduced amplitudes as compared to the fundamental component.

2.1 Design Specification for the Proposed Front-End Converter

- Input Voltage = 1432 Volts
- Output Voltage = 2800 Volts
- Supply Frequency = 50 Hz
- Switching Frequency, fsw = 60*11= 660 Hz
- Rated Power = 1400 Kw
- DC Link Capacitor = 9600 μF

From the above details the detailed specifications can be given as,
Input rms voltage, Vs (rms) = 1432 Volts

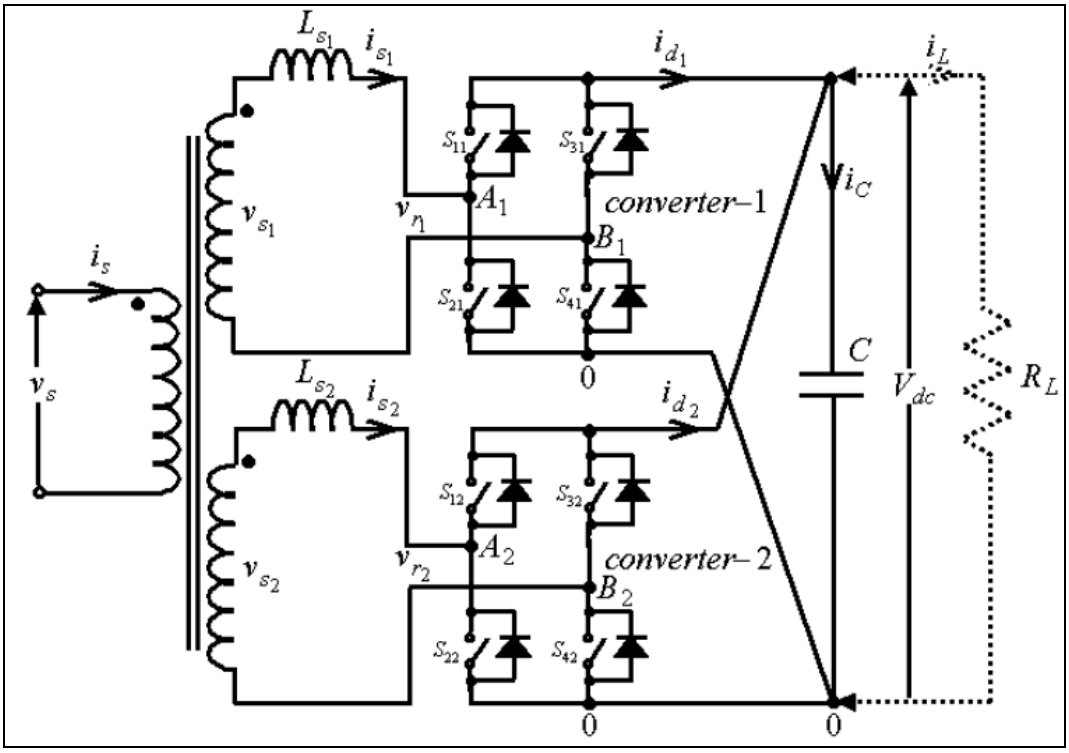

Fig.2.1 Proposed Front-End Converter

$$\text{Input peak Voltage, Vs (peak)} = \sqrt{2} \times Vs\,(rms)$$
$$= \sqrt{2} \times 1432$$
$$= 2025.1538 Volts$$
$$\cong 2025 Volts$$

$$\text{Rated load current, Idc (Max)} = \frac{\text{P}}{\text{Vdc}}$$
$$= \frac{1400 \times 10^3}{2800}$$
$$= 500\,Amp$$

Assuming efficiency of the converter, η = 98 %

$$\text{Rated rms input current, Is (max) rms} = \frac{P}{Vs\,(rms) \times \eta}$$
$$= \frac{1400 \times 10^3}{1432 \times 0.98}$$
$$= 997.61\,Amp$$

$$\text{Rated peak input current, Is (max)}\,pk = \sqrt{2} \times \text{Is (max) rms}$$
$$= \sqrt{2} \times 997.61$$
$$= 1410.83\,Amp$$

Assuming modulation index, m (max) = 0.8,

Maximum peak converter input voltage,

$$Vr(\max)\,pk = m(\max) \times Vdc$$
$$= 0.8 \times 2800$$
$$= 2240\,Volts$$

Maximum rms converter input voltage,

$$Vr(\max)\,rms = \frac{Vr(\max)\,pk}{\sqrt{2}}$$
$$= \frac{2240}{\sqrt{2}}$$
$$= 1583.92\,Volts$$
$$\cong 1584\,Volts$$

Peak-to-peak ripple voltage,

$$\Delta V = 5\%\,of\,Vdc = \frac{5}{100} \times 2800$$
$$= 140\,Volts\,(p-p)$$

2.2 Theoretical Considerations

From the power schematic of proposed front-end converter shown in the fig.2.1, power balance equation at unity power factor is [4],

$$Vs\,Is = Vdc\,Id \tag{2.1}$$

As Id is summation of the current of converter -1 & 2, *equation* (2.1) *can be re – written as*

$$Vs\,Is = Vdc\,(Id1 + Id2) \tag{2.2}$$

$$\therefore Vdc = \frac{Vs\,Is}{Id1 + Id2} \tag{2.3}$$

From equation (2.3) it can observe that the Vdc is proportional to Is i.e. input current should be controlled to control the output voltage.

For the single phase system the voltage equation is,

$$Vs(t) = Ls\frac{di_s(t)}{dt} + Vr(t)$$

$$\therefore \frac{di_s(t)}{dt} = \frac{Vs(t) - Vr(t)}{Ls} \tag{2.4}$$

The input and output power must be balanced for dc link voltage should be remained constant. As shown in fig.2.2 taking three different cases for lagging and unity power factor for forward and reverse flow, it is observed that power flow depends on phase angle displacement between Vs & Vr.

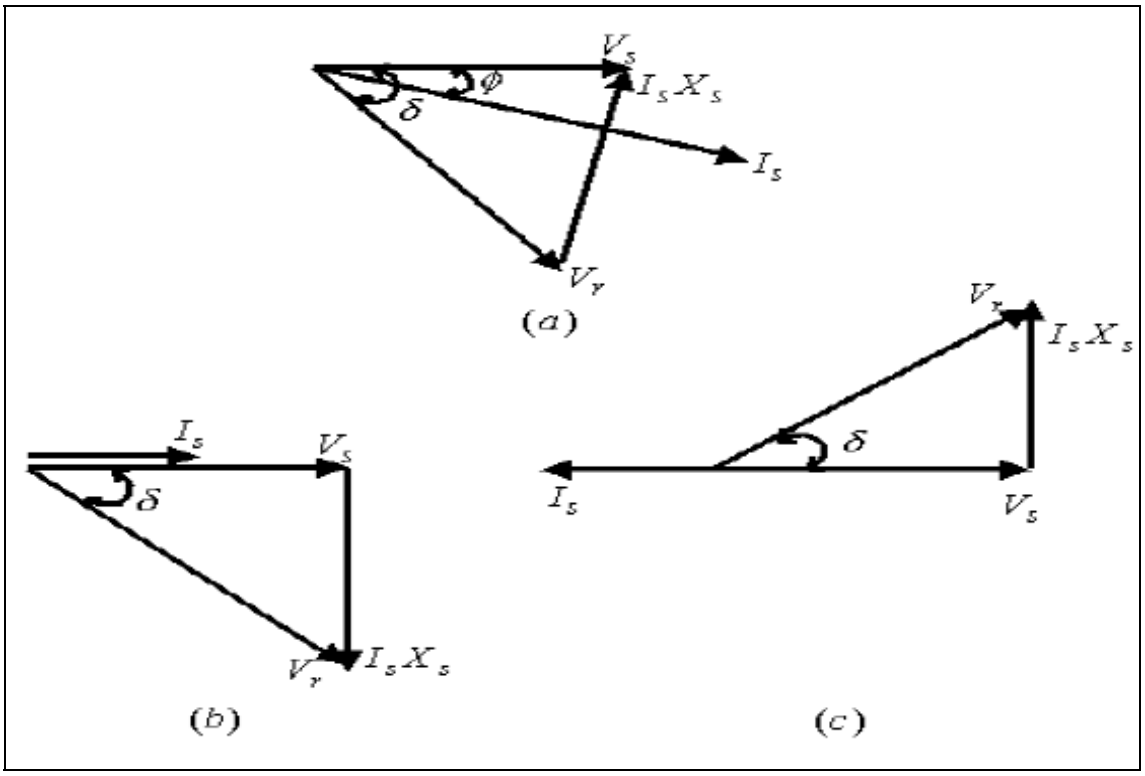

Fig.2.2 Phasor diagram of front-end converter
(a) Lagging PF (b) UPF forward power flow (c) UPF reverse power flow

From the fig. 2.2 (a),

$$Is\cos\Phi=\frac{Vr\sin\delta}{Xs} \tag{2.5}$$

$$Is\sin\Phi=\frac{(Vs-Vr\cos\delta)}{Xs} \tag{2.6}$$

If reactive power drawn by the system is zero, then power factor must be unity. Hence from the equation (2.5) & (2.6),

$$Is\,Xs=Vr\sin\delta \tag{2.7}$$

$$Vs=Vr\cos\delta \tag{2.8}$$

Where,

Vr = RMS value of the fundamental component of voltage generated at the ac terminal of the inverter.

Vs = RMS value of the ac supply voltage.

δ = Phase displacement angle between voltage phasor Vr & Vs.

Φ = Power factor angle.

Squaring the equations (2.7) & (2.8) and adding them,

$$Vr = \sqrt{Vs^2 + (Is\,Xs)^2} \tag{2.9}$$

Under the full load condition,

$$Vr_{fl} = Vs\sqrt{1+\left(\frac{Is\,Xs}{Vs}\right)^2} \tag{2.10}$$

$$Vr_{fl} = Vs\sqrt{1+X^2 p.u.} \tag{2.11}$$

Where

$$Xp.u. = \frac{Is_{fu}\ Xs}{Vs}$$

Equation (2.11) indicates that Vr > Vs by the factor $\sqrt{1+X^2 p.u.}$, which is known as boost factor. So, the range of variation of value of Vr can be given as,

$$Vs \le Vr \le Vs\sqrt{1+X^2 p.u.} \tag{2.12}$$

Value of L_s is selected in such a way that the maximum modulation index at which the inverter operates is as close to one. This is because under this condition V_r varies over a wide range making the control less sensitive to errors in the controller gains, components etc. The minimum value of modulation index m is decided by the fact that the minimum value of V_r is equal to V_s; i.e.

$$m_{\min} = \frac{Vs}{Vdc/\sqrt{2}}$$

$$m_{\min} = \frac{\sqrt{2}\ Vs}{Vdc} \tag{2.13}$$

Value of Ls is selected in such a way that the maximum modulation index at which the inverter operates is as close to one. This is because under this condition Vr varies over a wide range making the control less sensitive to errors in the controller gains, components etc. If a very low value of Ls selected than variation of Vr becomes very sensitive to the above errors.

Input source inductance Ls from equation (2.9) is,

$$
\begin{aligned}
m\,Vdc &= Vr_{pk} \\
&= \sqrt{Vs_{pk}^{\,2} + (Is_{pk}\ Xs)^2} \\
&= \sqrt{Vs^2 + Is_{pk}^{\,2}\,\omega^2 Ls^2} \\
\therefore Ls &= \sqrt{\frac{Vr_{pk}^{\,2} - Vs_{pk}^{\,2}}{Is_{pk}^{\,2}\,\omega^2}} \qquad (2.14)
\end{aligned}
$$

Substituting the various values in equation (2.14) to find the value of Ls,

$$Ls = \sqrt{\frac{(2240)^2 - (2025)^2}{(2 \times \Pi \times 60)^2\,(1410)^2}}$$

$$\therefore Ls = 1.8015\,mH$$

For the analysis of control, converter is modeled as a first order lag. Converter transfer function can be given as; $\frac{G}{1+sTr}$ where, Tr = triangular carrier period = $\frac{1}{11 \times 60} = 1.515 \times 10^{-3}\,ms.$

$$G = mVdc = 2240$$

$$
\begin{aligned}
m = 0.8 (\because m &= \text{modulation index} \\
&= \max i.\,amplitude\,of\ \sin r\ reference / amplitude\,of\ triangular\ carrier \\
&= 1/1.25)
\end{aligned}
$$

$$Vdc = \frac{2240}{0.8} = 2800\ Volts$$

CHAPTER-3
DESIGN OF CONTROL LOOPS

There are two control loops i.e. current control loop and voltage control loop. In the control strategy there is a faster inner current control loop and outer voltage control loop. The output dc voltage is controlled by matching the input power from the converter to the output power demand from the load, while maintaining unity power factor at all the loads. Another technique named Harmonic Resistance Emulator can also be used for the single phase power factor correction [5]. A stationary reference frame model is used for the simulation study, as it involves with only fixed frequency operation. The outer voltage loop is working with DC quantities and the inner current loop is working with sinusoidal quantities. The reference sine wave for the inner current control is derived from the input mains.

While designing the control loops the two methods are used for finding the gain of current control loop and gain and integration time of PI controller in voltage control loop. The cases are taken for the under damped, critically damped and over damped system. The considered methods are:

(1) Unity modulus method

(2) Ziegler- Nichols method

3.1 Current Control Loop Design

If the desired response of current loop is a first order lag of T, then the dynamics of current loop can be described by,

$$T\left(\frac{d\,i_s(t)}{dt}\right)+i_s(t)=\frac{i_s{*}(t)}{ki} \tag{3.1}$$

Where,

T = lag of the converter according to the switching frequency

Ki = current feed back gain

* = Reference value

Equation (15) can be re-written as,

$$\left(\frac{di_s(t)}{dt}\right)=\frac{\frac{i_s*(t)}{ki}-i_s(t)}{T} \tag{3.2}$$

This phase lag can be compensated for by introducing a corresponding phase lead for the current reference, is*(t). In our design it comes out to be arctanωT = arctan (2xπx60x2x1.515X10-3) = 0.85 radian.

Comparing equations (2.4) & (3.2),

$$\frac{Vs(t)-Vr(t)}{Ls}=\frac{\frac{i_s*(t)}{ki}-i_s(t)}{T}$$

$$Vs(t)-Vr^*(t)G=\frac{Ls}{KiT}\left[is^*(t)-is(t)\cdot Ki\right]$$

$$Vr^*(t)=\frac{Vs(t)}{G}-\frac{Ls}{KiGT}\left[is^*(t)-is(t)\cdot Ki\right] \tag{3.3}$$

As inner current loop should be operating faster (i.e., respond to change in i_s (t)), $\frac{Vs(t)}{G}$ should be a feed forward component in the current control loop.

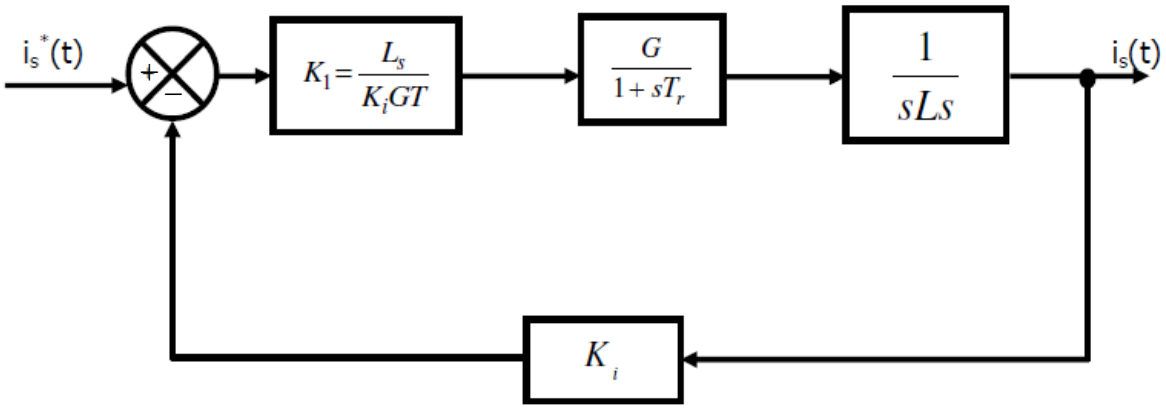

Fig.3.1 Block schematic of current control loop

Fig.3.1 shows the block diagram representation of the current control loop. Current control loop transfer function can be given as:

$$\frac{is}{is^*}=\frac{\frac{1}{Ki}}{S^2\,T\,Tr+S\,T+1} \tag{3.4}$$

$$\frac{is}{is^*} = \frac{\frac{1}{Ki}}{S^2 + \frac{1}{Tr}S + \frac{1}{T\,Tr}} \tag{3.5}$$

The standard form of second order equation is given by,

$$\frac{C(s)}{R(s)} = \frac{\omega n^2}{S^2 + 2\xi\omega n + \omega n^2} \tag{3.6}$$

Comparing equations (3.5) & (3.6),

$$\omega n^2 = \frac{1}{T\,Tr} \tag{3.7}$$

$$2\xi\omega n = \frac{1}{Tr} \tag{3.8}$$

If considered reference current amplitude = 1, then

$$Ki = \frac{1}{Rated\ \ Peak\ Current}$$

$$\therefore Ki = \frac{1}{1410} \tag{3.9}$$

From the above the gain of the current control loop for various cases of the system can be obtained. The equation for finding the same is,

$$K1 = \frac{Ls}{Ki\,G\,T} \tag{3.10}$$

3.2 PI Controller

The PI controller is unquestionably the most commonly used control algorithm in the control industry. In the control strategy of the proposed converter the parameters of the PI controller have been found with the help of traditional Ziegler-Nichols method and Unity Modulus (Magnitude optimum method).

The fig.3.2 shows the model of the PI controller [6] for the proposed converter. The block diagram representation of the same is shown in fig.3.3.

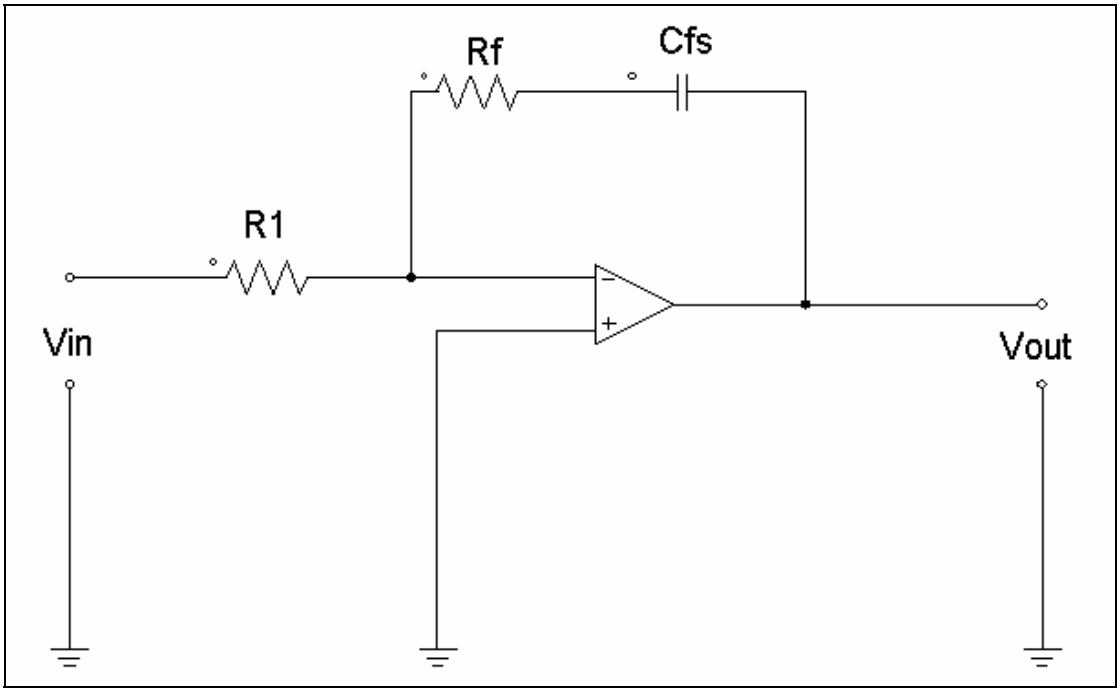

Fig.3.2 PI Controller in S domain

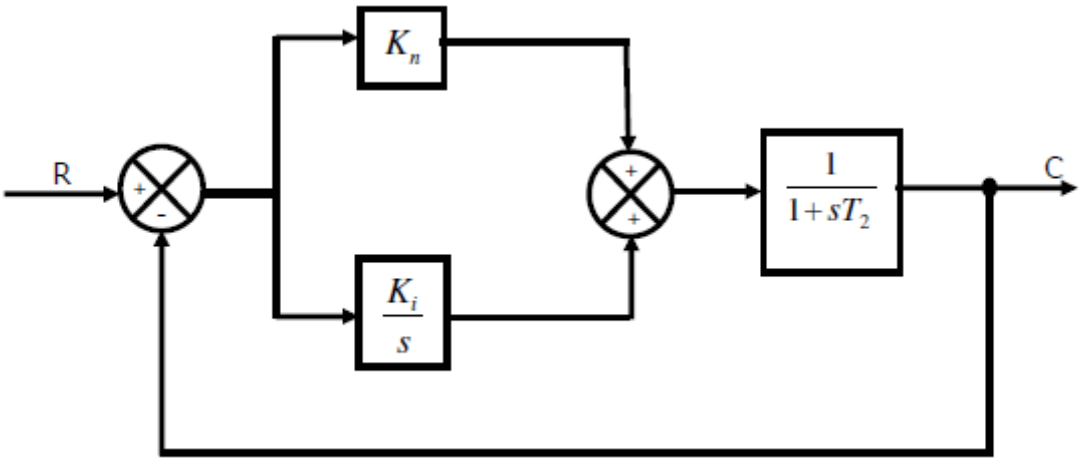

Fig.3.3 Block diagram of PI controller

From the model and block diagram representation, the transfer function for the PI controller can be written as,

$$\frac{Vo(s)}{Vin(s)} = \frac{R_f}{R_1} + \frac{1}{R_1 C_F s}$$

$$= Kn + \frac{1}{Ti\, s}$$

Where,

Kn = Proportional gain = R_f/R_1

Ti = Time constant = $R_1 C_f$

$$\therefore \frac{Vo(s)}{Vin(s)} = Kn\left[1+\frac{1}{Kn\,Ti\,s}\right]$$

$$= Kn\left[1+\frac{1}{\frac{R_f}{R_1}R_1 C_f\, s}\right]$$

$$= Kn\left[1+\frac{1}{R_f C_f\, s}\right]$$

$$= Kn\left[1+\frac{1}{Tn\,s}\right]$$

$$\therefore \frac{Vo(s)}{Vin(s)} = Kn\left[\frac{1+s\,Tn}{s\,Tn}\right]$$

Where, Tn = $R_f C_f$

By adjusting Kn and Tn, the steady state error can be controlled and the output can be obtained accordingly.

3.3 Voltage Control Loop Design

As T is greater then Tr neglecting the term S^2TTr of equation (3.4). So equation (3.4) will become,

$$\frac{is}{is^*} = \frac{\frac{1}{Ki}}{1+sT} \tag{3.11}$$

Also considered the worst case for designing the voltage loop that is load is thrown off. From fig.3.4 the transfer function of the voltage control loop is given by,

$$\frac{Vdc}{Vdc^*} = \frac{\left(\sqrt{2}\,Vs\,Tn\,Kn\right)s+\sqrt{2}\,Vs\,Kn}{\left(Ki\,Tn\,T\,2Vdc\,C\right)S^3+\left(Ki\,Tn\;2Vdc\,C\right)S^2+\left(Kn\,Kv\sqrt{2}Vs\,Tn\right)S+Kn\,Kv\sqrt{2Vs}} \tag{3.12}$$

The solution of the above equation, which is a third order, is given by two methods.

(1) Unity Modulus Method:

The unity modulus method is also known as the magnitude optimum method. The aim of this method is to decrease the rise time of the control system reference step response, while retaining a low overshoot and well-damped form of the reference step response and also retaining its optimal quasia periodic form. In such method it is assumed that all the zeros of the feedback system transfer function is stable and well dumped and therefore be cancelled by the poles [7].

For a general third order transfer function equation, as given below, to get the modulus of the transfer function as unity, to arrive on some conditions.

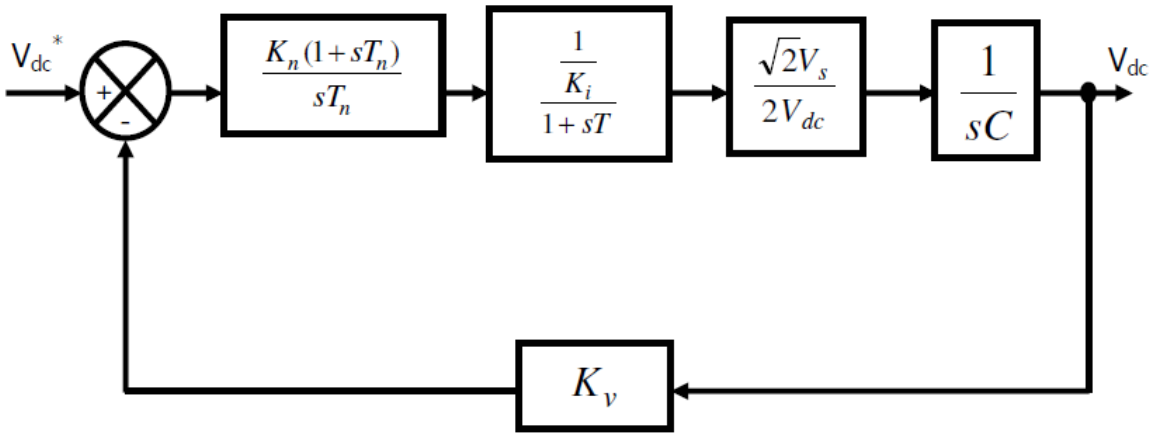

Fig.3.4 Block schematic of Voltage control loop

$$F(j\omega)=\frac{b_0+j\omega b_1}{a_0+j\omega a_1+(j\omega)^2 a_2+(j\omega)^3 a_3} \tag{3.13}$$

For low frequencies following two conditions considered for getting unity modulus of the transfer function.

$$b_0=a_0 \tag{3.14}$$

$$b_1=a_1 \tag{3.15}$$

Equation (27) can be rewritten as,

$$F(j\omega)=\frac{a_0+j\omega a_1}{a_0+j\omega a_1-\omega^2 a_2-j\omega^3 a_3} \tag{3.16}$$

$$\therefore F(j\omega)=\frac{a_0+j\omega a_1}{a_0-\omega^2 a_2+j\omega(a_1-\omega^2 a_3)}$$

$$\therefore |F(j\omega)|=\sqrt{\frac{{a_0}^2+\omega^2 {a_1}^2}{{a_0}^2+\omega^2({a_1}^2-2a_0 a_2)+\omega^4({a_2}^2-2a_1 a_3)+\omega_6 {a_3}^2}} \tag{3.17}$$

So here to satisfy the requirement of unity modulus, from equation (3.17), two more conditions are obtained in addition to equation (3.14) and (3.15). The conditions are:

$${a_1}^2=2a_0 a_2 \tag{3.18}$$

$${a_2}^2=2a_1 a_3 \tag{3.19}$$

Ultimately the following equation is obtained for modulus of transfer function.

$$|F(j\omega)| = \sqrt{\frac{1+\omega^2\left(\frac{a_1}{a_0}\right)^2}{1+\omega^6\left(\frac{a_3}{a_0}\right)^2}} \tag{3.20}$$

Now, from equations (3.12), and (3.19) the relation between the PI controller gain and time parameters for the voltage control loop can be obtained.

$$\left(Kn\ Kv\sqrt{2}\,Vs\ Tn\right)^2 = 2\left(\sqrt{2}\,Vs\ Kn\ Kv\right)\left(2\,Vdc\ Ki\ Tn\ C\right)$$

$$\therefore Kn = \frac{4\,Vdc\ Ki\ C}{\sqrt{2}\ Kv\ Tn\ Vs}$$

$$\therefore Kn = \frac{0.11}{Tn} \tag{3.21}$$

And from equations (3.12), (3.18), and (3.21) the PI controller gain and time parameters for the voltage control loop are calculated.

$$\left(2\,Vdc\ Ki\ Tn\ C\right)^2 = 2\left(2\,Vdc\ Ki\ Tn\ T\ C\right)\left(Kn\ Kv\sqrt{2}\,Vs\ Tn\right)$$

$$\therefore Kn = \frac{0.02746}{T} \tag{3.22}$$

(2) Ziegler-Nichols Method:

PI controllers have traditionally been tuned by Ziegler-Nichols method. The method has great advantage of requiring very little information about the plant or process. There is however, a significant disadvantage because the method inherently gives poor damping [8]-[9].

In Ziegler-Nichols method first it is considered that time for the integration is infinite i.e. Tn = ∞ and Td = 0. Now increase the gain of the controller, Kn from 0 to a critical value, Kcr at which the output first exhibit the sustained oscillation. Thus the value of critical gain and the corresponding period Pcr are approximately determined. Ziegler-Nichols suggested the set of values as shown in table-3.1 [10].

Table 3.1 Ziegler-Nichols rules for tuning the PID controller

Type of controller	**Kn**	**Tn**	**Td**
P	0.5 Kcr	0	0
PI	0.45 Kcr	$\frac{1}{1.2}$ Pcr	0

Now as the K_n and T_n are the parameters of the PI controller of proposed converter, the relationship should be established between values coming from the Ziegler-Nichols method in required form. So a relationship is developed between the both parameters values. As per the rule Ziegler-Nichols method $T_i = \infty$. If $T_i = \infty$ in PI controller than either $R_1 = \infty$ or $C_f = \infty$. But assumption for $R_1 = \infty$ is not proper because if $R_1 = \infty$ then $K_n = 0$, which wrong and hence let us assume that $C_f = \infty$. By this assumption it is observed that $K_n = K_p$.

Now,

$$T_i = R_1 C_f \text{ and } T_n = R_f C_f$$

Taking the ratio of the both parameters,

$$T_n = K_n T_i$$

Which is the relationship between the integration time as per requirement.

By applying such method the voltage block of the fig. 3.4 reduced as shown in fig.3.5.

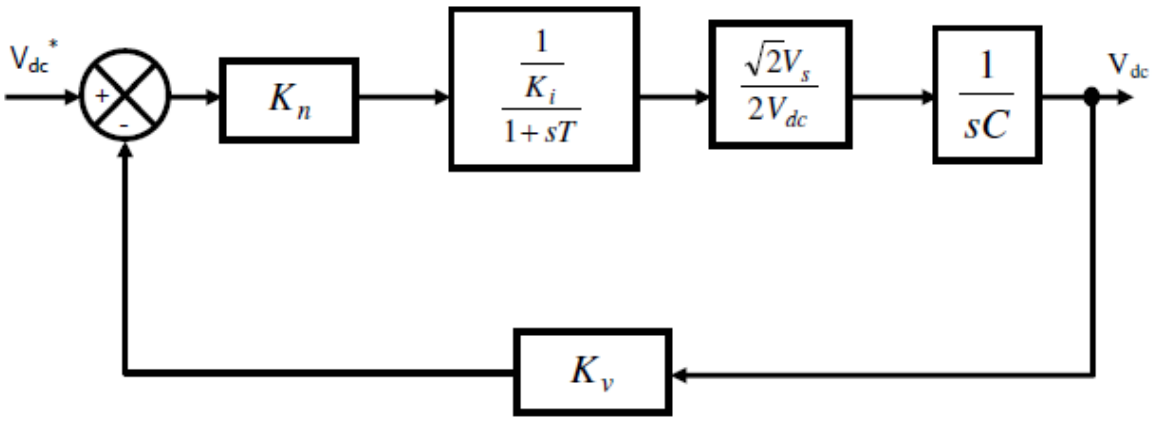

Fig.3.5 Block schematic of Voltage control loop from Ziegler-Nichols Method

The solution of the voltage control loop in the form of transfer function is given as,

$$\frac{Vdc}{Vdc^*} = \frac{\sqrt{2} Vs\, Kn}{(2Vdc\, Ki\, C\, T)S^2 + (2Vdc\, C\, Ki)S + \sqrt{2}\, Vs\, Kn\, Kv} \tag{3.23}$$

Substituting values of known parameters in above equation,

$$0.3972\, T\, S^2 + 0.3972\, S + 0.7233\, Kn = 0 \tag{3.24}$$

Compare equation (3.24) with standard characteristic equation.

From the equation (3.24) the critical gain of the system can be found. The gain of the voltage control loop can found as per rules of table-3.1. To find the integration time Tn, the following equation should be used,

$$Tn = \frac{1}{1.2} Pcr$$

$$\therefore Tn = \frac{1}{1.2}\left(\frac{2\Pi}{\omega_n}\right) \tag{3.25}$$

Taking the various values of the damping ratio, § and accordingly find the various parameters for current and voltage control loop from equations (3.7), (3.8), (3.10), (3.23), (3.24) & (3.25). The results obtained for the different values of damping ratio and different values of parameters from both methods are tabulated in table-3.2.

Table 3.2 Comparison of PI controller parameters for voltage control Loop

Type Of the System	**Values of PI Controller Parameters**			
	Unity Modulus Method		**Ziegler-Nichols Method**	
	K_n	**T_n**	**K_n**	**T_n**
Under Damped System (ζ = 0.707)	9.06	0.01214	4.08	0.0914
Critically Damped System (ζ = 1)	4.5307	0.02428	1.1989	0.0647
Over Damped System (ζ = 1.2)	3.1463	0.03496	0.4917	0.0539

In proposed converter the value of capacitor is taken as 9600 μF ≈ 10000 μF. Value of the capacitor can be calculated as shown below:

From the power balance equation,

$$V_r(t) i_s(t) = V_{dc} I_d$$

$$\therefore I_d = \frac{V_r(t) i_s(t)}{V_{dc}}$$

$$\therefore I_d = \frac{V_r \sin(\omega t - \delta) i_s \sin(\omega t)}{V_{dc}}$$

$$\therefore I_d = \frac{V_r i_s}{2V_{dc}}\left[\cos\delta - \cos(\omega t - \delta)\right] \tag{3.26}$$

The equation (3.26) has a dc component and a fluctuating component. This second harmonic current should pass through the filter capacitor such that the voltage ripple ΔV should be 5 % of V_{dc}. Hence,

$$\Delta V \geq \frac{Vr\ Is}{2Vdc\,2\,\omega C}$$

$$\therefore C \geq \frac{Vr\ Is}{4\times 2\pi f\times Vdc\,\Delta V}$$

$$\geq \frac{m\,Vdc\ Is}{4\times 2\pi f\times Vdc\,\Delta V}$$

$$\geq \frac{m\ Is}{4\times 2\pi f\times \Delta V}$$

$$\geq \frac{0.81410}{4\times 2\pi\times 60\times 140}$$

C is taken as = 10000 μF

Fig. 3.6 shows the block schematic of voltage regulation scheme with current control in stationary co-ordinates.

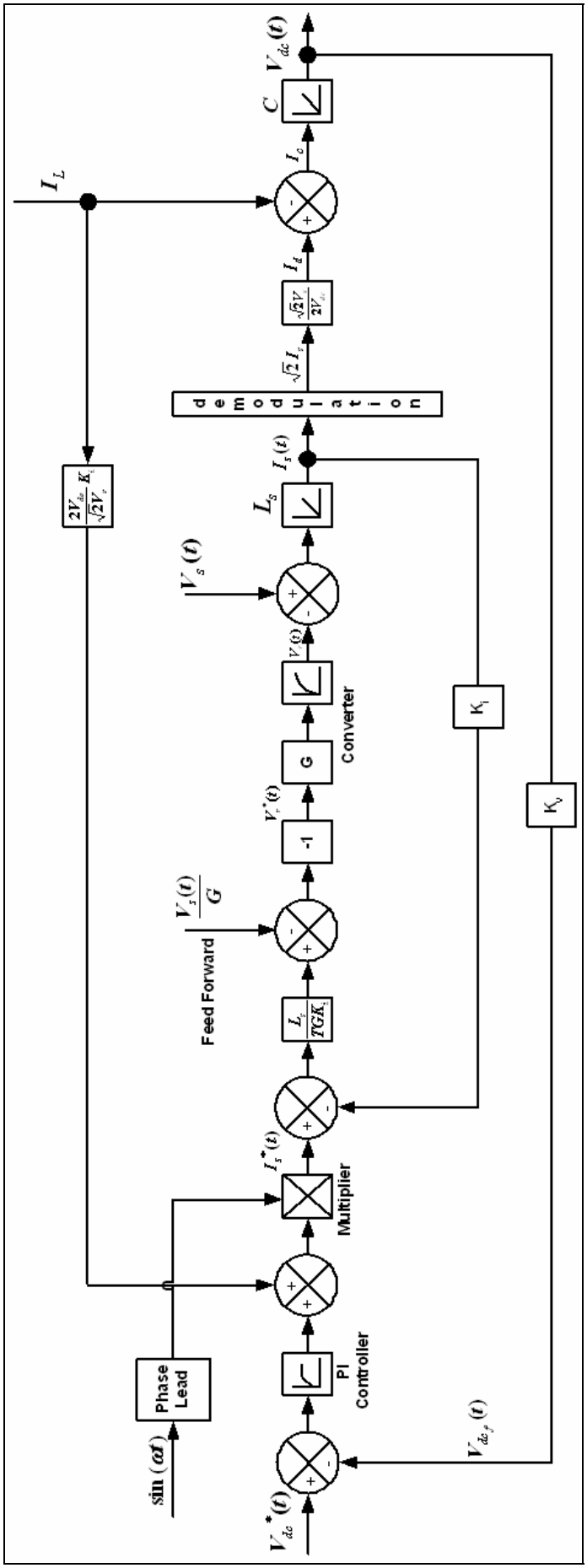

Fig.3.6 Block schematic of voltage regulation scheme with current control in stationary co-ordinates

CHAPTER-4
SIMULATION AND MATLAB PROGRAMMING RESULTS OF PROPOSED CONVERTER

The simulation for the proposed front-end converter is performed by using mathematical model in Matlab Simulink. The results are obtained with the help of both the methods i.e. Unity Modulus (Magnitude Optimum) method and Ziegler-Nichols method under transient and dynamic conditions considering under damped, critically damped and over damped system. The simulation results are obtained for motoring (forward) mode of operation, regenerative (reverse) mode and under the fault condition. The

4.1 Simulation Results for PWM Switching

The proposed front-end converter mathematical model of simulation and PWM switching waveforms for one converter and for both the converters are shown in fig. 4.1, 4.2 and 4.3 respectively. Sine-triangular PWM is used for the control of the converters. Same sine reference waveform is used for both the converters. For each converter, leg-B triangular waveform is 180° phase shifted compared to that of leg-A for the same converter. For leg-A of converter-2 triangular wave is phase shifted by 90° compared to that of converter-1 so that harmonic frequencies around the second multiple of carrier wave gets cancelled.

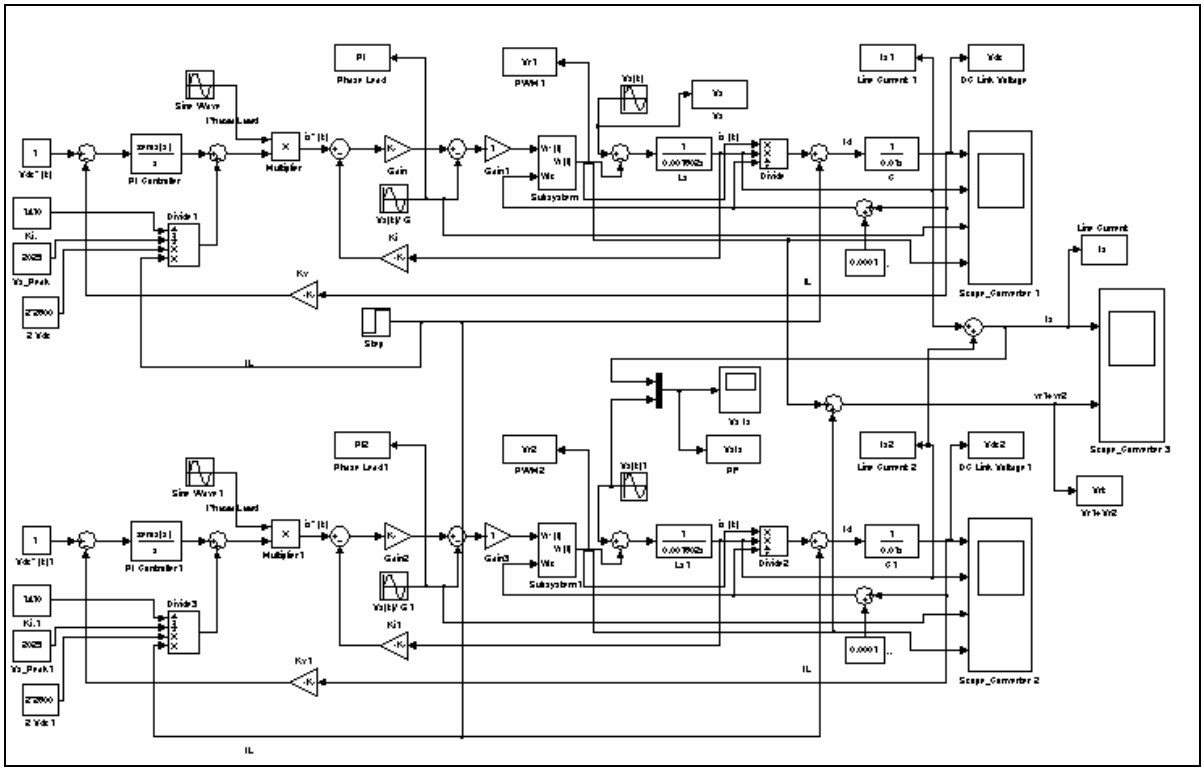

Fig.4.1 Simulation blocks of mathematical model for front-end converter

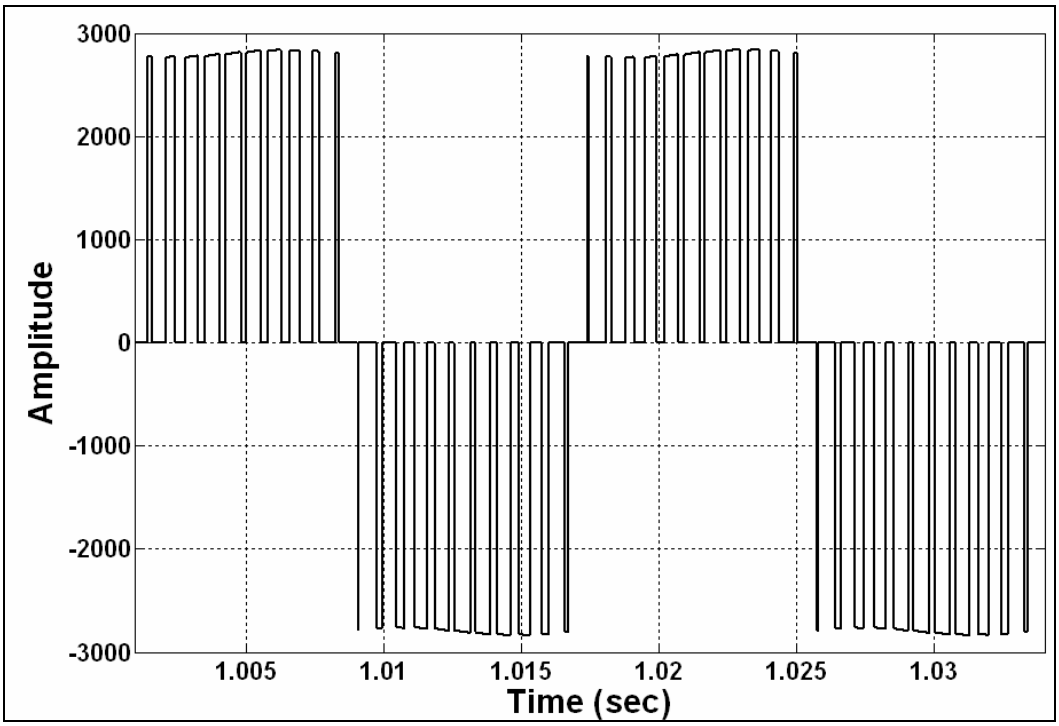

Fig.4.2 Voltage waveform $V_{A1B1}= V_{A10}-V_{B10}$ (i.e. V_{rl})

(scale: X-axis:1div. = 0.005 s, Y-axis: 1div. = 1000 V)

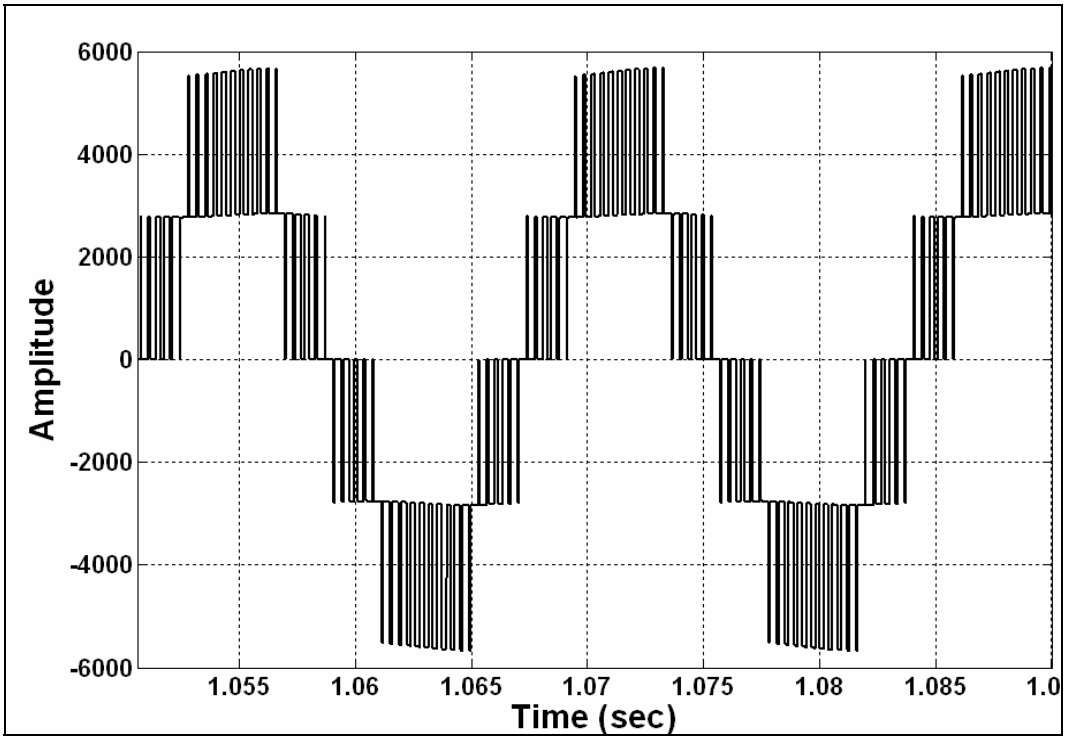

Fig.4.3 Voltage waveform $V_{AB}= V_{A1B1}+V_{A2B2}$ (i.e. V_r)
(scale: X-axis:1div. = 0.005 s, Y-axis: 1div. = 2000 V)

4.2 Simulation Results for Transient Condition

The simulation results are obtained for the transient condition for motoring and regenerative mode of operation as shown in fig. 4.4 to fig. 4.11. It can be observed that during the motoring and regenerative operation the unity power factor is maintained for under damped, critically damped and over damped system. The results obtained from both the methods are shown below.

A) Unity Modulus Method:

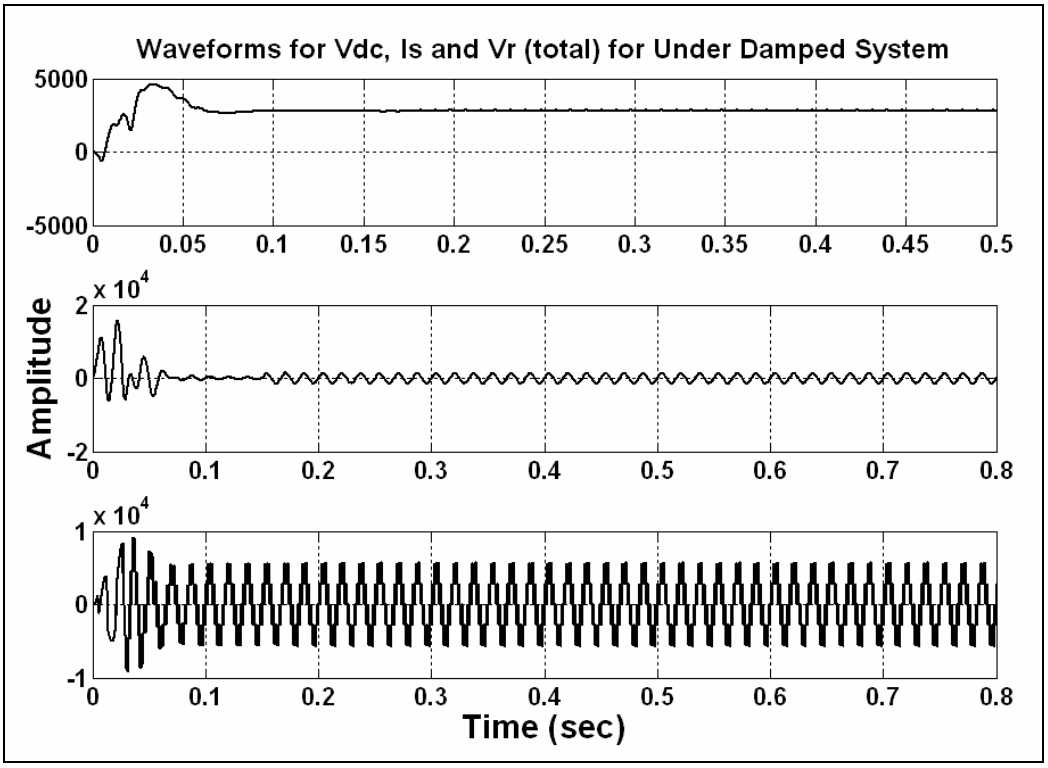

Fig.4.4 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for under damped system (Unity Modulus method)

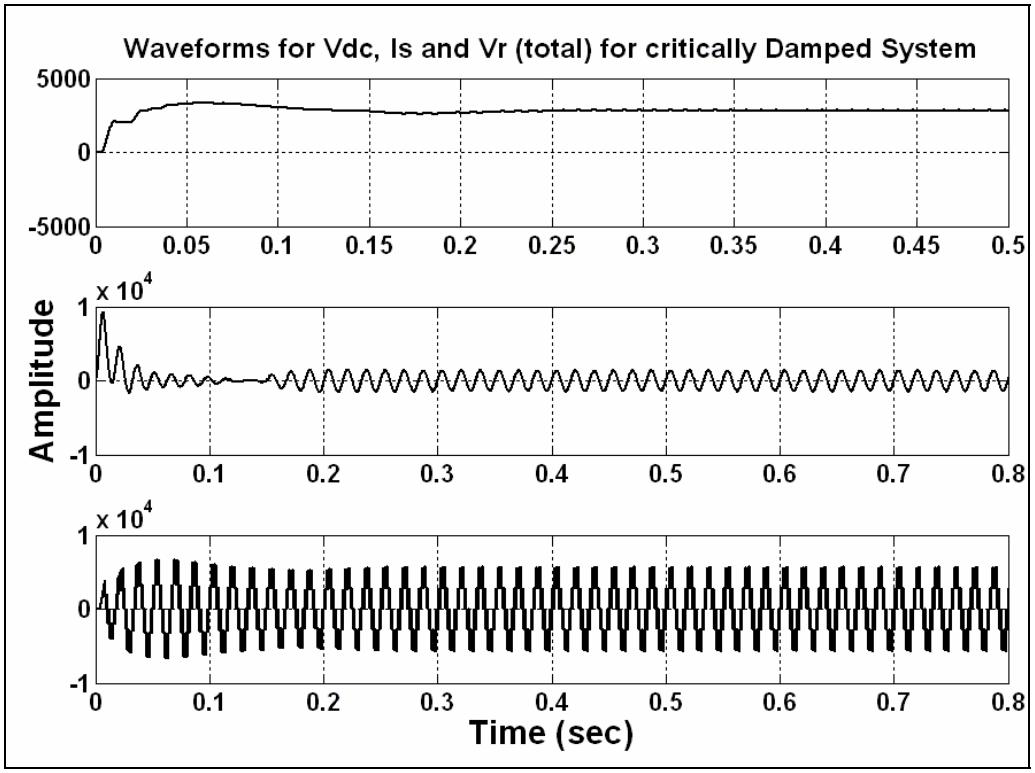

Fig.4.5 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for critically damped system (Unity Modulus method)

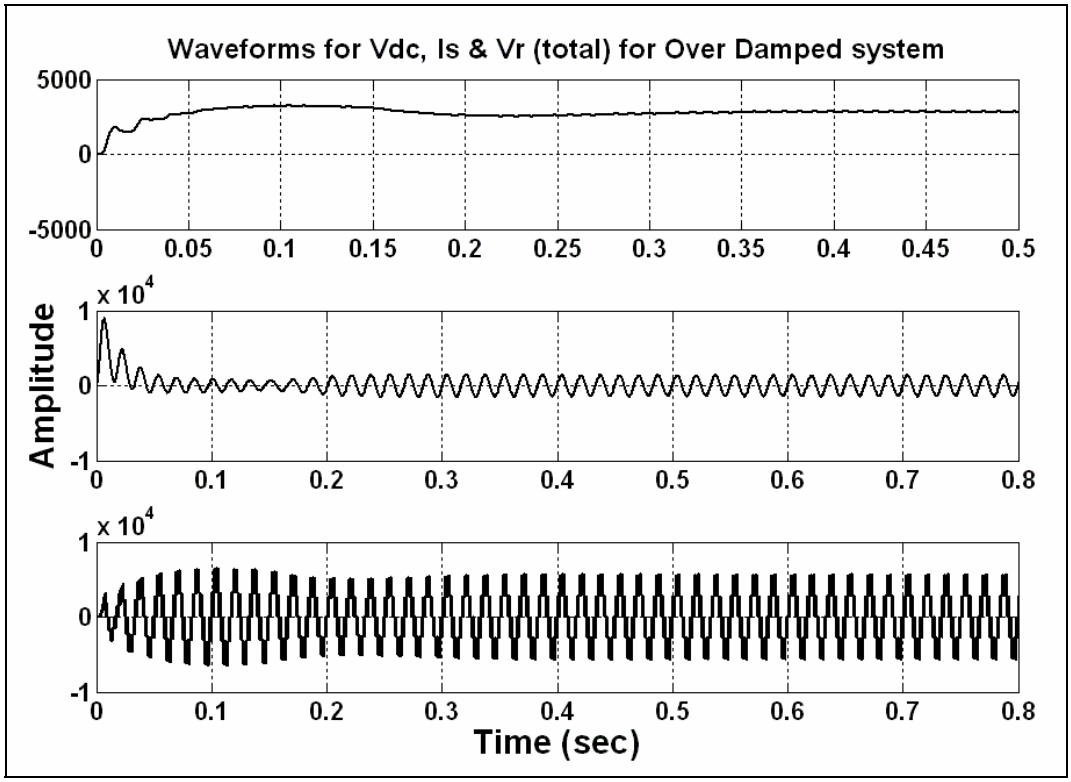

Fig.4.6 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for over damped system (Unity Modulus method)

B) Zeigler-Nichols Method:

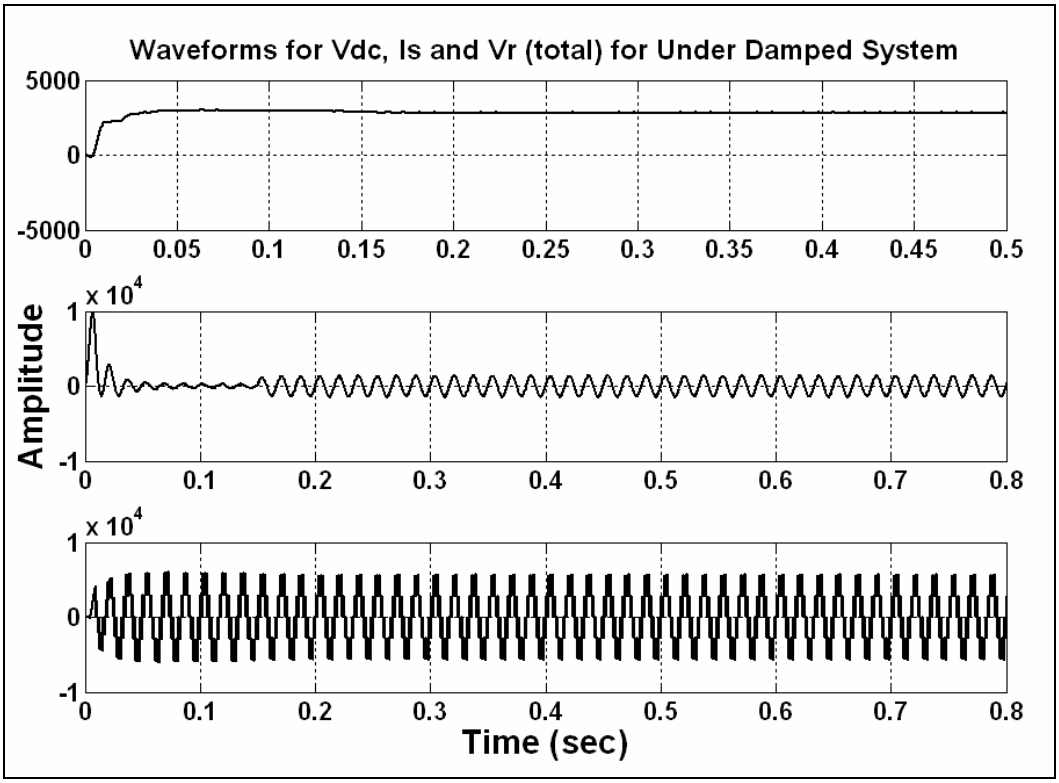

Fig. 4.7 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for under damped system (Ziegler-Nichols method)

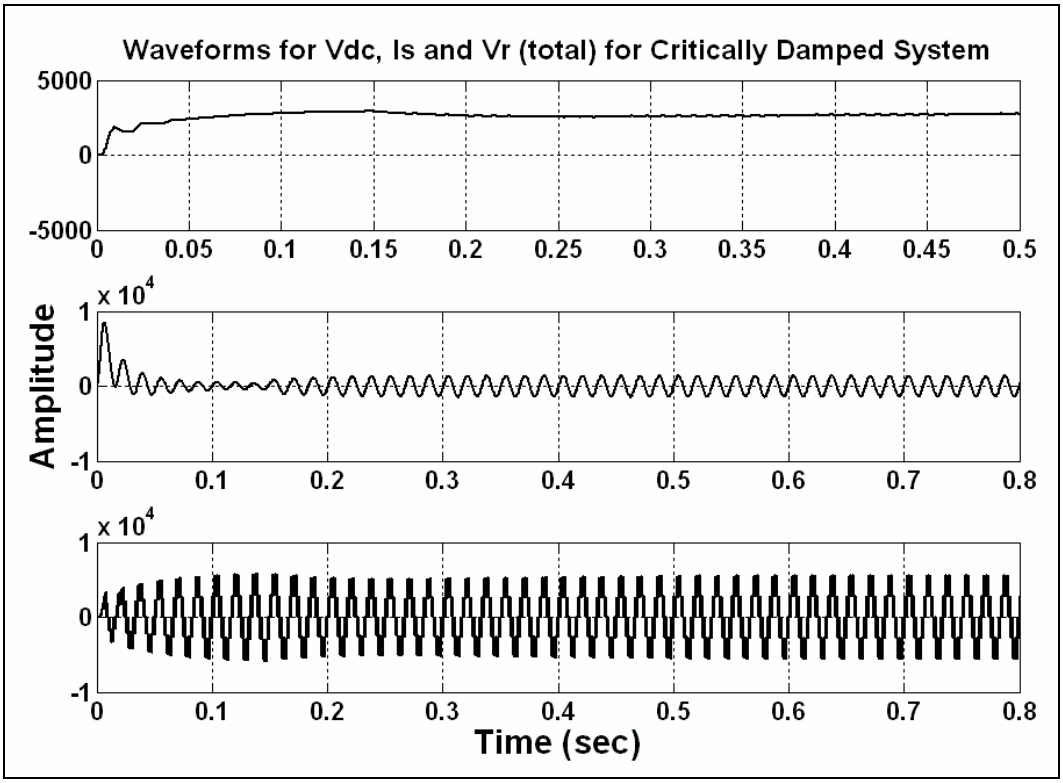

Fig. 4.8 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for critically damped system (Ziegler-Nichols method)

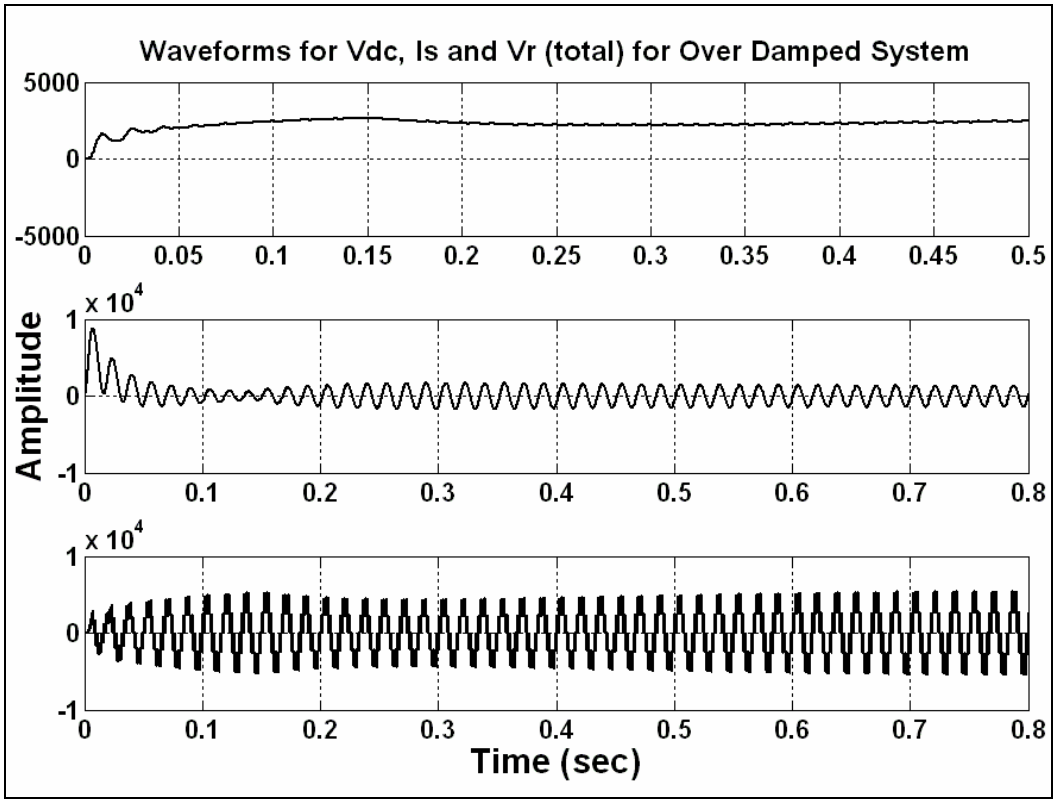

Fig. 4.9 V_{dc}, I_s & V_r (total) waveforms of the proposed converter for over damped system (Ziegler-Nichols method)

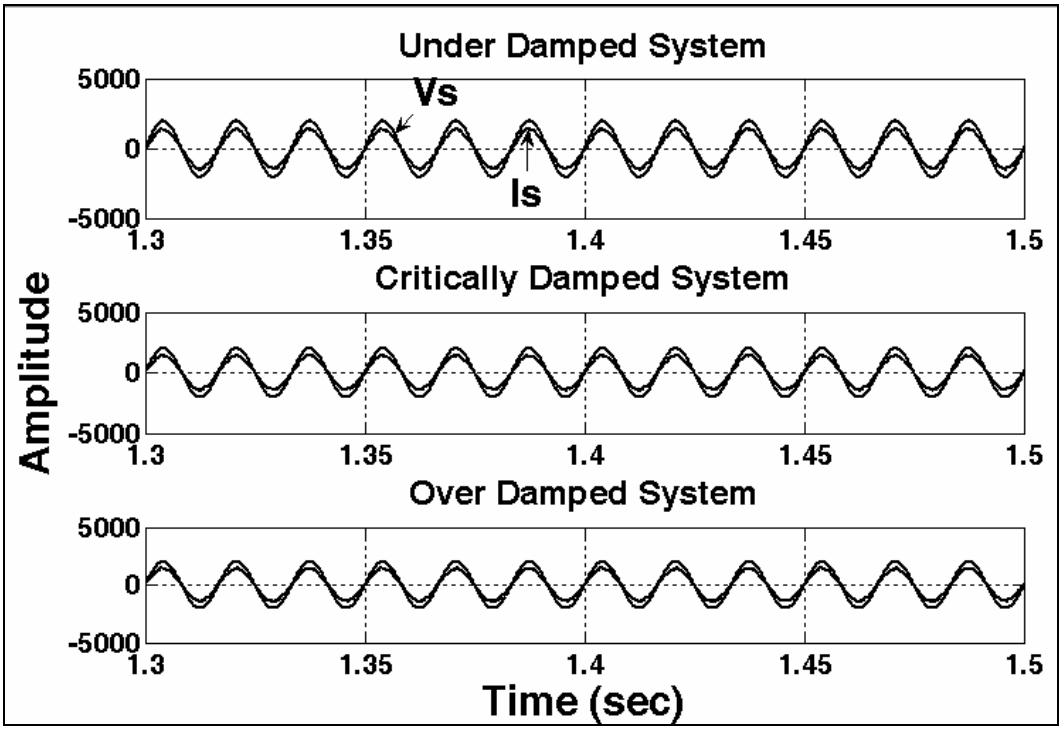

Fig.4.10 V_s and I_s waveforms under motoring mode of operation

(scale: X-axis:1div. = 0.05 s, Y-axis: 1div. = 5000 V)

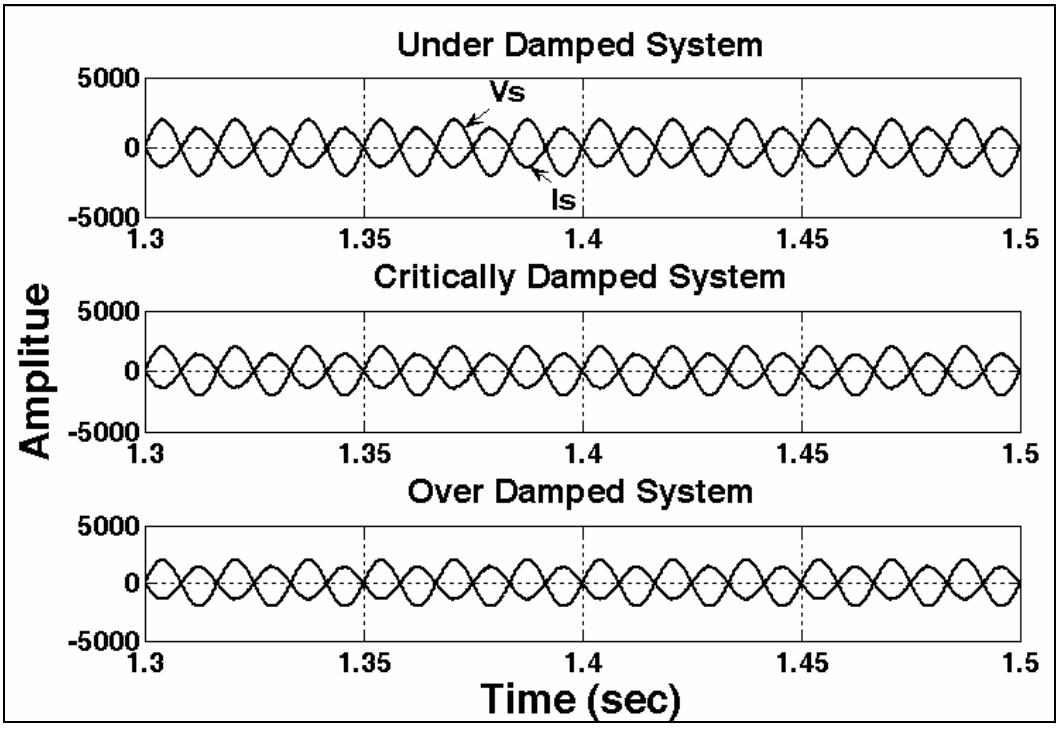

Fig.4.11 V_s and I_s waveforms under regenerative mode of operation

(scale: X-axis:1div. = 0.05 s, Y-axis: 1div. = 5000 V)

4.3 Simulation Results for Dynamic Condition

The simulation results are obtained for the dynamic condition having under damped, critically damped and over damped conditions. The results are compared for the Ziegler-Nichols and Unity Modulus method. The obtained results are shown in fig. 4.12 to fig.4.15. From the comparison it is quite evident that under the dynamic condition the stability of dc link voltage from Unity Modulus method is better than the Ziegler-Nichols method.

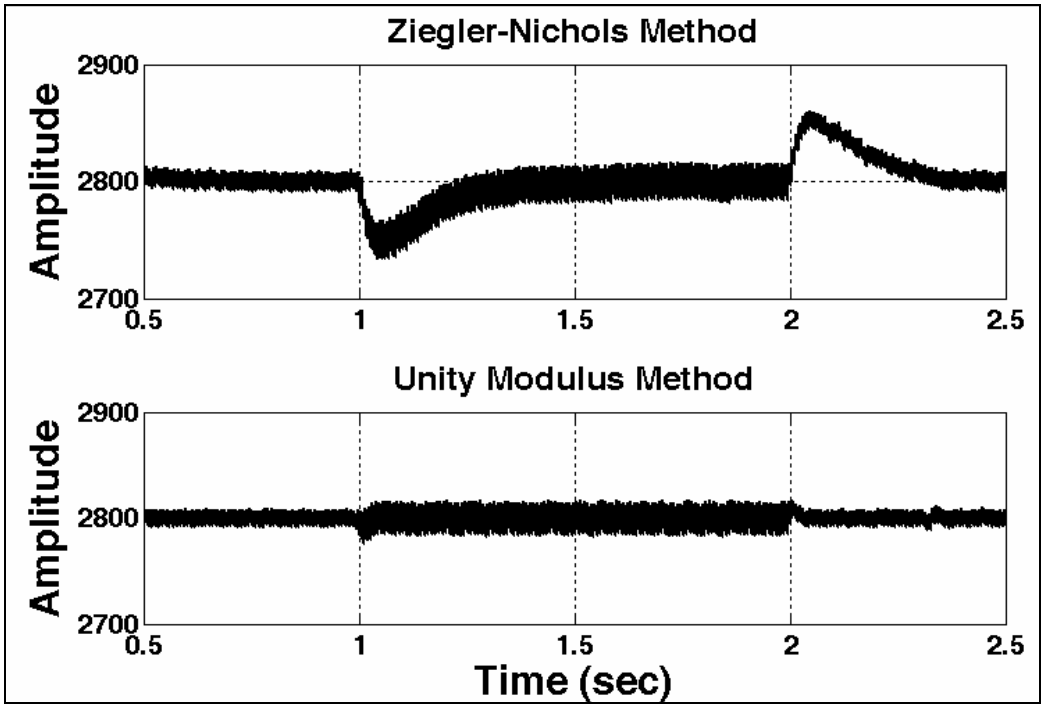

Fig.4.12 Waveforms of dc link voltage for under damped system

(scale: X-axis:1div. = 0.5 s, Y-axis: 1div. = 100 V)

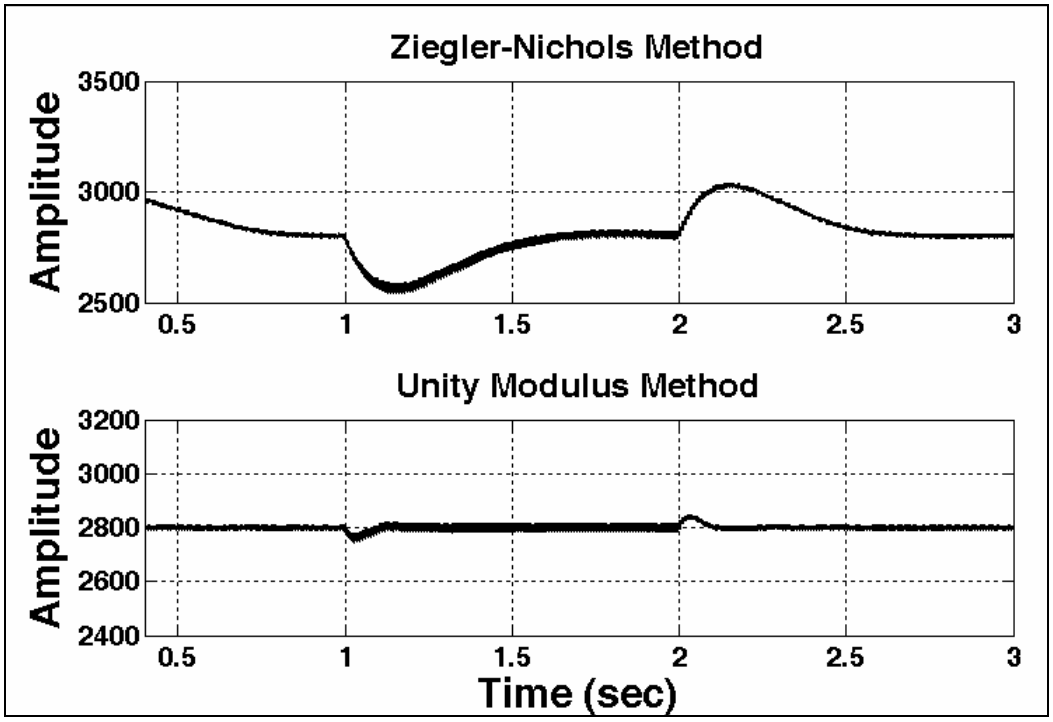

Fig.4.13 Waveforms of dc link voltage for critically damped system
(scale: X-axis:1div. = 0.5 s, Y-axis: 1div. = 200 V)

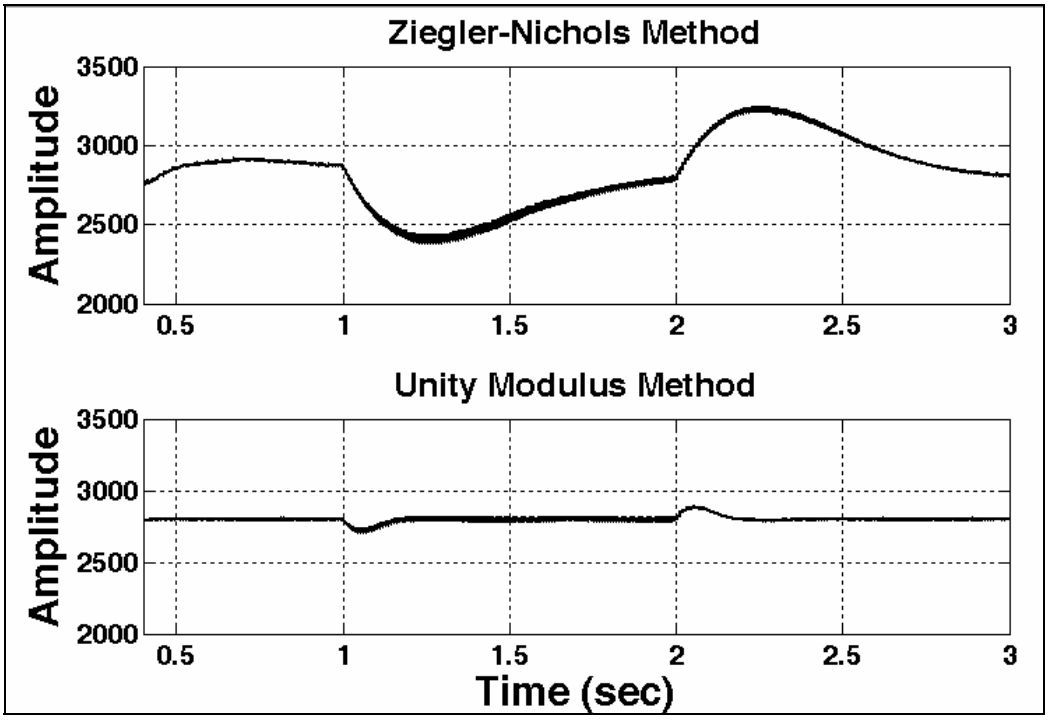

Fig.4.14 Waveforms of dc link voltage for over damped system

(scale: X-axis:1div. = 0.5 s, Y-axis: 1div. = 500 V)

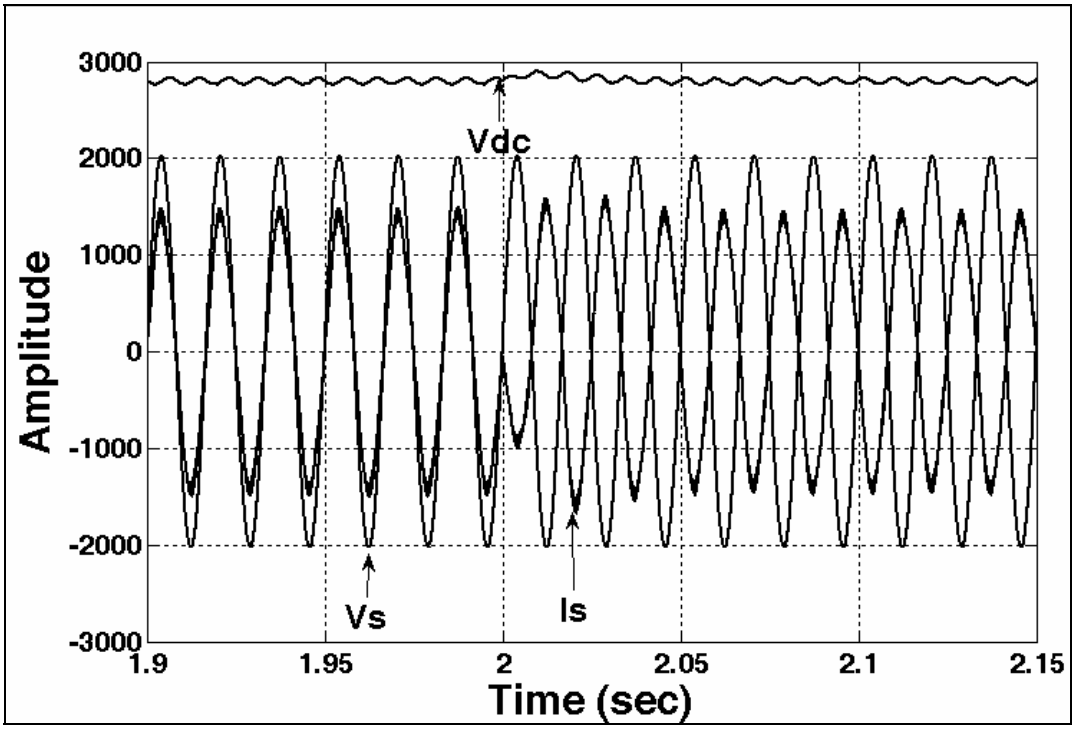

Fig.4.15 V_{dc}, V_s and I_s waveforms for under motoring to regenerative mode of operation
(scale: X-axis:1div.= 0.05 s, Y-axis: 1div. = 1000 V)

4.4 Simulation Results for Transition Mode of Operation

The simulation results for proposed front-end converter for the transition mode of operation i.e. motoring to regenerative and vice-versa under transient condition are obtained form both the methods i.e. Zeigler-Nichols method and Unity Modulus method. The obtained results are shown in fig. 4.16 to 4.19. The results are indicating that the unity power factor is maintained during all the conditions for motoring mode of operation and the results of the Unity Modulus method are better than the Ziegler-Nichols method.

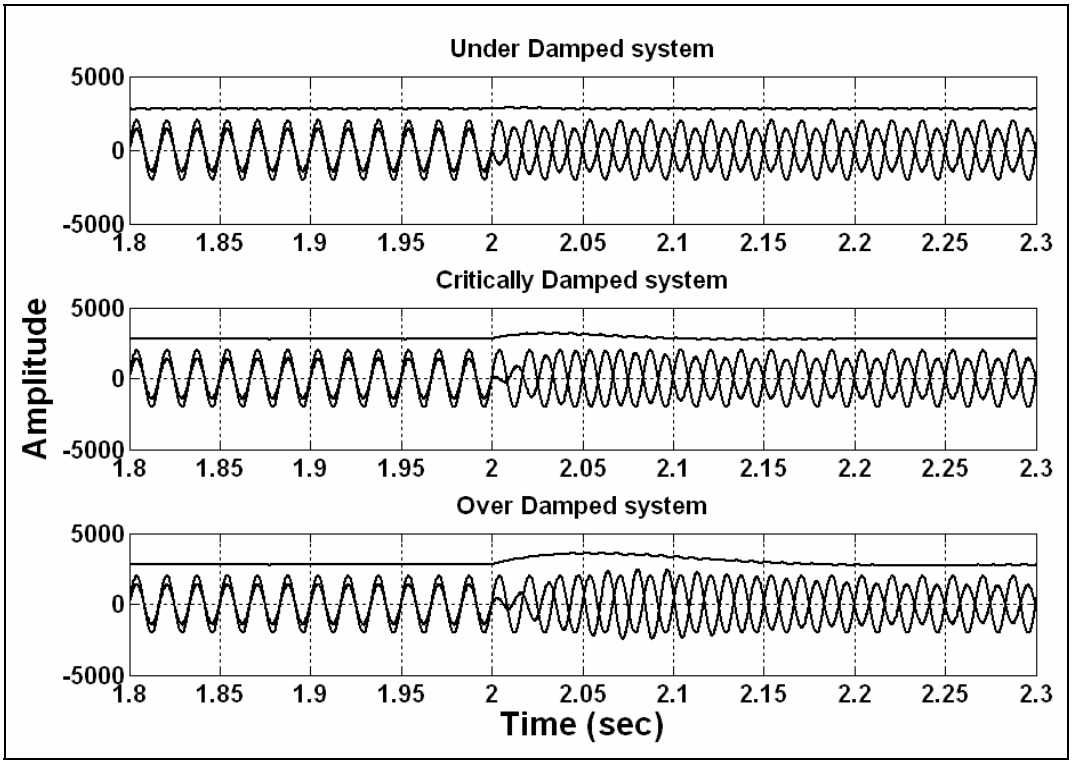

Fig. 4.16 Vdc, Vs and Is waveforms for transition from motoring to regenerative mode of operation (Unity Modulus Method) (scale: X-axis:1div. = 0.05 s, Y-axis: 1div. = 5000 V)

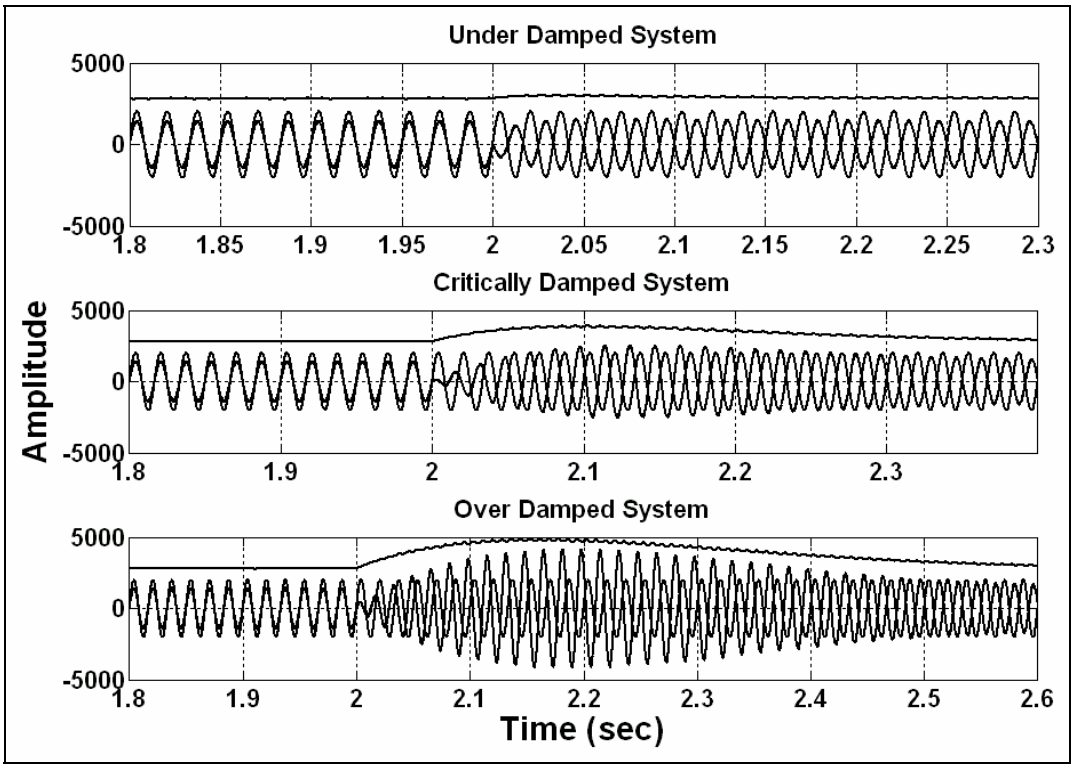

Fig. 4.17 Vdc, Vs and Is waveforms for transition from motoring to regenerative mode of operation (Zeigler-Nichols Method) (scale: X-axis:1div. = 0.1 s, Y-axis: 1div. = 5000 V)

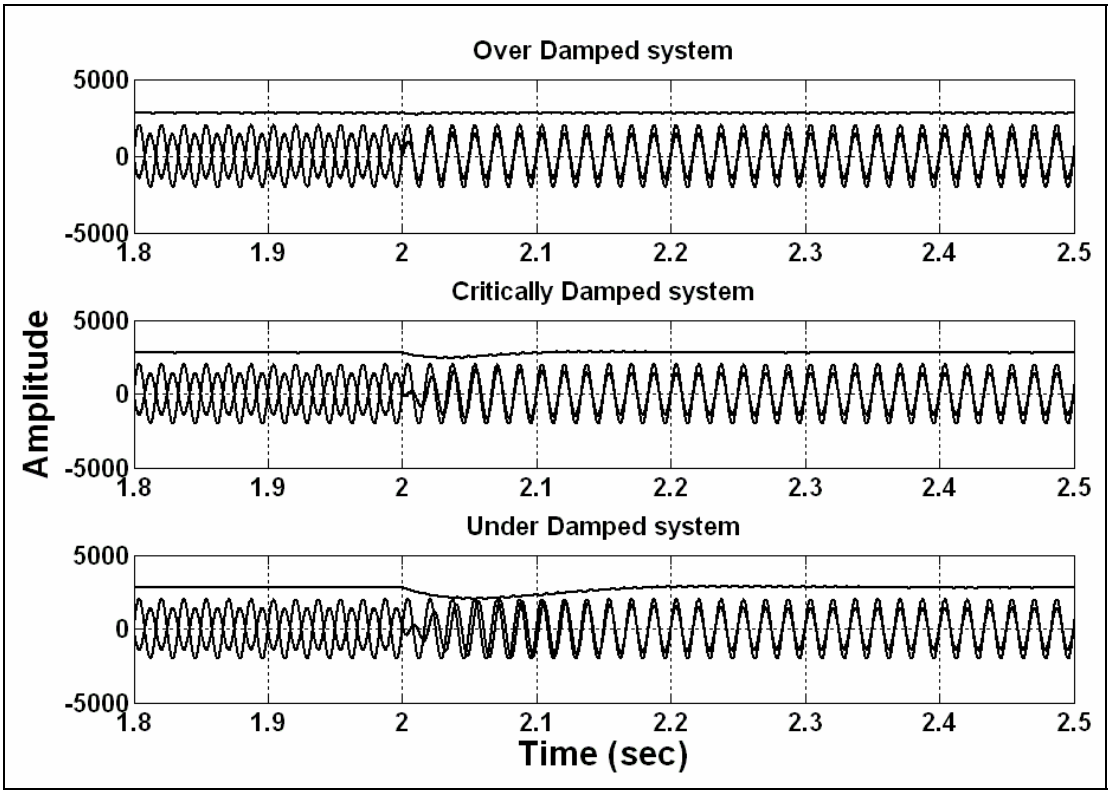

Fig. 4.18 Vdc, Vs and Is waveforms for transition from regenerative to motoring mode of operation (Unity Modulus Method) (scale: X-axis:1div. = 0.1s, Y-axis: 1div. = 5000 V)

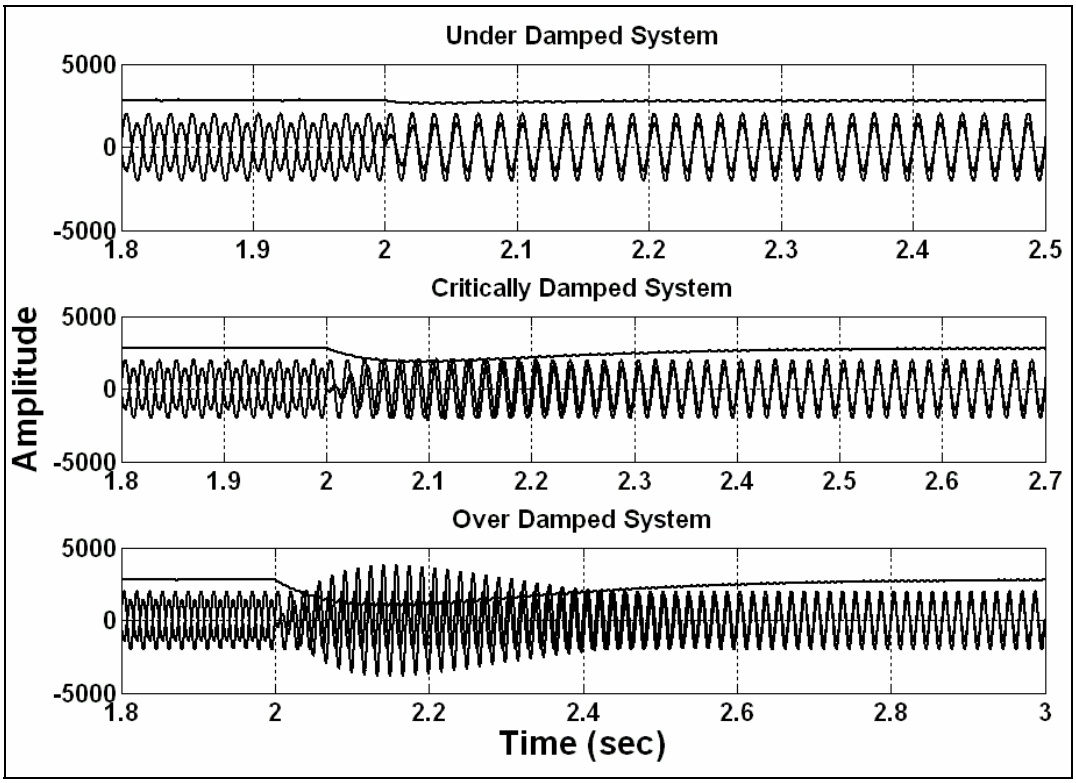

Fig. 4.19 Vdc, Vs and Is waveforms for transition from regenerative to motoring mode of operation (Zeigler-Nichols Method) (scale: X-axis:1div. = 0.1s, Y-axis: 1div. = 5000 V)

4.5 Simulation Results for Different Load Conditions

The simulation results are obtained for the different load conditions for the proposed front-end converter. The simulation results are obtained for both the methods i.e. Unity Modulus are Ziegler-Nichols, here only results from Unity Modulus method is shown, as from the above results it is evident that the results from the unity modulus method is much better and stable then the Ziegler-Nichols method. The results for the same are shown in fig. 4.20 to 4.23.

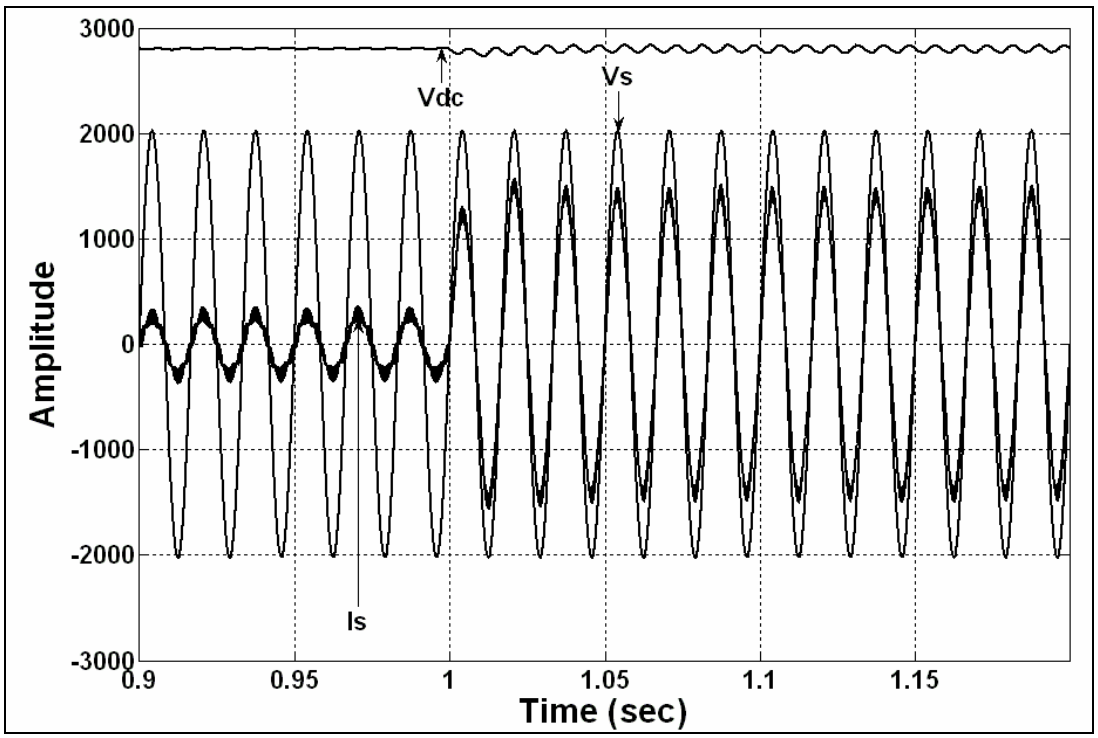

Fig. 4.20 V_{dc}, V_s and I_s waveforms from no load to full load under forward (motoring) mode of operation (scale: X-axis: 1div. = 0.05s, Y-axis: 1div. = 1000 V)

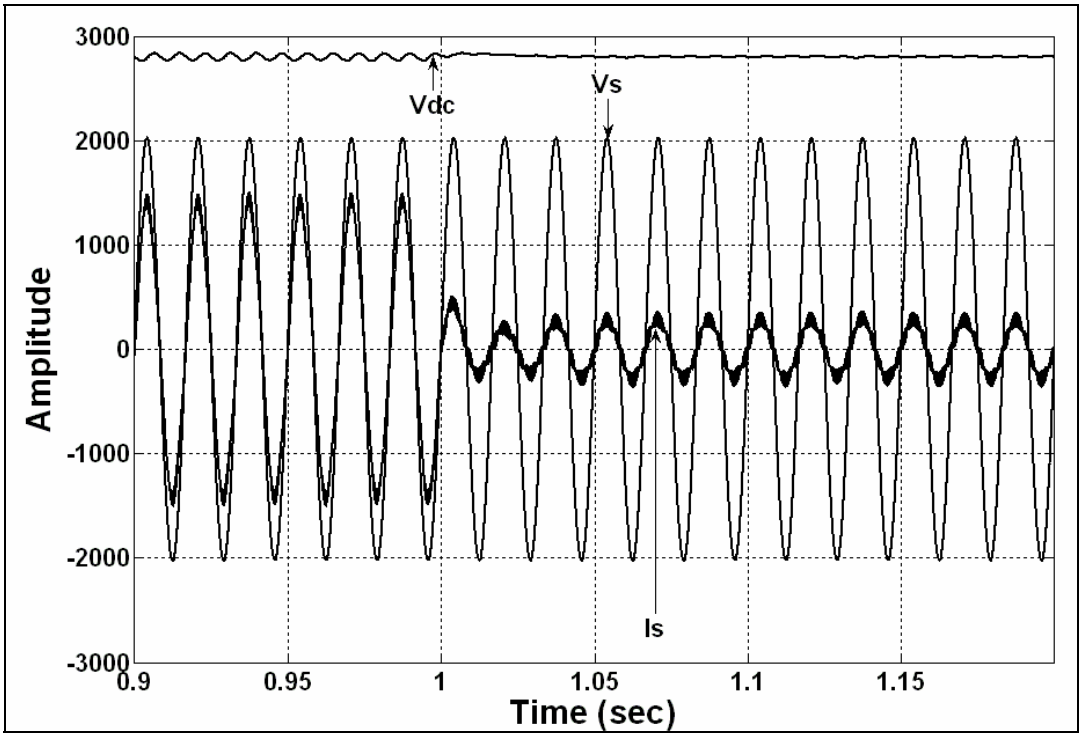

Fig. 4.21 V_{dc}, V_s and I_s waveforms from full load to no load under motoring mode of operation (scale: X-axis: 1div. = 0.05s, Y-axis: 1div. = 1000 V)

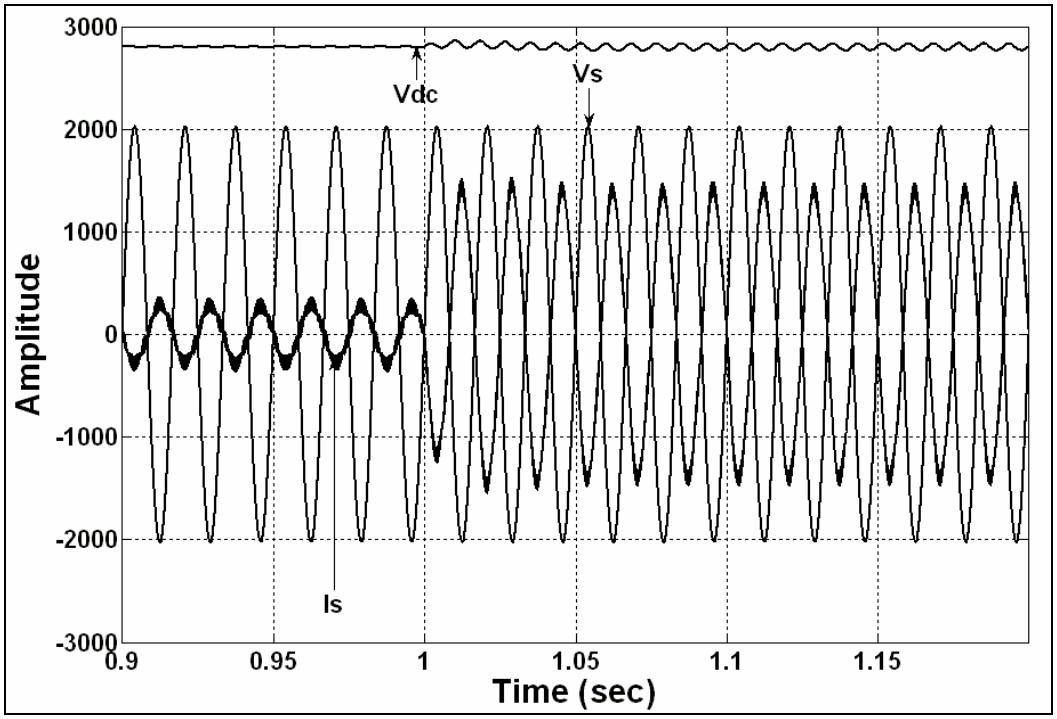

Fig. 4.22 V_{dc}, V_s and I_s waveforms from no load to full load under reverse (regenerative) mode of operation (scale: X-axis: 1div. = 0.05s, Y-axis: 1div. = 1000 V)

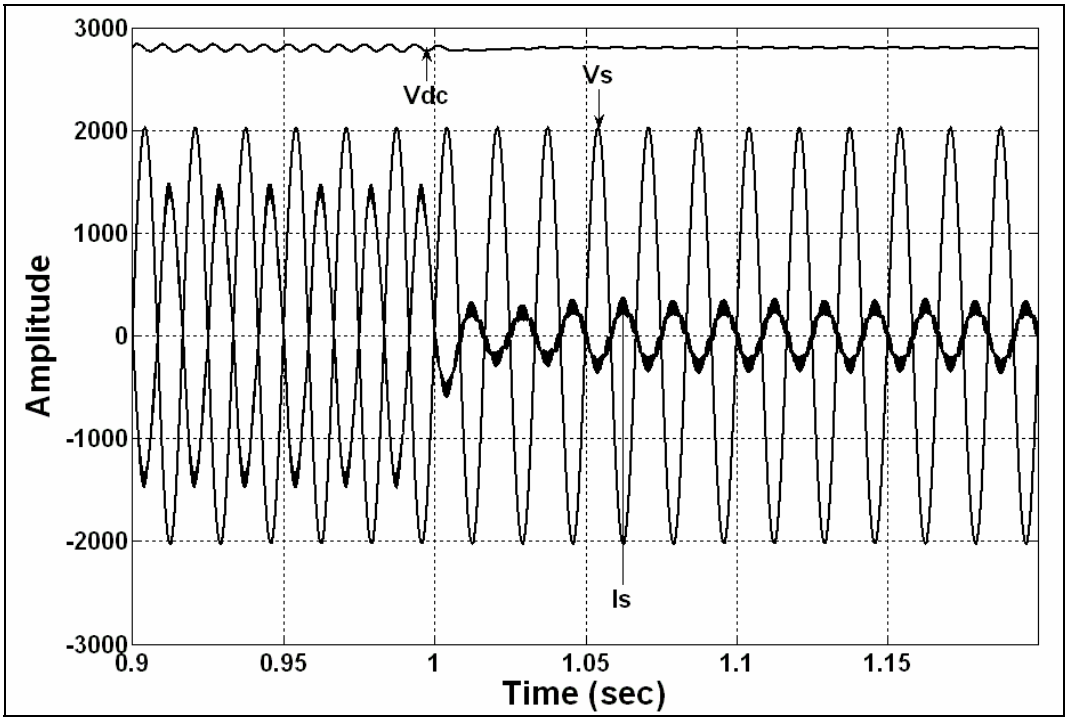

Fig. 4.23 V_{dc}, V_s and I_s waveforms from full load to no load under regenerative mode of operation (scale: X-axis: 1div.= 0.05 s, Y-axis: 1div. = 1000 V)

4.6 Simulation Results for Fault Condition

For the proposed front-end converter simulation results are also obtained under the fault condition. The simulation result for the transient condition of the system and considering Unity Modulus method only. The obtained simulation results are shown in fig. 4.24 to 4.26. The results are indicating that the unity power factor is maintained during fault condition. The simulation results are obtained for the motoring mode of operation and regenerative mode of operation, considering the transient condition of the system and Unity Modulus method. From the simulation result it is observed that the during the fault condition for both the motoring and regenerative mode of operation the unity power factor is maintained at the supply side.

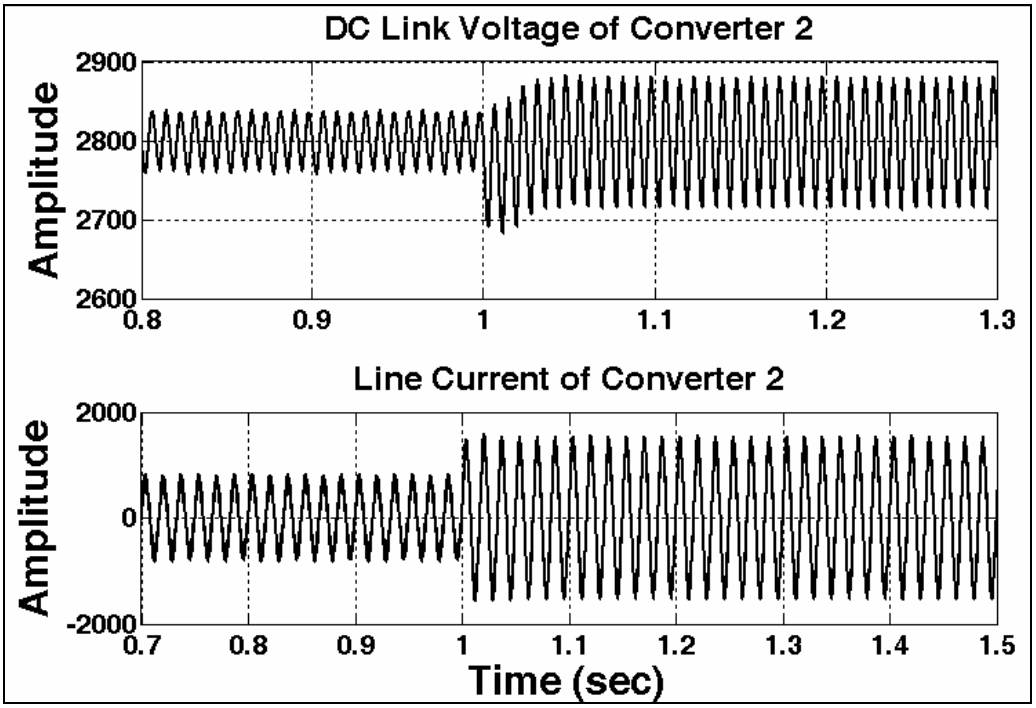

Fig. 4.24 Waveforms of dc link voltage and line current for under damped system during fault condition

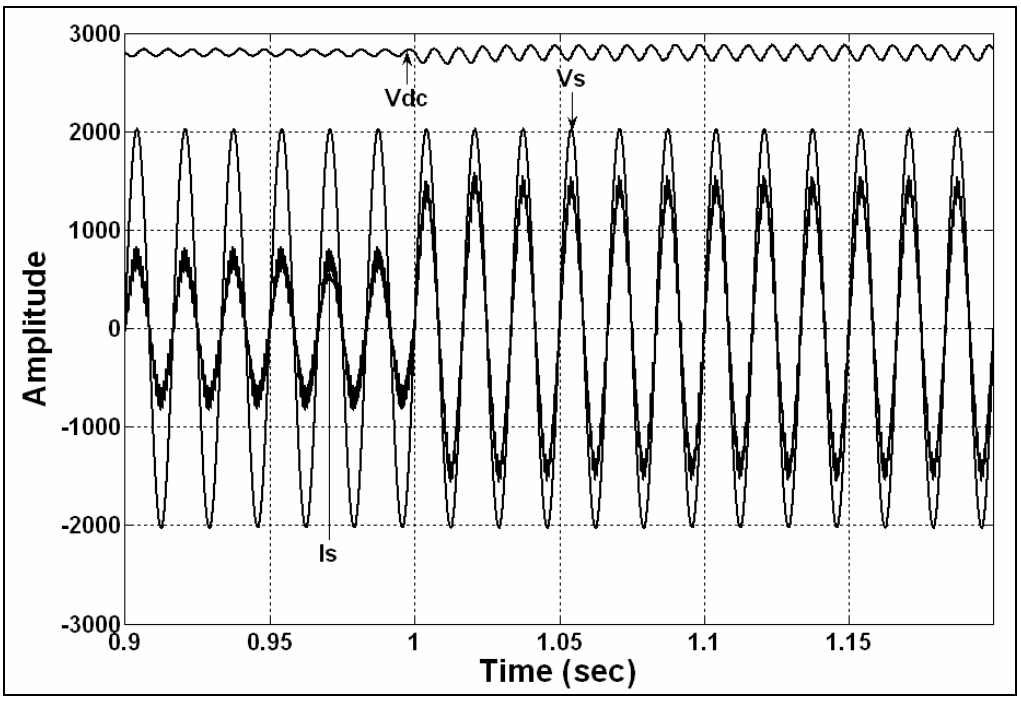

Fig. 4.25 V_{dc}, V_s and I_s waveforms during fault condition under motoring mode of operation

(Scale: X-axis: 1div. = 0.05 s, Y-axis: 1div. = 1000 V)

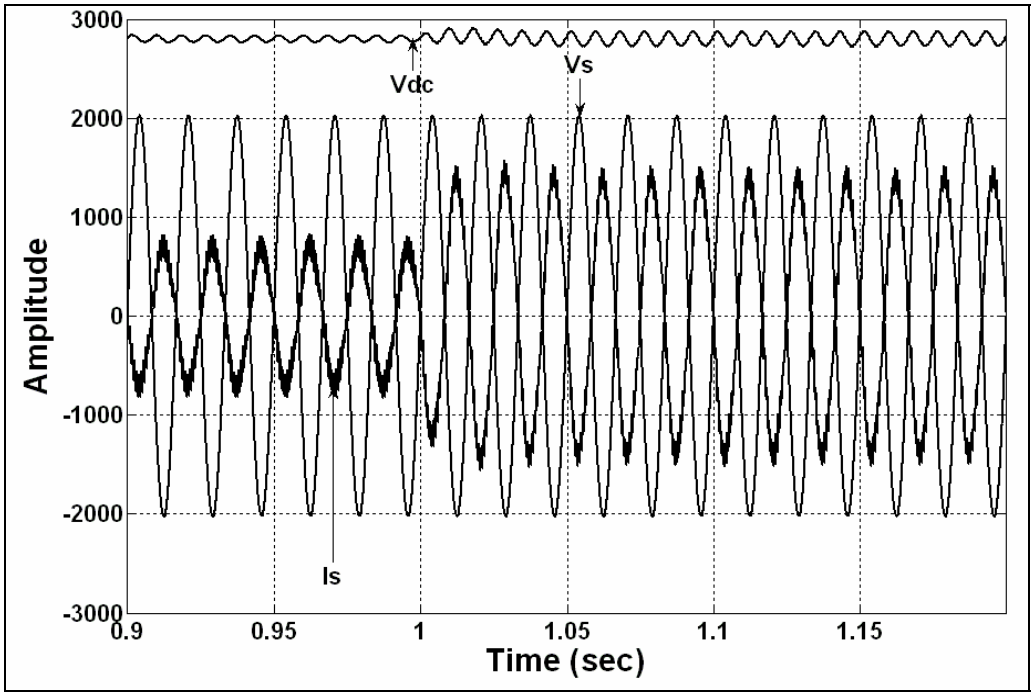

Fig. 4.26 V_{dc}, V_s and I_s waveforms during fault condition under regenerative mode of operation (scale: X-axis: 1div.= 0.05 s, Y-axis: 1div. = 1000 V)

4.7 FFT Analysis of Line Current

The FFT analysis of source side line current obtained from the simulation results is shown in fig.4.27 to 4.28. It can be observed that the % THD (4.078%) is very much less in case of proposed front-end converter compared to single phase diode bridge rectifier (328.50%).

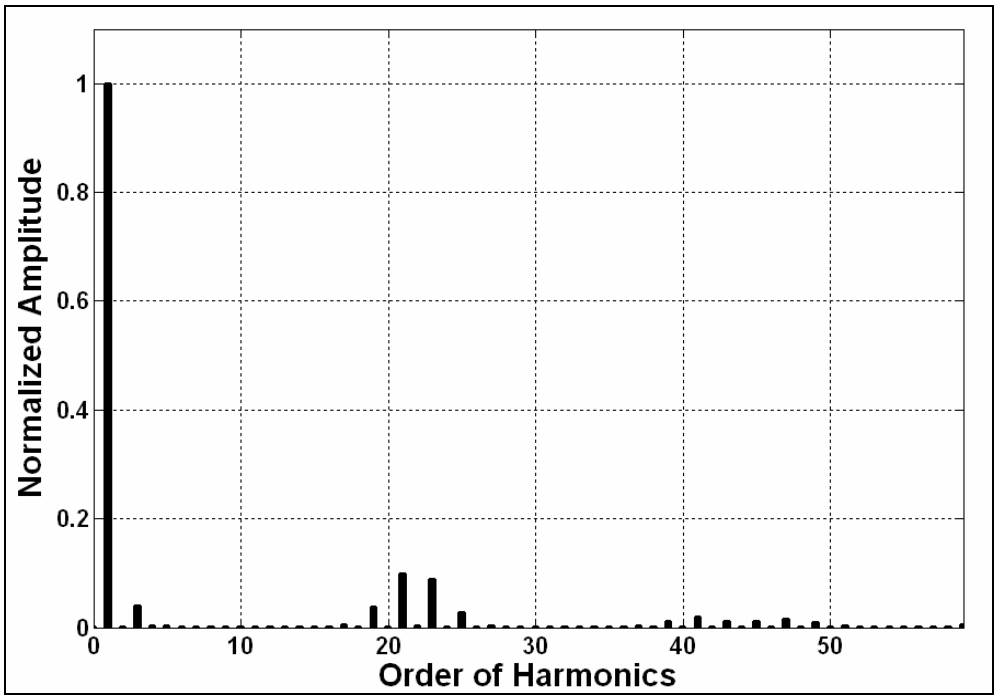

Fig. 4.27 Normalized harmonic spectrum of line current for one converter (i.e. I_{s1} or I_{s2})

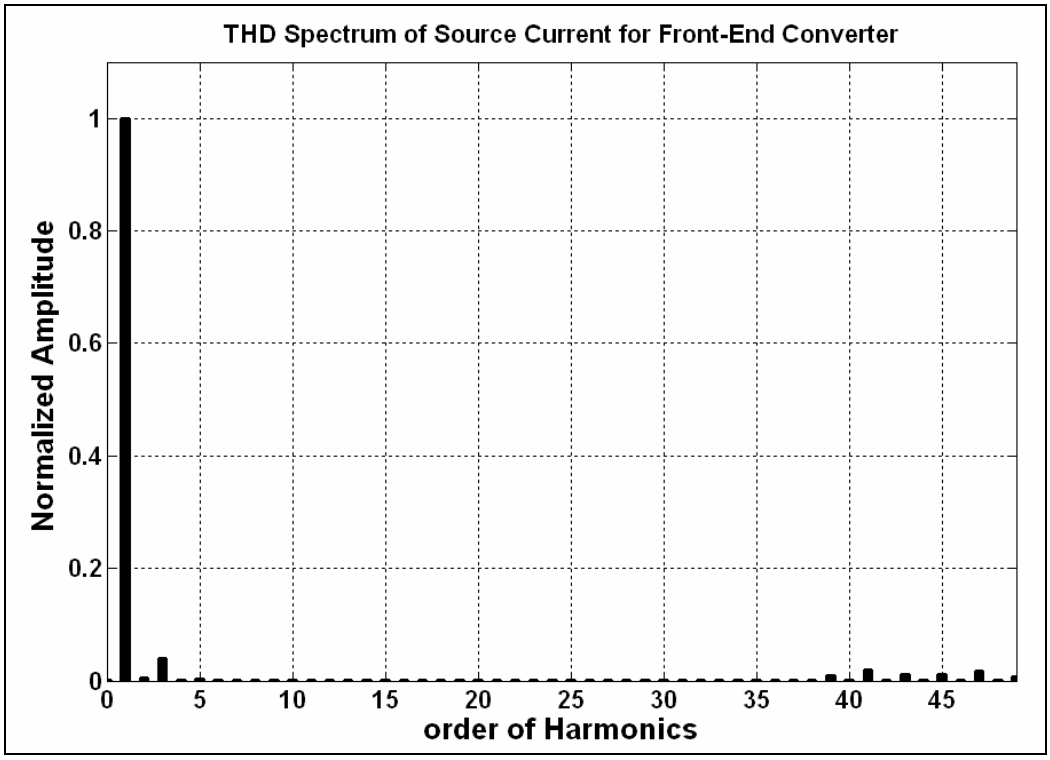

Fig. 4.28 Normalized harmonic spectrum of combined current reflected to primary (i.e. I_s)

Calculation of %THD:

$$\%THD(Upto11thOrder) = \left(\frac{\sqrt{\begin{array}{l}(4.076*10^{-3})^2+(0.0404)^2+(6.9602*10^{-4})^2+\\(2.998*10^{-3})^2+(1.8771*10^{-3})^2+(3.408*10^{-4})^2+\\(4.3356*10^{-4})^2+(1.3782*10^{-4})^2+\\(8.5587*10^{-4})^2+(4.632*10^{-4})^2\end{array}}}{(1)^2} \right) \times 100$$

$$\%THD(Upto11thOrder) = 4.078\%$$

4.8 MATLAB Programming of Proposed Converter and Results

The general program (M-File) is prepared for the calculation of the various parameters of current and voltage control loops of the proposed front-end converter. The various plots of step input and Nyquist plots are also taken with the help of program for different values of damping ratio.

The flow chart representation of the proposed front-end converter is shown in fig. 4.29. The flow chart indicates the steps included in the calculation of the various parameters of voltage and current control loop of the proposed front-end converter. The results are obtained from the MATLAB programming for current control loop are shown in fig. 4.30 and 4.31. The Nyquist diagram shows that the voltage control loops have the stability as (-1, 0) point is not encircled by the locus of the system. The results are obtained for all the conditions of the systems. The results are obtained using both the methods i.e. Unity Modulus method and Ziegler-Nichols method. The results are shown in fig. 4.32 to 4.37.

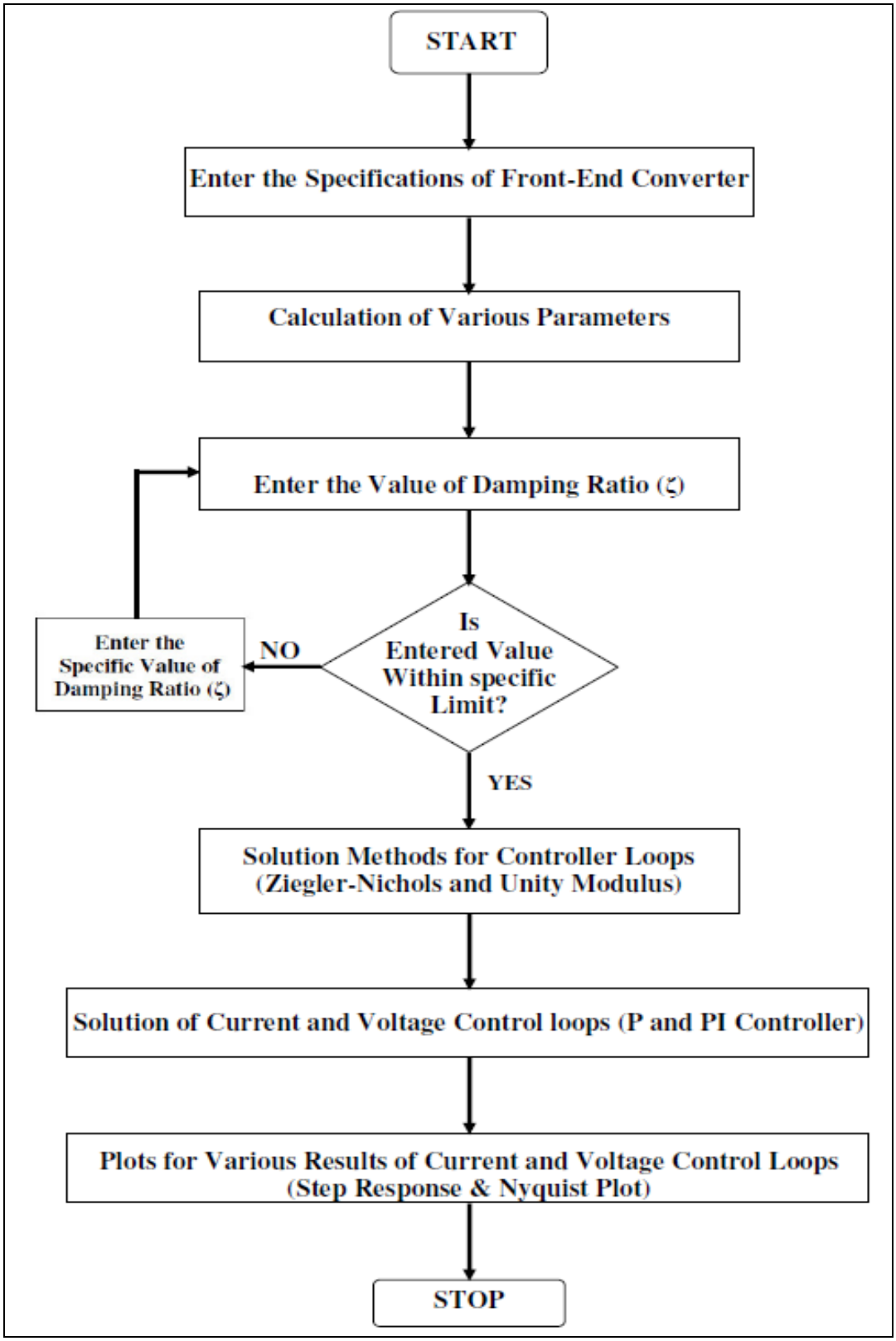

Fig. 4.29 Flow chart Representation of MATLAB Program for Front-End Converter

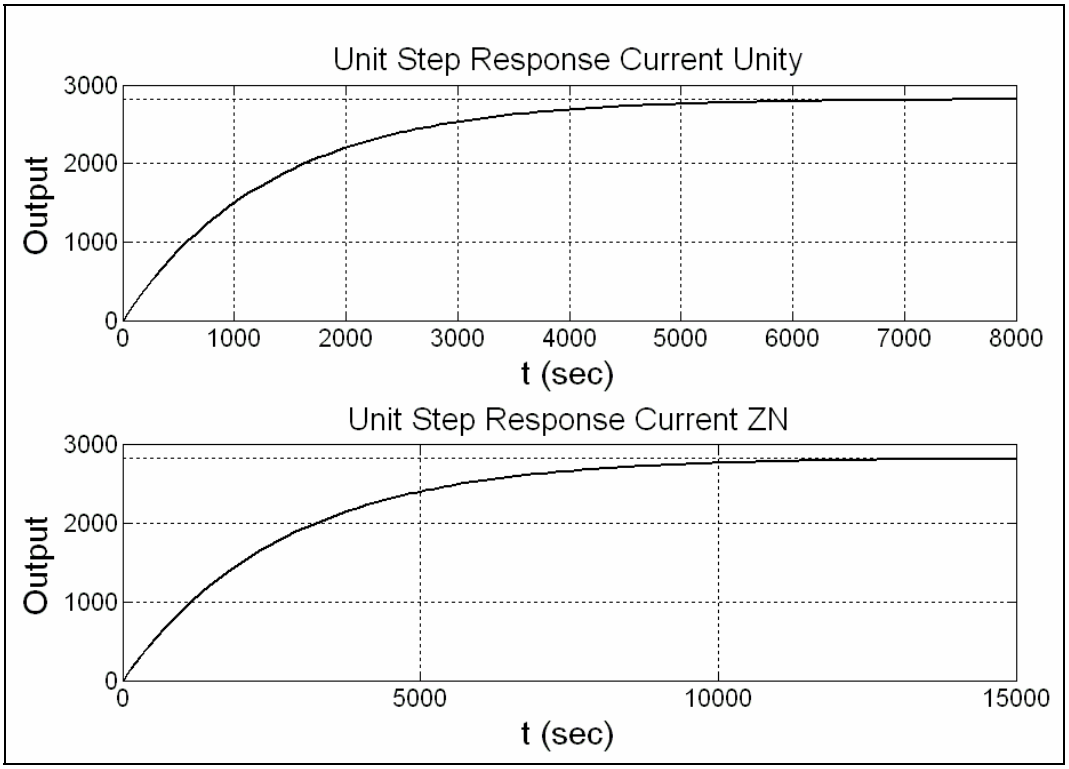

Fig. 4.30 Step response of current control loop for under damped system ($\zeta = 0.707$)

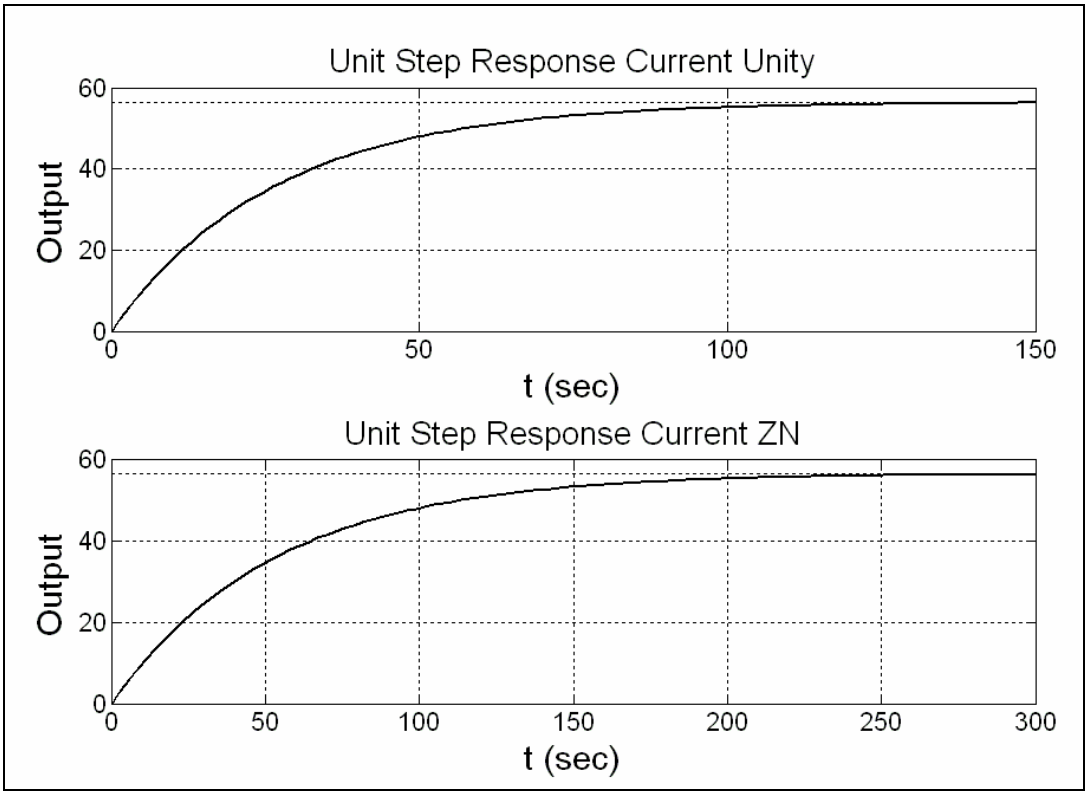

Fig. 4.31 Step response of current control loop for under damped system ($\zeta = 0.1$)

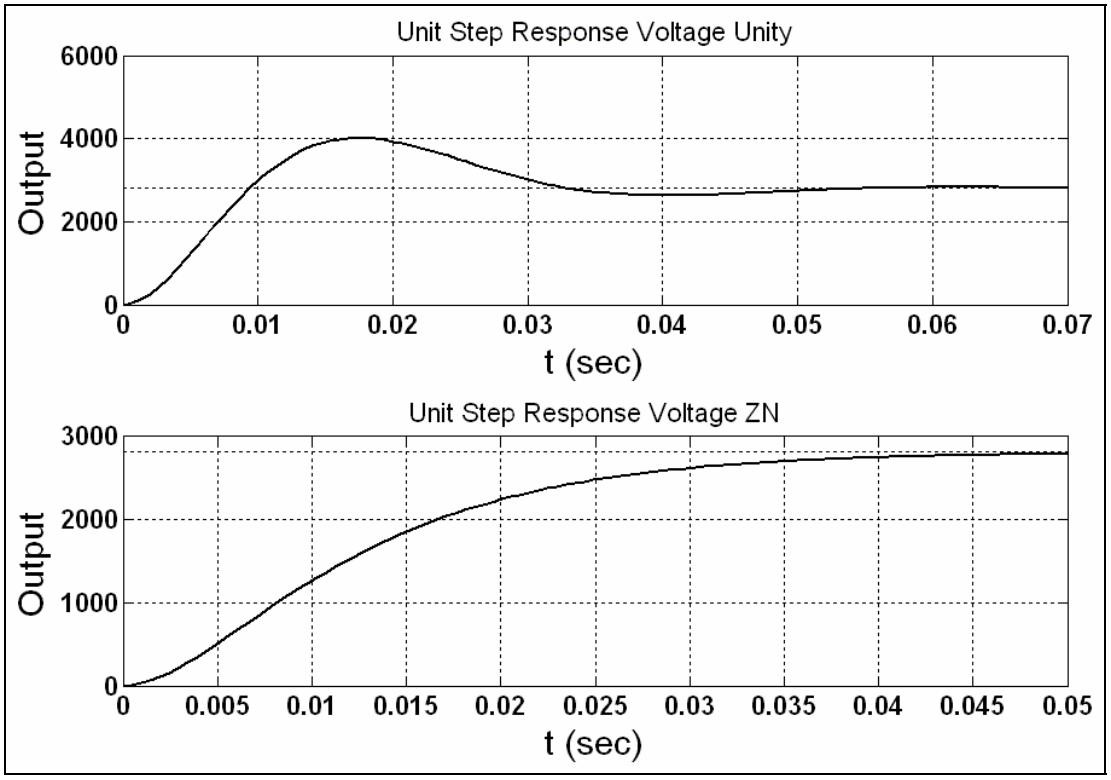

Fig. 4.32 Step response of voltage control loop for under damped system ($\zeta = 0.707$)

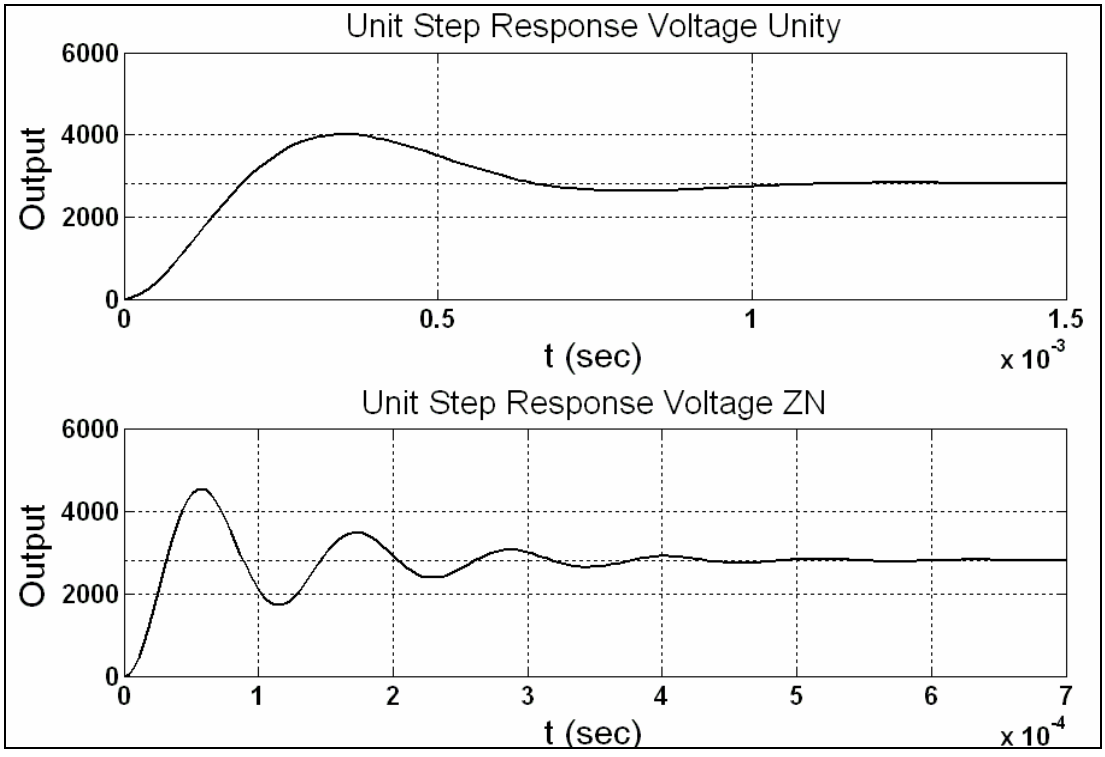

Fig. 4.33 Step response of voltage control loop for under damped system ($\zeta = 0.1$)

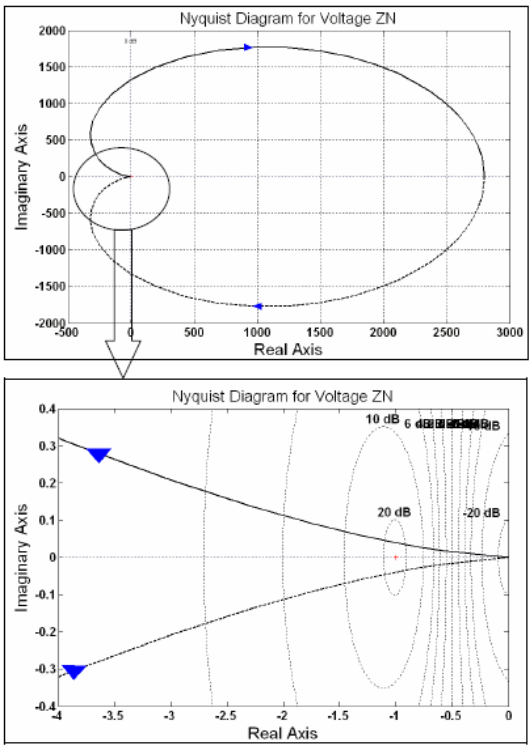

Fig. 4.34 Nyquist plot of Voltage control loop for under damped system (Ziegler-Nichols method, ζ = 0.707)

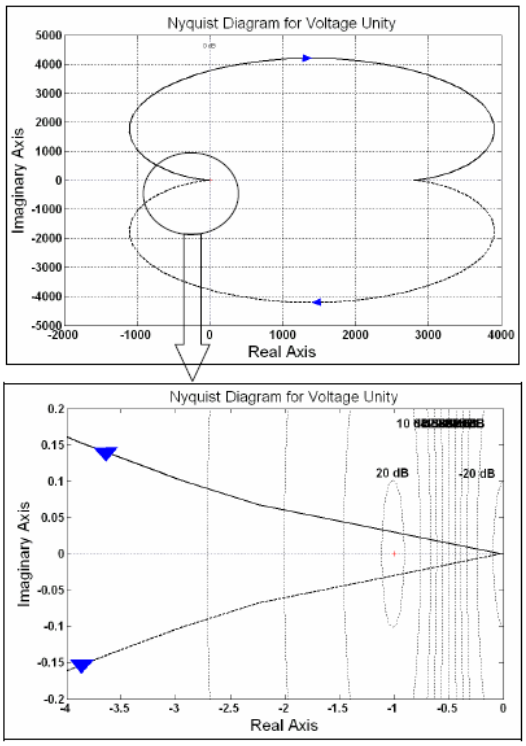

Fig. 4.35 Nyquist plot of Voltage control loop for under damped system (Unity Modulus method, ζ = 0.707)

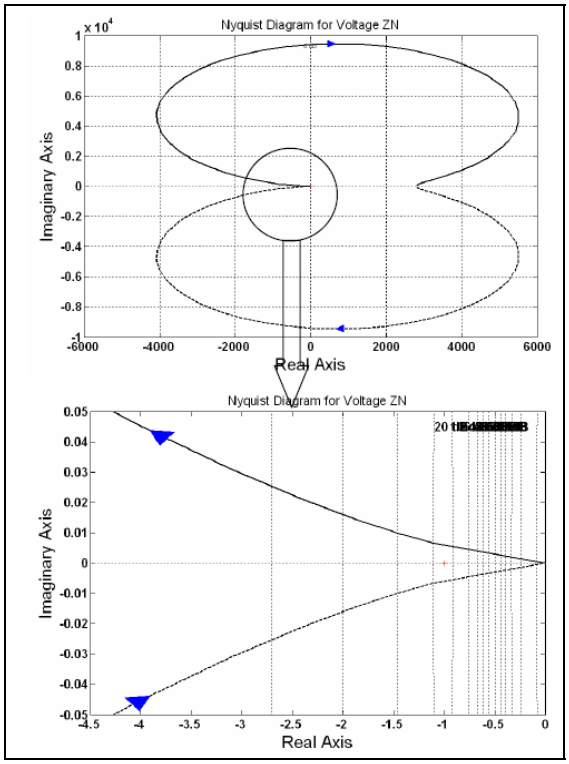

Fig. 4.36 Nyquist plot of Voltage control loop for under damped system (Ziegler-Nichols method, ζ = 0.1)

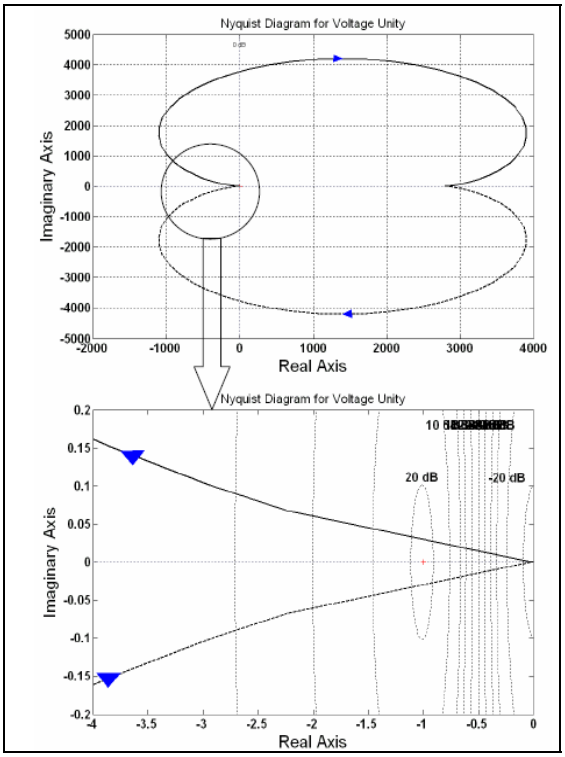

Fig. 4.37 Nyquist plot of Voltage control loop for under damped system (Unity Modulus method, ζ = 0.1)

CHAPTER-5
RATINGS OF PROTOTYPE CONVERTER AND SIMULATION RESULTS

The power schematic of prototype front-end converter is shown in fig. 5.1. The ratings of the prototype front-end converter are decided by considering the available ratings of the equipments in the laboratory, from the safety point of view of laboratory, performer and cost of the required components. The results are obtained from the simulation and MATLAB programming for the prototype front-end converter.

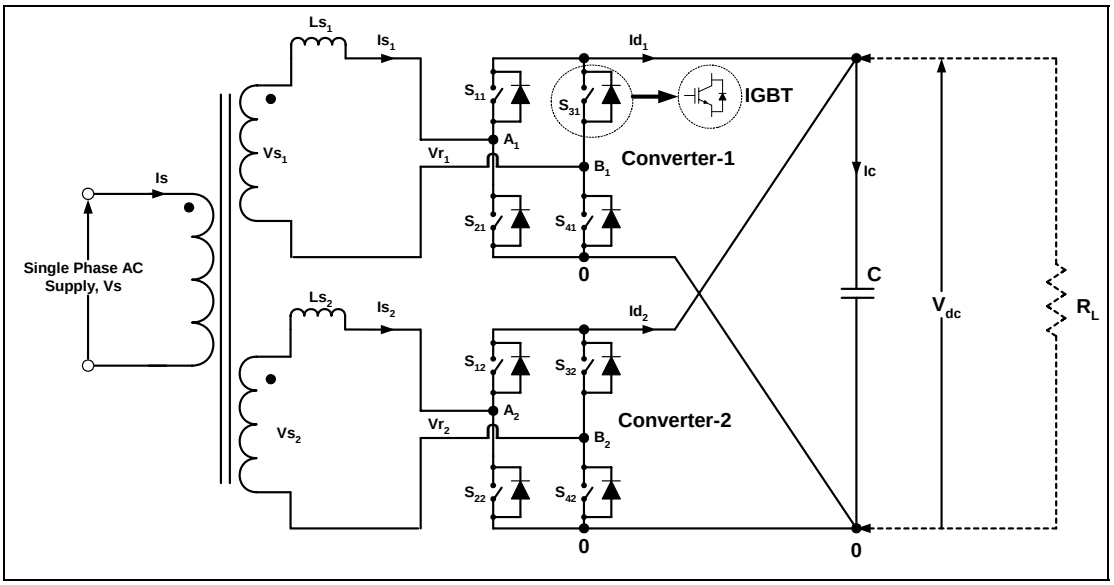

Fig.5.1 Schematic of prototype front-end converter

5.1 Specifications of Prototype Converter

The power ratings of the prototype front-end converter are as below:

- Input voltage = 30 V
- Output voltage = 60 Vdc
- Input supply frequency = 50 Hz
- Rated power = 750 W
- DC link capacitor = 9.37 mF

From the above details the various parameters related to the prototype front-end converter can be determined as shown below:

Input rms voltage, Vs (rms) = 30 V (ac)

$$\text{Input peak Voltage, } Vs_{(peak)} = \sqrt{2} \times Vs_{(rms)}$$
$$= \sqrt{2} \times 30$$
$$= 42.4264V$$
$$\cong 42V$$

$$\text{Rated load current, } I_{dc\,(Max)} = \frac{P}{V_{dc}}$$
$$= \frac{750}{60}$$
$$= 12.5\,A$$

Assuming efficiency of the converter, η = 80 %

$$\text{Rated rms input current, } Is_{(max)\,rms} = \frac{P}{Vs_{(rms)} \times \eta}$$
$$= \frac{750}{30 \times 0.8}$$
$$= 31.25\,A$$

$$\text{Rated peak input current, } Is_{(max)\,pk} = \sqrt{2} \times Is_{(max)\,rms}$$
$$= \sqrt{2} \times 31.25$$
$$= 44.19\,A$$

Assuming modulation index, m (max) = 0.8,

Maximum peak converter input voltage,

$$Vr_{(max)\,pk} = m_{(max)} \times V_{dc}$$
$$= 0.8 \times 60$$
$$= 48V$$

Maximum rms converter input voltage,

$$Vr_{(max)\,rms} = \frac{Vr_{(max)\,pk}}{\sqrt{2}}$$
$$= \frac{48}{\sqrt{2}}$$
$$= 33.94V$$
$$\cong 34V$$

Peak-to-peak ripple voltage,

$$\Delta V = 5\%\, of\ Vdc = \frac{5}{100} \times 60$$
$$= 3V\,(p-p)$$

The other calculations like to find P and PI controller parameters are performed with the help of MATLAB (M-file) program. The calculations are performed for the under damped system and results for the same are listed below.

Triangular Carrier Period,

$$T_r = \frac{1}{f_{sw}}$$
$$= \frac{1}{550}$$
$$= 1.8182 * 10^{-3}\, S$$

Input Source Inductance,

$$L_s = \sqrt{\frac{(48)^2 - (42.4264)^2}{(2 \times \Pi \times 50)^2 (44.19)^2}}$$
$$\therefore L_s = 1.6171 mH$$

The Current feed back gain is given by,

$$K_i = \frac{1}{Rated\ Peak\ Current}$$
$$\therefore K_i = \frac{1}{44.19}$$
$$\therefore K_i = 0.02263$$

The Gain of Current Control Loop (P-Controller) is given by,

$$K_1 = \frac{L_s}{K_i\ G\ T}$$
$$\therefore K_1 = \frac{1.6171\ * 10^{-3}}{0.02263\ * 48 * 2 * T_r}$$
$$\therefore K_1 = \frac{1.6171\ * 10^{-3}}{0.02263\ * 48 * 2 * 1.8182\ * 10^{-3}}$$
$$\therefore K_1 = 0.4095$$

The voltage feed back gain is given by,

$$K_v = \frac{1}{DC\,Link\,Voltage}$$

$$\therefore K_v = \frac{1}{60}$$

$$\therefore K_v = 0.01667$$

The gain and time parameters of voltage control loop can be obtained as follows:

$$K_n = \frac{K_i * V_{dc} * C}{\sqrt{2} * K_v * V_{s(rms)} * T}$$

$$\therefore K_n = \frac{0.02263 * 60 * 9.37 * 10^{-3}}{\sqrt{2} * 0.01667 * 30 * 2 * 1.8182 * 10^{-3}}$$

$$\therefore K_n = 4.9489$$

$$T_n = \frac{4 * K_i * V_{dc} * C}{\sqrt{2} * K_v * V_{s(rms)} * K_n}$$

$$\therefore T_n = \frac{0.02263 * 60 * 9.37 * 10^{-3}}{\sqrt{2} * 0.01667 * 30 * 2 * 4.9489}$$

$$\therefore T_n = 0.01454$$

5.2 Simulation Results of Prototype Converter

The simulation results are obtained for the under damped system considering transient condition and motoring mode of operation. The parameters of the P and PI controllers are obtained with the help of Unity Modulus (Magnitude Optimum) method.

The simulation results are shown in fig. 5.2 to 5.7. From the simulation results it can be observed that the for the prototype front-end converter the unity power factor is maintained for the supply side considering the under damped system and for the transient condition of the system. The simulation results are also obtained for motoring mode of operation, regenerative mode of operation and for fault conditions. The FFT analysis of source side line current obtained from simulation result is shown in fig. 5.8.

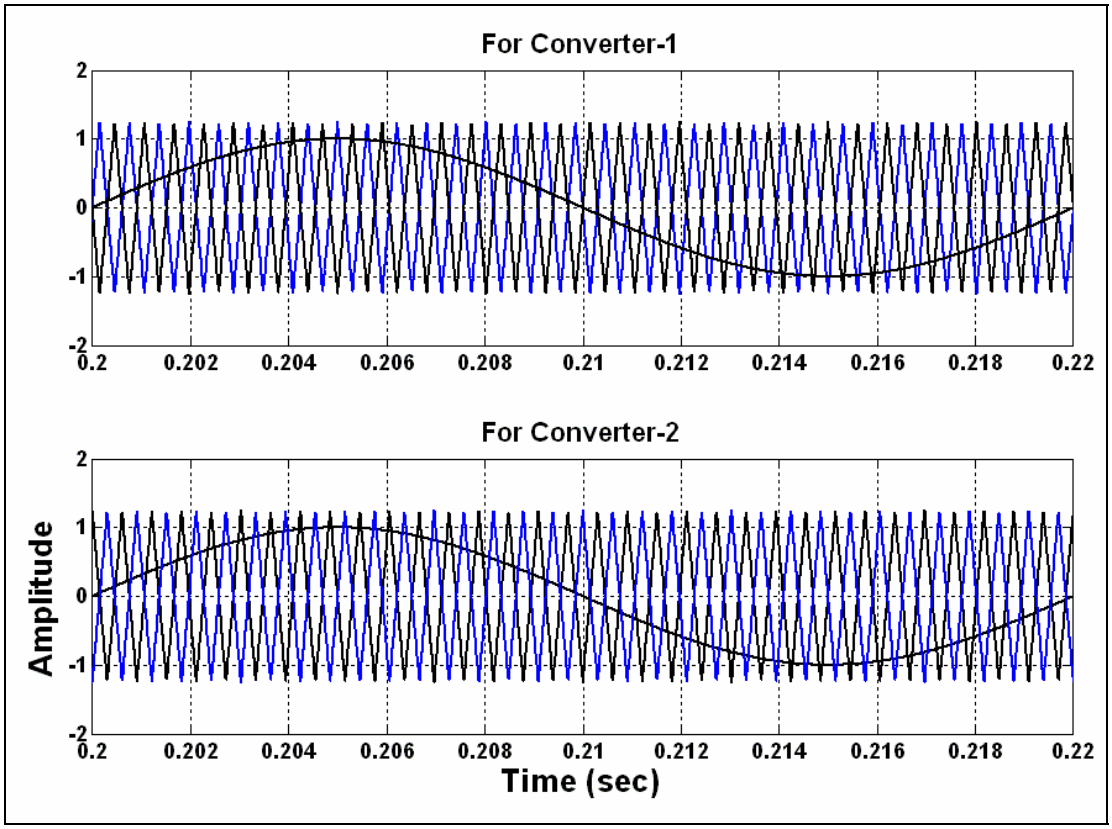

Fig.5.2 Carrier and reference waveforms for both converters
(scale: X-axis: 1div. = 0.002 s, Y-axis: 1div. = 1 V)

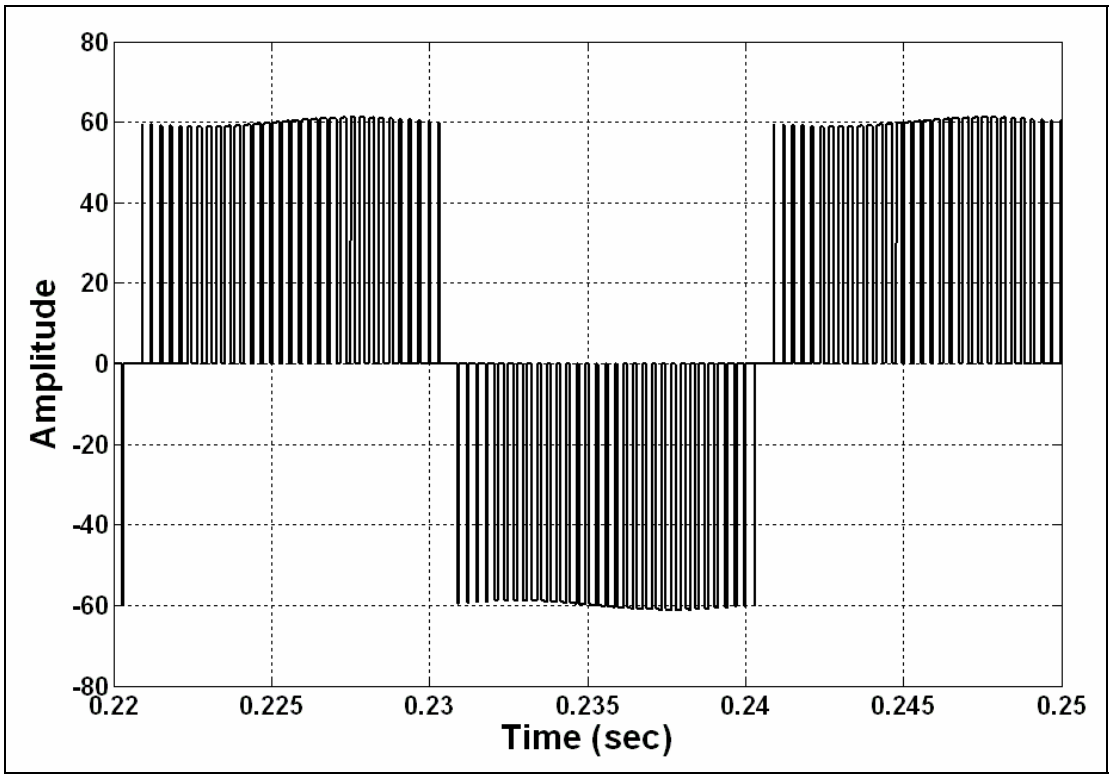

Fig.5.3 Voltage waveform V_{A1B1}= V_{A10}-V_{B10} (i.e. V_{rl})
(scale: X-axis: 1div. = 0.005 s, Y-axis: 1div. = 20 V)

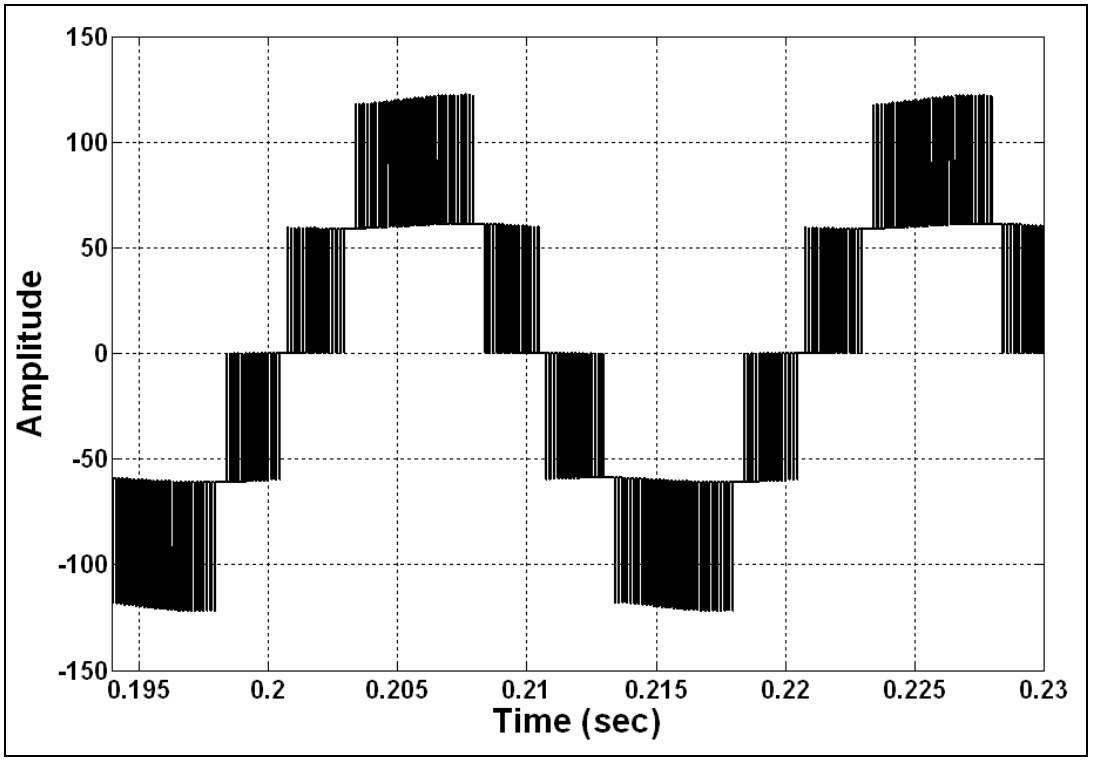

Fig.5.4 Voltage waveform $V_{AB}= V_{A1B1}+V_{A2B2}$ (i.e. V_r)

(scale: X-axis: 1div. = 0.005 s, Y-axis: 1div. = 50 V)

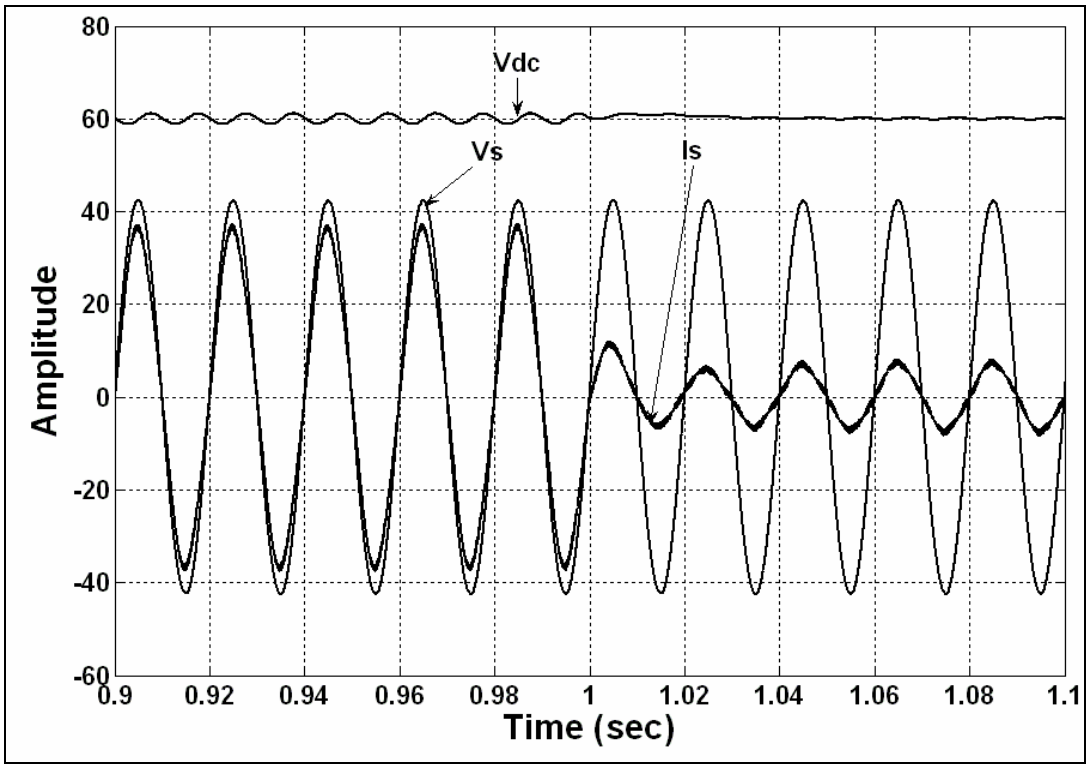

Fig. 5.5 V_{dc}, V_s and I_s waveforms from full load to no load under motoring mode of operation

(scale: X-axis: 1div. = 0.02 s, Y-axis: 1div. = 20 V)

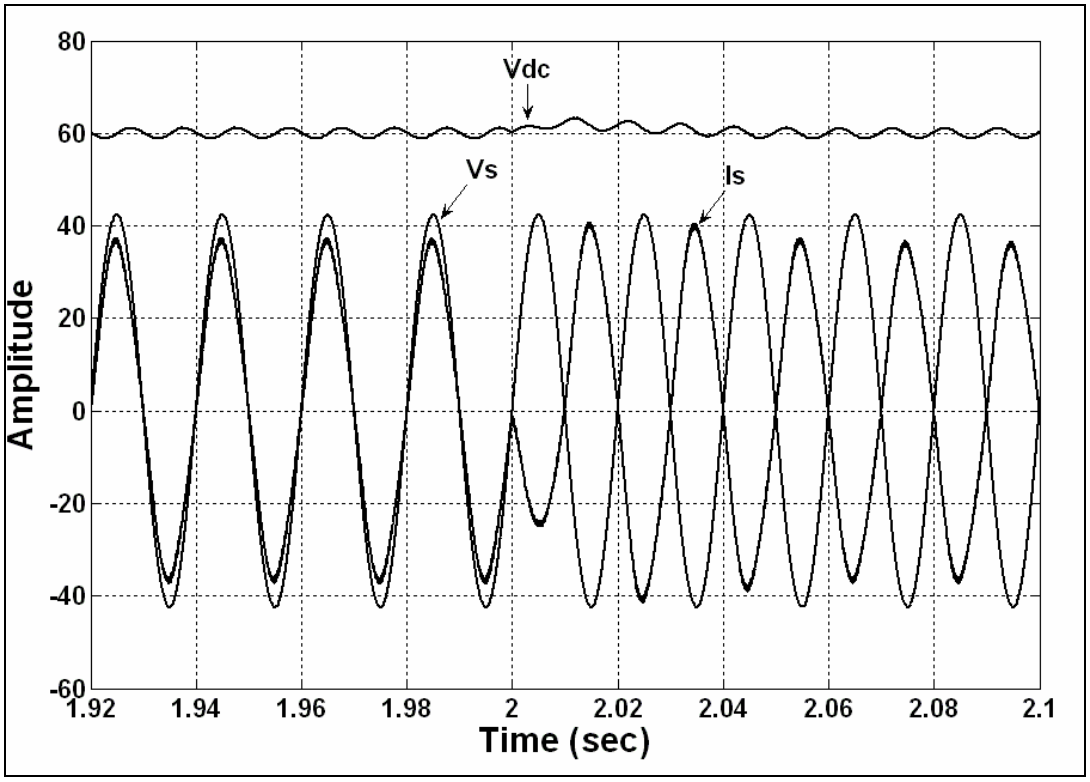

Fig. 5.6 V_{dc}, V_s and I_s waveforms for transition from motoring to regenerative mode of operation (scale: X-axis: 1div. = 0.02 s, Y-axis: 1div. = 20 V)

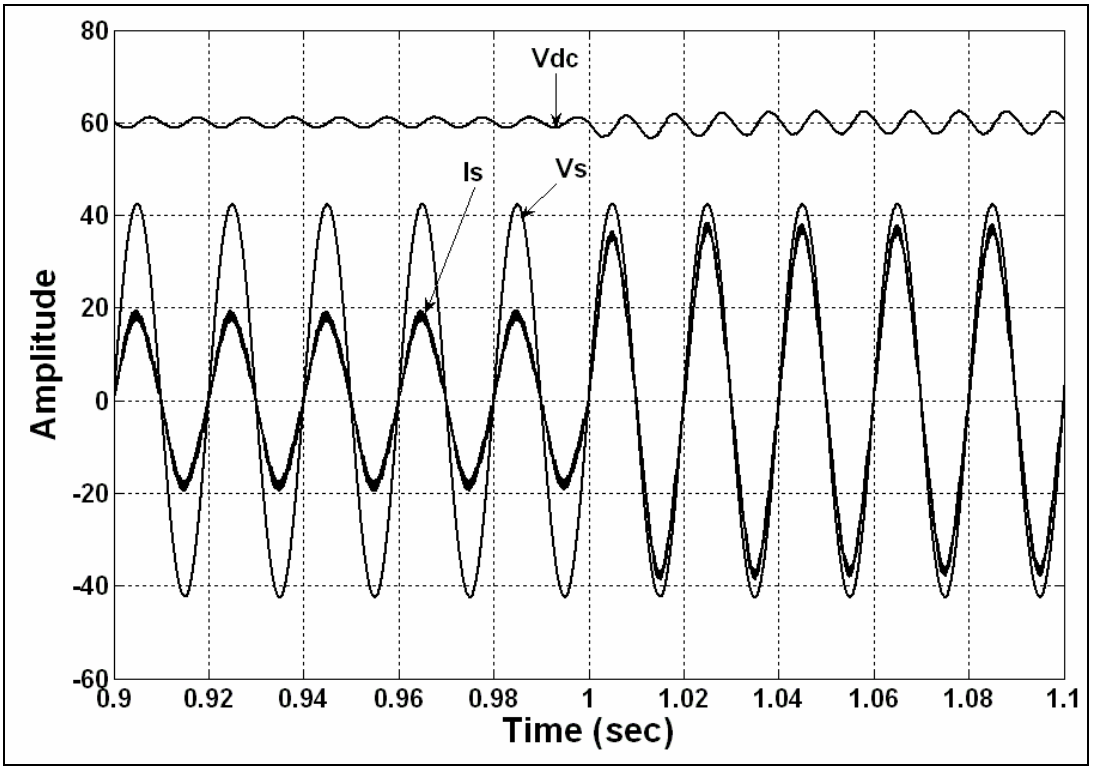

Fig. 5.7 V_{dc}, V_s and I_s waveforms during fault condition under motoring mode of operation (scale: X-axis: 1div. = 0.02 s, Y-axis: 1div. = 20 V)

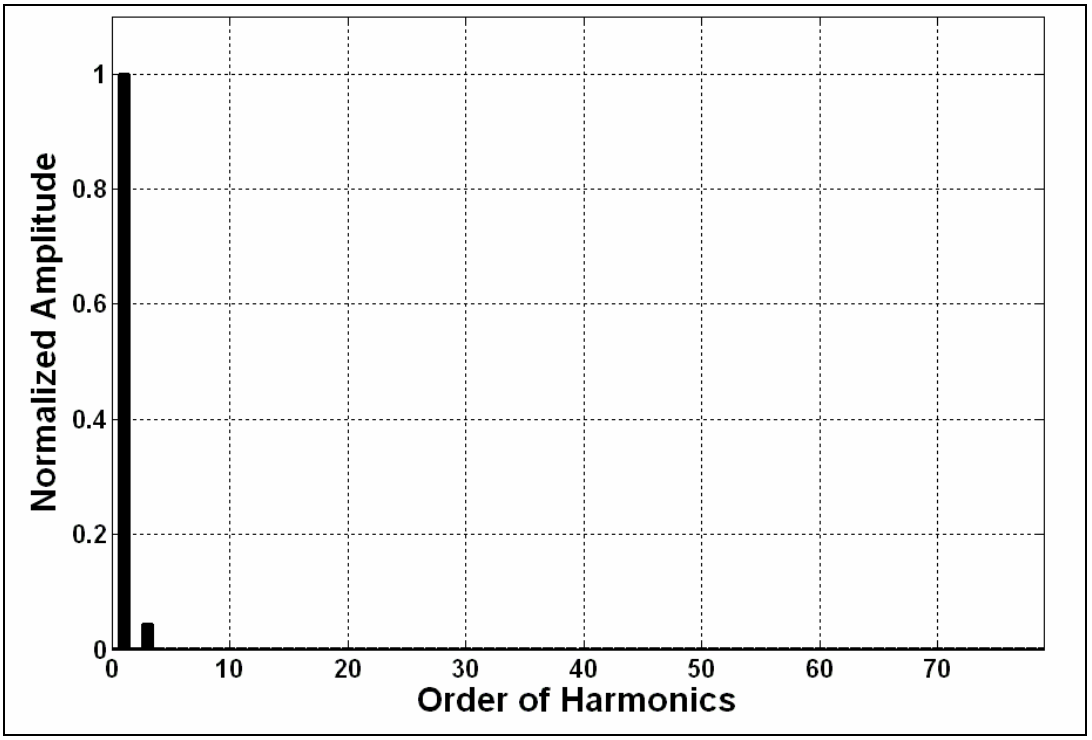

Fig.5.8 Normalized harmonic spectrum of combined current reflected to primary (i.e. I_s)

Calculation of %THD:

$$\%\,THD\ (Up\ to\ 11th\ Order\ ) = \left(\sqrt{\frac{\begin{array}{l}(3.3665 * 10^{-3})^2 + (0.0437)^2 + (5.0719 * 10^{-3})^2 + (2.7645 * 10^{-3})^2 + \\ (4.2751 * 10^{-4})^2 + (3.8107 * 10^{-5})^2 + (9.1662 * 10^{-4})^2 + \\ (1.2151 * 10^{-3})^2 + (9.7678 * 10^{-4})^2 + (5.76 * 10^{-4})^2\end{array}}{(1)^2}} \right) * 100$$

$$\%\,THD\,(Up\,to\,11^{th}\ Order) = 4.35\%$$

5.3 M-File Results of Prototype Converter

The general program (M-File) is prepared for the calculation of the various parameters of current and voltage control loops of the prototype front-end converter. The results are taken only from the unity modulus method. The various plots are also taken with the help of program is shown in fig, 5.9 to 5.11.

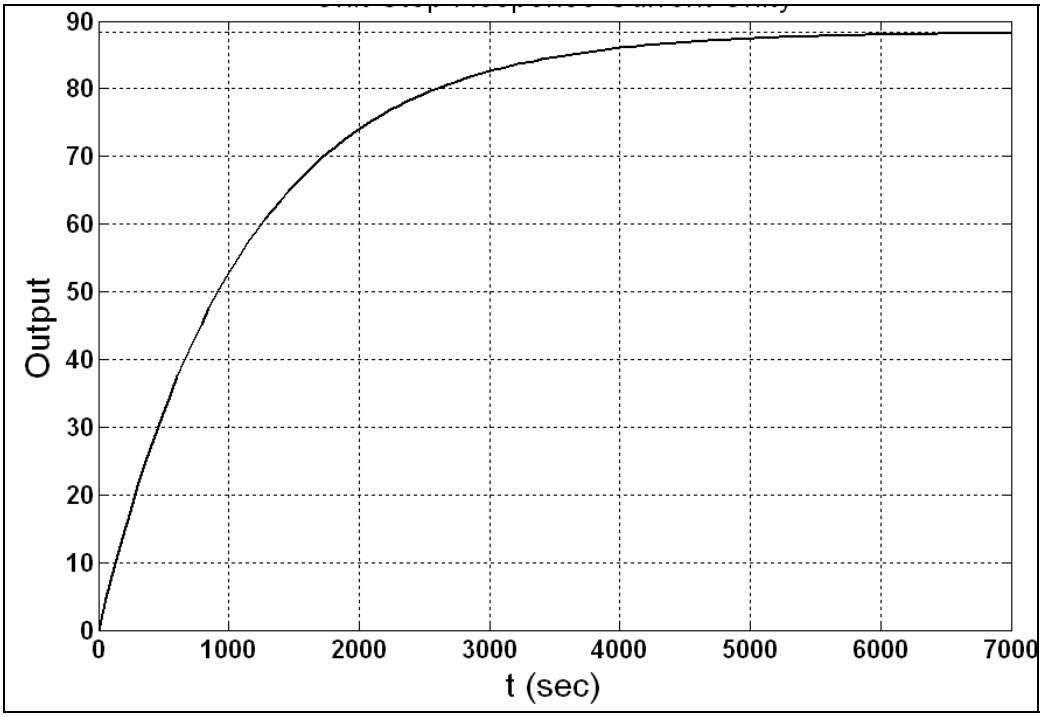

Fig. 5.9 Step response of current control loop for under damped system

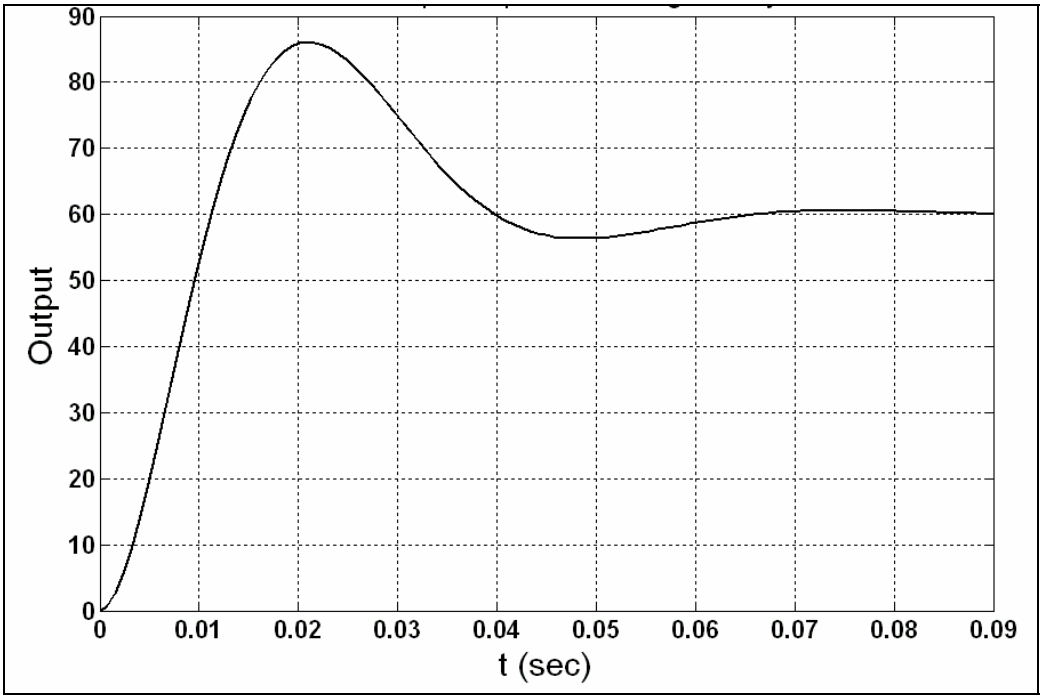

Fig. 5.10 Step response of voltage control loop for under damped system

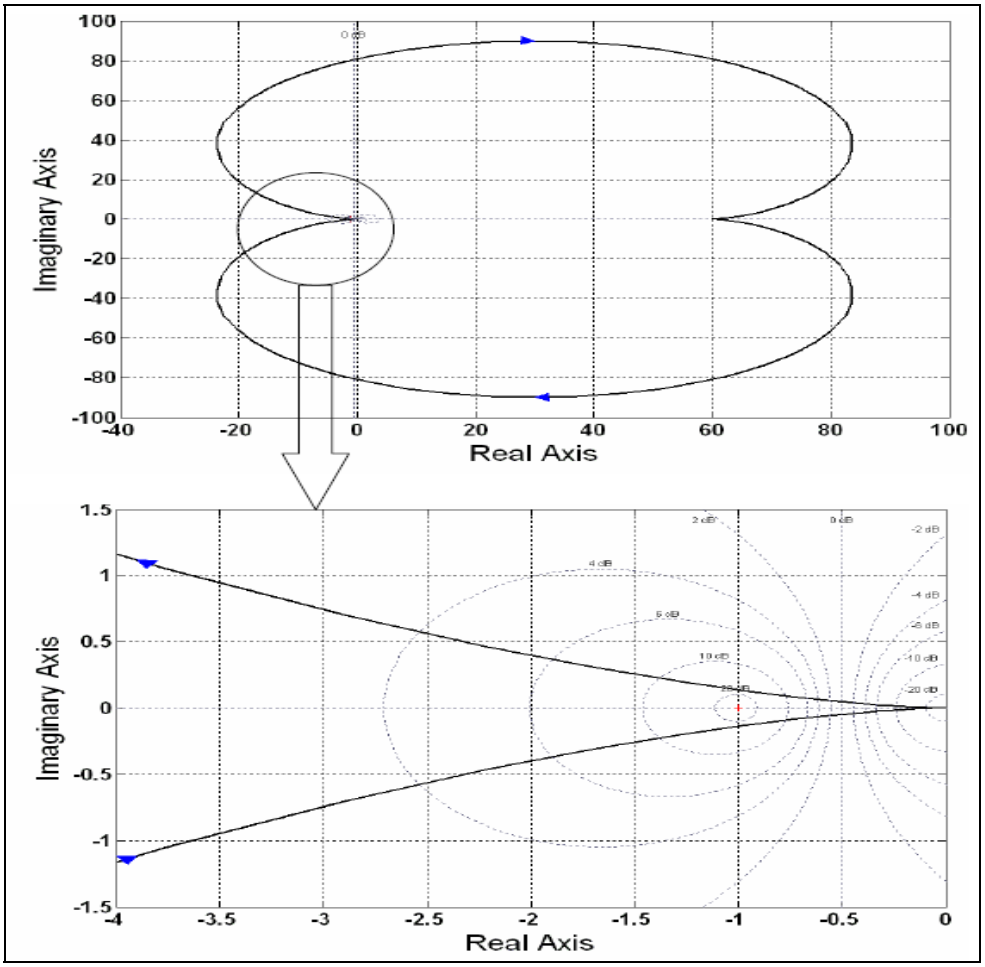

Fig. 5.11 Nyquist plot of Voltage control loop for under damped system

CHAPTER-6
OVERVIEW OF DSP TMS320LF2407A

6.1 Introduction

The TMS320LF240xA and TMS320LC240xA devices [11], new members of the TMS320C24x™; generation of digital signal processor (DSP) controllers, are part of the TMS320C2000™; platform of fixed-point DSPs. The 240xA devices offer the enhanced TMS320™; DSP architectural design of the C2xx core CPU for low-cost, low-power, and high-performance processing capabilities. Several advanced peripherals, optimized for digital motor and motion control applications, have been integrated to provide a true single-chip DSP controller. While code-compatible with the existing C24x™; DSP controller devices, the 240xA offers increased processing performance (40 MIPS) and a higher level of peripheral integration.

The 240xA generation offers an array of memory sizes and different peripherals tailored to meet the specific price/performance points required by various applications. Flash devices of up to 32K words offer a cost-effective reprogrammable solution for volume production. The 240xA devices offer a password-based "code security" feature which is useful in preventing unauthorized duplication of proprietary code stored in on-chip Flash/ROM. Note that Flash-based devices contain a 256-word boot ROM to facilitate in-circuit programming. The 240xA family also includes ROM devices that are fully pin-to-pin compatible with their Flash counterparts.

All 240xA devices offer at least one event manager module which has been optimized for digital motor control and power conversion applications. Capabilities of this module include center- and/or edge-aligned PWM generation, programmable dead band to prevent shoot-through faults, and synchronized analog-to-digital conversion. Devices with dual event managers enable multiple motor and/or converter control with a single 240xA DSP controller. Select EV pins have been provided with an "input-qualifier" circuitry, which minimizes inadvertent pin-triggering by glitches.

The high-performance, 10-bit analog-to-digital converter (ADC) has a minimum conversion time of 375 ns and offers up to 16 channels of analog input. The auto sequencing capability of the ADC allows a maximum of 16 conversions to take place in a single conversion session without any CPU overhead.

A serial communications interface (SCI) is integrated on all devices to provide asynchronous communication to other devices in the system. For systems requiring additional communication interfaces, the 2407A, 2406A, 2404A, and 2403A offer a 16-bit synchronous serial peripheral interface (SPI). The 2407A, 2406A, and 2403A offer a controller area network (CAN) communications module that meets 2.0B specifications. To maximize device flexibility, functional pins are also configurable as general-purpose inputs/outputs (GPIOs).

To streamline development time, JTAG-compliant scan-based emulation has been integrated into all devices. This provides non-intrusive real-time capabilities required to debug digital control systems. A complete suite of code-generation tools from C compilers to the industry-standard Code Composer Studio™; debugger supports this family. Numerous third-party developers not only offer device-level development tools, but also system-level design and development support.

6.2 Features of TMS320LF2407A

1. High-Performance Static CMOS Technology

- 25-ns Instruction Cycle Time (40 MHz)
- 40-MIPS Performance
- Low-Power 3.3-V Design

2. Based on TMS320C2xx DSP CPU Core

- Code-Compatible With F243/F241/C242
- Instruction Set and Module Compatible With F240

3. Flash (LF) and ROM (LC) Device Options

- LF240xA: LF2407A, LF2406A, LF2403A, LF2402A
- LC240xA: LC2406A, LC2404A, LC2403A, LC2402A

4. On-Chip Memory

- Up to 32K Words x 16 Bits of Flash EEPROM (4 Sectors) or ROM
- Programmable “Code-Security” Feature for the On-Chip Flash/ROM
- Up to 2.5K Words x 16 Bits of Data/Program RAM
  - 544 Words of Dual-Access RAM
  - Up to 2K Words of Single-Access RAM

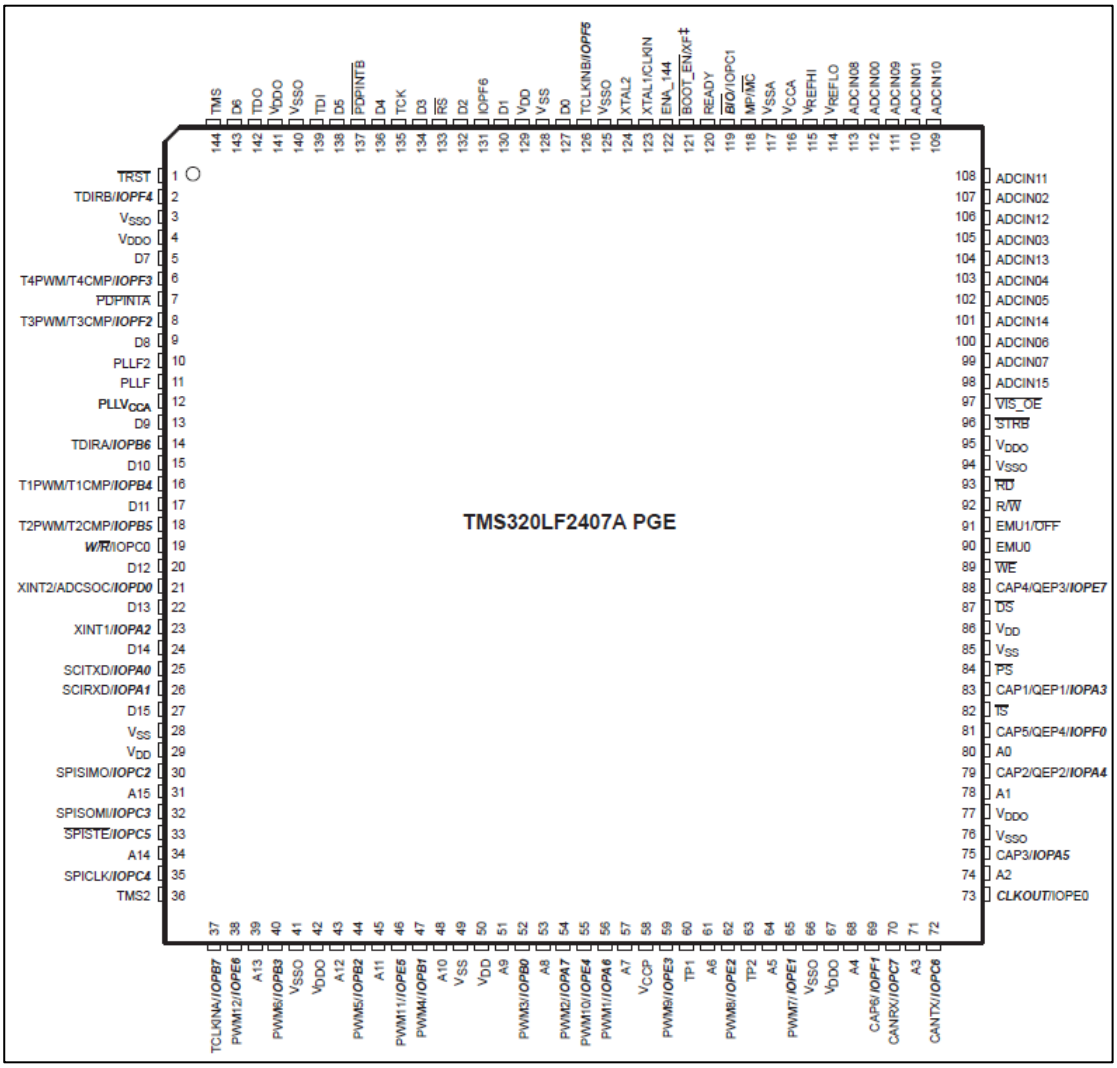

Fig. 6.1 Pin outs of TMS320LF2407A

5. Boot ROM (LF240xA Devices)

- SCI/SPI Boot loader

6. Up to Two Event-Manager (EV) Modules (EVA and EVB), Each Includes

- Two 16-Bit General-Purpose Timers
- Eight 16-Bit Pulse-Width Modulation (PWM) Channels Which Enable:
  - Three-Phase Inverter Control
  - Center- or Edge-Alignment of PWM Channels
  - Emergency PWM Channel Shutdown With External PDPINTx Pin
- Programmable Dead band (Dead time) Prevents Shoot-Through Faults
- Three Capture Units for Time-Stamping of External Events
- Input Qualifier for Select Pins
- On-Chip Position Encoder Interface Circuitry

- Synchronized A-to-D Conversion
- Designed for AC Induction, BLDC, Switched Reluctance, and Stepper Motor Control
- Applicable for Multiple Motor and/or Converter Control

7. External Memory Interface (LF2407A)

- 192K Words x 16 Bits of Total Memory:
  64K Program, 64K Data, 64K I/O

8. Watchdog (WD) Timer Module

9. 10-Bit Analog-to-Digital Converter (ADC)

- 8 or 16 Multiplexed Input Channels
- 500-ns MIN Conversion Time
- Selectable Twin 8-State Sequencers Triggered by Two Event Managers

10. Controller Area Network (CAN) 2.0B Module (LF2407A, 2406A, 2403A)

11.Serial Communications Interface (SCI)

12.16-Bit Serial Peripheral Interface (SPI) (LF2407A, 2406A, LC2404A, 2403A)

13.Phase-Locked-Loop (PLL)-Based Clock Generation

14. Up to 40 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins

15. Up to Five External Interrupts (Power Drive Protection, Reset, Two Mask able Interrupts)

16. Power Management

- Three Power-Down Modes
- Ability to Power Down Each Peripheral Independently

17. Real-Time JTAG-Compliant Scan-Based Emulation, IEEE Standard 1149.1† (JTAG)

18. Development Tools Include:

- Texas Instruments (TI) ANSI C Compiler, Assembler/Linker, and Code Composer Studio ™ Debugger
- Evaluation Modules
- Scan-Based Self-Emulation (XDS510)
- Broad Third-Party Digital Motor Control Support

19. Package Options

- 144-Pin LQFP PGE (LF2407A)

- 100-Pin LQFP PZ (2406A, LC2404A)
- 64-Pin TQFP PAG (LF2403A, LC2403A, LC2402A)
- 64-Pin QFP PG (2402A)

20. Extended Temperature Options (A and S)

- A: − 40°C to 85°C
- S: − 40°C to 125°C

6.3 Functional Block Diagram

A functional block diagram of the ’C24x DSP controller architecture is shown in fig.6.2. The ’C24x DSP architecture is based on a modified Harvard architecture, which supports separate bus structures for program space and data space. A third space, the input/output (I/O) space, is also available and is accessible through the external bus interface. To support a large selection of peripherals, a peripheral bus is used. The peripheral bus is mapped to the data space and interfaced to the data bus through a special system module. Thus, all the instructions that operate on the data space also operate on all the peripheral registers. Separate program and data spaces allow simultaneous access to program instructions and data. For example, while data is multiplied, a previous product can be added to the accumulator, and at the same time, a new address can be generated. Such parallelism supports a set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. The ’C24x also includes control mechanisms to manage interrupts, repeated operations, and function/subroutine calls. Fig.6.3 shows the graphical overview of the 240xA device, which is helpful in understanding the availability of the system peripherals and devices available with controller in general.

➢ ’C24x CPU Internal Bus Structure

The ’C24x DSP, a member of the TMS320 family of DSPs, includes a ’C2xx DSP core designed using the ’2xLP ASIC core. The ’C2xx DSP core has an internal data and program bus structure that is divided into six 16-bit buses. The six buses are:

PAB: The program address bus provides addresses for both reads from and writes to program memory.

DRAB: The data-read address bus provides addresses for reads from data memory.

DWAB: The data-write address bus provides addresses for writes to data memory.

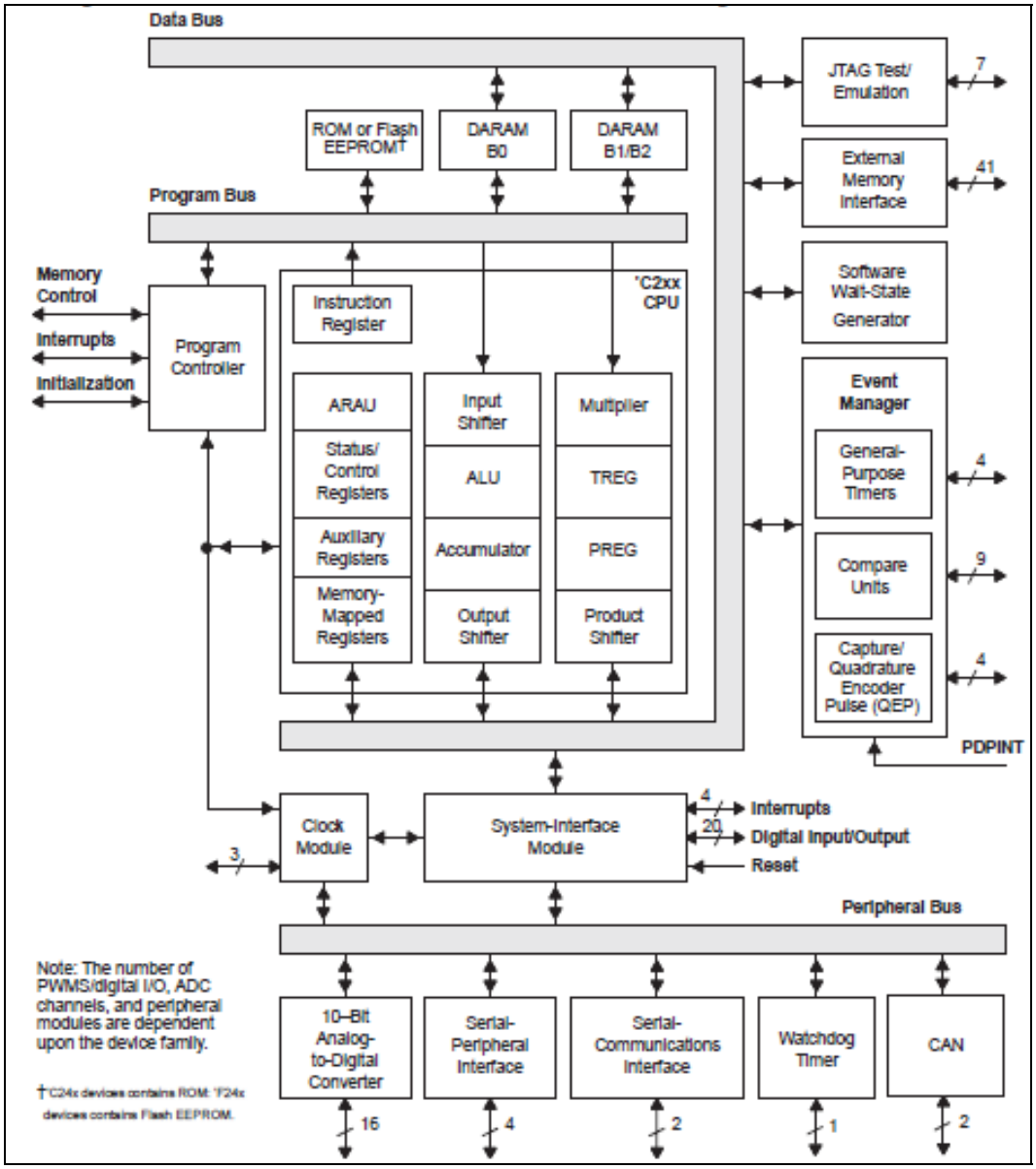

Fig. 6.2 TMS320C24x DSP controller functional block diagram

PRDB: The program read bus carries instruction code and immediate operands, as well as table information, from program memory to the CPU.

DRDB: The data-read bus carries data from data memory to the central arithmetic logic unit (CALU) and the auxiliary register arithmetic unit (ARAU).

DWEB: The data-write bus carries data to both program memory and data memory.

Having separate address buses for data reads (DRAB) and data writes (DWAB) allows the CPU to read and write in the same machine cycle.

➢ Memory

The ’C24x contains the following types of on-chip memory:

Dual-access RAM (DARAM)

Flash EEPROM or ROM (masked)

The ’C24x memory is organized into four individually-selectable spaces:

Program (64K words)

Local data (64K words)

Global data (32K words)

Input/Output (64K words)

These spaces form an address range of 224K words.

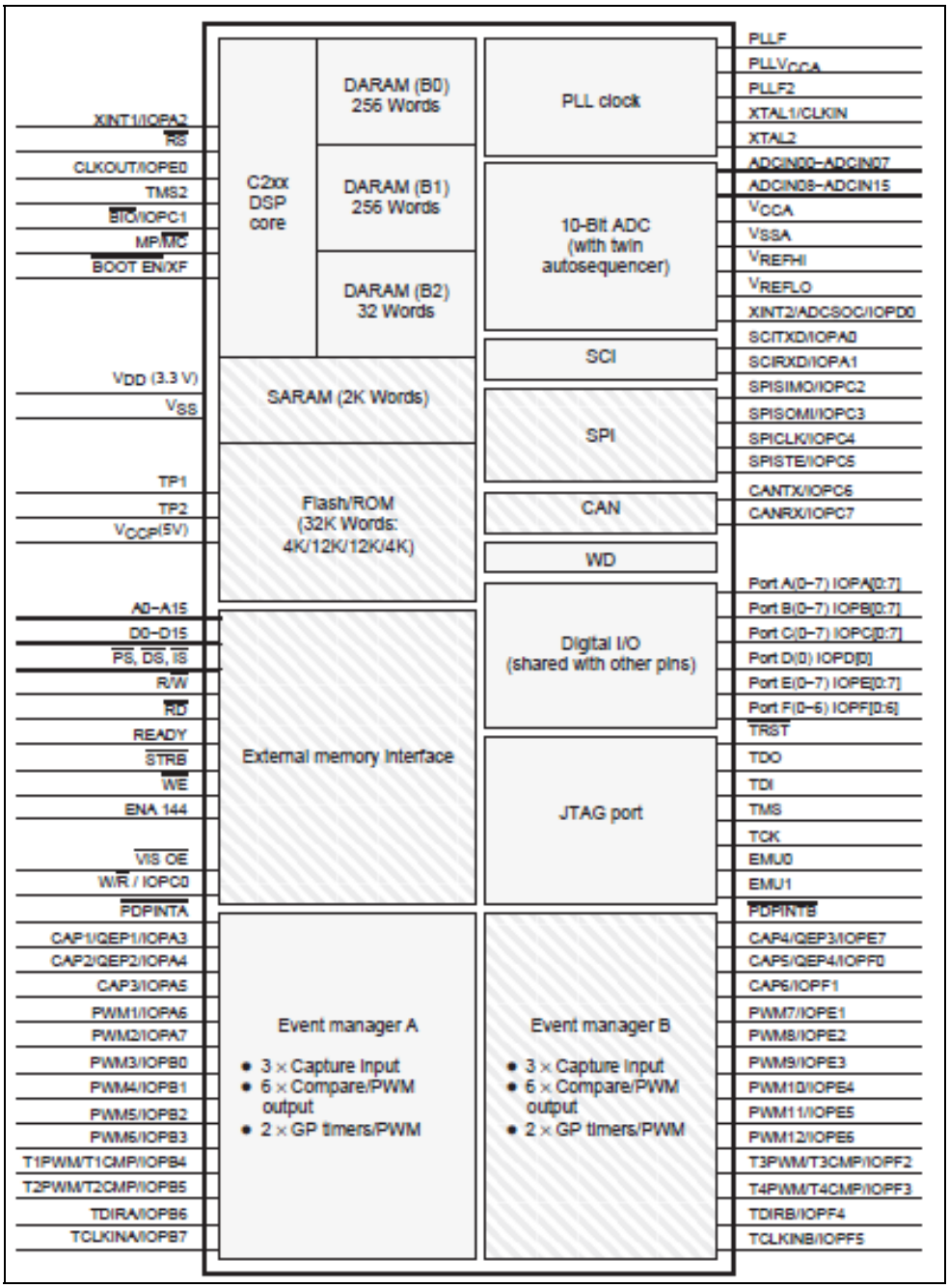

Fig.6.3 A graphical overview of 240xA device

➢ **On-chip Dual Access RAM (DARAM):**

The ’C24x has 544 words of on-chip DARAM, which can be accessed twice per machine cycle. This memory is primarily intended to hold data, but when needed, can also be used to hold programs. The memory can be configured in one of two ways, depending on the state of the CNF bit in status register ST1.

When CNF = 0, all 544 words are configured as data memory.

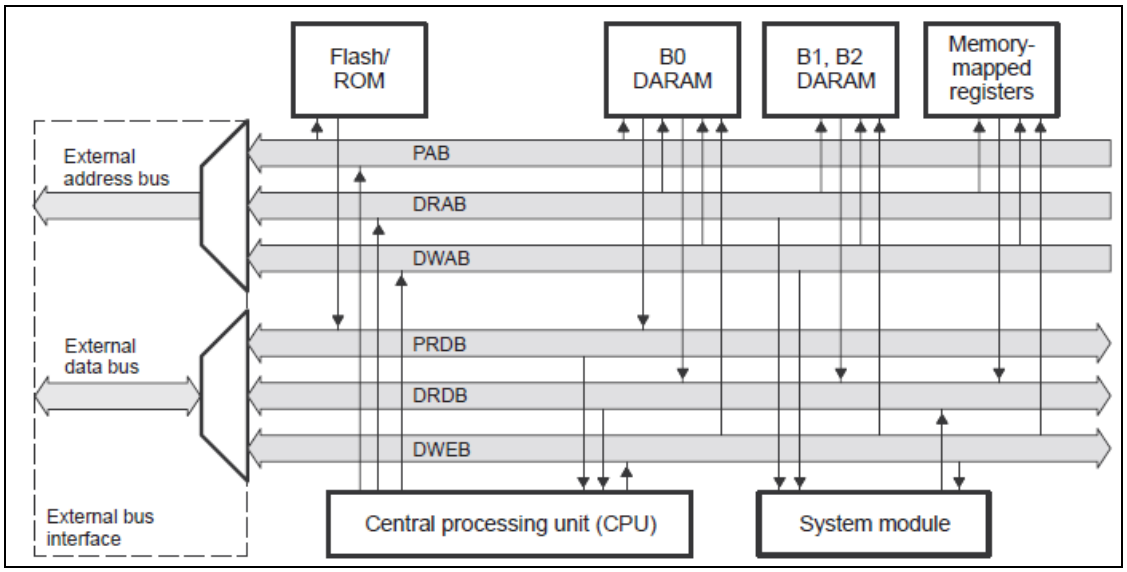

Fig. 6.4 ’C24x address and data bus structure

When CNF = 1, 288 words are configured as data memory and 256 words are configured as program memory.

Because DARAM can be accessed twice per cycle, it improves the speed of the CPU. The CPU operates within a 4-cycle pipeline. In this pipeline, the CPU reads data on the third cycle and writes data on the fourth cycle. However, DARAM allows the CPU to write and read in one cycle; the CPU writes to DARAM on the master phase of the cycle and reads from DARAM on the slave phase. For example, suppose two instructions, A and B, store the accumulator value to DARAM and load the accumulator with a new value from DARAM. Instruction A stores the accumulator value during the master phase of the CPU cycle, and instruction B loads the new value in the accumulator during the slave phase. Because part of the dual-access operation is a write, it only applies to RAM.

➢ **Central Processing Unit**

The ’C24x is based on TI’s ’C2xx CPU. It contains:

➢ A 32-bit central arithmetic logic unit (CALU)

➢ A 32-bit accumulator

- Input and output data-scaling shifters for the CALU
- A 16-bit × 16-bit multiplier
- A product-scaling shifter
- Data-address generation logic, which includes eight auxiliary registers and an auxiliary register arithmetic unit (ARAU)
- Program-address generation logic

6.4 Architecture of TMS320LF2407A

The TMS320LF2407A DSP controller is a programmable digital controller. The controller combines the power CPU with the on-chip memory and the peripherals. The controller offers 40 MIPS (million instruction per second) performance. This fast performance is well suited for processing control parameter in application where large amount of calculation are to be computed quickly.

The various parts of TMS320LF2407A architecture are:

1) C2xx DSP Core:

The C2xx DSP core is a 16-bit fixed point processor i.e. it works with 16-bit binary number. The DSP core consists of several sub components to perform arithmetic operations with 16-bit binary numbers. The components of C2xx DSP core:

I. Central Arithmetic Logic Unit (CALU)
II. Accumulator
III. Data scaling shifters
IV. Multiplier
V. Product scaling shifters
VI. Auxiliary register and auxiliary arithmetic unit (ARAU)

I. Central Arithmetic Logic Unit (CALU):

The DSP core performs 2's complement arithmetic using the 32-bit CALU. The CALU uses 16-bit words taken from the data memory, derived from an immediate instruction or from the 32-bit multiplier result. In addition to arithmetic operations, the CALU can perform Boolean operations.

II. 32-BIT Accumulator:

The accumulator stores the output from the CALU and provides an input to the CALU. The accumulator also performs shift and rotate operations. Its word length is 32-bit. The accumulator is divided into a high order word (bits 31 through 16) and a lower

order word (bits 15 through 0). Instructions in assembly language are provided for storing and loading the higher and lower order accumulator words to data memory.

III. Shifters:

The core contains the three 32-bit shifters that allow for scaling, bit extraction, extended arithmetic and overflow-prevention operation. The scaling shifters make possible commands that shift data left or right. The three different shifters are as below:

- **Input data-scaling shifters:** This shifters left shifts 16-bit input data by 0 to 16 bits to align the data to the 32-bitinput to the CALU.
- **Output data-scaling shifters:** This shifter left-shifts data from the accumulator by 0 to 7 bits before the output is stored to data memory. The content of the accumulator remain unchanged.
- **Product-scaling shifter:** The product register (PREG) receives the output of the multiplier. The product shifter shifts the output of the PREG before that output is sent to the input of the CALU. The product shifter has four product shift modes i.e. no shift, left shift by one bit, left shift by four bits and right shift by six bit, which are useful for performing multiply/ accumulate operations, fractional arithmetic or justifying fractional products.

IV. 16x16 bit parallel multiplier:

The multiplier perform a 16-bit two's complement multiplication with a 32-bit result in a single instruction cycles. The multiplier consists of three units: the T- register, P-register and multiplier array. The 16-bit T- register temporarily stores the multiplicand and the P-register stores the 32-bit product. Multiplier values either come from the data memory or delivered immediately from the MPY (Multiplier immediate) instruction words. The fast on-chip multiplier allows the device to perform fundamental operations such as convolution, correlation and filtering. Two multiply/ accumulate instructions in the instruction set fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously.

V. Auxiliary register arithmetic unit (ARAU) and Auxiliary registers:

The ARAU generates data memory addresses when an instruction uses indirect addressing to access data memory. Eight auxiliary registers (AR0 through AR7) supports the ARAU, each of which can be loaded with a 16-bit value from data memory or directly from an instruction. Each auxiliary registers are mainly used as "pointers" to data memory locations to more easily facilitate looping or repeating algorithms. The auxiliary register pointer (ARP) embedded in statue register ST0 references the auxiliary register.

2) Event Manager (EV):

There are two identical Event Managers (EV A and EV B) on TMS320LF2407A. The event manager is a most important peripheral in the digital motor control. It supports the functions needed for controlling the electromechanical devices. Each EV module in the TMS320LF2407A contains the following sub components:

I. Interrupt logic
II. Two general purpose timers
III. Three compare units
IV. Three capture units
V. Quadrature encoder pulse circuit

I. Interrupt Logic:

EV interrupt sub-system is slightly different from the main interrupt and are arranged into three groups (A, B and C) and each group has its own mask and flag register and is assigned to particular CPU interrupt priority level at the PIE. EV interrupt are happen to be only at INT2, INT3 and INT4 CPU priority levels.

II. GP Timer:

A general purpose timer is configured to count up, down or continuously up and down. Each EV has two GP timers. Timer 1 & 2 for EV A and timer 3 & 4 for EV B. Timers are configured to generate interrupt or trigger another peripheral on certain cases such as timer overflow, underflow or compare.

III. Compare Unit:

A PWM signal can also be generated using compare unit. Their functions are identical to GP Timer compare units. The PWM outputs associated with the compare unit allows for generation of six PWM outputs per EV whereas GP timer associated for two PWM outputs.

IV. Capture Unit:

The capture unit on TMS320LF2407A allows an event on the capture pin to be time stamped by selected GP Timer. Capture units 1, 2 and 3 are associated with EV A while capture units 4, 5 and 6 are associated with EV B.

V. Quadrature Encoder Pulse:

QEP's are two sequences of pulses which have a variable frequency and are 90º out of phase with each other. QEPs' are usually generated by position speed sensing device such as a rotary optical encoder. Each EV module has a QEP circuit associated with capture unit.

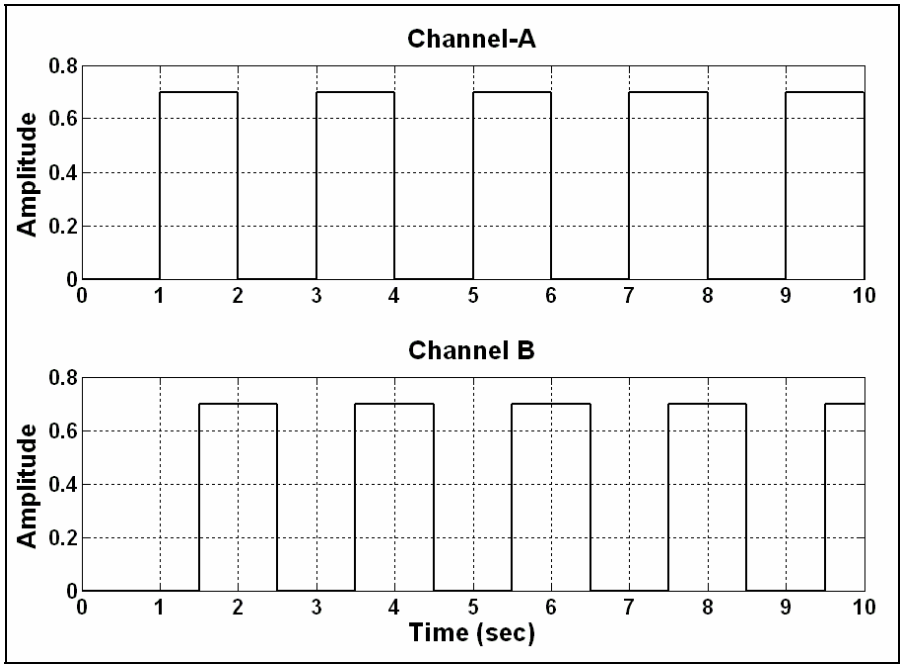

Fig. 6.5 Quadrature encode pulses

3) Controller Area Network (CAN):

CAN module is a useful peripheral for specific application of TMS320LF2407A. The CAN module is used for multi-master serial communication between external hardware. The CAN bus has a high level of data integrity and is ideal for operation in noisy environment such as in automobile, or industrial environments that requires reliable communication and data integrity.

4) Serial Parallel Interface:

The SPI is a high speed synchronous serial input/ output port that allow a serial bit stream of program length to be shifted in and out of device at a programmed bit transfer rate. SPI mainly used for communication between DSP and external peripherals or another DSP devices. Typical uses of SPI include communication with external shift register, display drivers or ADC's.

5) Serial Communication Interface:

The programmable SCI module that supports asynchronous serial digital communication between CPU and another asynchronous peripherals that uses standard NRZ (non return to zero) format. It is used for communication between external device and CPU.

The SCI transmits and receives serial data one bit at a time at programmable bit rate. The SCI's receivers and transmitter are double buffered and each has its own separate enable and interrupts bits. Both may be operated independently or

simultaneously in full-duplex mode. To ensure data integrity, the SCI checks data that has been received for break detection, parity, overrun and framing errors. The speed of bit rate is programmable to over 64K different speeds through a 16-bit baud select register.

6) Watch Dog Timer (WD):

The watchdog timer (WD) peripherals assets a system reset when it's internal counter overflows. The WD timer will count for special amount of time. It is necessary for the user's software to reset the WD timer periodically so that unwanted reset does not occur. When the software enters into endless loop or CPU is disturbed, the WD timer will overflow and DSP reset will occurs which cause the DSP program to branch to its starting point. In this way WD ensures reliability of CPU, thus ensuring system integrity.

7) Phase Lock Loop Clock Module (PLL):

The PLL module is basically an input clock multiplier that allows the user to control the input clock frequency of DSP processor. External to the processor a clock reference is generated by a oscillator crystal. This signal is then used to clock the DSP core and is multiplied or divided by PLL. Use multiplication factor ranges from 0.5x to 4x that of the external clock signal. The default value of PLL is 0.5x.

8) Analog to Digital Converter:

The ADC on TMS320LF2407A allows the DSP to sample the analog voltage signals. The O/P of ADC is an integer number which represent voltage level sampled, ADC will generate a 10-bit numbers for every conversion it performs. The10 MSB's are ADC results and LSB's are filled with zero, hence value in resultant register is simply right shifted by six places.

9) Join Test Action Group (JTAG) Port:

JTAG provides a standard method for emulation and development by interfacing the personal computer and TMS320LF2407A DSP controller. The XDS510PP+ or equivalent emulator pod provides the connection between the JTAG module on TMS320LF2407A and the personal computer. The JTAG allows PC to make full control over DSP processor and it can be used with code composer.

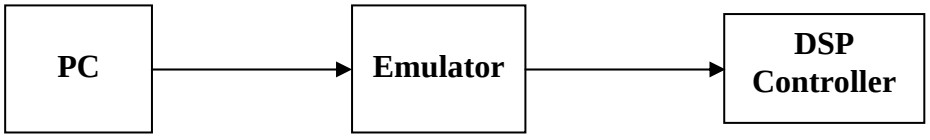

Fig.6.6 Interfacing of PC to Micro-2407

CHAPTER-7
DESCRIPTION OF MICRO-2407 TRAINER BOARD

7.1 Features of Micro-2407

- Based on TMS320F2407 DSP Processor.
- 16kw On-board PM
- 32kw on-board DM
- Battery backup facility for on-board RAM
- Expansion connector facility for project purpose
- 16 × 2 LCD Display for standalone operation
- On-board IBM AT keyboard interface
- Built-in 230V AC at 50Hz SMPS Power Supply
- Connector provision for ADC input and PWM outputs
- On-chip serial interface
- Debugger software with Assembler & Dissembler
- Dual channel DAC with 12 bit resolution
- Isolated serial port
- 16 bit digital output lines

The pictorial view of the Micro-2407 is shown in fig. 7.1 [12]. The list of the components on the Micro-2407 board is as follows:

Table 7.1 List of components on Micro-2407

Sr. No	Name of the component	Reference on kit
1.	Regulator IC LM317	VR1
2.	ADC Buffer IC's 3403	U27 U28 U29 U30
3.	DAC IC AD8582	U32
4.	IC TL084	U31
5.	EPROM IC's W 27C512	U1 U5
6.	RAM IC's 71204	U2

		U3 U6 U7
7.	74LS 214 IC's	U33 U34 U35
8.	Back up battery	X1
9.	Buffer IC's 74LS245	U17 U18 U19 U20
10.	DC to DC Converter Ic DC010505	U4
11.	MAX232	U21
12.	IC7406	U9 U10
13.	6N137	U15 U16
14.	Switches	SW1 SW2 SW3 RES
15.	74LS273 IC's	U25 U26
16.	CD 4015 IC's	U36 U37
17.	PAL 16L8	U12 U13
18.	IC 273	U8 U14
19.	IC 74LS14	U11
20.	IC 70151	U38
21.	SIP Resistor	SIP
22.	7400 IC's	U23

		U24
23.	Power Supply	P1 P3
24.	Serial Port Connector	P2
25.	40 Pin FRC Connector	P4
26.	14 Pin Male Connector	P5
27.	26 Pin FRC Connector	P6
28.	3 Pin J801 Connector	P7
29.	34 Pin FRC Connector	P8
30.	IBM PC/ AT KB Connector	P9
31.	Trim pot (100 k)	TP1
32.	Trim pot (10 k)	TP2
33.	Trim pot (100 k)	TP3
34.	Trim pot (10 k)	TP4
35.	Trim pot (100 k)	TP5

7.2 Front Panel Description

Front panel of Micro-2407 consists of the following:

I. ADC section
II. DAC section
III. PWM section
IV. Opto Coupler section
V. Inverter section
VI. SIP register section
VII. LCD and Keyboard interface
VIII. PAL section
IX. Signal Conditioning
X. Switches

1. ADC section:

The 16 ADC channels are terminated to the 26 pin header and the remaining 10 pins are grounded. The input analog signals are buffered using ICs 3403 (U27, U28, U29 and U30). Each buffer IC (3403) consists of four buffers. The ADC inputs are given

through the protection section to the processor. The protection section is built out of Zener regulators to prevent the processor from high voltage flow of above 3.3 volts.

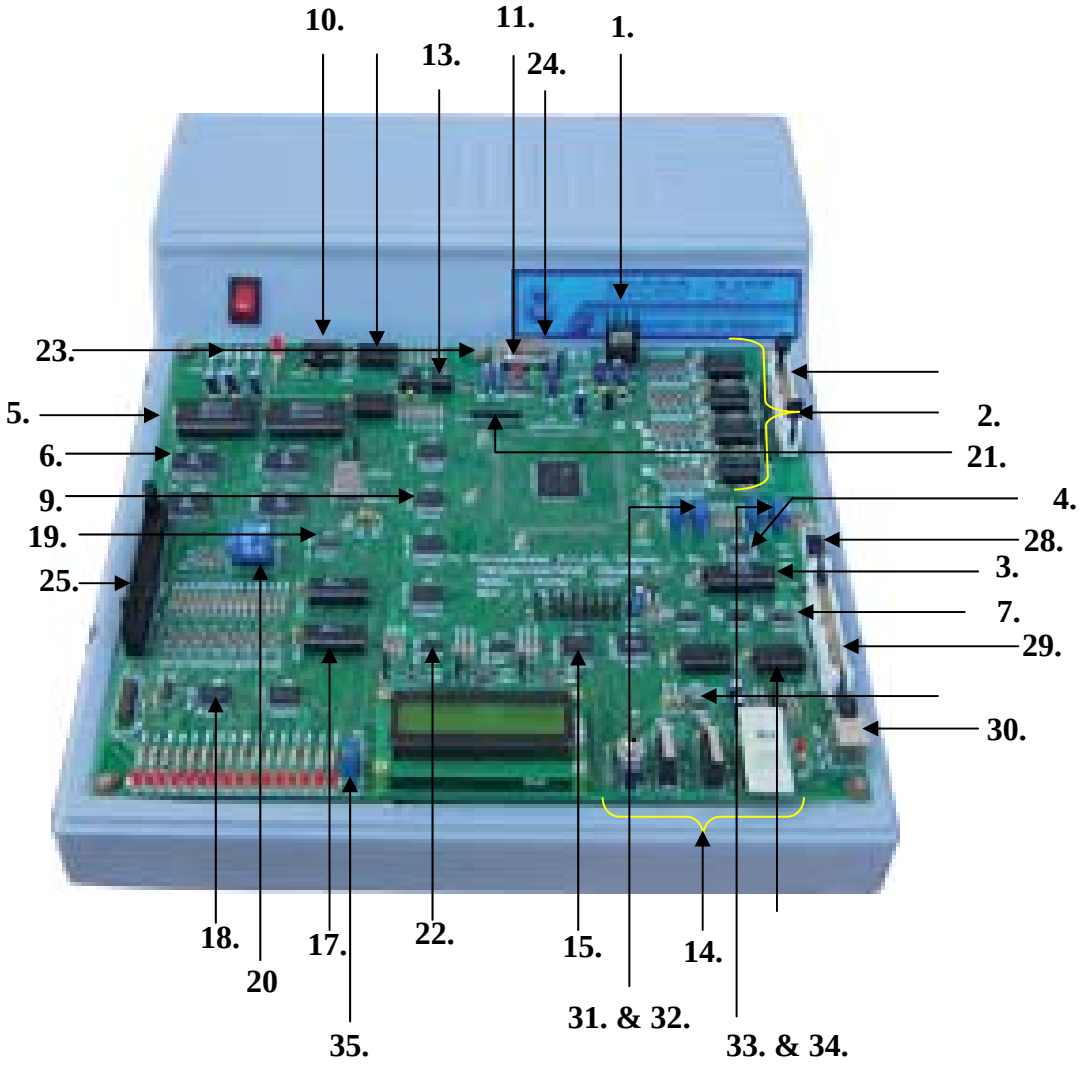

Fig. 7.1 Pictorial view of Micro-2407

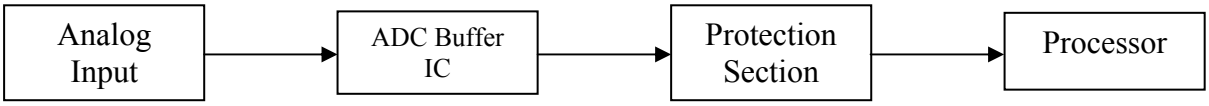

Fig. 7.2 Block diagram of ADC section

2. DAC Section:

The digital output from the processor is converted into analog using IC AD8582 (U32). It is a 2 channel DAC IC. The output from the DAC is of low voltage; hence IC TL084 is placed at the output of the DAC to amplify the DAC output. The trim ports are

provided at the output of DAC to adjust the offset and gain of channel-5. The output of DAC is terminated at the 3 pin J801 connector named as P7.

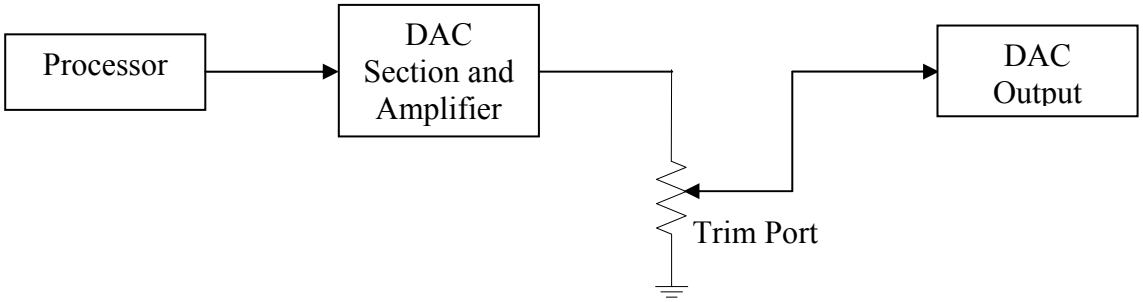

Fig. 7.3 Block diagram of DAC section

Table 7.2 Trim port functions

Trim Port	Functions
TP1	To adjust the offset of channel 2
TP2	To adjust the gain of channel 2
TP3	To adjust the offset of channel 1
TP4	To adjust the gain of channel 2

3. PWM Section:

In the PWM section three numbers of 74LS14 (U34, U 33, U35) ICs are provided. The default PWM output of the processor is high signals. The 74LS14 IC is provided to invert the PWM outputs to avoid shoot through faults. The 34 pin FRC header (P8) is provided to connect the PWM outputs from the processor. In this 34 pin header 4 pins are provided for TIMER PWM output and 6 pins are provided for capture inputs to the processor. Capture input is a square pulse input for e.g. Speed feedback from an encoder.

4. Opto Coupler Section:

To operate the kit through PC a MAX232 level detector along with the buffer inverter ICs 7436 (U9 and U10) and 6N137 (U15 and U16) are used for serial communication. The 6N137 opto-coupler IC is placed in between the two 7406 IC's to isolate the high voltage serial port side from the low voltage processor side.

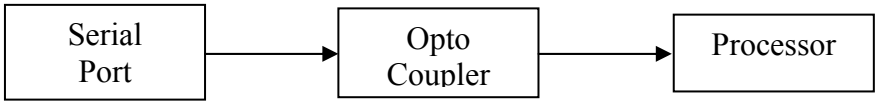

Fig. 7.4 Opto Coupler Block diagram

5. Inverter Section:

The IC 74LS14 (U11) is used to generate $\overline{RST}$

6. SIP Resistor:

The SIP resistor SIP1 of 10K is used to pull up the interrupts in the processor which are to be kept high.

7. LCD and Keyboard Interface:

The IC's 74LS273 (U25 and U26) are used for the LCD display and trim pot TP5 is used to adjust the brightness of the LCD. The IC's CD4015 (U36 and U37) are used as keyboard interface IC's for interfacing the keyboard to Micro-2407 trainer to work in mode2 (stand alone mode).

8. PAL Section:

Two numbers of PAL16V8B are used for the purpose of chip selection. The IC74LS273 (U14 and U18) are used as latch IC for LED's. Each IC 273 is used for 8 LED's glow. If a chip is selected through PAL, digital output is given to IC74LS173 and the data output to the corresponding address is high and the particular LED glows.

9. Signal Conditioning:

The power supply P3 provided to supply the analog V_{dd} (A V_{dd}) of the processor. The regulator (LM 317) VR1 is placed in between the power supply and the processor for converting the supply voltage 5V to desired 3.3V. The IC DC010505 (U4) is a DC voltage conversion IC to convert the input voltage of 5V to 3.3V for the isolated serial communications. The IC 70151 (U38) is used to divide the input voltage of 5V to 3.3V and 1.8V and given to (digital V_{dd}) processor. A 3.6V Ni-Cd battery backup is provided to supply RAM during power off.

10. Switches:

Two number of 7400 (U23, U24) ICs are placed at Micro-2407 kit. These ICs are provided to connect the processor I/O pins to the switches SW1, SW2 and SW3. The different switches and their function are described in table-7. 3.

Table 7.3 Switch functions

Switches	Functions
SW1	To select mode-1 or mode-2
SW2	Input switch
SW3	Input switch
RES	Processor reset switch

7.3 Jumper placed on MICRO-2407

The jumpers are one of the important parts of the trainer kit because as per the requirement the position of the jumper can be changed and accordingly the results can be obtained. The detailed information regarding the position and working of the each jumper places on the MICRO-2707 kit are described in the table 7.4

Table 7.4 Jumper Details

Jumper	Position	Function
J1	STRAP (Default)	To supply the protection circuit and ADC buffer ICs from regulator.
J2	STRAP A	To select B10 I/ O lines to high.
	STRAP B	To select B10 I/ O lines to low.
J3	STRAP A (Default)	To select microprocessor mode.
	STRAP B	To select micro controller mode.
J4	STRAP A	To select Vcc to high.
	STRAP B (Default)	To select Vcc to low.
J5	STRAP B (Default)	To connect PWM10 to ground.
J6	STRAP B (Default)	To connect PWM11 to ground.
J7	STRAP B (Default)	To connect PWM12 to ground.
J8	STRAP B (Default)	To connect T4 PWM10 to ground.
J9	STRAP B (Default)	To connect CAP5 to ground.
J10	STRAP B (Default)	To connect CAP6 to ground.
J11	STRAP B (Default)	To connect INT B (PDPINTB-) to ground.
J12	STRAP A	TRST high with emulator.
	STRAP B	TRST low with emulator.
J13	STRAP A (Default)	To operate in mode I.
	STRAP B	To operate in mode II.
J14	STRAP A (Default)	SW2 to decrease the speed.
J15	STRAP B (Default)	SW3 to increase the speed.
J16	STRAP (Default)	To have 3.3V for processor from voltage divider.

7.4 Connector Details

The following connectors are available on Micro-2407 trainer board.

P1- 5 pin Unicon Connector

P2- 9 pin Serial port Connector

P3- 2 pin J801 Connector

P4- 40 pin FRC Connector

P5- 14 pin JTAG Connector

P6- 26 pin FRC Connector

P7- 3 pin J801 Connector

P8- 34 pin FRC Connector

P9- 6 pin Keyboard Connector

- **Power Connector (P1):**

It is a single row 5 pin male connector. The details of the connector are shown in table 7.5

Table 7.5 Signal description of P1 connector

Pin	Details	Signal definition
1	GND	0 V reference ground
2	-12V	----
3	+12V	----
4	NC	No connection
5	VCC	+5 V power supply

- **Serial Port Connector (P2):**

It is a 9 pin male connector. The details of the connector are shown in table 7.6.

Table 7.6 Signal description of P2 connector

Pin	Details	Signal definition
1	NC	No connection
2	RxD	Receive data
3	TxD	Transmit data
4	NC	No Connection
5	GND	0 V reference ground
6	NC	No connection

7	RTS	Ready to send
8	CTS	Clear to send
9	NC	No connection

- **J801 2 Pin Connector (P3):**

It is a 2 pin connector. The details of the connector are shown in table 7.7.

Table 7.7 Signal description of P3 connector

Pin	Details	Signal definition
1	GND	0 V reference ground
2	+5V	+5 V power supply

- **General Purpose Input/ Output Connector (P4):**

It is a 40 male and female connector, which contains the PWM and GP timers for the use at various levels.

- **JTAG Connector (P5):**

It is a 14 connector with female socket of the same pin as output. JTAG (Join Test Action Group Port) is used for the interfacing between personal computer and the DSP processor.

- **ADC input FRC Connector (P6):**

It is a double row header 26 (13*2) pin male connector. The details of the connector are shown in table 7.8

Table 7.8 Signal description of P6 connector

Pin	Details	Signal definition
1	ADC8	Analog to Digital Converter pins
2	ADC15	
3	ADC0	
`4	ADC7	
5	ADC9	
6	ADC6	
7	ADC1	
9	ADC10	
11	ADC11	
13	ADC2	

15	ADC12	
17	ADC3	
19	ADC13	
21	ADC4	
23	ADC5	
25	ADC14	
8, 10, 12, 14, 16, 18, 20, 22, 24, 26	GND	0 V reference ground

- **J801 3 Pin Connector (P7):**

It is a 3 pin connector. The connector allows taking the analog signal generated by the DSP kit or processor and one can visualize the same on CRO. The details of the connector are shown in table 7.9.

Table 7.9 Signal description of P7 connector

Pin	Details	Signal definition
1	GND	0 V reference ground
2	DAC1 Output	Digital to Analog Converter signal at channel 1.
3	DAC2 Output	Digital to Analog Converter signal at channel 2.

- **PWM Output 34 Pin FRC Connector (P8):**

It is a 34 pin connector. The connector allows checking of the PWM signal as per requirement and one can visualize the same on oscilloscope. The details of the connector are shown in table 7.10

Table 7.10 Signal description of P8 connector

Pin	Details	Signal definition
1	PWM1	Pulse Width Modulation signal at pin 1
2	PWM2	Pulse Width Modulation signal at pin 2
3	PWM3	Pulse Width Modulation signal at pin 3
4	PWM4	Pulse Width Modulation signal at pin 4
5	PWM5	Pulse Width Modulation signal at pin 5

6	PWM6	Pulse Width Modulation signal at pin 6
7	PWM7	Pulse Width Modulation signal at pin 7
8	PWM8	Pulse Width Modulation signal at pin 8
9	PWM9	Pulse Width Modulation signal at pin 9
10	T1PWM	Timer 1 compare/ PWM output
11	T2PWM	Timer 2 compare/ PWM output
12	T3PWM	Timer 3 compare/ PWM output
13	CAP1	Capture unit 1 input
14	CAP2	Capture unit 2 input
15	CAP3	Capture unit 3 input
16	CAP4	Capture unit 4 input
17	PDPINTA-	Power driver protection interrupt of unit A
28	PWM10	Pulse Width Modulation signal at pin 10
29	PWM11	Pulse Width Modulation signal at pin 11
30	PWM12	Pulse Width Modulation signal at pin 12
31	T4PWM/ T4CMP	Timer 4 compare/ PWM output
32	CAP5/ QEP4	Capture unit 5 input/ QEP circuit input 1
33	CAP6/ I/ O	Capture unit 6 input
34	PDPINTB-	Power driver protection interrupt of unit B
18	Vcc	+ 5 V power supply
19	Vcc	+ 5 V power supply
20-27	GND	0 V reference ground

- **IBM PC Keyboard Connector (P9):**

It is a 6 pin connector. The connector allows working with the DSP kit Micro-2407 in stand alone mode. The details of the connector are shown in table 7.11.

Table 7.11 Signal description of P9 connector

Pin	Details	Signal definition
1	NC	No connection
2	KBDATA	Serial data from key board
3	Vcc	+ 5 V power supply
4	GND	0 V reference ground

5	NC	No connection
6	KBCLK	key board clock

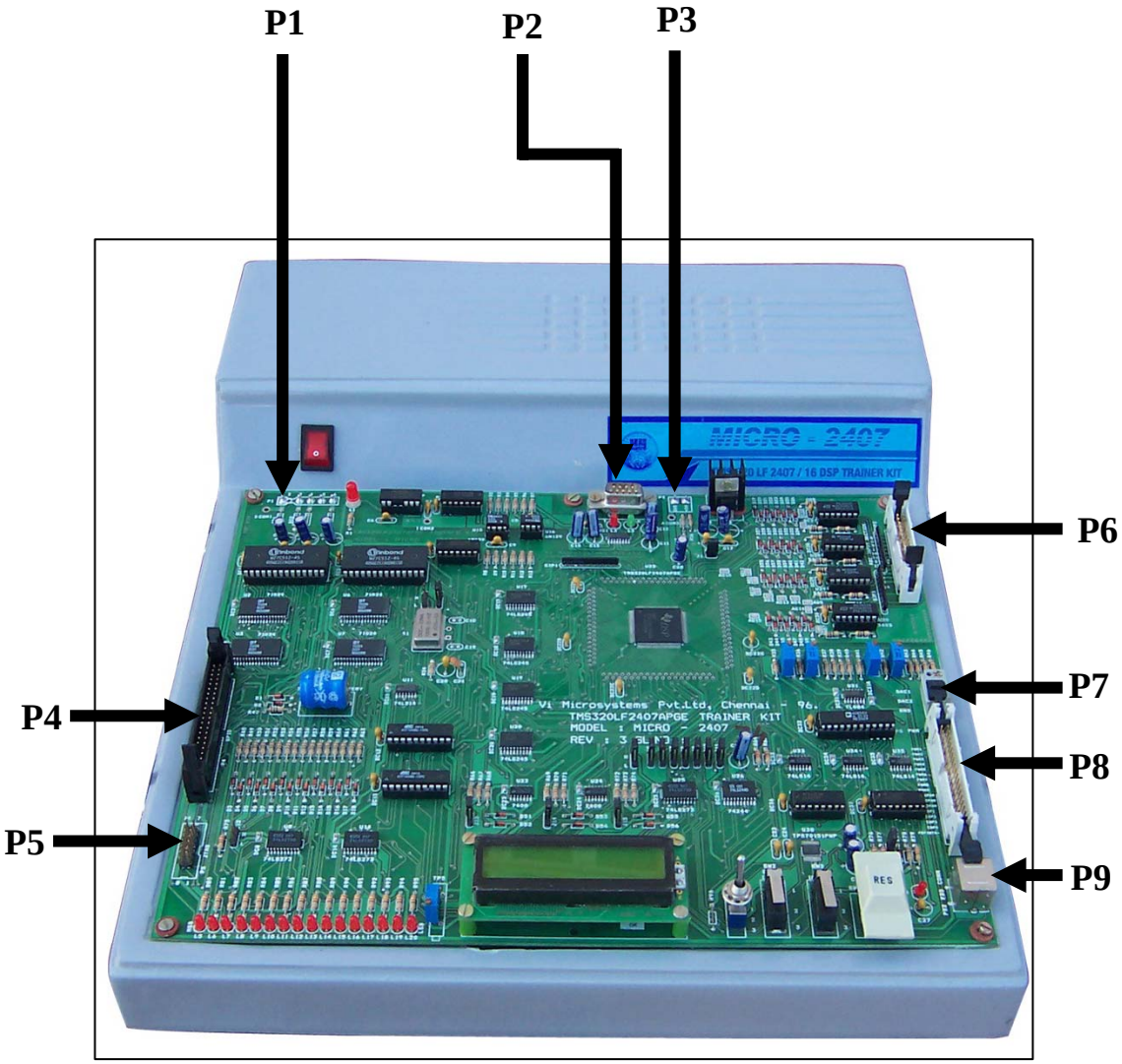

Fig. 7.5 Pictorial view of Micro-2407 with connector details

The place of the each connector on the kit is shown in the fig. 7.5. The details of the connectors with their notations are as under:

P1- Power connector

P2- Serial port connector

P3- J801 2 pin connector

P4- General purpose input/ output connector

P5- JTAG connector

P6- ADC input FRC connector

P7- J801 3 pin connector (DAC connector)

P8- PWM output FRC connector

P9- IBM PC keyboard connector

CHAPTER-8
DESIGN OF GATE DRIVER CIRCUIT

8.1 Design Consideration

The primary function of a driver circuit is to switch a power semiconductor device from the off state to the on state and vice versa [13]. In most situations the designer seeks a low cost drive circuit that minimize the turn-on and turn-off times so that the power device spends little time in traversing the action region where the instantaneous power dissipation is large. In the on state the drive circuit must provide adequate drive power to keep the power switch in the on state where conduction losses are low. Very often the drive circuit must provide reverse bias to the power switch control terminals to minimize turn-off times and to ensure that the device remains in the off-state and is not triggered on by stray transient signals generated by the switching of the other power devices.

The signal processing and control circuits that generate the logic-level control signals used to turn the power switch on and off are not considered part of the drive circuit. The drive circuit is the interface between the control circuit and power switch. The drive circuit amplifies the control signals to levels required to drive the power switch and provides electrical isolation when required between the power switch and the logic-level signal processing/ control circuits. Often the drive circuit has significant power capabilities compared to the logic-level control/ signal processing circuits.

In order to operate power semiconductor devices at high switching frequencies, drive circuit must be designed to turn-off the as rapidly as they turn-on. The descriptions of the switching characteristics of switching devices illustrate the need for a reverse bias to be applied to the control terminals of the power switch in order to affect the rapid turn-off. Drive circuit with unipolar outputs are unable to provide the needed reverse bias and thus are incapable of providing fast turn-off of power devices. In order to provide a reverse bias to the control terminals of the power device, the drive circuit must have a bipolar output (an output that can be either positive or negative). This in turn requires that the drive circuit be biased by a negative power supply as well as a positive power supply. The BJT base drive circuit is shown in fig. 8.1 where both a positive and negative voltage supply with respect to the emitter is used provides a fast turn-off.

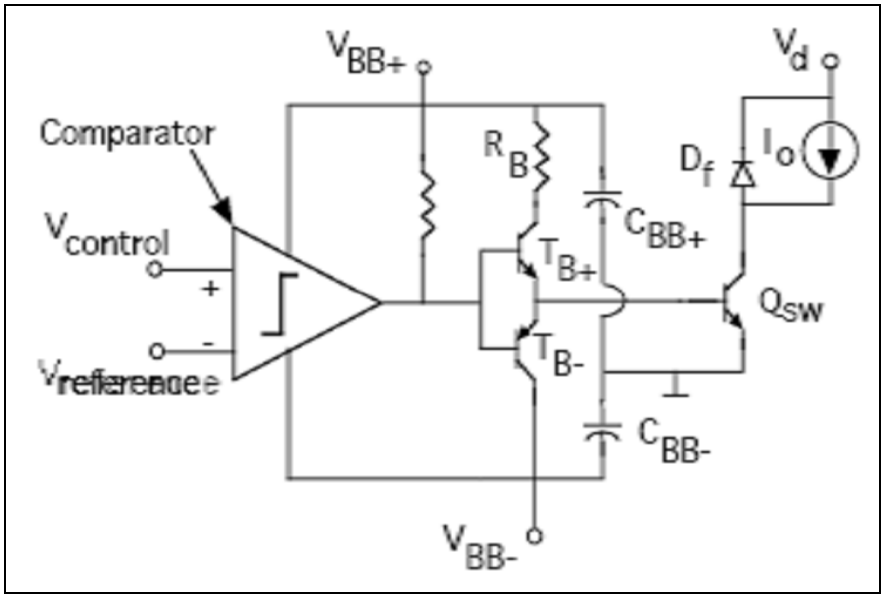

Fig.8.1 BJT base current driver circuit with both positive and negative voltages with respect to the BJT emitter for faster turn-off of the power device

8.2 Electrically Isolated Drive Circuit

There is a need for electrical isolation between the logic-level control signals and the drive circuits. The basic ways to provide electrical isolation are either by optocouplers, fiber optics or by transformers. The optocoupler shown in fig 8.2 consists of a light emitting diode (LED), the output transistor and a built-in Schmitt trigger. A positive signal from the control logic causes the LED to emit the light that is focused on the optically sensitive base region of a photo transistor. The light falling on the base region generates a significant number of electron-hole pairs in the base region that causes the photo transistor to turn on. The resulting drop in voltage at the photo transistor collector causes the Schmitt trigger to change the state. The output of the Schmitt trigger is the optocoupler output and can be used as the control input to the isolated drive circuit. The capacitance between the LED and the base of the receiving transistor within the optocoupler should be as small as possible to avoid the retriggering at both turn-on and turn-off of the power transistor due to the jump in the potential between the power transistor emitter reference point and the ground of the control electronics. To reduce the problem, optocouplers with electrical shields between the LED and the receiver transistor should be used.

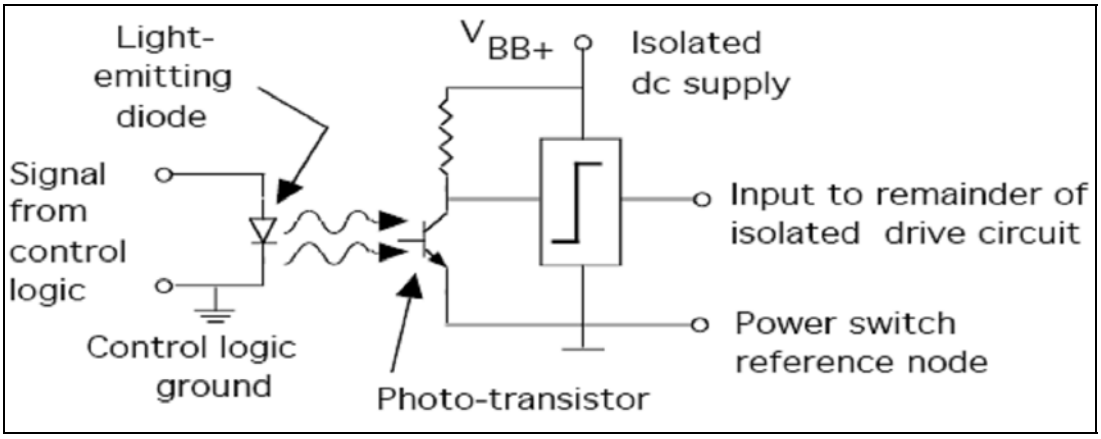

Fig.8.2 Schematic of an optocoupler used to couple signals to a floating (electrically isolated) drive circuit from a control circuit referenced with respect to the control logic ground (and power system neutral)

8.3 Optocoupler Isolated Drive Circuits

In optocoupler isolated drive circuits, the optocoupler itself is the interface between the output of the control circuit and the input of the isolated drive circuit. The input side of the optocoupler is directly coupled to the control circuit and the output side of the optocoupler is directly connected to the isolated drive circuit. The topology of the isolated drive circuit between the output of the optocoupler and the control terminal of the power switch can take many different forms.

An optocoupler-isolated drive circuit for a power BJT is shown in fig. 8.3. The drive circuit has a bi-polar output so that rapid turn-on and turn-off of the BJT can be achieved. An npn-pnp totem circuit couples the appropriate dc voltage to the base of the power BJT to turn it on or off as required. The isolated split dc power supplies are implemented by the circuit segment in lower left side of fig. 8.3.

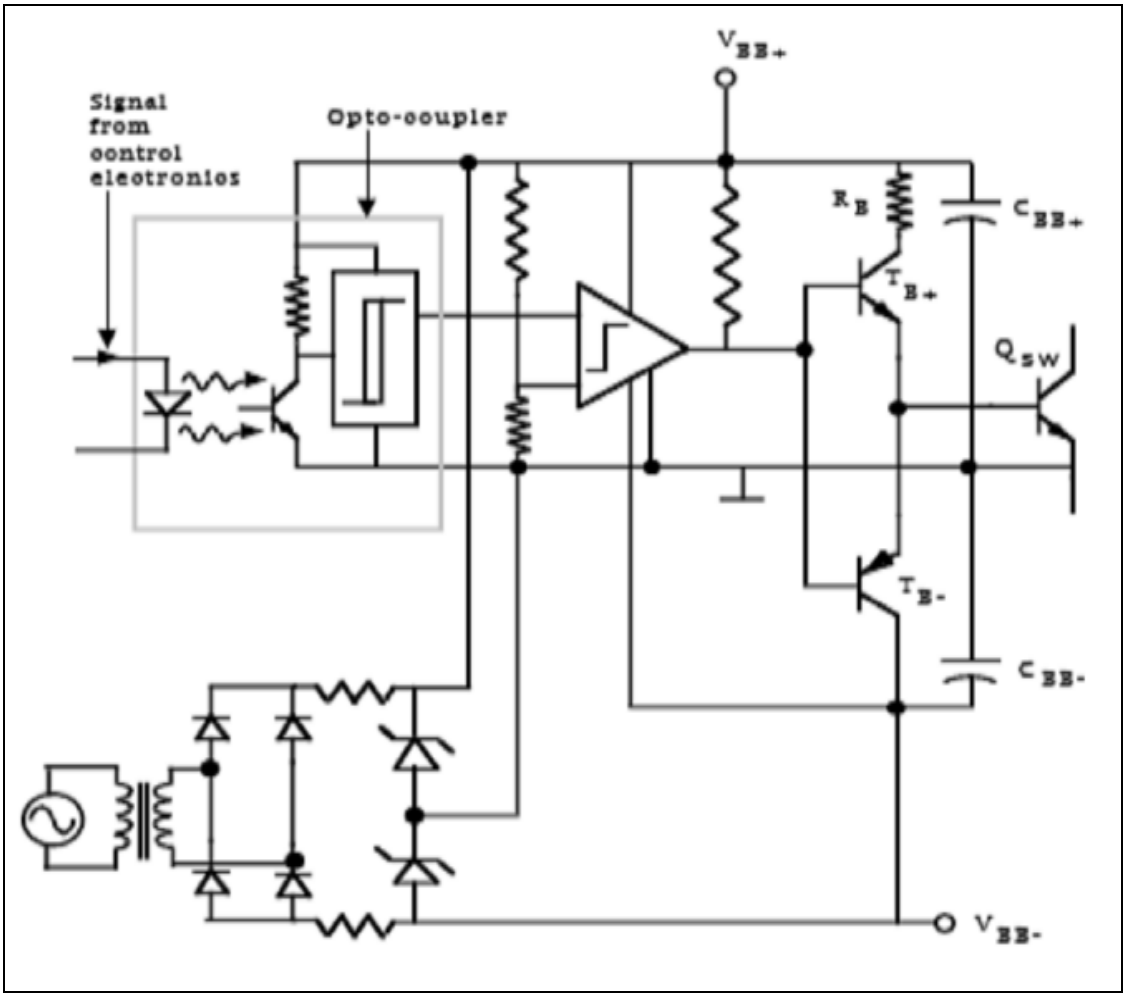

Fig.8.3 Opto coupler isolation of base drive circuits

8.4 IGBT Gate Drive Circuit

The schematic of IGBT based gate driver circuit used for the prototype front-end converter is shown in fig 8.4. The list of the various components used for the IGBT based gate driver circuit is tabulated in table 8.1.

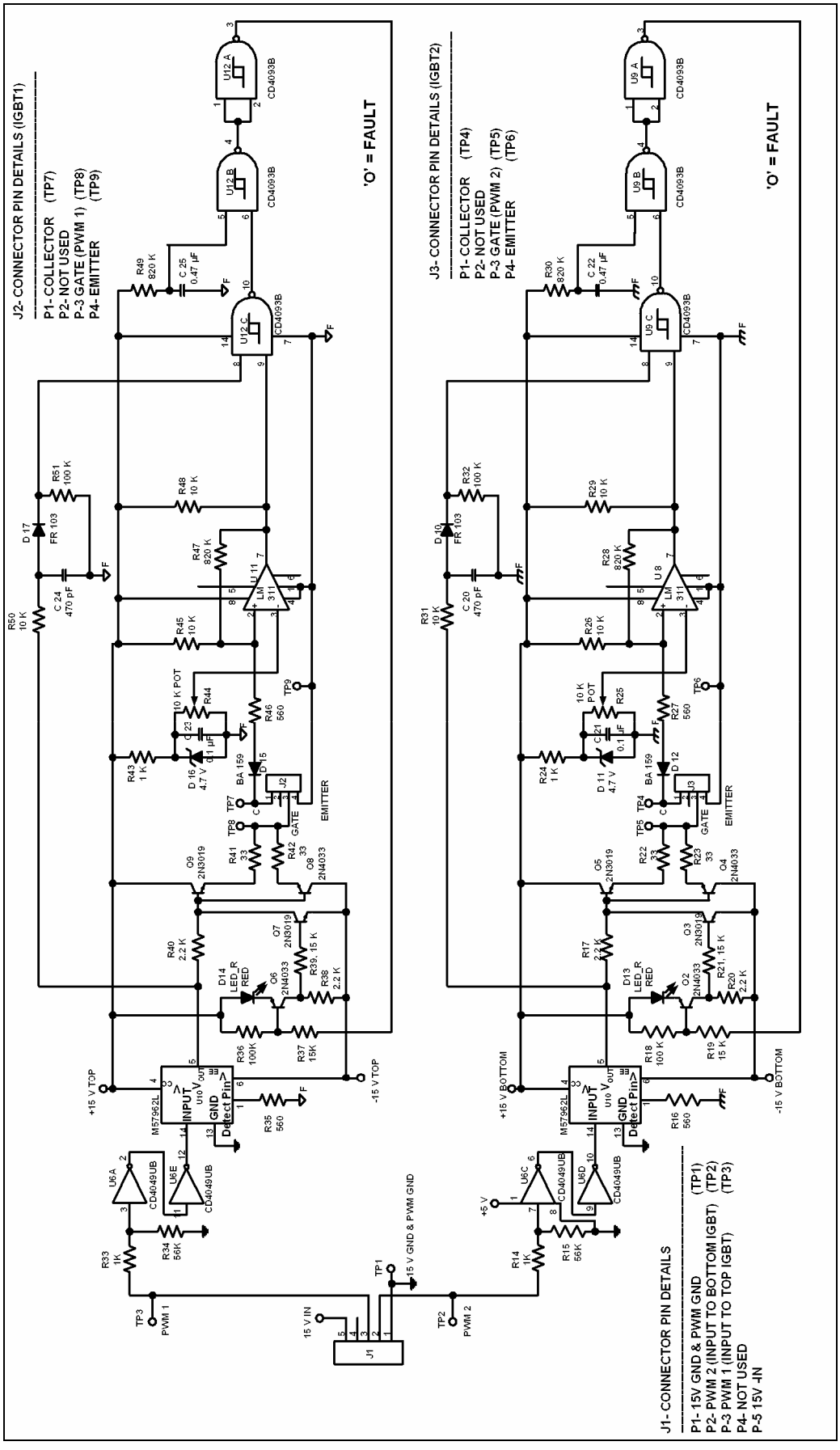

Fig 8.4 Schematic of IGBT based gate driver circuit used for the prototype front-end converter

Table-8.1 Components list for IGBT gate driver

Sr. No.	Quantity	Reference	Part No.
ICs			
2	4	U2, U3, U4, U5	LM7815
3	1	U6	CD4049UB
4	2	U12, U9	CD4093B
5	2	U7, U10	M57962L OPTO ISOLATOR
6	2	U11, U8	LM311
Transistors			
8	4	Q2, Q4, Q6, Q8	2N4033
9	4	Q3, Q5, Q7, Q9	2N3019
Diodes			
10	8	D2, D3, D4, D5, D6, D7, D10, D17	FR103
11	2	D12, D15	BA159
13	2	D14, D13	LED RED
14	2	D11, D16	4.7V ZENER DIODE
Capacitors			
15	2	C20, C24	470 pF
18	6	C11,C12,C13,C14,C21,C23	0.1 μF
19	2	C22,C25	0.47 μF
Electrolytic Capacitors			
21	4	C6, C7, C8, C9	47 μF/ 35V
22	5	C15, C16, C17, C18, C19	10 μF/ 25V
Resistors			
23	4	R22, R23, R41, R42	33 Ω

25	4	R16, R27, R35, R46	560 Ω
27	4	R14, R24, R33, R43	1 KΩ
28	4	R17, R20, R38, R40	2.2 KΩ
30	6	R26, R29, R31, R45, R48, R50	10 KΩ
31	4	R19, R21, R37, R39	15KΩ
33	2	R34, R15	56 KΩ
34	4	R18, R32, R36, R51	100 KΩ
35	4	R28, R30, R47, R49	820 KΩ
Trim Port			
36	2	R25, R44	100 KΩ POT

8.5 Results of Gate Drive Circuit

According to the requirement of the prototype front-end converter the gate driver circuit was prepared on the bread board for one converter only and results are obtained stage by stage i.e. across the each component of the gate driver circuit. The obtained results are satisfactory and as per the requirement. The obtained results are shown in fig. 8.5 to 8.10.

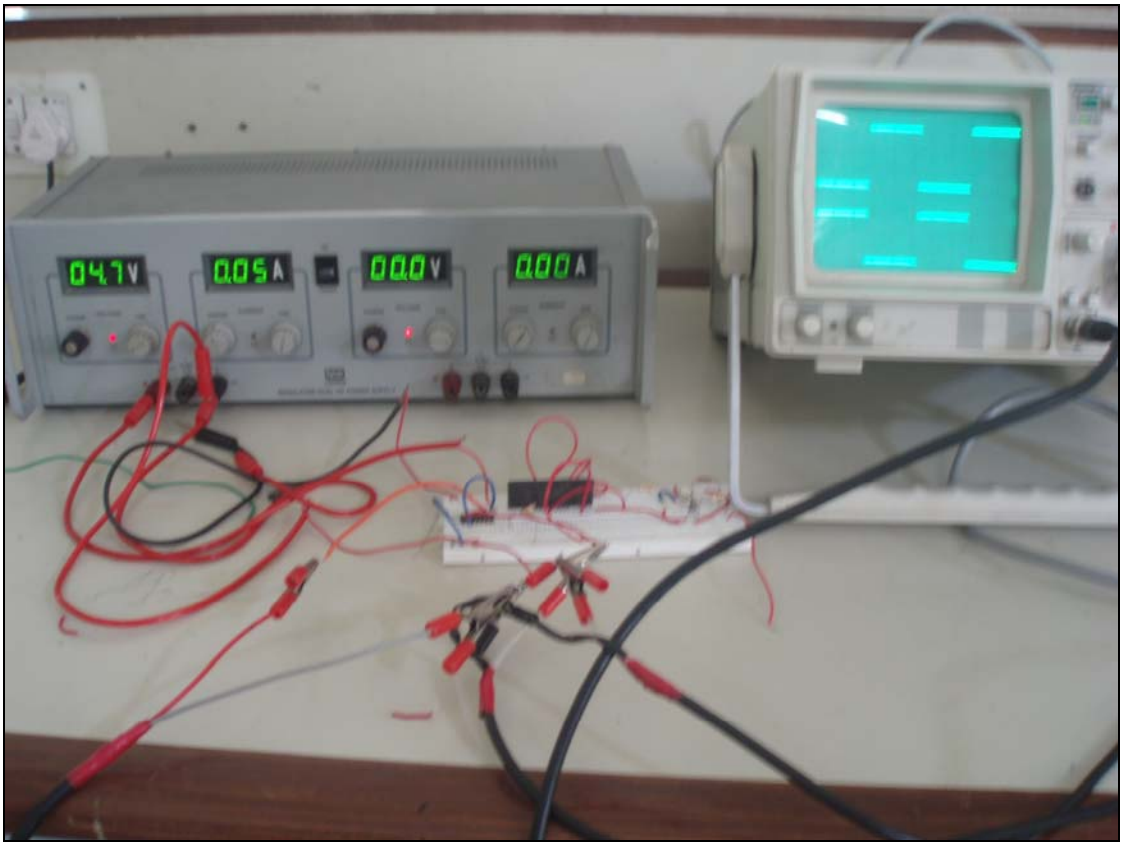

Fig.8.5 Pictorial view of test setup of IC CD4049UB

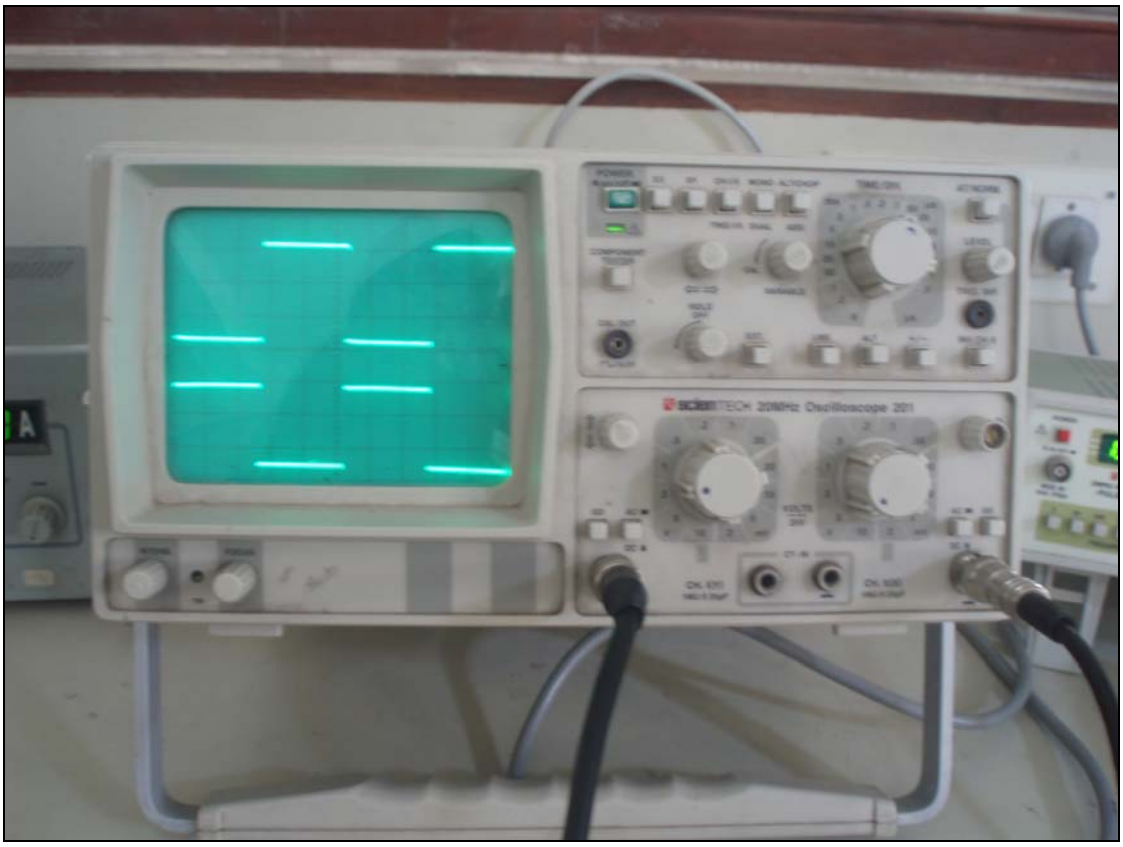

Fig.8.6 Pictorial view of output at IC CD4049UB

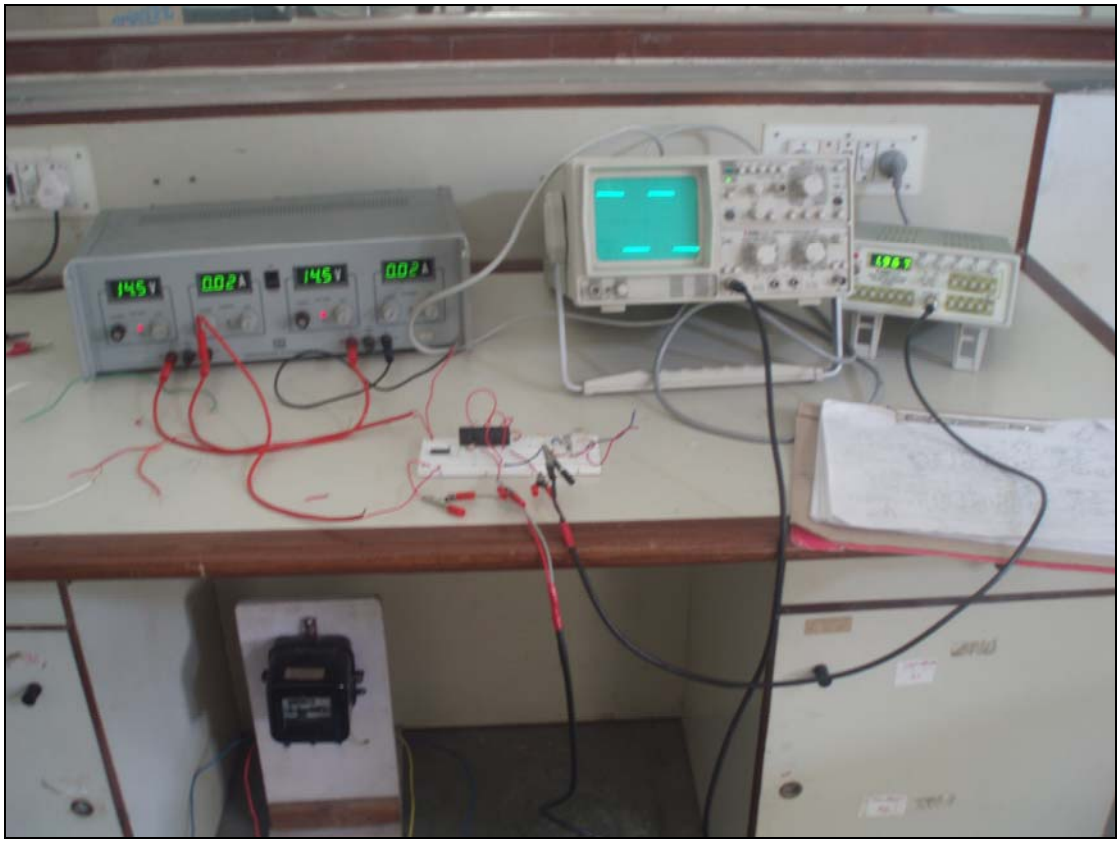

Fig.8.7 Pictorial view of test setup of IC M57962L

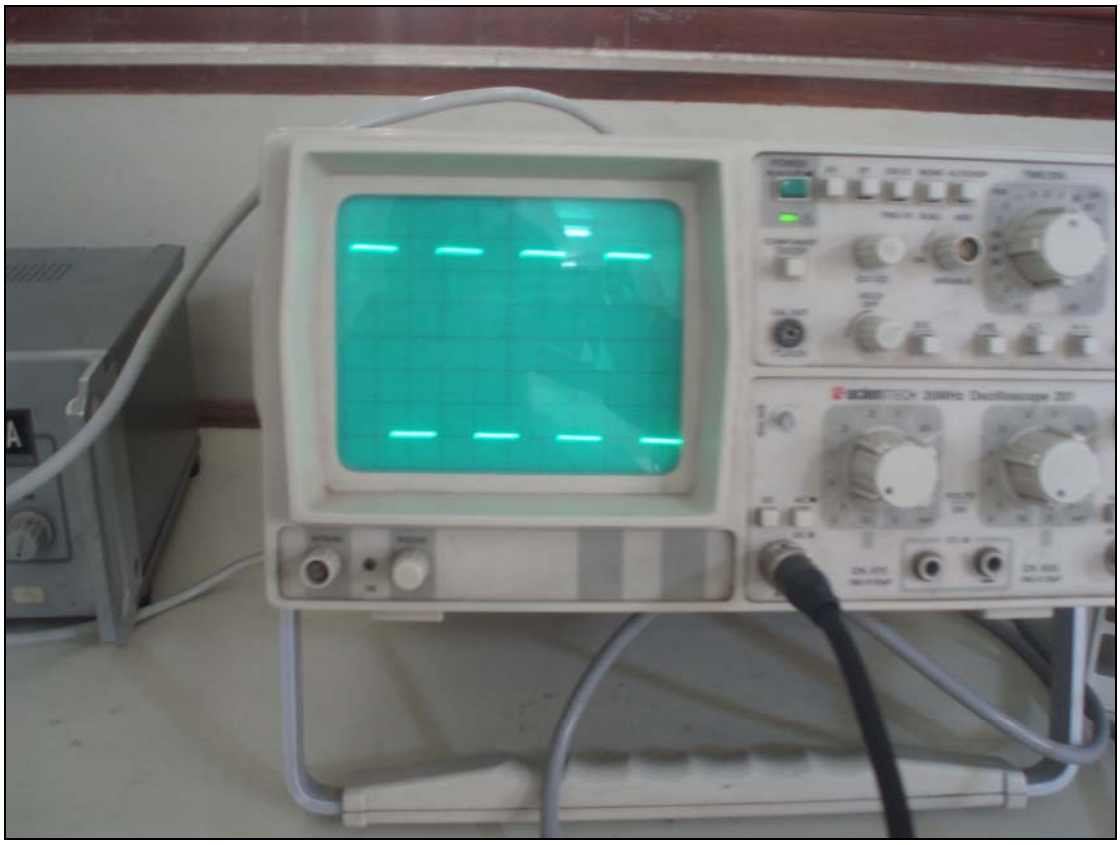

Fig.8.8 Pictorial view of output at IC M57962L

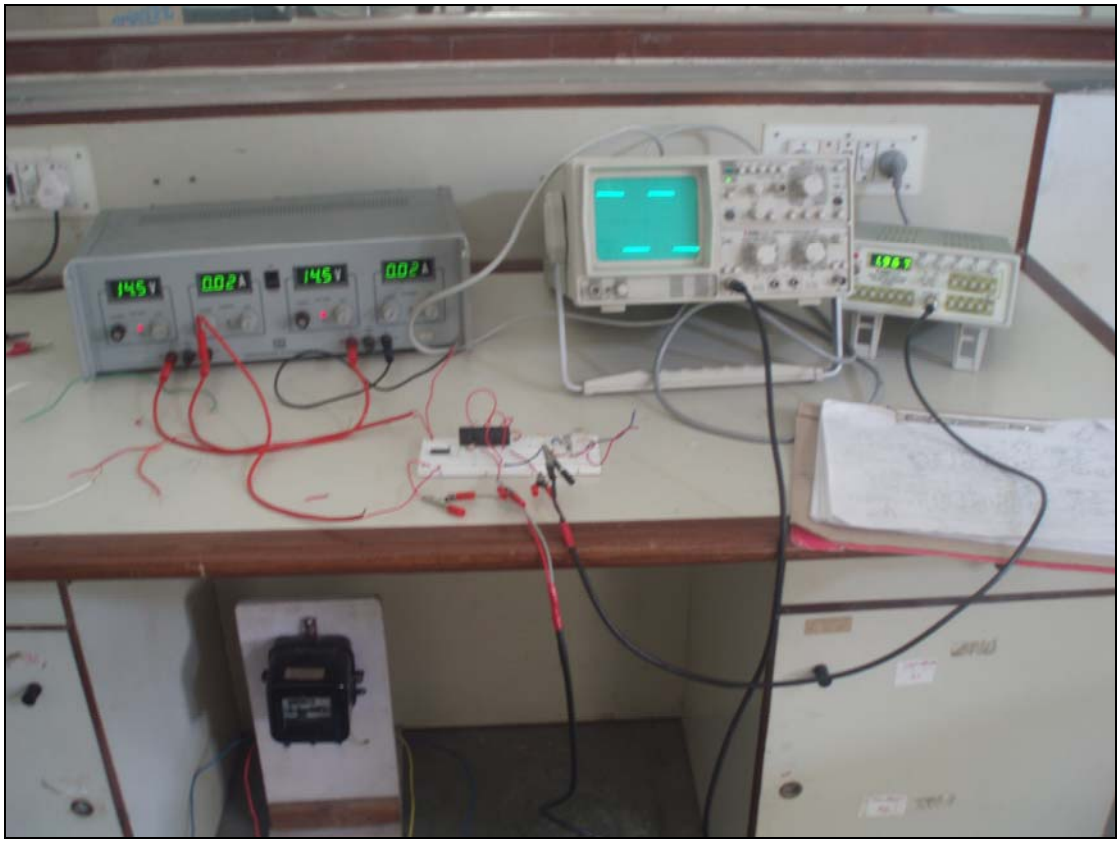

Fig.8.9 Pictorial view of output up to IC M57962L (OPTOCOUPLER ISOLATOR)

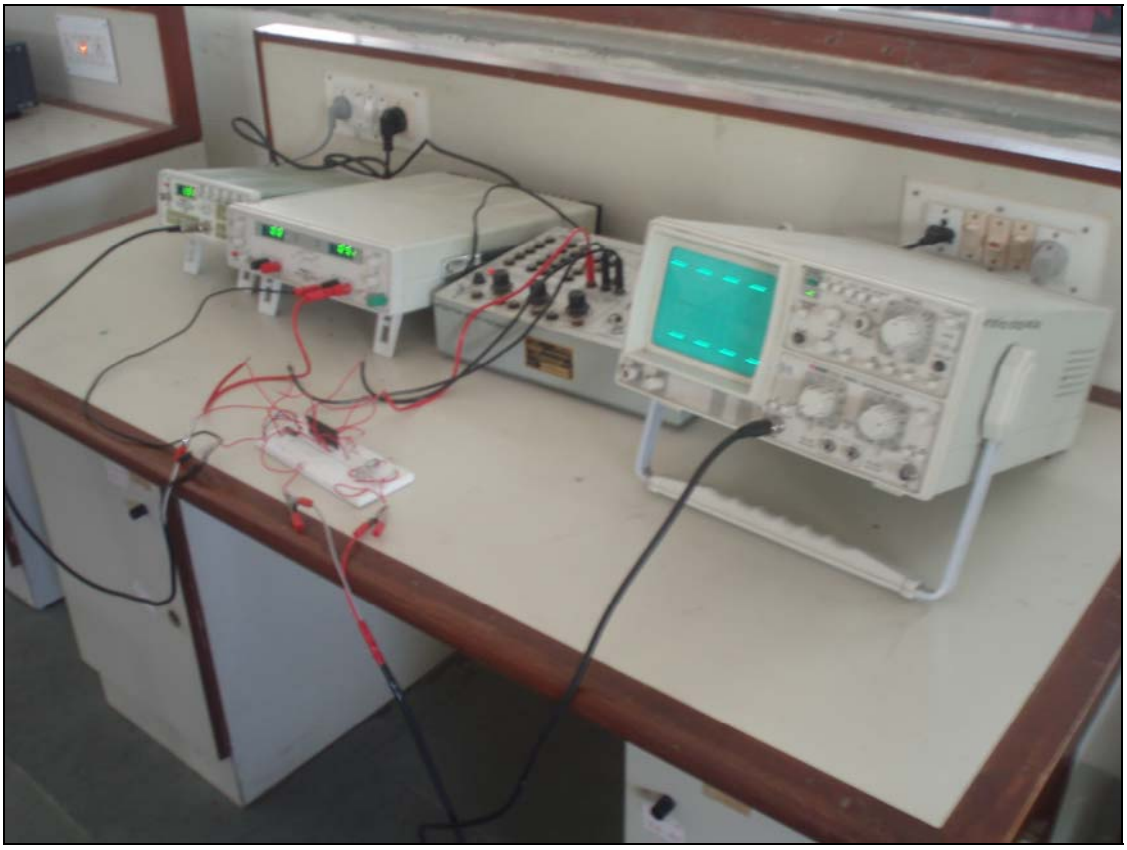

Fig.8.10 Pictorial view of output up to port TR_8 (Gate pulse)

8.6 Over Current Protection and Blanking Times for Bridge Circuits

In some applications the potential may exist for currents to flow through a power device that exceeds the device's capabilities. If the device is not somehow protected against the over currents, it may be destroyed. Power devices can't be protected against the over currents by fuses because they can't act fast enough. Over currents can be detected by measuring the device current and comparing it against a limit. At above the currents the power device is turned off by a protection network in the drive circuit.

A cheaper and normally better way of providing over current protection is to monitor the instantaneous output voltage of the device, for example, the collector-emitter on-state voltage of a BJT or drain-source voltage of a MOSFET. Fig. 8.11 shows a simple circuit to provide over current protection to a BJT based on this principle.

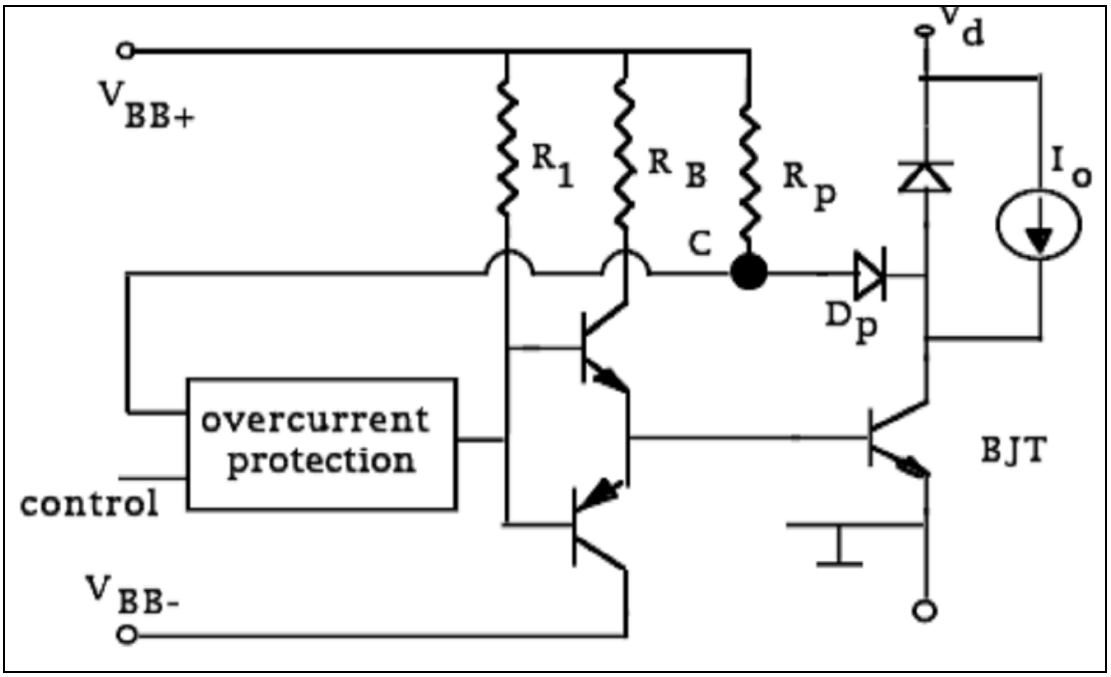

Fig.8.11 Over current protection by measuring the instantaneous on-state collector-emitter voltage of the power transistor

The voltage during the on-state at point C will be one forward-bias voltage drop above $V_{CE,\ sat}$. This voltage signal is one of the inputs to the over current protection block that requires the control signal as another input. When the transistor is supposed to be on, if the voltage at point C with some delay is above predetermined threshold, the over current is detected, and the protection block causes the base driver to turn the BJT off. Depending on the design philosophy, the over current system may be shut down after such an over current protection and may have to be manually reset.

In the half-bridge and full-bridge circuits, where two power devices i.e. transistor for example here, are connected in series in one converter leg, it is important to provide a blanking time so that turn-on control input to one transistor is delayed with respect to turn-off control input of the other transistor in the inverter leg. This blanking time should be chosen conservatively to be greater than worst-case maximum storage time of the transistor being used to avoid the cross conduction.

Under normal operation, such a conservatively chosen blanking time will cause a dead time equal to the blanking time minus the actual delay time to occur in which both the transistor in the inverter leg are off. This dead time introduces an unwanted nonlinearity in the converter transfer characteristics. This dead time can be minimize by the use of design enhancement to drive circuits, which minimize turn-on and turn-off delay times in power semiconductor devices being used as the power switches.

This blanking time in the control inputs can be introduced by the means of the circuit shown in fig. 8.12 where the control signal is common to both the BJTs of the converter leg. When control signal is high, the upper transistor T_+ should be on and vice versa. The polarized RC network and the Schmitt trigger introduce a significant time delay in the turn-on of the BJT and almost no time delay in the turn-off of the transistor. The difference of these two is the blanking time needed. The waveforms are shown in fig. 8.13 where when the bridge control input goes low, a significant time delay occurs in the control signal to turn on the bottom transistor T_- and almost no time delay occurs in turning off the upper transistor T_+. The blanking time and dead time are shown in fig. 8.13.

The schematic diagram of the dead time and blanking time circuit used for generating the dead band for the two IGBT of the same leg for the proposed converter is shown in fig. 8.14.

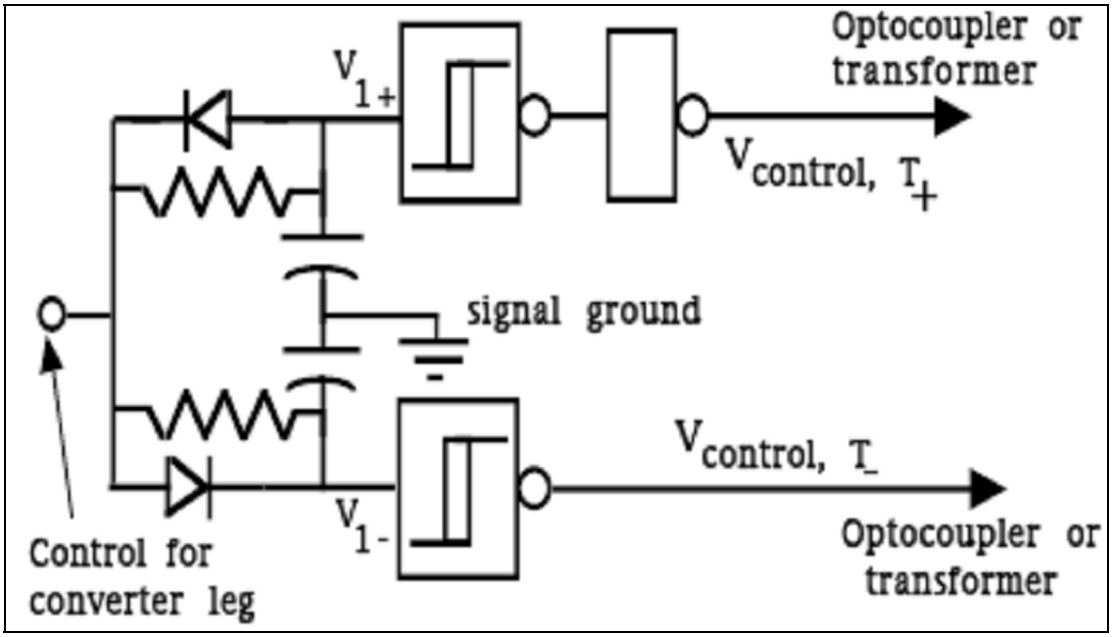

Fig.8.12 Circuit to provide blanking times to the base drivers

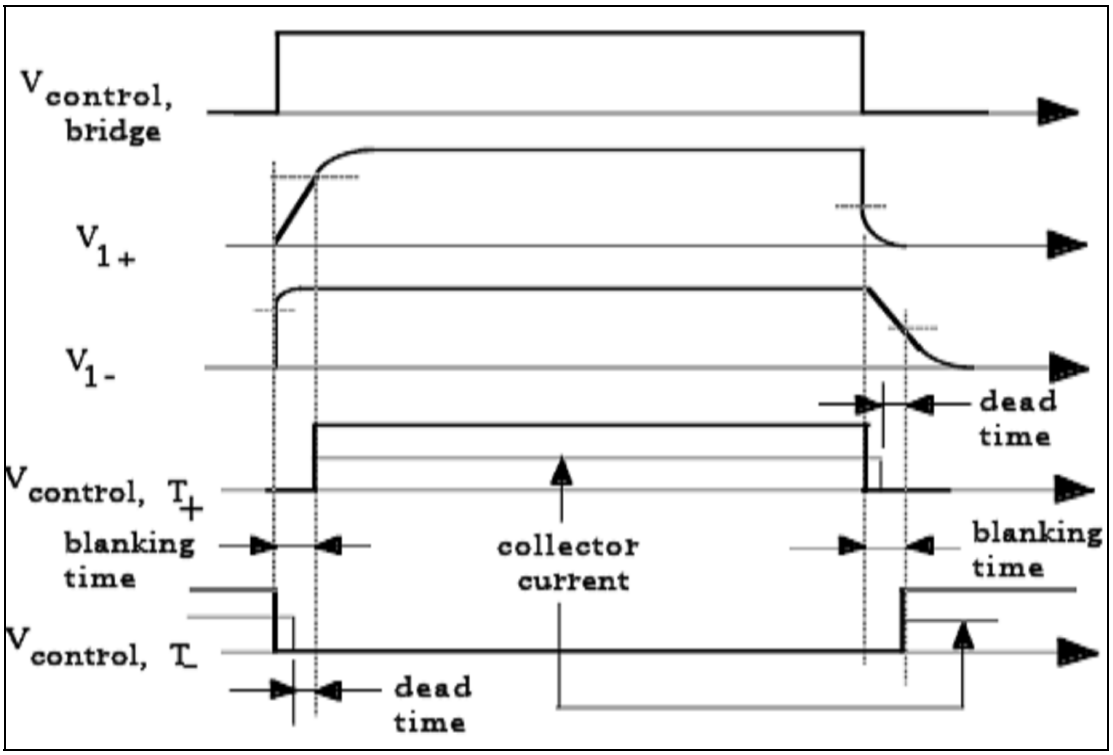

Fig.8.13 Collector current waveforms showing dead time and blanking time

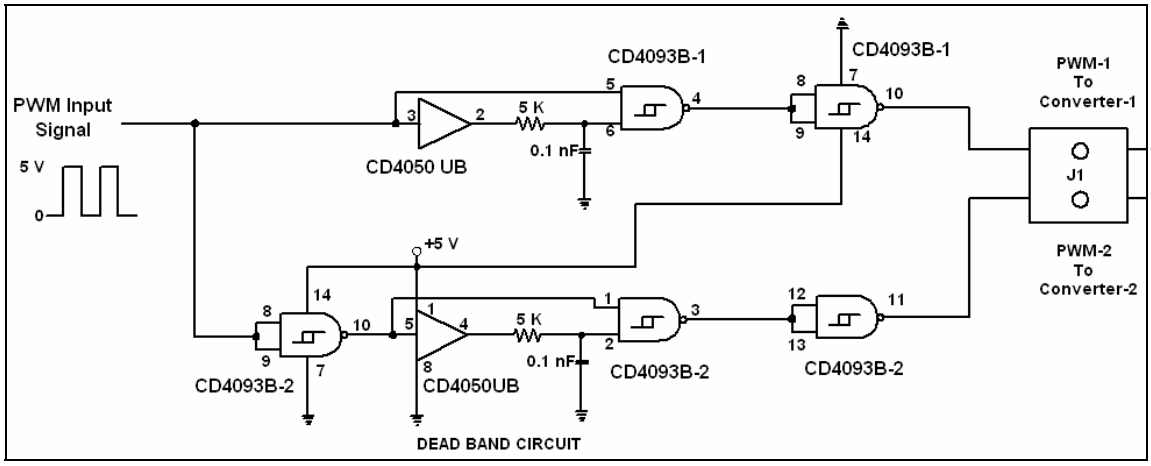

Fig.8.14 Schematic of dead band circuit

8.7 Results of Protection and Dead Band Circuit

According to protection requirement and blanking time the circuits are prepared on the bread board at initial stage and the various results are obtained. The obtained results are shown in fig. 8.15 to 8.22 and obtained results shows the satisfactory operation of protection circuit and dead band circuit for the prototype front-end converter.

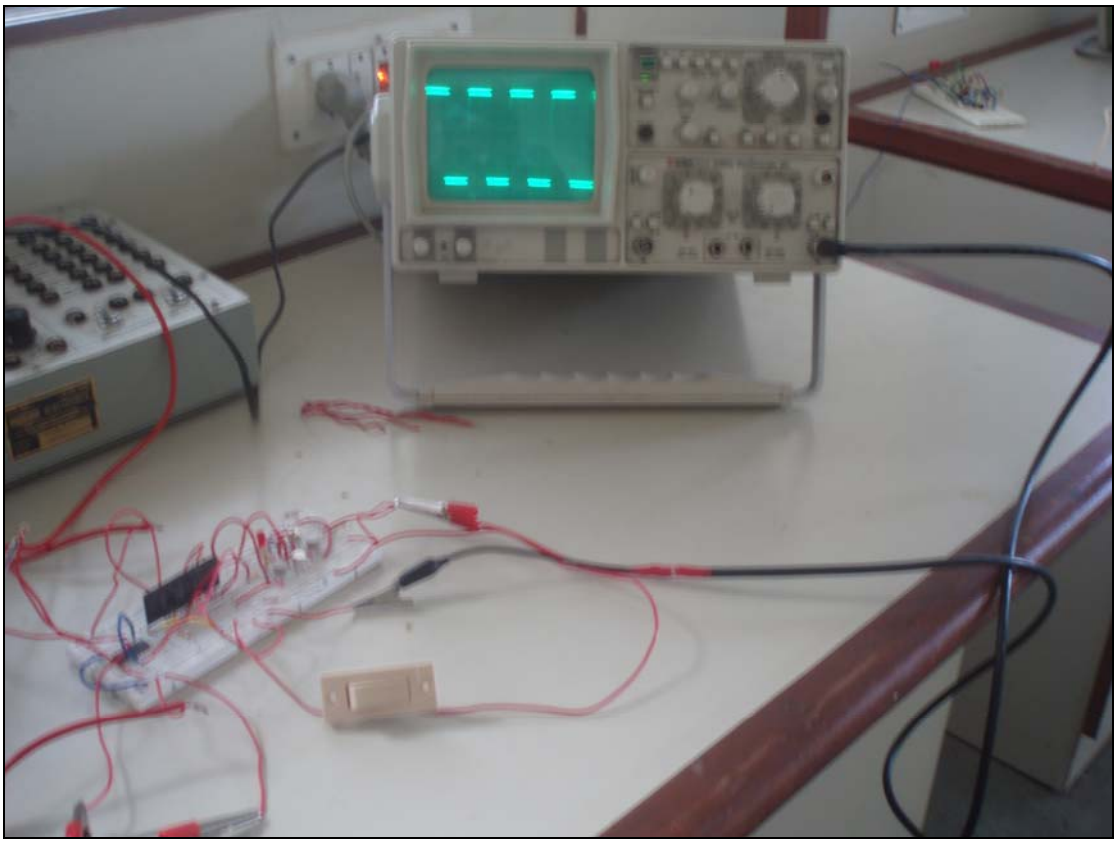

Fig.8.15 Pictorial view of setup for manual fault creation at output of port TR_8 (Gate pulse)

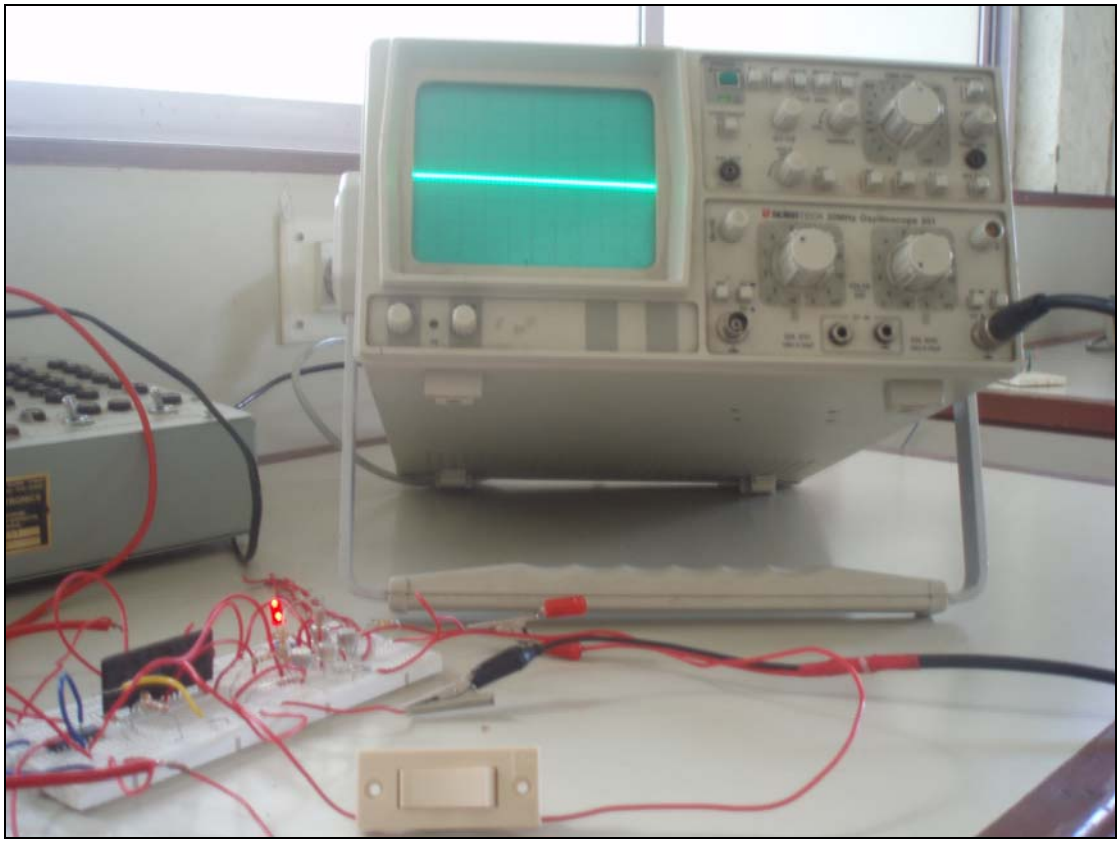

Fig.8.16 Pictorial view of output at port TR_8 (Gate pulse) after fault

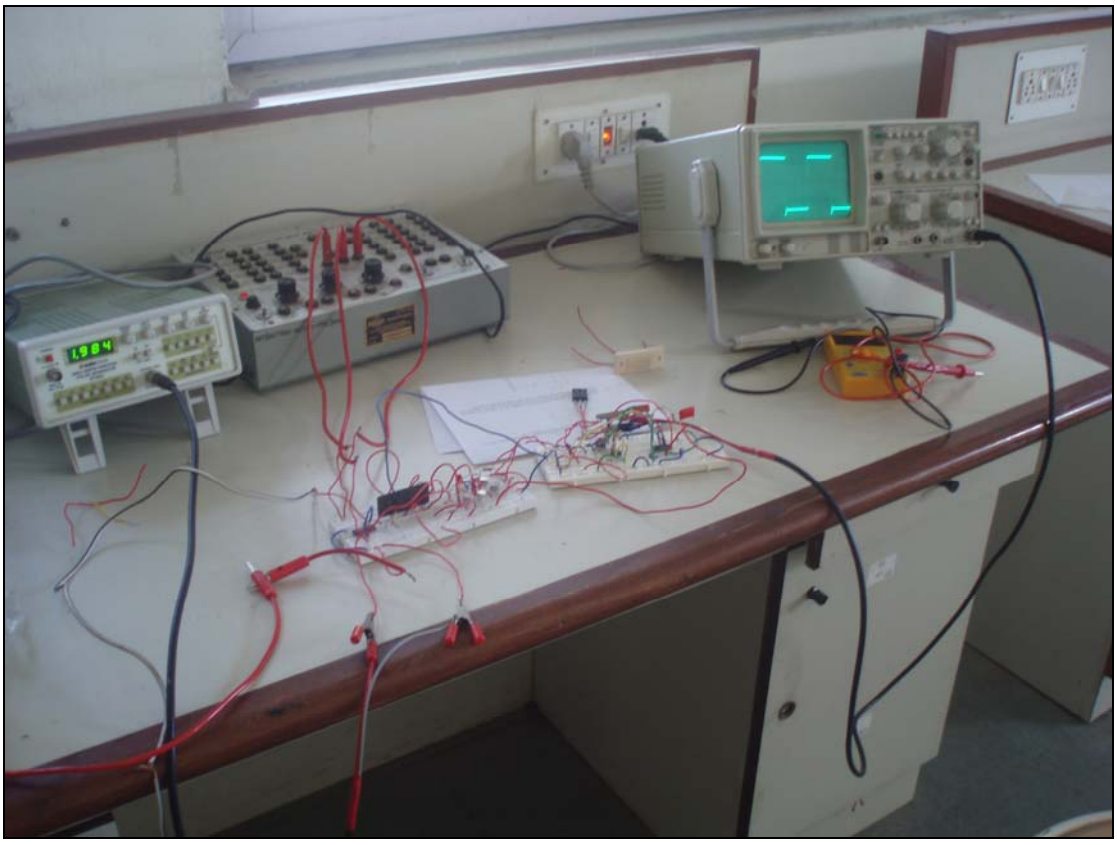

Fig.8.17 Pictorial view of setup for fault creation at port TP_7 (connection of IGBT)

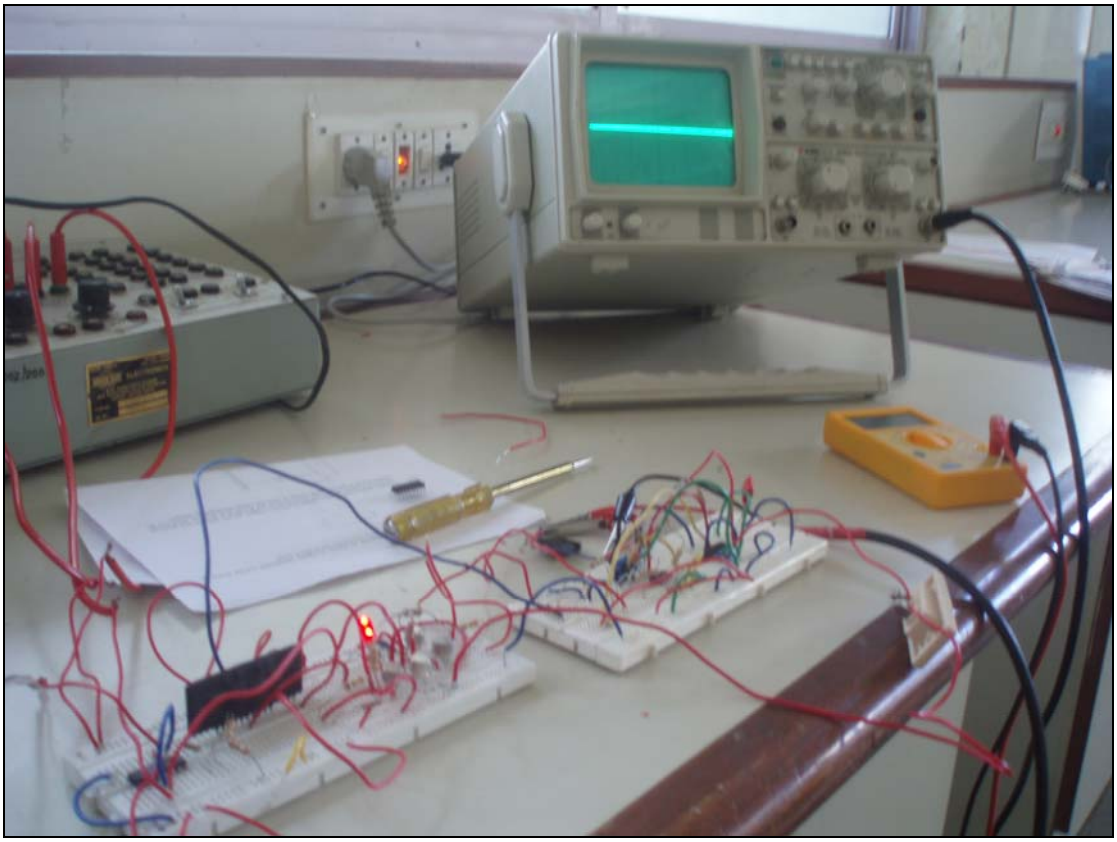

Fig.8.18 Pictorial view of output at port TP_7 after fault (connection of IGBT)

Fig.8.19 Pictorial view of setup for sort circuit protection of IGBT

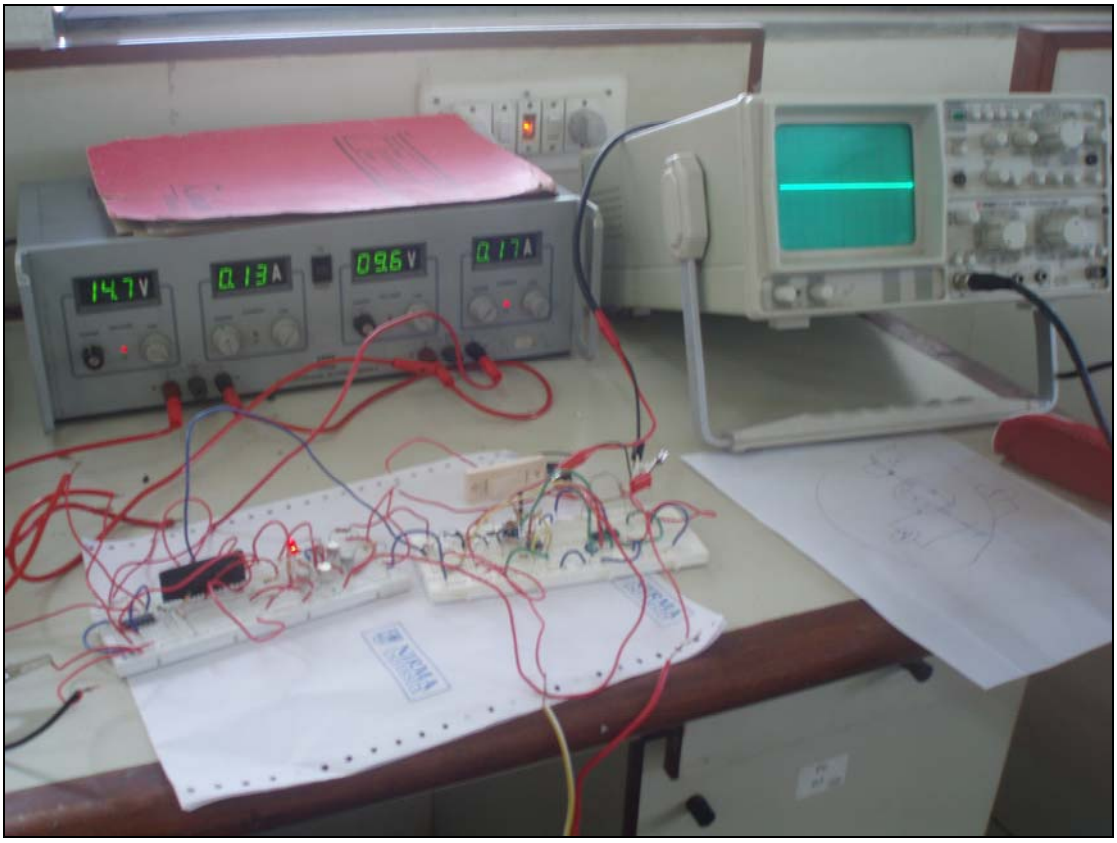

Fig.8.20 Pictorial view of output for sort circuit protection of IGBT

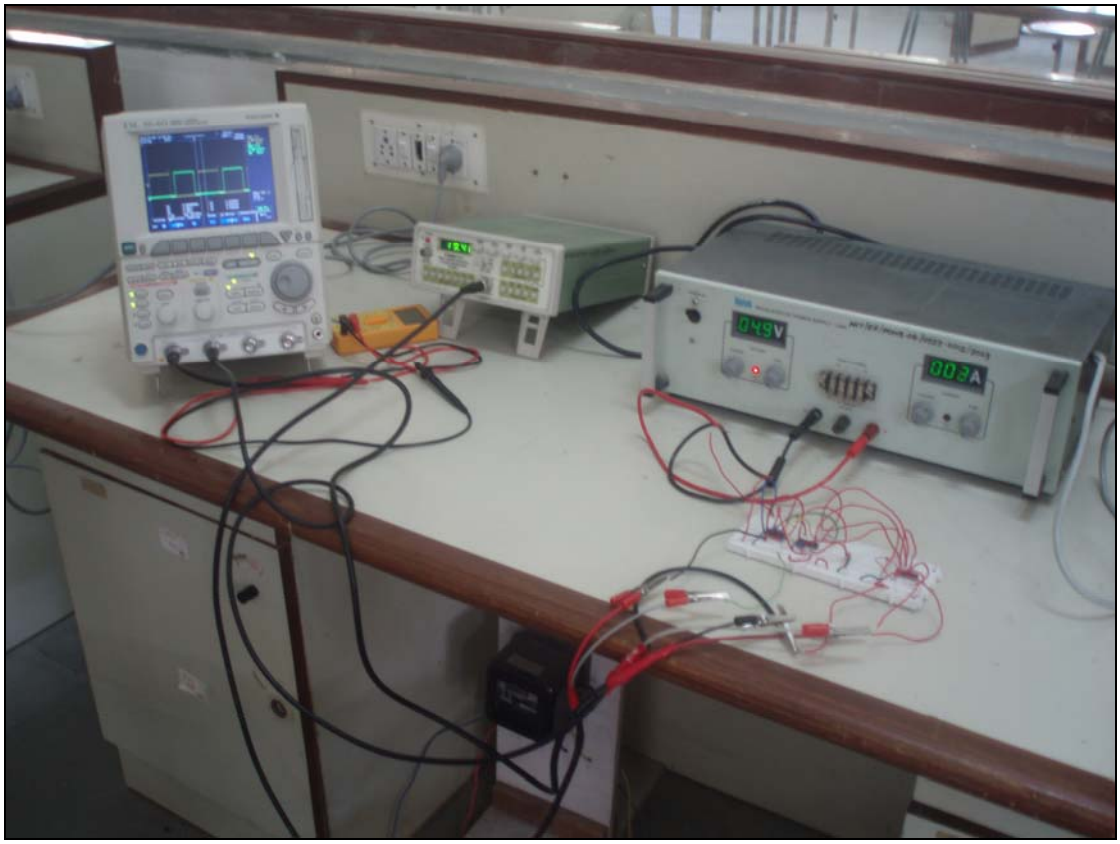

Fig.8.21 Pictorial view of setup for testing of dead band circuit

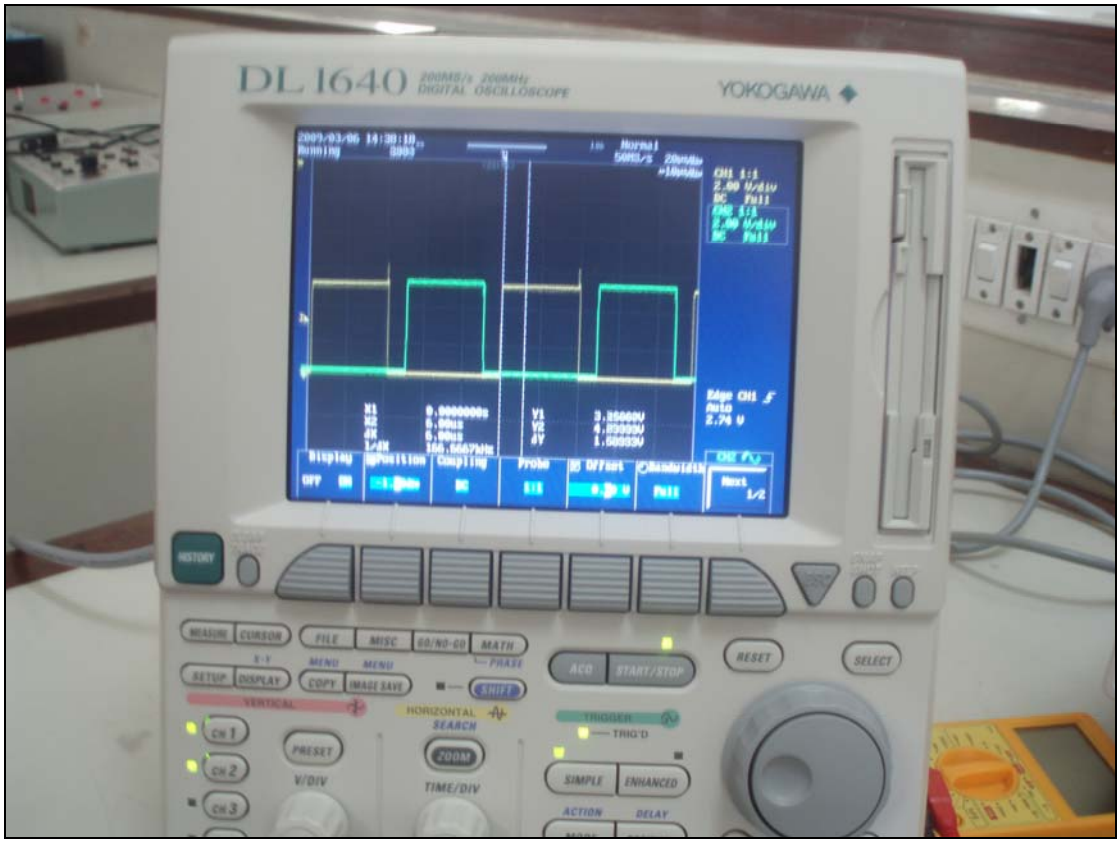

Fig.8.22 Pictorial view of results from dead band circuit

CHAPTER-9
FABRICATION OF GATE DRIVER CIRCUIT AND RESULTS

9.1 Layout of Gate Driver Circuit

The various pictorial views for the fabrication of the printed circuit board (PCB) [14] designing are shown in fig 9.1 to 9.3. Such diagrams are useful in under standing the construction of the PCB and after the final layout of the PCB the checking for the operation can be verified with the help of such diagrams.

The fig. 9.1 shows the silk screen layer of the gate driver circuit with dead band and protection circuit which gives the location of every component of the gate driver circuit mounted on the PCB and location of the jumper also. The fig 9.2 shows the bottom layer of the gate driver circuit with dead band and protection circuit which gives the connection information of the component placed on the PCB. The fig 9.3 shows the bottom solder mark layer of the PCB which gives the idea about the soldering point on the PCB.

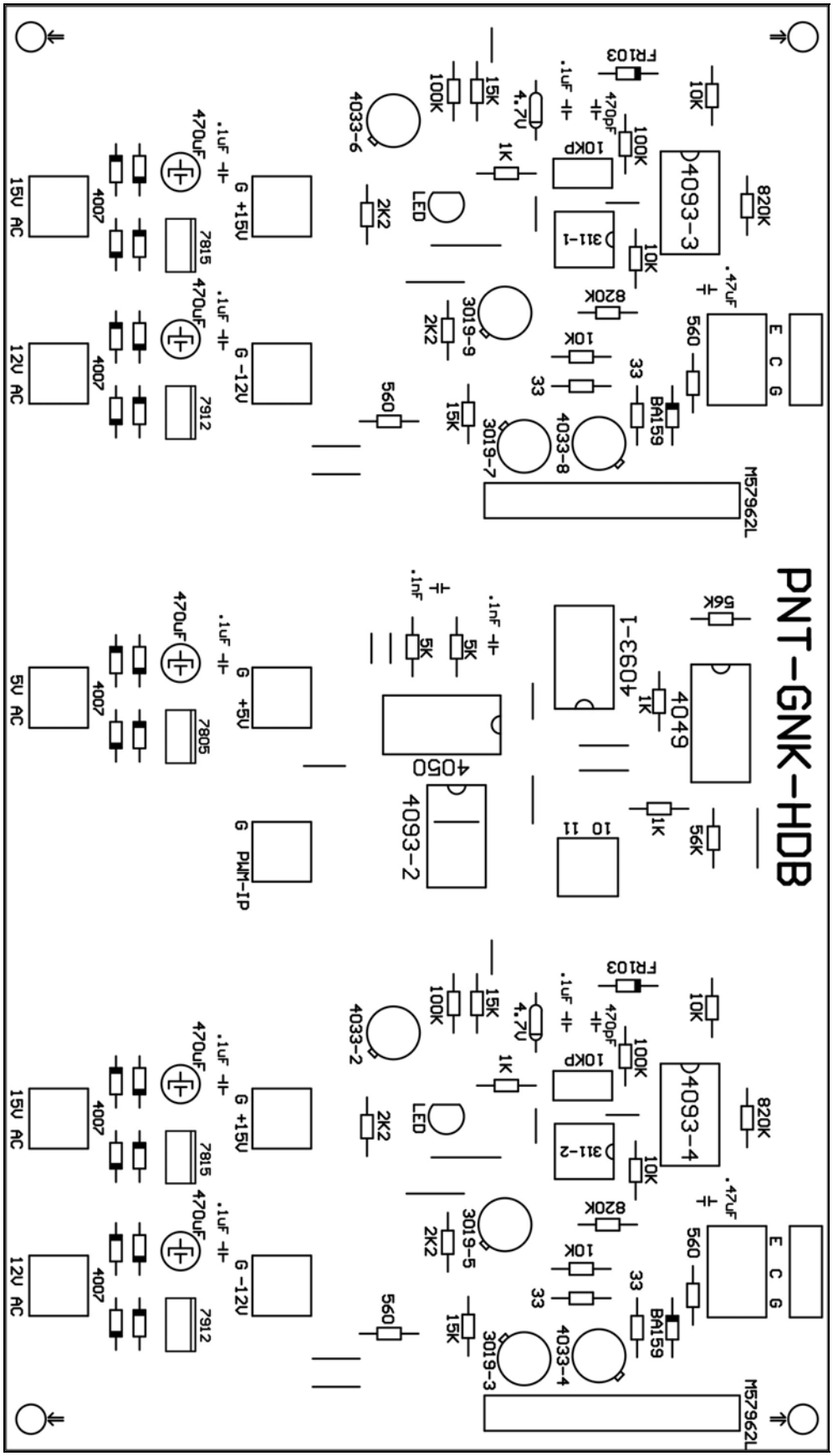

Fig. 9.1 Silk screen layer of the gate driver circuit with dead band and protection circuit and jumper details

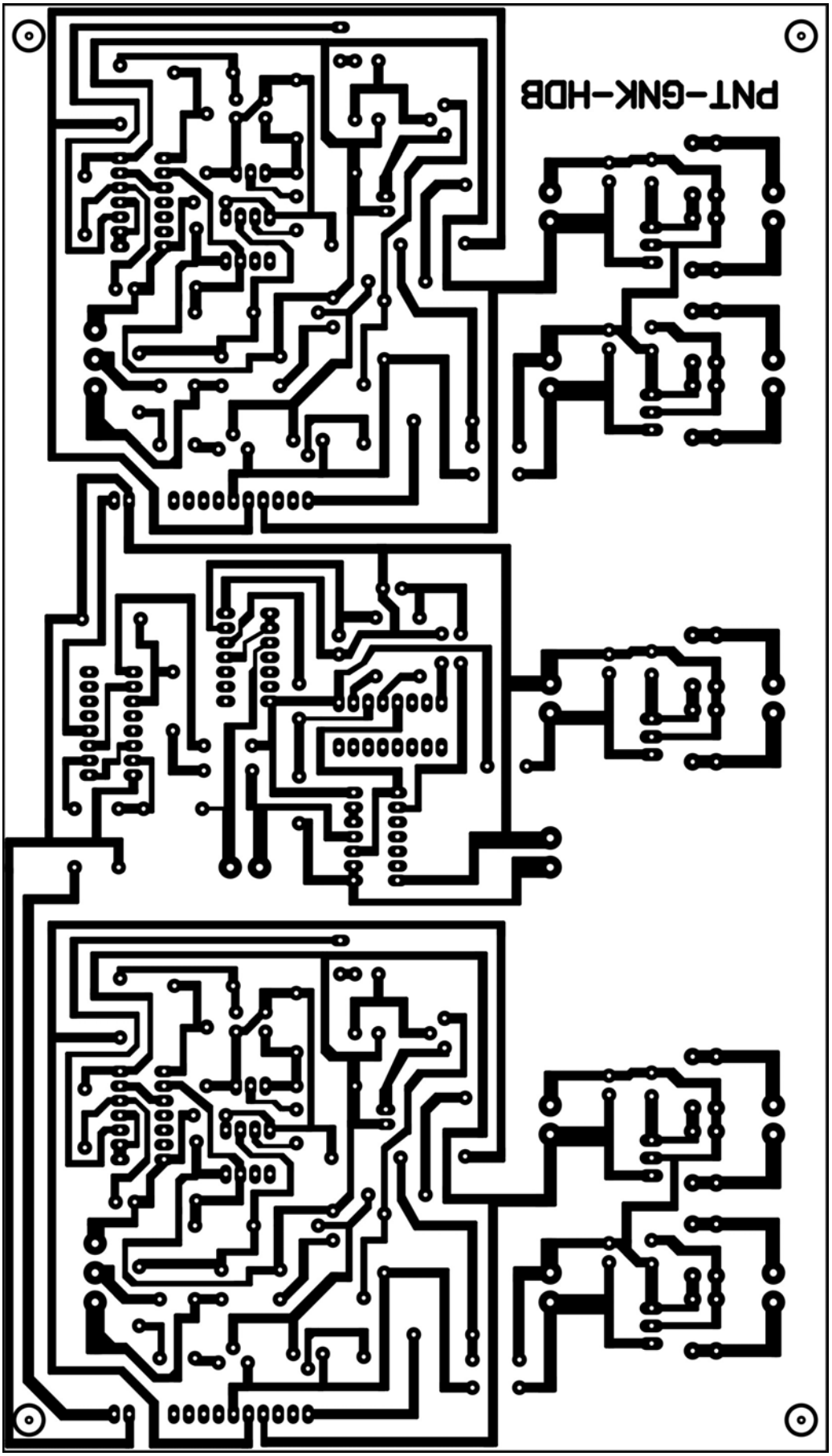

Fig. 9.2 Bottom layer of the gate driver circuit with dead band and protection circuit

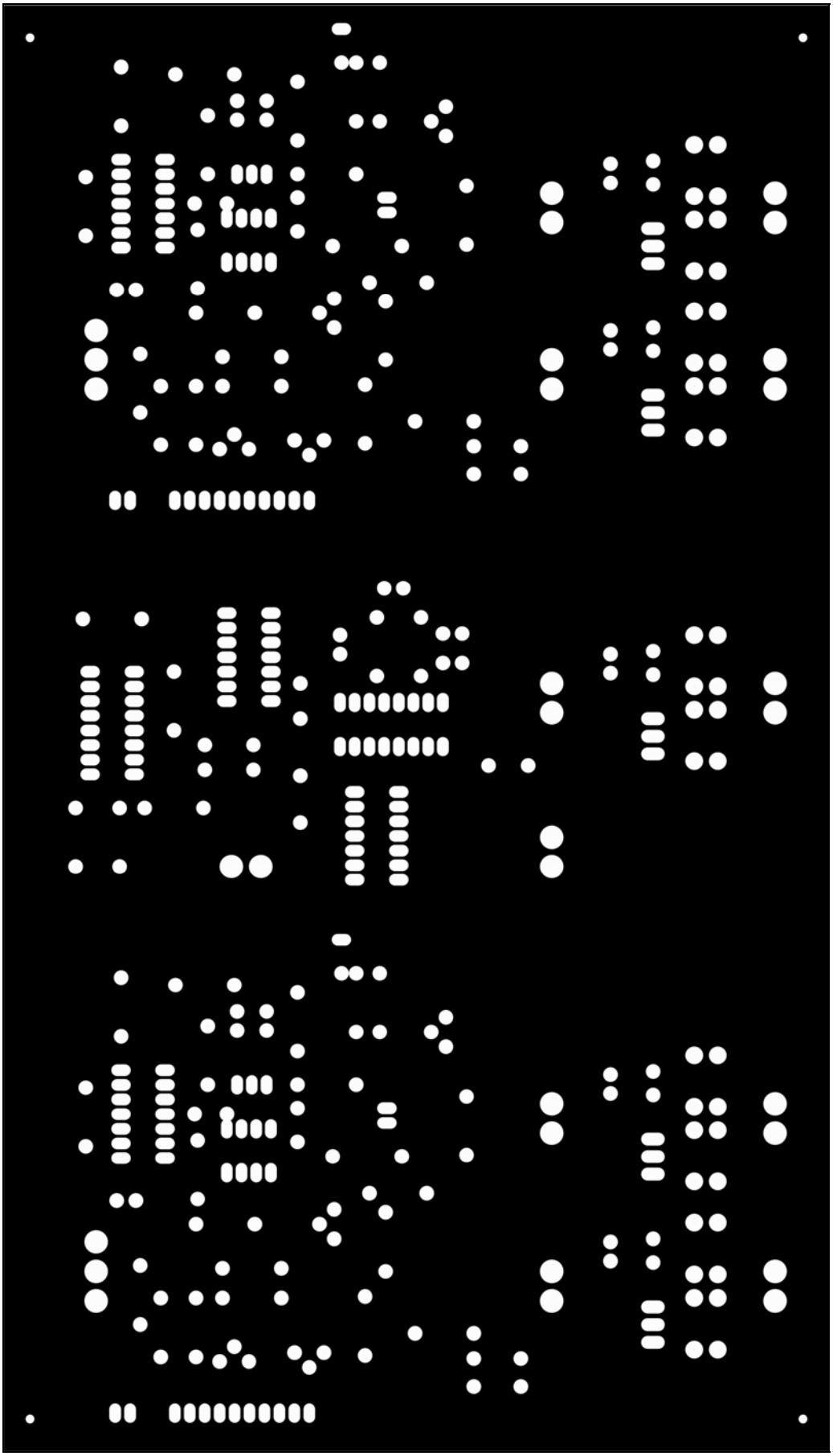

Fig.9.3 Solder mark layer of the PCB

9.2 IGBT Based Fabricated Gate Drive Circuit and Results

The schematic of IGBT based gate driver circuit used for the prototype front-end converter is shown in fig 9.4. The list of the various components used for the IGBT based gate driver circuit is tabulated in table 9.1.

According to the requirement of the prototype front-end converter the PCB of gate driver circuit prepared and results are obtained stage by stage i.e. across the each component of the gate driver circuit. The obtained results are satisfactory and as per the requirement. The obtained results are shown in fig. 9.5 to 9.10.

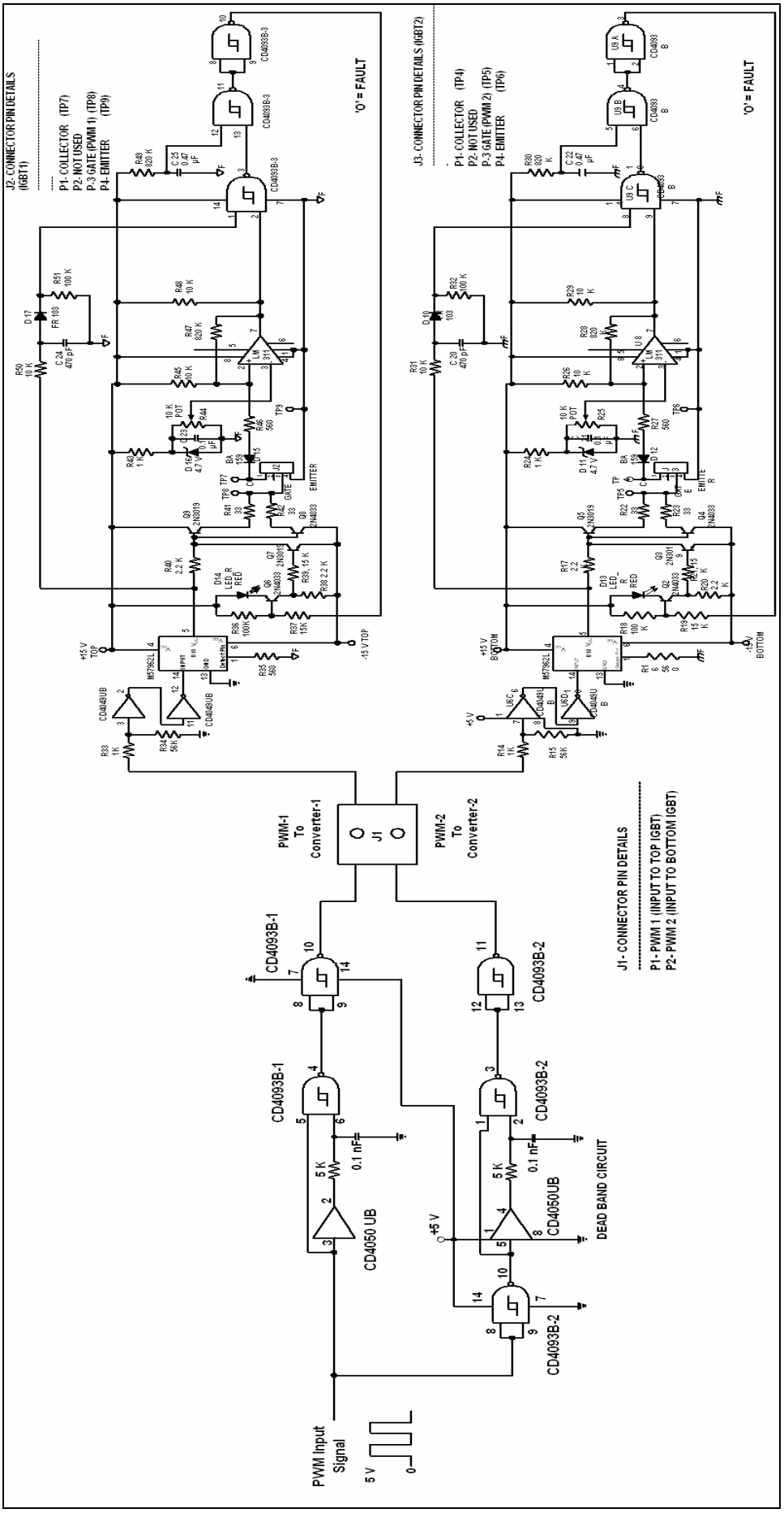

Fig 9.4 Schematic of IGBT based gate driver circuit used for the prototype front-end converter

Table-9.1 List of components for gate driver circuits (for one card only)

Sr. No.	Components Name/ Part No.	Location	Qty.
1.	Diode IN 4007	Power Supply	20
2.	Connector (2 pin)	Power Supply	10
3.	Capacitor 470 μF, 16 V	Power Supply	05
4.	Capacitor 0.1 μF, (104)	Power Supply	05
5.	Positive Voltage Regulator IC (7815)	Power Supply	02
6.	Negative Voltage Regulator IC (7912)	Power Supply	02
7.	Positive Voltage Regulator IC (7805)	Power Supply	01
8.	CD 4050UB Non-Inverting Buffer IC	Dead Band Circuit	01
9.	Connector 16 pin for IC CD 4050UB	Dead Band Circuit	01
10.	CD 4093UB 2 Input NAND Schmitt Triggers IC	Dead Band Circuit	02
11.	Connector 14 pin for IC CD 4093UB	Dead Band Circuit	02
12.	Connector (2 pin) to check Dead Band Signal	Dead Band Circuit	02
13.	Resistance-5 KΩ	Dead Band Circuit	02
14.	Capacitor 0.1 nF, (103)	Dead Band Circuit	02
15.	Resistance-1KΩ	Converter-1& 2	04
16.	Resistance-56 KΩ	Converter-1& 2	02
17.	CD 4049UB Inverting Buffer IC	Converter-1& 2	01
18.	Connector 16 pin for IC CD 4049UB	Converter-1& 2	01
19.	OptoCoupler IC (M57962L)	Converter-1& 2	02
20.	14 pin one line connector for OptoCoupler IC (M57962L)	Converter-1& 2	02
21.	Resistance- 560 Ω	Converter-1& 2	04
22.	Resistance- 100 KΩ	Converter-1& 2	04
23.	Resistance- 15 KΩ	Converter-1& 2	04
24.	Resistance- 2.2 KΩ	Converter-1& 2	04
25.	LED_Red	Converter-1& 2	02
26.	Transistor-2N 4033	Converter-1& 2	04
27.	Transistor-2N 3019	Converter-1& 2	04
28.	Resistance- 33 Ω	Converter-1& 2	04
29.	IGBT- HGTG20N60C3D	Converter-1& 2	02
30.	Connector (3 pins) for IGBT	Converter-1& 2	02
31.	Diode BA 159	Converter-1& 2	02
32.	IC LM 311	Converter-1& 2	02

Sr. No.	Components Name/ Part No.	Location	Qty.
33.	Connector 8 pins for IC LM 311	Converter-1& 2	02
34.	Resistance- 10 KΩ	Converter-1& 2	06
35.	Resistance- 820 KΩ	Converter-1& 2	04
36.	FR 103 Fast Recovery Diode	Converter-1& 2	02
37.	Zener Diode, 4.7 V	Converter-1& 2	02
38.	Potentiometer- 10 KΩ	Converter-1& 2	02
39.	Capacitor 0.1 µF, (104)	Converter-1& 2	02
40.	Capacitor 470 pF	Converter-1& 2	02
41.	Capacitor 470 µF, (470)	Converter-1& 2	02
42.	CD 4093UB 2 Input NAND Schmitt Triggers IC	Converter-1& 2	02
43.	Connector 14 pin for IC CD 4093UB	Converter-1& 2	02

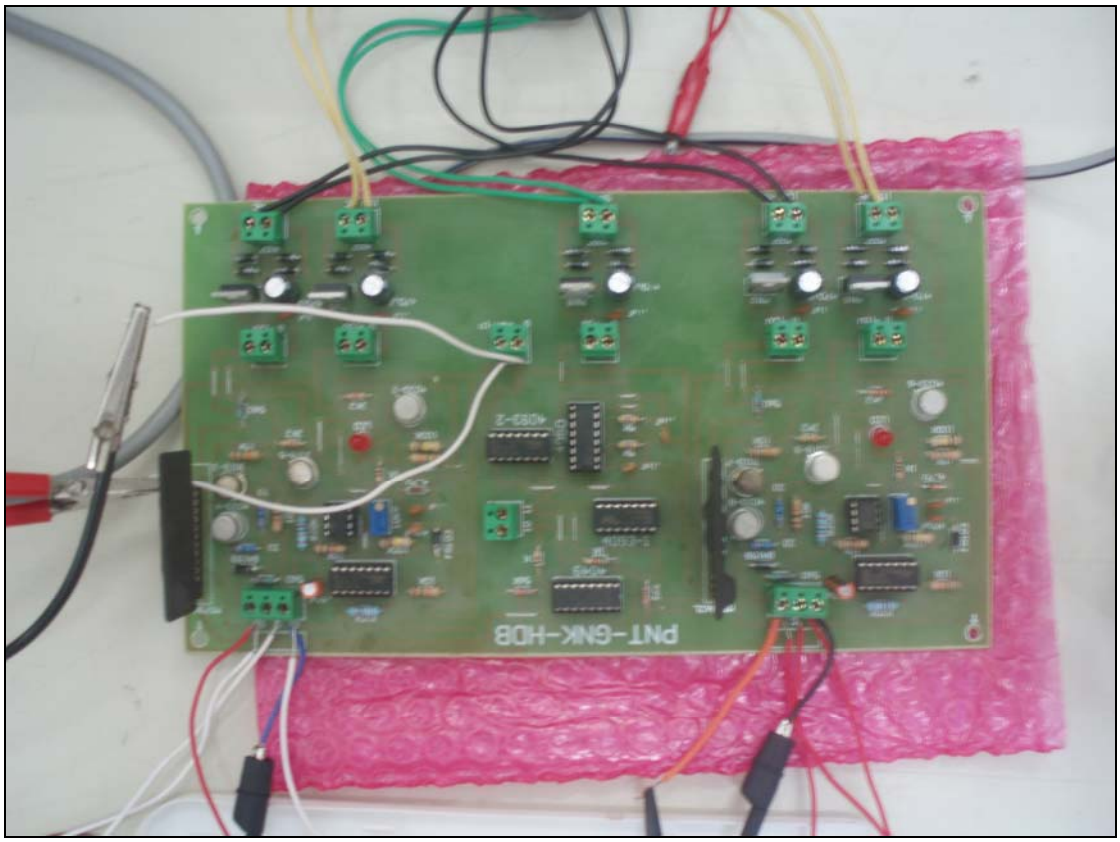

Fig 9.5 Top view of fabricated IGBT gate driver card for one leg of prototype converter

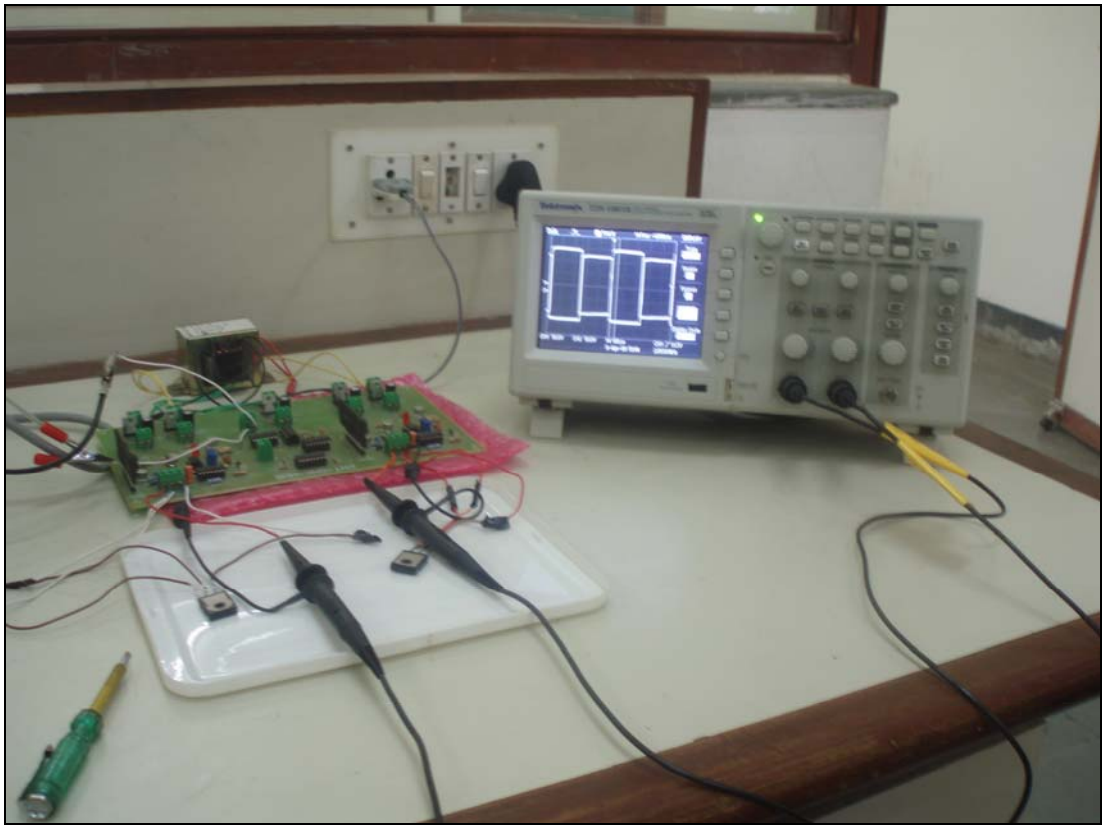

Fig 9.6 Results of gate driver card for one leg of prototype converter

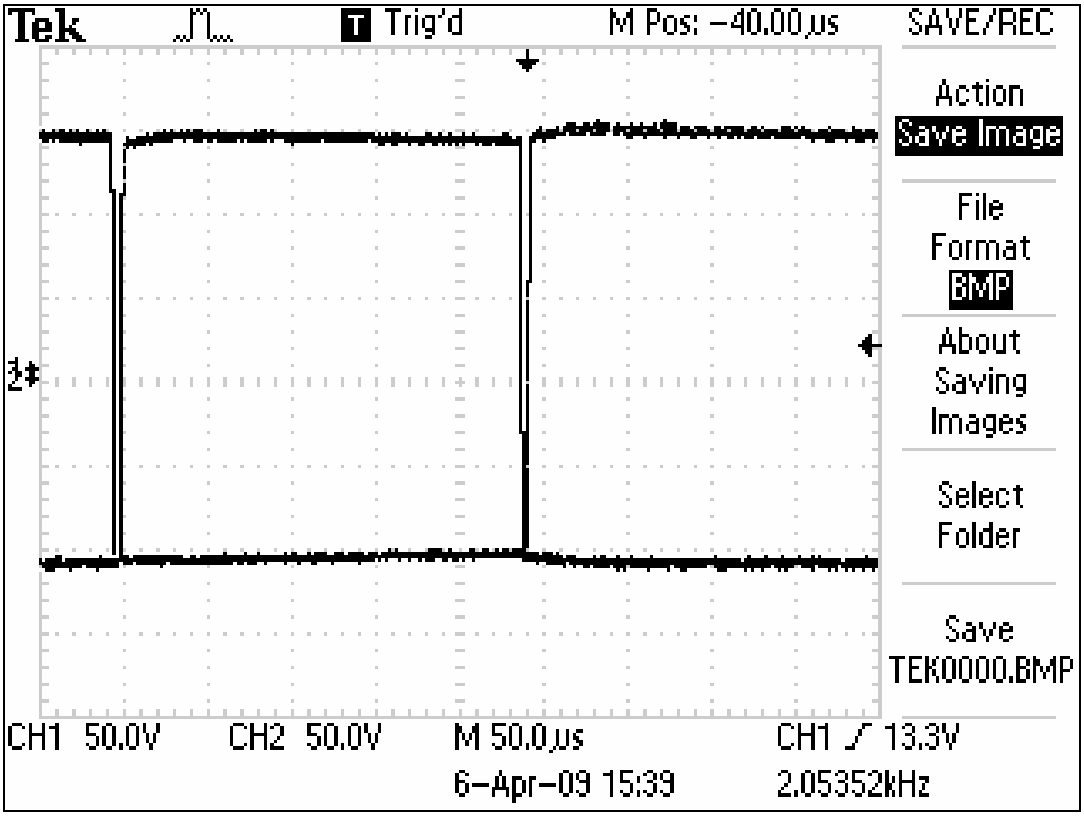

Fig 9.7 Complementary switching patterns with dead band obtained using gate driver card
(scale: X-axis:1division=50 µ sec, Y-axis: 1division= 5 volt)

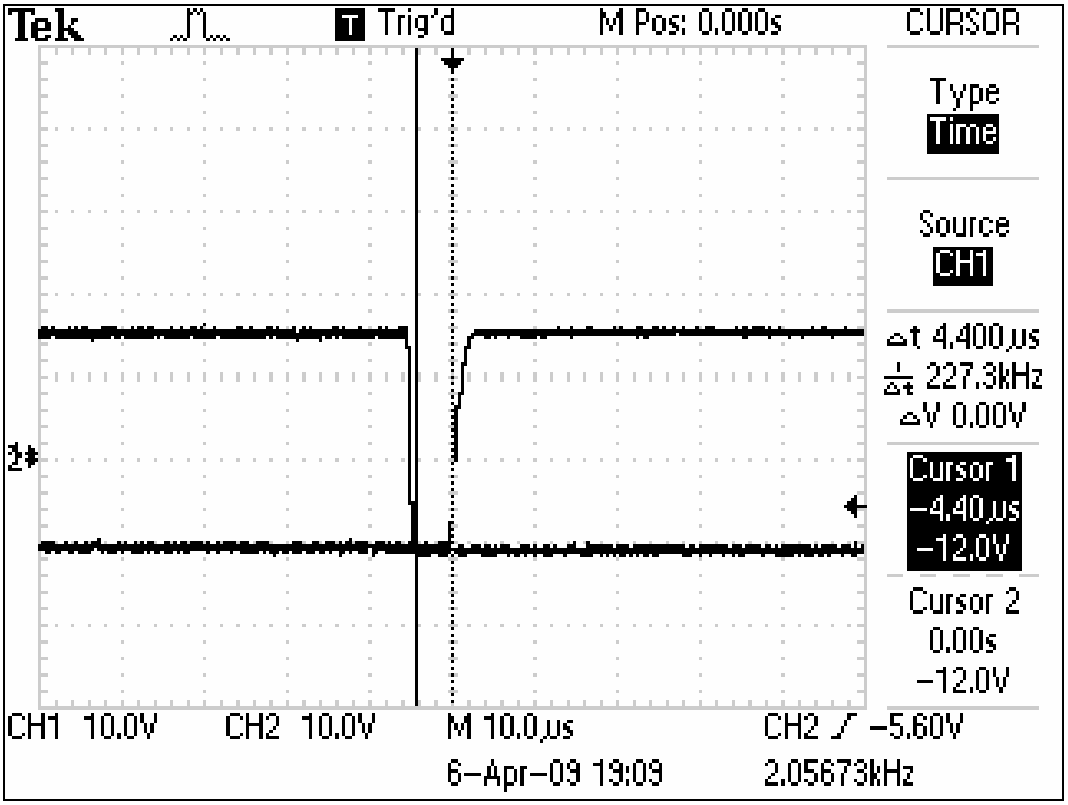

Fig 9.8 Dead band of 4.4 µ sec obtained using dead band circuit of gate driver circuit
(scale: X-axis:1division=10 µ sec, Y-axis: 1division= 10 volt)

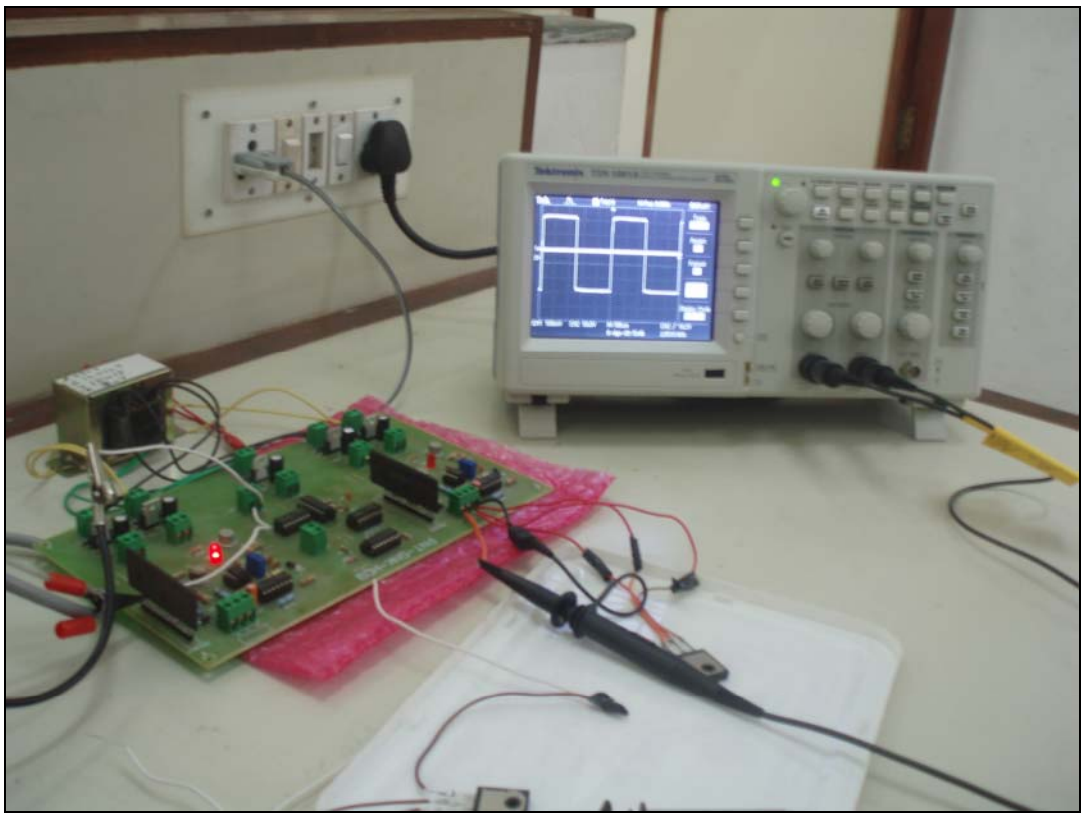

Fig 9.9 Results for gate driver card when only one converter in working mode

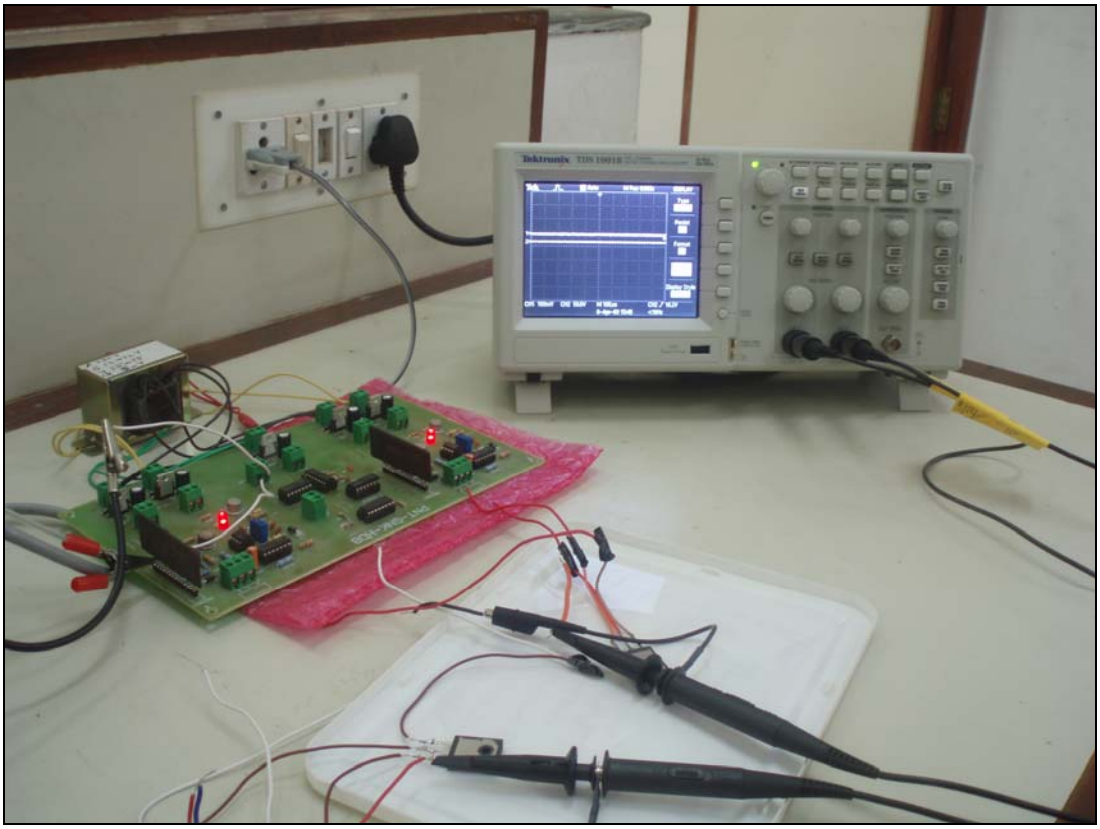

Fig 9.10 Results for gate driver card when both converter are at fault condition

CHAPTER-10
PROGRAMMING AND EXECUTION

10.1 Installation of Trainer Kit (MICRO-2407A)

The installation of the trainer board can be done in two modes [15]:

(1) Serial monitor mode also known as mode-1

(2) Stand alone mode also known as mode-2

At this moment the exercise for the programming is performed in the serial monitor mode i.e. in mode-2 only and hence procedure, programming and relevant results are obtained for the mode-1 only.

- **Procedure for installing Micro-2407 in mode-1:**

1. Keep the SPDT switch SW1 to the downward direction.
2. Connect the 3 pin power chord to the backside of the trainer.
3. Connect the PC serial port to the serial port connector of the kit.
4. Power on the kit.
5. Run the serial communication software XTALK to work with the trainer through PC.

10.2 Examples on Serial Monitor Mode (Mode-1)

In this session the exercise is performed to understand the working of the kit and to support the various programs are tested with the help of DSP kit. The programming of generation of sine wave, square wave, triangle wave and one adding program of two 16 bit values is included and accordingly results are obtained for the same. The pictorial view of the obtained results are shown in fig. 10.1 to 10.5

Result on MICRO-2407 Kit:

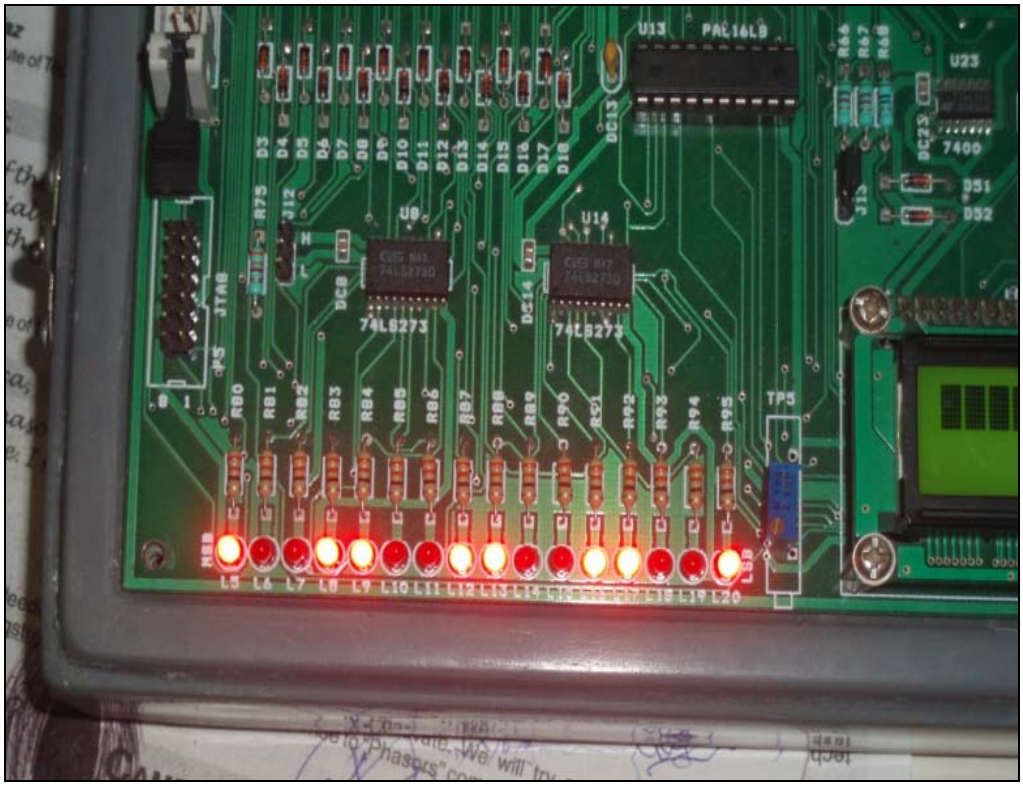

Fig. 10.1 Pictorial view of results for addition of values

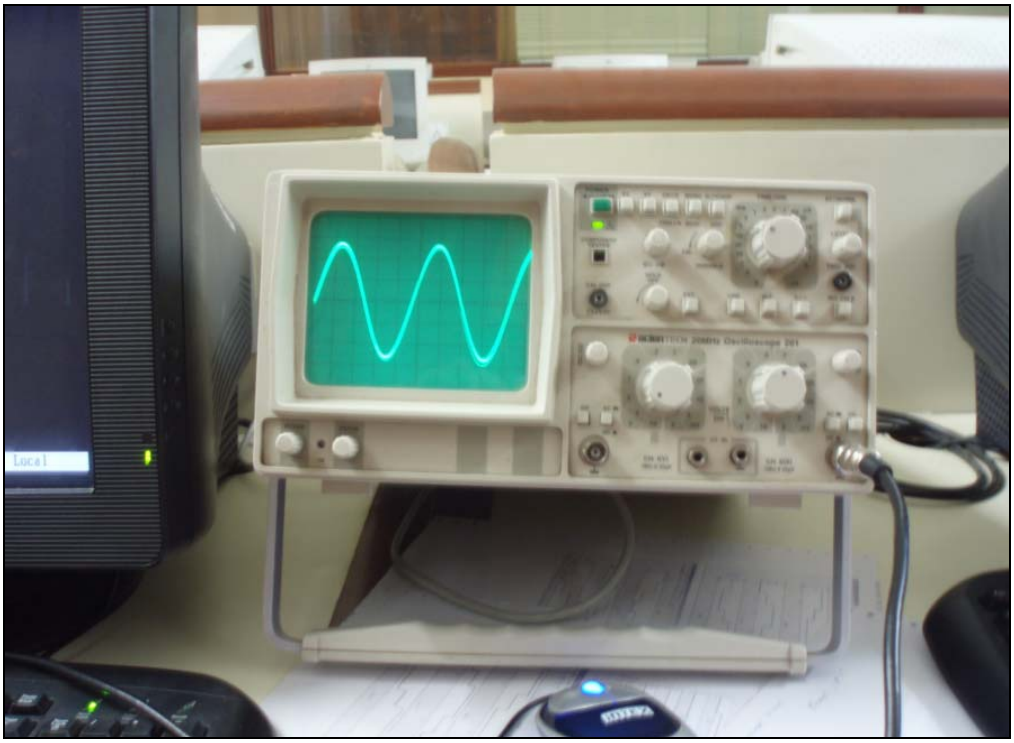

Fig. 10.2 Pictorial view of results for sine wave generation

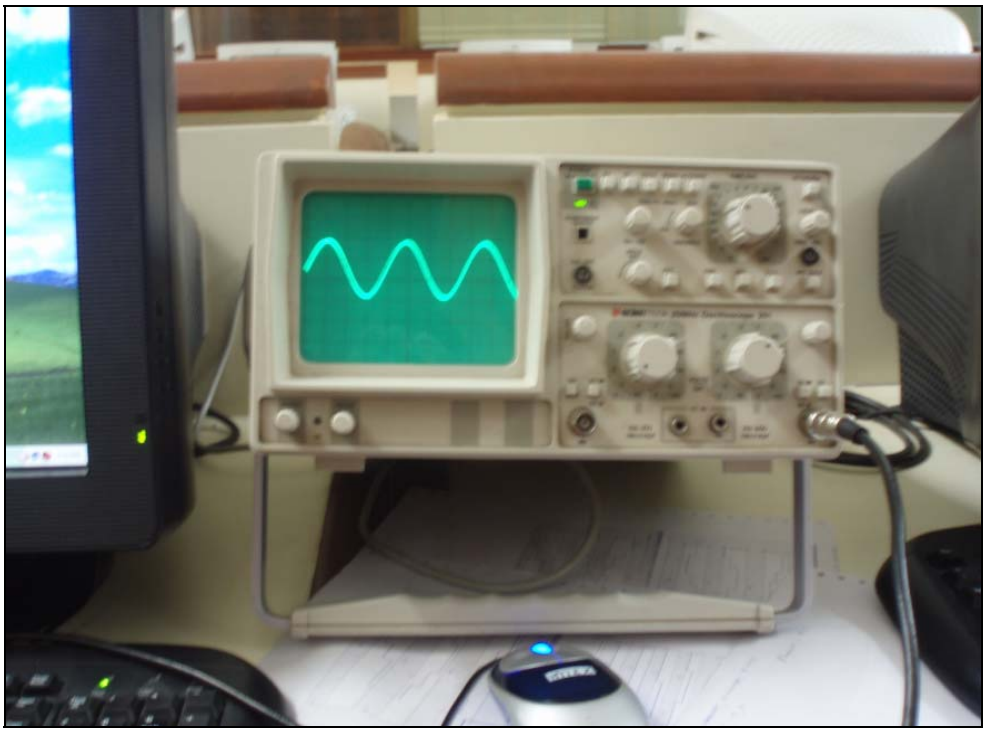

Fig. 10.3 Pictorial view of sine wave generation (1V and 50 Hz)

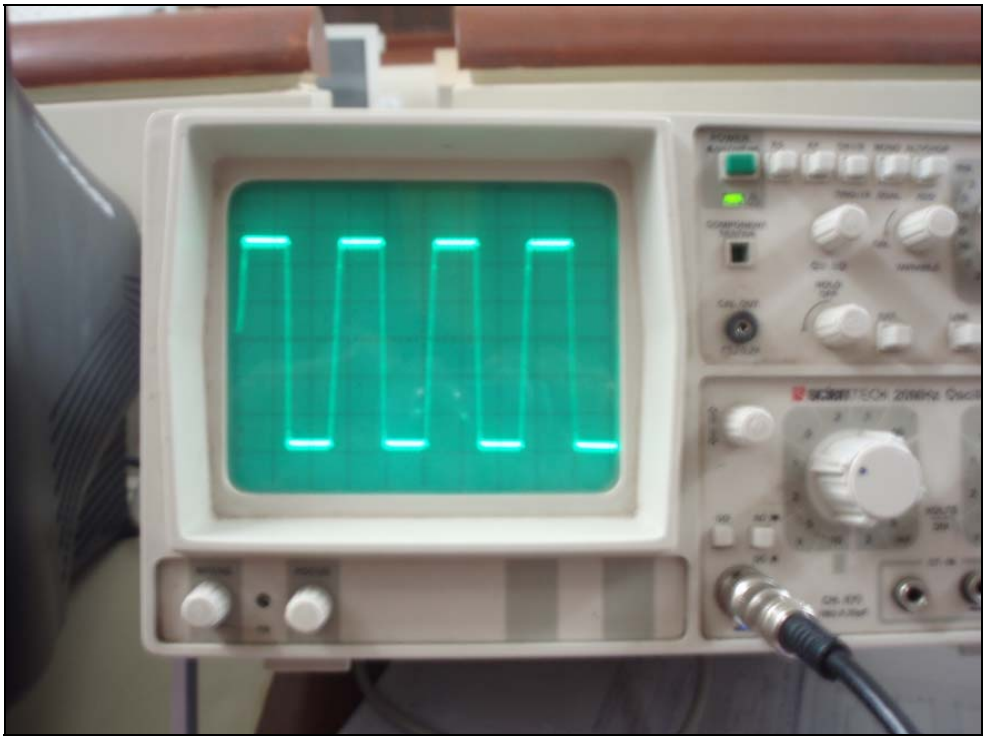

Fig. 10.4 Pictorial view of square wave generation

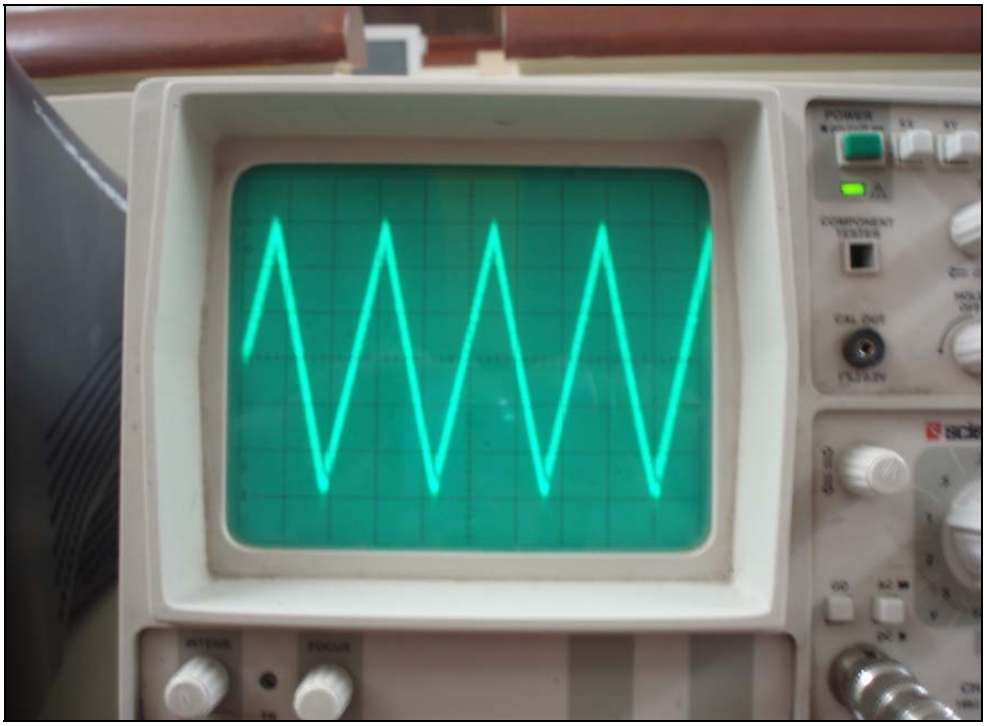

Fig. 10.5 Pictorial view of triangle wave generation

10.3 PWM Waveform Generation with Compare Units and PWM Circuits

A pulse width modulated (PWM) signal is a sequence of pulses with changing pulse widths [16]. The pulses are spread over a number of fixed-length periods so that there is one pulse in each period. The fixed period is called the PWM (carrier) period and its inverse is called the PWM (carrier) frequency. The widths of the PWM pulses are determined, or modulated, from pulse to pulse according to another sequence of desired values, the modulating signal. In a motor control system, PWM signals are used to control the on and off time of switching power devices that deliver the desired current and energy to the motor windings. The shape and frequency of the phase currents and the amount of energy delivered to the motor windings control the required speed and torque of the motor. In this case, the command voltage or current to be applied to the motor is the modulating signal. The frequency of the modulating signal is typically much lower than the PWM carrier frequency.

Both asymmetric and symmetric PWM waveforms can be generated by every compare unit on the EV module. In addition, the three compare units together can be used to generate 3-phase symmetric space vector PWM outputs. PWM generation with GP

timer compare units has been described in the GP timer sections. Generation of PWM outputs with the compare units is discussed in this section.

All three kinds of PWM waveform generations with compare units and associated circuits require configuration of the same Event Manager registers. The setup process for PWM generation includes the following steps:

- Setup and load ACTRx
- Setup and load DBTCONx, if dead-band is to be used
- Initialize CMPRx
- Setup and load COMCONx
- Setup and load T1CON (for EVA) or T3CON (for EVB) to start the operation
- Rewrite CMPRx with newly determined values

➢ Asymmetric PWM Waveform Generation

The edge-triggered or asymmetric PWM signal is characterized by modulated pulses which are not centered with respect to the PWM period, as shown in fig. 10.6. The width of each pulse can only be changed from one side of the pulse.

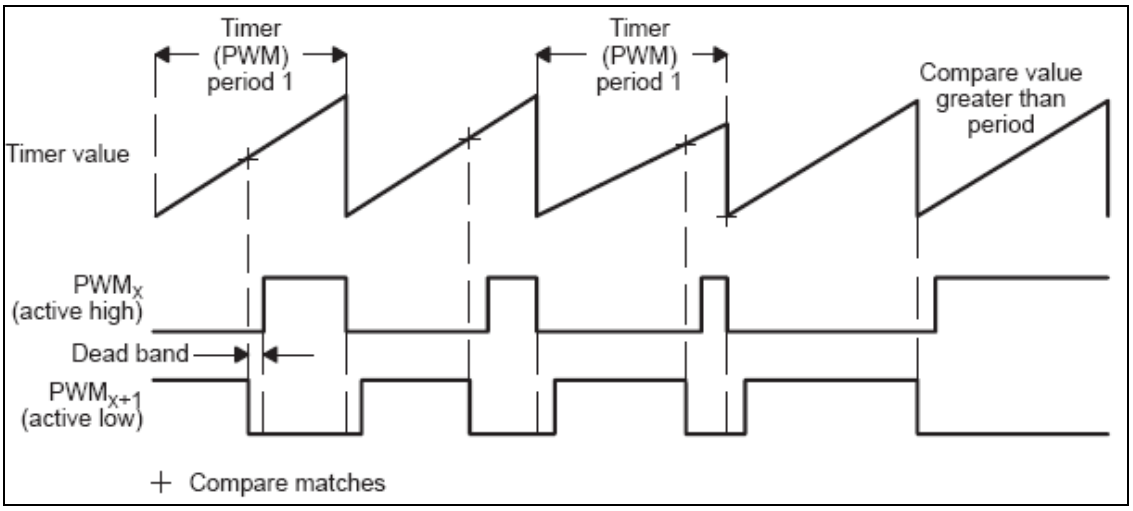

Fig.10.6 Asymmetric PWM waveform generation with compare unit and PWM circuits (x = 1, 3, or 5)

To generate an Asymmetric PWM signal, GP timer 1 is put in the continuous up-counting mode and its period register is loaded with a value corresponding to the desired PWM carrier period. The COMCONx is configured to enable the compare operation, set the selected output pins to be PWM outputs, and enable the outputs. If dead-band is enabled, the value corresponding to the required dead-band time should be written by software into the DBT (3:0) bits in DBTCONx(11:8). This is the period for the 4-bit

dead-band timers. One dead-band value is used for all PWM output channels. By proper configuration of ACTRx with software, a normal PWM signal can be generated on one output associated with a compare unit while the other is held low (or off) or high (or on), at the beginning, middle, or end of a PWM period. Such software controlled flexibility of PWM outputs is particularly useful in switched reluctance motor control applications.

After GP timer 1 (or GP timer 3) is started, the compare registers are rewritten every PWM period with newly determined compare values to adjust the width (the duty cycle) of PWM outputs that control the switch-on and -off duration of the power devices. Since the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

- **Symmetric PWM Waveform Generation**

A centered or symmetric PWM signal is characterized by modulated pulses which are centered with respect to each PWM period. The advantage of a symmetric PWM signal over an asymmetric PWM signal is that it has two inactive zones of the same duration: at the beginning and at the end of each PWM period. This symmetry has been shown to cause fewer harmonic than an asymmetric PWM signal in the phase currents of an AC motor, such as induction and DC brushless motors, when sinusoidal modulation is used. Fig 10.7 shows two examples of symmetric PWM waveforms.

The generation of a symmetric PWM waveform with a compare unit is similar to the generation of an asymmetric PWM waveform. The only exception is that GP timer 1 (or GP timer 3) now needs to be put in continuous up-/down-counting mode. There are usually two compare matches in a PWM period in symmetric PWM waveform generation, one during the upward counting before period match, and another during downward counting after period match. A new compare value becomes effective after the period match (reload on period) because it makes it possible to advance or delay the second edge of a PWM pulse. An application of this feature is when a PWM waveform modification compensates for current errors caused by the dead-band in AC motor control. Because the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

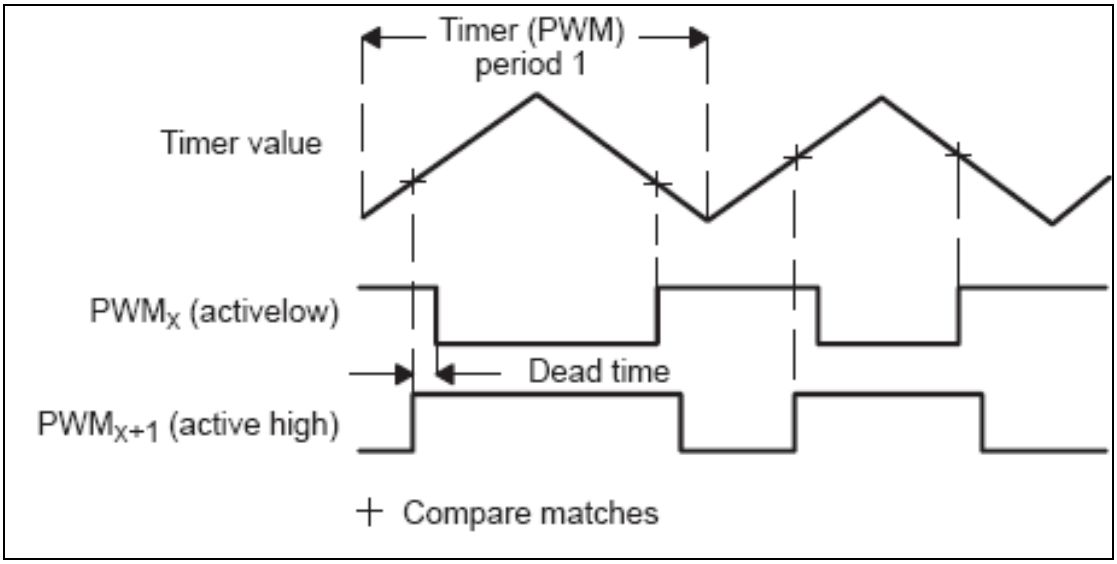

Fig.10.7 Symmetric PWM waveform generation with compare units and PWM circuits (x = 1, 3, or 5)

10.4 Results of PWM Waveform Generation from MICRO-2407

According to requirement of the prototype front-end converter and gate driver circuits the PWM signals are generated with the help of MICRO-2407 kit. The result is obtained for the both legs of the converter and it is observed that obtained the results is satisfactory and as per the requirement. The obtained results are shown in fig. 10.8 to 10.12.

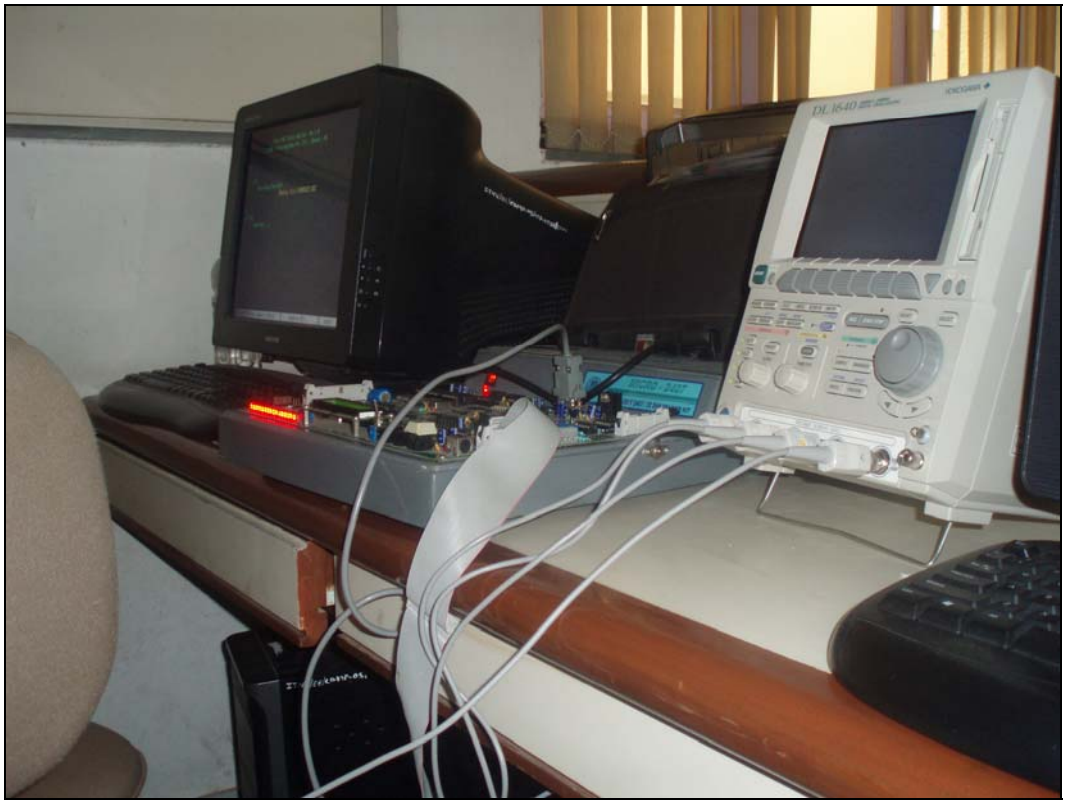

Fig. 10.8 Pictorial view of setup for generation of PWM signals from MICRO-2407 kit

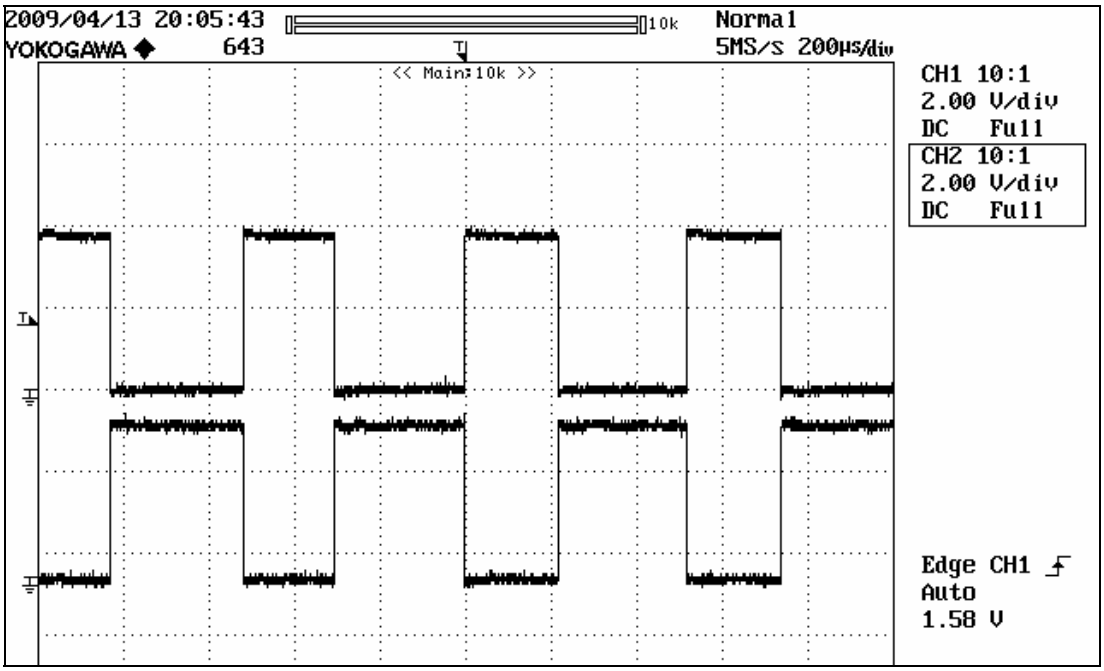

Fig. 10.9 Generation of PWM signals for converter-1

(Scale: X-axis:1 division = 200 µ sec, Y-axis: 1division= 2 volt)

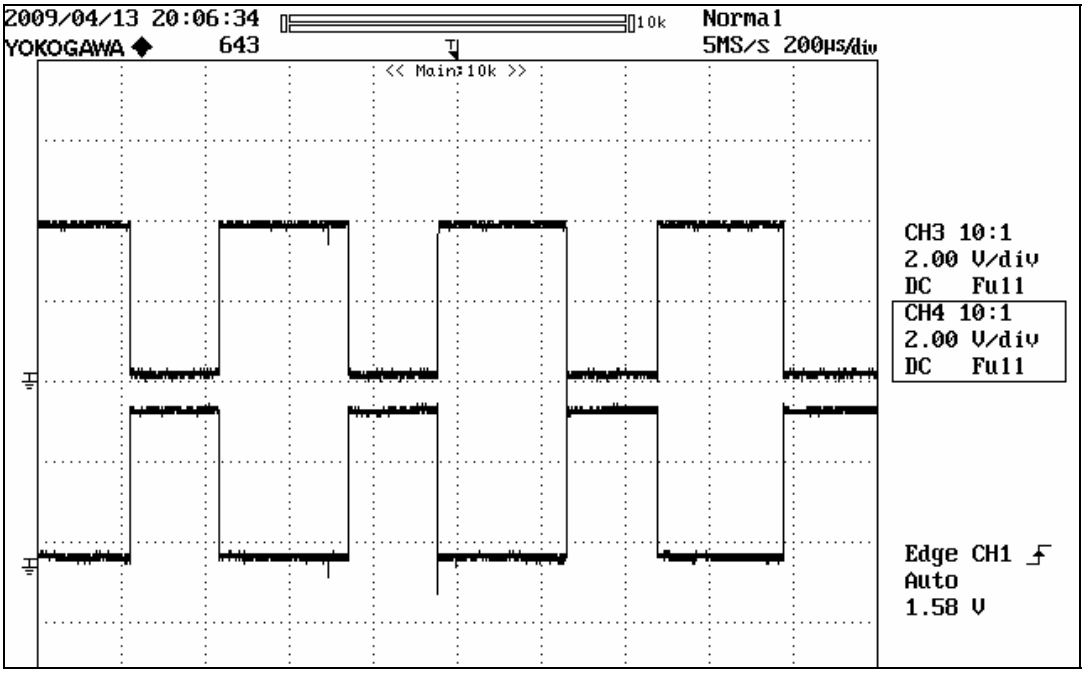

Fig. 10.10 Generation of PWM signals for converter-2

(Scale: X-axis: 1 division 200 µ sec, Y-axis : 1 division = 2 volt)

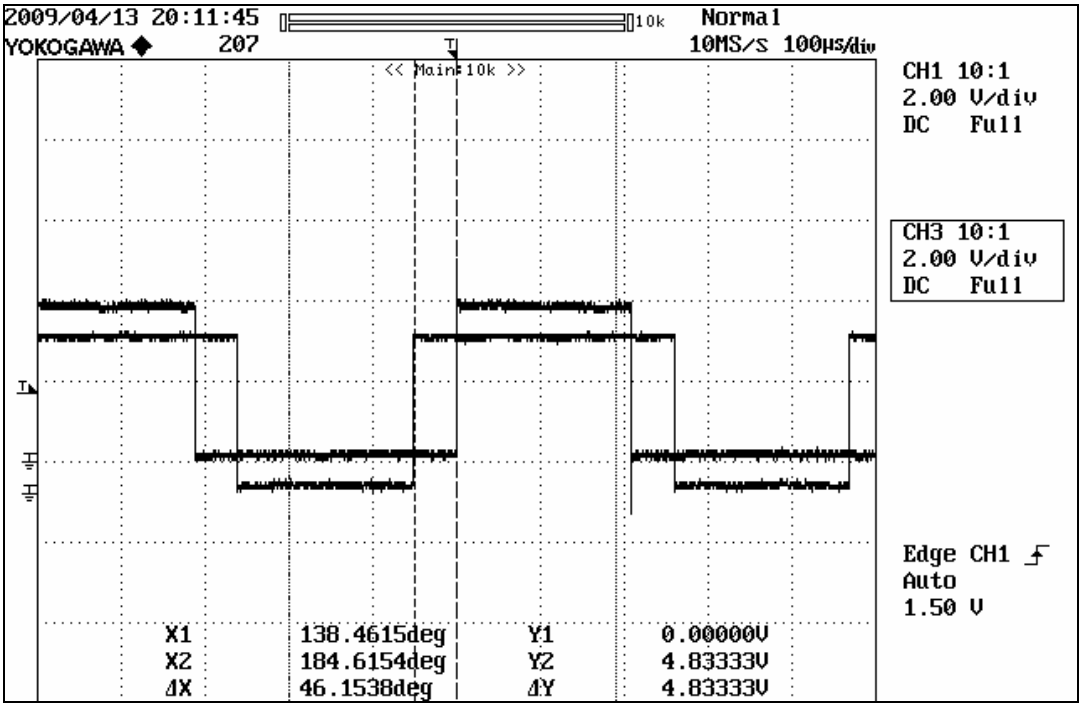

Fig. 10.11 Generation of PWM signals for same legs of converter-1 & 2

(Scale: X-axis: 1 division 100 µ sec, Y-axis : 1 division = 2 volt)

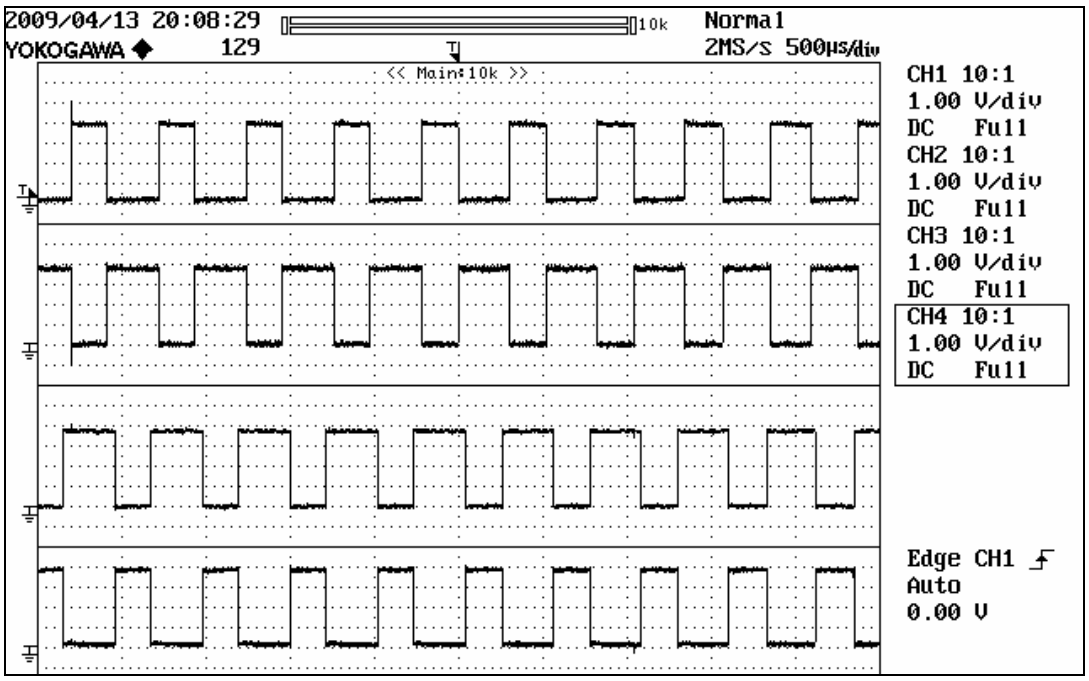

Fig. 10.12 Generation of PWM signals for converter-1 & 2

(Scale: X-axis: 1 division 500 µ sec, Y-axis : 1 division = 1 volt)

CHAPTER-11
CONCLUSION

11.1 Conclusion

The parameters of the control loops i.e. current and voltage control loop for the proposed front-end converter topology is found with Unity Modulus (Magnitude Optimum) method and Ziegler-Nichols method. The simulation results are obtained for the various values obtained from both the methods with the help of mathematical modeling in simulink (MATLAB). The simulation is performed for transient and dynamic conditions. For all the cases results form the unity modulus method found more suitable then Ziegler-Nichols method except the transient condition for under damped case where the Ziegler-Nichols method found more suitable then unity modulus method. The % THD of line current in the case of the diode bride rectifier is 328.50 % and it is observed 4.078% in the case of proposed front-end converter.

The simulation is also performed for the proposed converter having regenerative, transition mode of operation and for various loads conditions. The results are obtained by Unity Modulus (Magnitude Optimum) method and Ziegler-Nichols method. The results found satisfactory as per the requirement and it is observed that the unity power factor is maintained on the supply side for the various load condition and also during the fault condition.

A general MATLAB program is developed to find the controller parameters of the front-end converter. The plots are also obtained for current and voltage control loop under all the conditions i.e. under damped, critically damped and over damped system using both the solution methods. The parameters of P and PI controller are found almost same with the help of manual and program calculation. With help of MATLAB programme plots it is observed that the results for step input and Nyquist diagram for Unity Modulus method are better than the Ziegler-Nichols method.

The simulation is performed for the prototype front-end converter only under the transient condition system and for the under damped system. The results are obtained with the help of the Unity Modulus (Magnitude Optimum) method. The results found satisfactory as per the requirement and it is observed that the unity power factor is maintained on the supply side for such condition. With help of MATLAB program plots

are obtained for step input and Nyquist diagram for current and voltage control loops for Unity Modulus method.

The testing of the dead band and gate driver circuit is performed on the first on to the bread board and after wards the fabricated gate driver circuit. The results are obtained form both the circuits and obtained results are found satisfactory and as per the requirement. It is also observer that the protection circuit is working satisfactorily. The dead band of 4.4 μ sec is observed between two switches of the same leg.

The PWM signals are also generate for the both the leg of the converter of prototype converter and the results shows satisfactory generation of the PWM signals as per the requirement.

11.2 Future work

At present the author has presented work related to the prototype front-end converter having the open loop system i.e. no feedback is taken in to the system. In the further stages, the close loop operation of the circuit is possible. The regenerative mode of operation for the prototype front-end converter can also be performed.

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