Re-engineering of SLM with Automated Testing

Submitted By Jayendra Vyas 14MCEC30



DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING INSTITUTE OF TECHNOLOGY NIRMA UNIVERSITY

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Re-engineering of SLM with Automated Testing

Major Project

Submitted in complete fulfillment of the requirements

for the degree of

Master of Technology in Computer Science and Engineering

Submitted By Jayendra Vyas (14MCEC30)

Guided By Prof. Jitali Patel



DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING INSTITUTE OF TECHNOLOGY NIRMA UNIVERSITY AHMEDABAD-382481

May 2016

Certificate

This is to certify that the major project entitled "Re-engineering of SLM with automated testing" submitted by Jayendra Vyas (Roll No: 14MCEC30), towards the complete fulfillment of the requirements for the award of degree of Master of Technology in Computer Science and Engineering of Nirma University, Ahmedabad, is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project part-II, to the best of my knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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This is to certify that the major project entitled "Re-engineering of SLM with automated testing" submitted by Jayendra Vyas (Roll No: 14MCEC30), towards the fulfillment of the requirements for the award of degree of Master of Technology in Computer Science & Engineering (CSE) of Nirma University, Ahmedabad, is the record of work carried out by her under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination.

Date: Project guide Mr Krishna Kumar CPD Department, STMicroelectronics, India I, Jayendra Vyas, Roll. No. 14MCEC30, give undertaking that the Major Project entitled "Re-engineering of SLM with automated testing" submitted by me, towards the accomplishment of the requirements for the degree of Master of Technology in Computer Science & Engineering of Institute of Technology, Nirma University, Ahmedabad, contains no material that has been awarded for any degree or diploma in any university or school in any territory to the best of my knowledge. It is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. It contains no material that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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> - Jayendra Vyas 14MCEC30

Abstract

This project is about re-engineering of SLM model where SLM stands for system level memory. SLM is a memory model used internally in ST Microelectronics to simulate memory in verification phase of SoC design. Existing SLM is based on flexperf library which is obsolete now. So, We are re-engineering SLM with re-creating classes which are independent of flexperf library functions. Automation of existing testcases of SLM allows developers to test code regressively. SLM GUI is also an integral part of this project which provides different views for memory instances .

Abbreviations

\mathbf{SLM}	System Level Memory
GUI	Graphical User Interface
HDL	Hardware Description language
VHDL	Verilog Hardware description language
SoC	System On Chip

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Chapter 1

Introduction

1.1 Our Team

Our team work with the development of software models for IPs and specifically this report work is related to memory model. "System Design Solutions" is responsible for software modelling of different type of memories. These software models are then delivered to others teams within ST for incorporating with their simulators for verification purpose. Our team deals with one such memory model known as System Level Memory and its brief overview has been presented in the upcoming sections.

1.2 What is SLM Model?

In embedded system SoC is used to exhibit its functionalities. Fabrication of SoC is a very time consuming and costly process. So, it is designed very precisely and simulated to check its performance. SoC design process consists of following phases.

SoC Design Process Steps :-

- 1. Architecture Design
- 2. IP selection
- 3. Verification.
- 4. Integration
- 5. Validation

6. Physical Synthesis

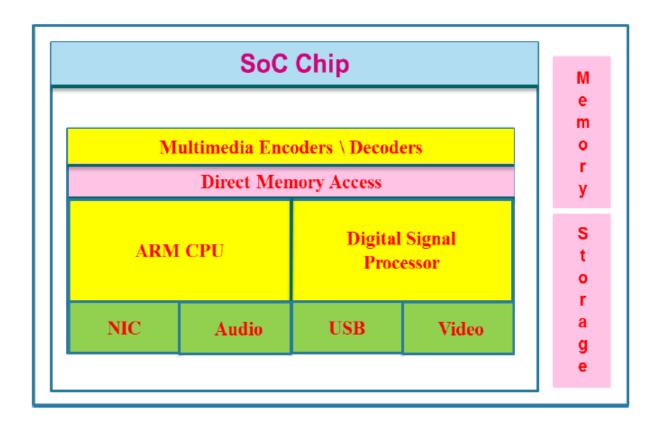


Figure 1.1: SoC design Components

Verification is the phase which takes maximum time in design process. In this phase various components are simulated on simulator like cadence, mentor graphics etc. Different component models are used in order to check the performance.

SLM model is used for simulating memory in ST Microelecronics. SLM model provides simulation of memory to add ease for developers in debugging memory in design process. Major functionalities of SLM are memory browsing and backdoor access to memory instances. Apart from that it provides wide range of functionality.

There are 3 major components in re-engineering of SLM

1. Classes of SLM

They depict functionality of SLM in following categories.

- (a) Utility
- (b) Verification
- (c) Recording
- (d) Access
- (e) Co-verification
- (f) Debug

2. SLM GUI

It provides memory browsing for different memory instances to add ease in debugging. It provides information about different memory instances. It has reach set of features like hierarchical view, Property view, searching data at specific address, range of data. Currently it is standalone software developed in C++/Tk.

3. Automated Testcases

These testcases are automated to be executed when we build SLM. It regressively checks for any differences in expected output and obtained output. Every testcase generates log while running testcase. It has following 2 test suits.

(a) HDL testsuit

It contains testcases in verilog. They Check for HDL Code functionality in different simulators environment.

(b) CPP testsuit

It contains testcases in C++. They check for C++ code functionality for SLM core.

Chapter 2

Literature survey

2.1 Existing SLM:

As mentioned earlier, SLM is a memory model to simulate memory in verification process of SoC design. It is ST Microelctronics's proprietary software. It is used internally in projects to simulate memory on different simulators. It can be used to verify anu functional design that require complex memory operations.

SLM is a mixed HDL/C++ model. It reduce the physical memory overhead by simply giving a 'C' moemory view to the physical memory. It is heavily integrated with flexperf library functions. Flexperf library is again ST Microelecronics's internal tool. This library is very old and not compatible with modern GCC. So, there is a need to re-engineer SLM Classes which are independent of flexperf library functions.

SLM provides services in following categories.

- 1. Utility
- 2. Verification
- 3. Recording
- 4. Access
- 5. Co-verification

SLM GUI is developed with SLM to provide GUI to end users and developers to view and access instances. It facilitates developers in debugging.

There are two test suits in co-ordination of SLM to test code regressively. HDL test

suit checks HDL code and CPP test suite checks CPP code in order to check fro any differences between expected outcome and obtained outcome.

2.2 SLM GUI

It is used to communicate with SLM Core. It allows developers to browse memory and zero time access to memory instances.SLM GUI was initially implemented in JAVA. In current version it is implemented in CPP/Tk which is very light in comparison of JAVA version.

In the current version it provides services to display memory instances. It also provides different views like Property view which gives detail about properties of current memory instance, Hierarchical view which gives relation of daughter memory instance with other parent memory and Memory grid view which gives grid view for current memory instance. It also allows to dump memory instance in required format.

2.3 Testcases

Testcases for HDL and CPP check code for identifying any differences in obtained output after modification in given code. These testcases are automated to check code regressively and less time consuming.

Testcases are built with the same time when SLM is built. if they are not automated then it is very lengthy and complicated process.

Testcases contains test cases for different perspectives. For example, Access category from CPP test suit contains testcase which checks address scrambling in SLM. It yields results whether address scrambling has been affected or not after modification in code.

Chapter 3

Technological Review

3.1 Language and Tools

SLM models are mixed HDL/C++ memory models. They correspond to HDL functional architectures where assignments of the memory models are replaced by C/C++subroutine calls. This way the storage becomes C storage in place of the former HDL register/variable. To connect HDL logic together with the C array and related access functions, the simulator-specific HDL/C interface are used. SLM C storage and services are delivered as prebuilt C dynamic libraries.

3.1.1 C++/Tk

SLM GUI is implemented in C++/Tk. It is an interface to the Tk GUI toolkit. C++/Tk uses templates, operator overloading and implicit conversions. Each C++/Tk expression ends up as equivalent Tcl/Tk command in the string format which is passed to underlying Tcl interpreter. It means that C++/Tk uses and depends on Tcl/Tk environment.[1]

3.2 Supported Operating Systems

- 1. Solaris
- 2. Linux

3.3 Supported Logic Simulators

- 1. Cadence NCsim
- 2. Mentor Modelsim

- 3. Synopsis vcs-mx
- 4. Verisity Xsim (Axis)

3.4 SLM functionalities

SLM provides functionalities in basically 2 categories.

- 1. Internal functions for SLM Model providers
 - (a) Registration
 - (b) Read and write access
 - (c) Subset of verification features (Load, Reset system memory)
- 2. External functions for End users
 - (a) Utility

These are help and information functions.

(b) Verification

Verification functions are meant to be used in either in the HDL test bench or from logic simulator console. They rely on backdoor access. They are executed in 0-HW time. Accesses to SLM cuts are not simulated by the logic simulator hence reducing simulation time.

(c) Recording

These functions help in logging the memory events in different formats .

(d) Debug

These functions are used for debugging purpose.

(e) System

These functions are related to creation and building of system memories.

(f) HW/SW co-verification

Functions used in parallel of hardware design.

3.5 How SLM works?

SLM 'C' storage and services are delivered as pre-built 'C' dynamic libraries. In order to connect HDL logic together with the C array and related access functions, the simulator specific HDL/C interface are used.

3.6 SLM GUI

SLM GUI can be divided in following components.

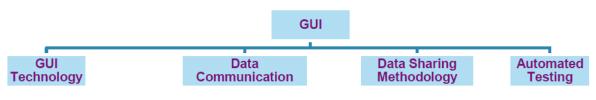


Figure 3.1: GUI Components

Chapter 4

Requirement Analysis

4.1 Objectives for SLM GUI

4.1.1 Functional Objectives

1. Debug existing SLM GUI code implemented in C++/Tk

SLM GUI was a stand alone software earlier. Debugging was required to ensure functionalities which were supposed to be delivered.

2. Optimize code

it includes identifying redundant functions, variables and memory leaks. As some of the functions may not be contributing in depicting functionality of SLM GUI. Some global variables may also not be used in code. SLM GUI takes memory instances as input file and generates various log and error files. So, It is also important to check traces of memory leaks.

3. Add Partial Search feature

Existing SLM GUI was exhibiting search feature which gave an address of data we look for. But, it did not support partial search. In partial search, GUI finds all partial matches at binary level and displays.

4. Integrating SLM GUI into SLM Core

Initially it was standalone application. Afterwards need arose to integrate it into SLM core. So that it can get invoked whenever we build SLM Core. All the files are directly passed from SLM core to SLM GUI to be displayed by it. Initially the files which we wanted to display on SLM GUI were used to be dumped in a specific location and GUI was accessing those files from those locations.

4.1.2 Software Objective

- 1. Modular and extensible
- 2. Simple integration setup

4.2 Objectives for SLM core

4.2.1 Functional Objective

1. Abstract analysis of SLM core

This objective is about to understand relations between existing files. It includes understanding flow of SLM Core.

2. Analysis of plugin point for SLM GUI

Currently SLM GUI is stand alone software. It is not integrated with SLM. To allow SLM GUI communicate directly with SLM, we need to integrate it with SLM core. So that we can invoke SLM GUI from within SLM.

3. Analysis of classes to be re-engineered

Before re-engineering the SLM Core classes, through analysis was required to carry out re-engineering.

4. Re-engineering of classes

After thorough analysis of classes built with flexperf library functions, new classes were supposed to be developed in order to provide dependency on flexperf library.

5. Integration of re-engineered classes

All re-engineered classes were supposed to be integrated to ensure functionalities. Separate testcases were also supposed to be developed to ensure individual functionalities.

4.3 Objective for Test cases

4.3.1 Functional objectives

- Abstract analysis of existing test suits Initially there were two test suits
 - (a) HDL Test suit

It contains test cases to check whether they are carrying out functionality. Every functionality is checked with content of different simulators.

(b) CPP test suit

It contains test cases to check functionality of C++ code whether they are carrying out functionality.

2. Automate C++ testcases

It is cumbersome to run testcases manually. There are 25 testcases implented in C++ checking different aspects of SLM. They need to be automated to check test results without manual intervention. We can set specific flags while building SLM which can also build test cases at same time.

They generate log files and error reports to add ease in debugging. These log files and error reports are very helpful in case some errors are there in code. Automation of testcases saves plenty of time and makes debugging very simple.

Chapter 5

Implementation details

- 5.1 Snapshots of SLM GUI
- 5.1.1 SLM GUI architecture

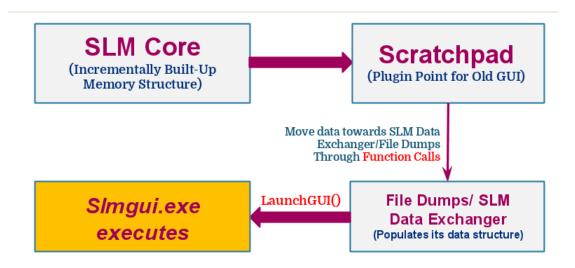


Figure 5.1: SLM GUI architecture

5.1.2 SLM GUI communication process

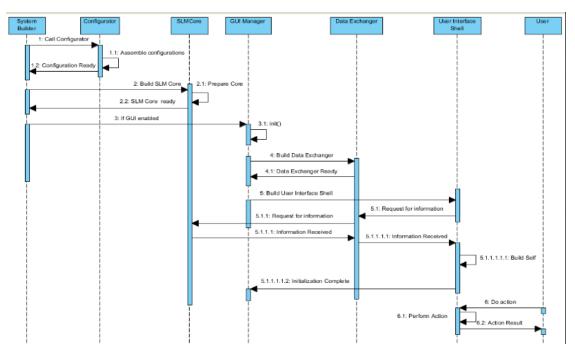


Figure 5.2: Overall Communication process

5.1.3 SLM GUI splash screen

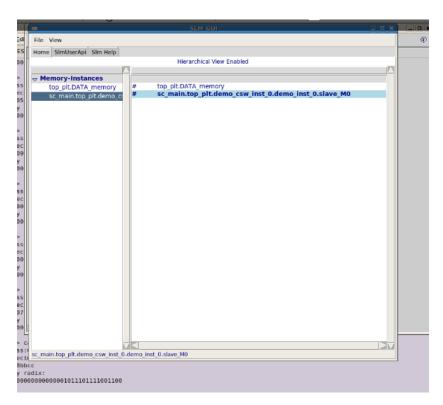


Figure 5.3: SLM GUI Home

5.1.4 SLM GUI property view window

-	SLM	I GUI		
File View				
Home SimUserApi Sim Help				
	Propert	y View E	nabled	
		,		
- Memory-Instances				
top_plt.DATA_memory				
sc_main.top_plt.demo_c	Logical_Name		top_plt.DATA_memory	
sc_main.top_pic.demo_c	Logical_Name_current		top_plt.DATA_memory	
	Alias			
	ID		1	
	Width Depth	-	32 67108864	
	MAU		32	
	Address Bus Size		9	
	NMAU NMAU		8	
	Begin Address		0	
	End Address	1	0	
	Assertions	1		
	Memory_Type	1	Physical Memory	
top. plt.DATA memory				>

Figure 5.4: SLM GUI Property View

5.1.5 SLM GUI Output window

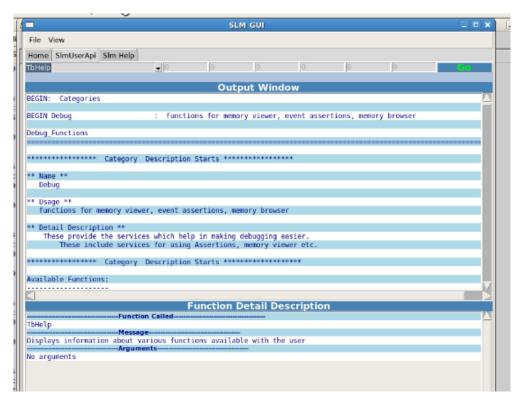


Figure 5.5: SLM GUI Output Window

5.1.6 SLM help command in Unix

```
rtlsoc@crx1052{Bist362 :slmhelp
How To Proceed
   1. Give First argument as -h to know the possible usages of help command
   2. Can use this for getting help on any
                      Function
Error Message
Context
                      Category
          Just Give the first argument as the search string for any of the above
 ** Categories Available **
                                                                              registration of physical memory instances for usage in the SLM models
memory access functions for usage in the SLM models
functions for verification purpose callable from simulator prompt or HDL
miscellaneous lower added value functions
system memory registration and definition functions
functions for handling SDI2/DBI/Console recording
functions for memory viewer, event assertions, memory browser
cpu and address space registration, mapping and optimization settings
  registration
   access
verification
utility
   system
recording
   debug
coverification
 ** Contexts Available **
                                                                               to model memory in verilog language.
to use SLM services through verilog code.
to use SLM services at nosim simulator prompt(console),
to use SLM services at modelsim simulator prompt(console).
to model memory in VHDL.
to use SLM services through VHDL code.
to use SLM services in C++ language.
to use SLM services for co-verfification/ISS.
to use SLM services through c language.
to use SLM services through specman/ e language.
  verilog_memory_model
verilog_testbench
ncsim_console
vhdl_memory_model
vhdl_testbench
   c++
isskit
c-lang
specman
rtlsoc@crx1052{Bist}63 :
                                                                                                                                                                                                                                                    1 0
```

Figure 5.6: SLM help command in Unix

5.1.7 System Memory instance Properties

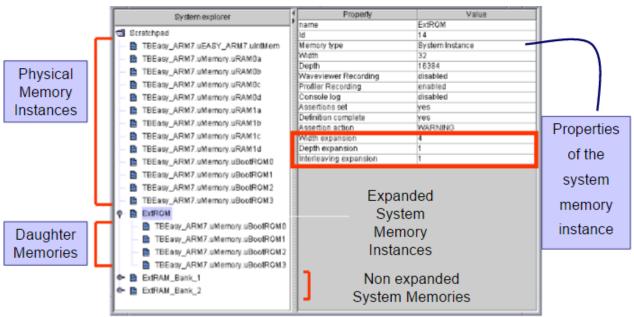


Figure 5.7: System Memory instance Properties

5.1.8 Daughter Memory instance Properties

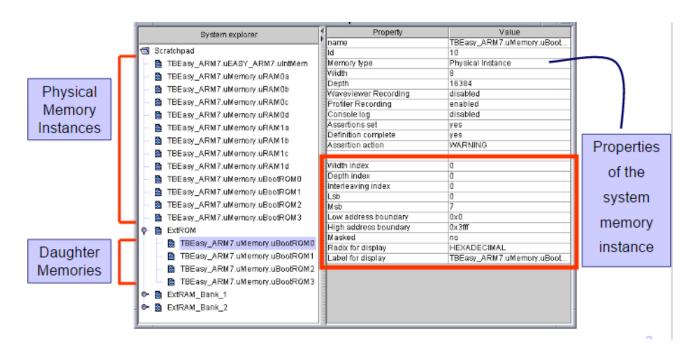


Figure 5.8: Daughter Memory instance Properties

5.1.9 Memory Layout

ExtROM : 0	tx0-0x100 8 bit	s/column		r⊧ I	a" 🖂		
≣ ∢ ▶ ⊞	🚹 🗂 🕐						Word Split
T= 280.31200	. 31-24	23-16	15-8	7-0			
0×0	0xe0	0x5f	0×0	0xf	-		into 8
0x1	0xe3	0xa0	0×0	0×0	12		
0x2	E EVIDOM	0x0-0x100 16 bit	electures assesses	onder lander kanne		rd 🛛	bits/coloumn
0x3	L LANGER .		1010000	02020202020			
0x4 0x5	∄ ◀ ▶ 8	🗄 🌆 🐨 🛞 –					
0x6 0x6	T= 280.3120	30 pc	31-16	_	15-0		
0x8 0x7	0x0	0xe06f	31-10	Oct	13-0		
Ox8	0x1	0xe3a0		0×0		100	
0x9	0×2						Word Split
0xa	0x3	ExtROM : Dxt	D-0x100 CUSTO	M 32 bits/co	lumn sesses	r 12	
0xb	0x4	iii ∢ ▶ 🖽 I	• C ®				into 16
Oxc	0x5	22					
Ord	0×6	T= 280.312000			31-0		bits/coloumn
0xe	0×7	0×0	0xe05f000				
0xf	0x8	0x1 0x2	0xe3a0000				
0x10	0x9	0x2	0xe3a0100				
0x11	0xa 0xb	Ox3 Ox4	0xe3a0200				
0x12 0x13	0xp 0xc	0x5	0xe3a0300				-
0x13	Oxd	0×6	0xe3a0500				Word Not
0.0.1.4	Oxe	0x7	0xe3a0600				
	0xf	0x8	0xe3a0700	10			Split
	0x10	0x9	0xe3a0800	00			
	0x11	0xa	0xe3a0900	00			
	0x12	0xb	0xe3a0a00				
	0x13	Ожс	0xe3a0c00				
	0x14	Oxd	0xe3a0e00	30			
	0v16	Oxe	0xe59ff0fc				
	_	0xf	0×e59f00fc				
		0x10 0x11	0xe3a0142				-111
		0x11 0x12	0xe581000				-1.1.
		0x12 0x13	0xe3a0000				-1.1
		0x13 0x14	0xe5c1000				- 2
		0x16	0xe3e0100				

Figure 5.9: Memory Layout

5.2 Objectives achieved

We divided this project into 3 major components

1. SLM GUI

- (a) Analysis of SLM GUI
- (b) Optimize existing code
- (c) Partial search feature
- (d) Differentiate Hexadecimal and decimal mode in displaying memory content
- (e) Integrate Partial search feature into SLM GUI
- (f) Analysis for SLM GUI plugin oint into SLM Core
- (g) Integrate SLM GUI into SLM Core
- (h) Extending command line arguments set for SLM GUI
- (i) Internal release of SLM GUI

2. Testcases

- (a) Analysis of C++ testsuit
- (b) Optimize testcases
- (c) Automate C++ testcases
- (d) Integrate C++ testcases into SLM Core
- (e) Study of VHDL testcases

3. SLM Core

- (a) Analysis of existing code
- (b) Design of new classes
- (c) Re-engineer classes which are independent of flexperf library functions

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

This project is about Re-engineering. So, in the first phase project activities were largely dominated by analysis process. Initially SLM GUI was stand alone software. After adding features related to search it was integrated with SLM Core.

Existing SLM code is decade old and heavily integrated with flexperf library functions. This library is obsolote now. In the next phase major project activities were dominated by eleminating dependency of classes to flexperf library functions.

6.2 Future Scope

6.2.1 Objectives for SLM GUI

1. Add new features into SLM GUI

Currently all the objectives related to SLM GUI is achieved. In future we can add new features if the requirement arises.

6.2.2 Objective for SLM Core

- Analysis of SLM core classes which are dependent to flexperf library functions Thorough study of classes with dependency to flexperf library function will be required in next phase in order to re-engineering of them.
- 2. Re-engineering of remaining classes

This is the central activity of this project. In this project activity, new classes which

are independent of flexperf library functions will be re-engineered.

6.2.3 Objectives for testcases

1. Automation of HDL testcases

Currently HDL test suit is in debugging phase. After this phase they will be automated to facilitate developers to test their code.

2. Re-engineering of testcases for re-engineered classes

It may be required to re-engineer test cases for both cpp and HDL test suit to test code for re-engineered classes.

Bibliography

[1] M. Sobczak, "C++/tk documentation." http://cpptk.sourceforge.net, 2015.