STANDARD CELL DESIGN AND LIBRARIES DEVELOPMENT

Major Project Report

Submitted In Partial Fulfillment of the Requirements

for the Degree of

Master of Technology in

Electronics & Communication Engineering

(VLSI Design)

by

ANIKET WAGHIDE

(14MECV02)

Electronics & Communication Engineering Branch
Electrical Engineering Department
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Nirma University
Ahmedabad - 382481
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Declaration

This is to declare that

(a) The report comprises my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

(b) Due acknowledgement has been made in the text to all other material used.

ANIKET WAGHIDE
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Certificate

This is to certify that the Project Report entitled **STANDARD CELL DESIGN AND LIBRARIES DEVELOPMENT** submitted by **ANIKET WAGHIDE (14MECV02)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology** in **"VLSI DESIGN", NIRMA University, Ahmedabad** is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Certificate

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Abstract

Standard cells are the building blocks of the modern ASIC world. They can be thought of as the alphabet that allows the ASIC designer (or ASIC design team) to write the novel (that is, design the ASIC). They consist of several simple (in general) functions, usually in various strengths, that can be (potentially repeatedly) connected together in a network and then patterned on a piece of silicon, such that the result is a desired functional integrated circuit. Digital design kit (DDK) vendors, most often representing fabrication houses, usually offer them in a family of several hundred of the various functions and strengths.

The actual choosing of which standard cells in a family to use in a design and the actual placing of these at various locations on a piece of silicon, both of which can be done manually, is usually done by software provided by various engineering design automation (EDA) vendors.These various software tools, work with representative aspects of the various standard cell that are pertinent to the particular software's requirements in order to perform properly their specific function.

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Chapter 1

Introduction

Application Specific Integrated Circuits are used to design entire systems on a single chip. ASIC are interconnection of standard cells which have been standardized by fabrication houses. With the integration of more and more system components on a single IC, the complexity of IC fabrication has increased. Modern day system design involves complex layout issues.Vendors generally gives specifications of required libraries based on leakage, delay, area, power. As per the requirement the libraries are designed consisting of layout view,schematic view ,abstract view, verilog view, symbol view. They are verified by performing DRC, LVS checks and given to Standard Cell front end team for characterisation.

1.1 ASIC Design Flow based on Standard Cells

As we know that the complexity in the designs is increasing rapidly, this is making the task of layout designer difficult to design layouts manually. Hence a custom ASIC cell library approach is desirable. The major advantage of using standard cell based designs is that Standard cell provides reusability of basic cells for various designs and gives optimal level of abstraction. The cell based ASIC design flow diagram shown in Figure 1.1 categorizes the entire design procedure into tasks that fall under several design teams. For designing an application specific integrated circuit using standard cells we need fully characterised libraries.The steps to follow in an asic design flow when using such libraries is as follows:

1. A high level description language is used to model a design. This HDL language provides sufficient data to tools which helps them to synthesize the code in to register transfer level or gate level design.The different HDL languages used are Verilog and VHDL.

2. After the synthesis of design, the functional verification of design is carried out design by providing stimulus using various simulator tools.

3. The partitioning of the design is done to make the design into a cluster of small blocks.

4. The deisgn is synthesized using standard cell libraries. This provides a gate-level net list depicting standard cells and electrical connections between them.

5. The functional verification followed by STA analysis is carried out. This gives us the knowledge of the critical path and the timing violations in the design.The timing optimisation can also be performed using various Vt cells.

6. The netlist of the design is given to Place and route tool Floor planning, power planning, placement . In Place and route tool placement Optimization and trial route are performed on RTL level netlist imported. Clock tree synthesis and timing analysis are performed. All the partitioned blocks are brought together at place and route level.

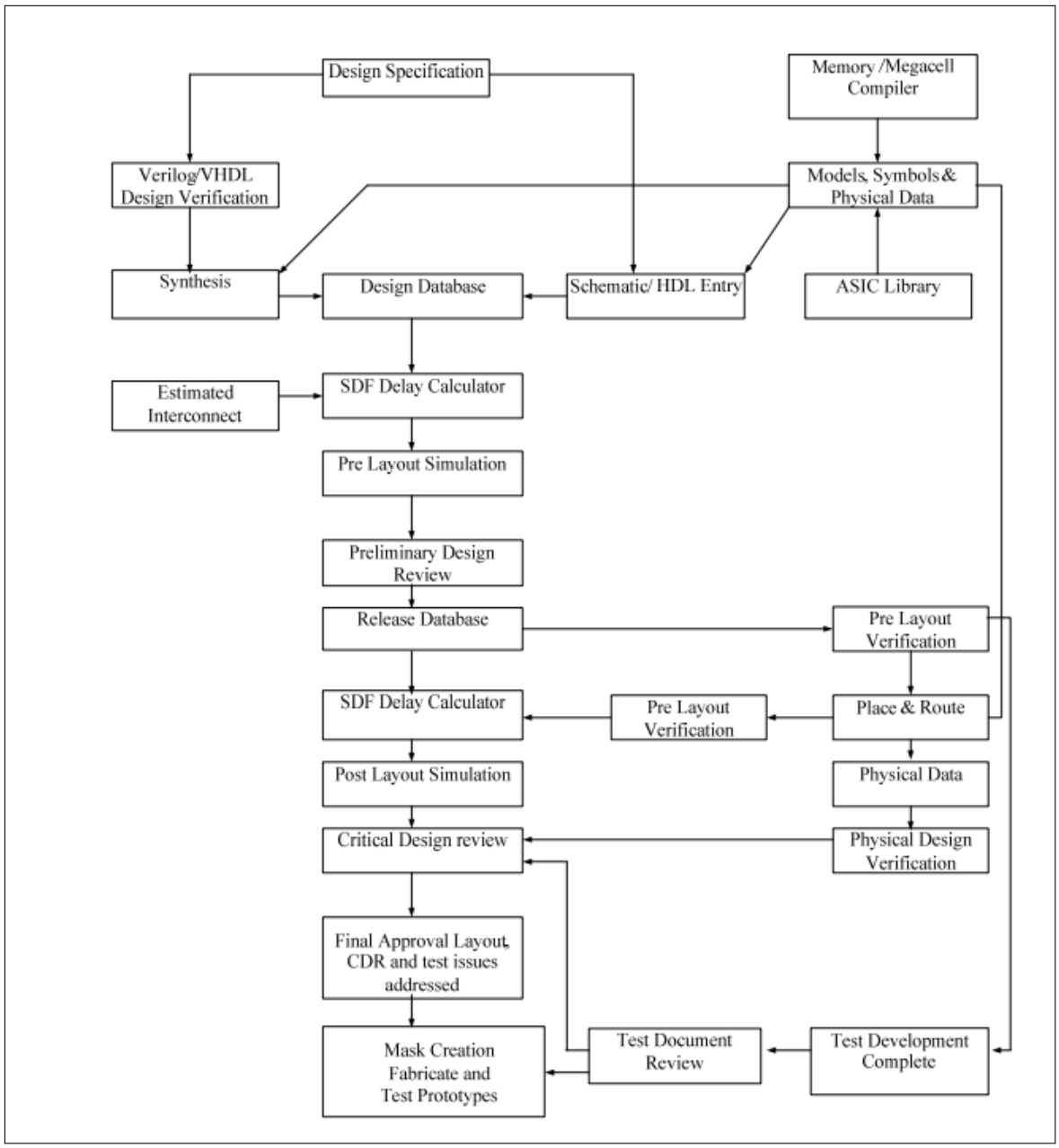

Figure 1.1.1: ASIC Design Flow

1.2 Objective of Standard Cell Libraries

As we know during the logic synthesis step in ASIC Design flow, .lib file is taken as input for synthesis. Thus to yield better synthesis results it is necessary to design library in optimized way to meet the requirements. The functional specifications can be in any form like designing of library with respect to optimization in terms of threshold voltages, area optimized, speed optimized, power optimized, etc. Thus to design such library keeping factors like drive strength, poly bias, is the main objective. Although there are advancements in lithographic processes, there are some limitations like to design the cells for getting better yield or to ensure the proper functioning when circuit is actually implemented on the silicon.This makes the designer responsible to follow the guidelines on his end while designing as well as verifying by performing various checks. This makes a robust library which will help to meet the yield of chip.

Chapter 2

Literature survey

Standard cell library developed is at 28nm FDSOI technology in the project. There is plenty of literature available on Fully Depleted Silicon on Insulator (FDSOI) technology and device physics. This section gives brief overview of FDSOI technology with more focus on ST Microelectronics's planer Ultra-Thin Body and Buried Oxide (UTBB) FDOI device.

2.1 Limitations of bulk cmos technology

The conventional bulk CMOS process is facing tremendous challenges to meet the requirements at 28nm node, the major performance hurdles are transistor variability, device electrostatics and increased leakage power [1]. As given in Fig. 2.1[2], Random Dopant Fluctuations (RDF) which represents the variability in number and position of dopants present in the transistor channel causes random differences in threshold voltage of the device, due to different transistors inside the same chip will show different electrical behavior called transistor variability. At very low technology nodes, this effect is predominant because there remain very less number of dopant atoms in the channel due to shrinked dimensions [2]. This degrades the stability and leakage power is increased at chip level affecting the chip performance and making corner sign off more difficult due to threshold voltage variations.

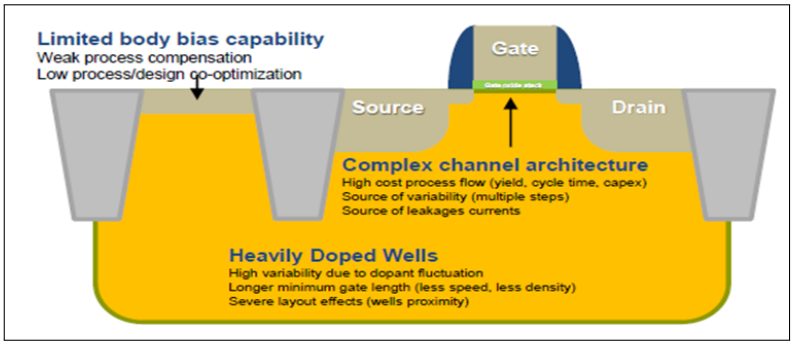

Figure 2.1.1: Cross sectional view of conventional CMOS

At lower technology nodes, short channel effects drastically impacts the performance of the chip especially the sub-threshold slope and drain induced barrier lowering (DIBL) effects seriously degrade performance/leakage trade-off of circuits [1]. Due to impurity scattering carrier mobility is degraded, along with that gate tunneling leakage current is increased

because of thinner oxide and, due to shallower junctions leakage currents are increased at low technology node. This reduces the potentially dynamic power savings at chip level. At lower nodes the CMOS process has limited body biasing capabilities. To increase the speed for low power application various techniques have been adopted such that multi-Vt, body biasing etc. This techniques depends on the efficiency body effect. Short channel effects at deep technology nodes reduces the efficiency of these power management techniques induced due to Vt variability. Undoped thin-film planar fully depleted silicon-on-insulator (FDSOI) device is promising alternative to bulk devices in 32-nm node and below because of their excellent short-channel electrostatic control, low-leakage currents, and immunity to random dopant fluctuation[1,2].

2.2 UTBB FDSOI: A Promising solution

ST Microelectronics's UTBB FDSOI offers wide range of advantages to cope up with the limitations of conventional bulk CMOS technology. This section describes the advantages and features of the UTBB FDSOI.

FDSOI has excellent electrostatic behavior by reducing random dopant fluctuation because of no channel doping required, thereby reducing VT variability along with that the DIBL effects are a drastically reduced in FDSOI devices [3]. These two facts improve the efficiency of multi-VT, multi-VDD, Dynamic Voltage and Frequency Scaling (DVFS) techniques, enabling logic and memories to function at very low supply voltage with better power management at chip level [4, 5].

FDSOI exhibits good control over short channel effects because of reduced junction depth. FDSOI devices does not require halo implant thereby natively offering good analog behavior. The devices comes with reduced Soft error Rates (SER) giving easy radiation hardening to the logic developed [6],as there is no channel doping, the device exhibits improved carrier mobility. The device does not form source/bulk and drain/bulk junctions, thereby reducing leakage power dissipation. The device use thick gate dielectrics so the gate tunneling leakage is reduced. The leakage currents in FDSOI are less sensitive to the temperature variations. FDSOI device does not have latch up effect. FDSOI offers wide Vt ranges for leakage power optimization along with that the device offers extended body biasing range as compared bulk CMOS facilitating efficient speed/leakage optimization.

The device has reduce source and drain area thereby reducing parasitic and thus lowering dynamic power, Carriers are confined from source to drain so channel leakage current is reduced. The device has good sub-threshold slope with reduced junction capacitance and diode leakage thereby improving the leakage power dissipation. Isolated substrate provides good substrate noise immunity.

One more crucial advantage with FDSOI is that the fabrication process very simple as compared to FinFET device, it requires 85 percent process steps as compared to bulk CMOS. Very easy migration is possible for existing IPs to migrate to FDSOI platform. The interconnect fabrication steps are same as bulk CMOS process.

2.3 UTBB FDSOI for power optimization

Wide range of low power techniques are employed in today's complex SoC for efficient speed vs. dynamic power trade-off and leakage power optimization. Various device architecture level features gives FDSOI upper edge for better deployment of the low power techniques.Multi-Vt support, extended body biasing capabilities and poly biasing techniques are discussed in the chapter.

2.3.1 Body bias or back bias:

In Body bias or back bias technique, a voltage is applied to the substrate or the body, thereby changing the threshold voltage of the device. Speed and power trade-off can be achieved by the application of the voltage at the substrate or body. It is used to dynamically boost the performance at the expense of increased leakage power with forward body bias and to reduce the leakage with loss in performance typically during idle time through reverse body bias .For NMOS negative body to source voltage is applied for reverse body bias and positive body to source voltage is applied for forward body bias for NMOS with vice-versa for PMOS device. Forward bias means Vbs>0, that is bringing gnds above gnd – and reverse bias is the opposite as shown in Fig, 2.3.1. Conversely for PMOS, forward bias means Vbs<0, that is bringing Vdds below Vdd.

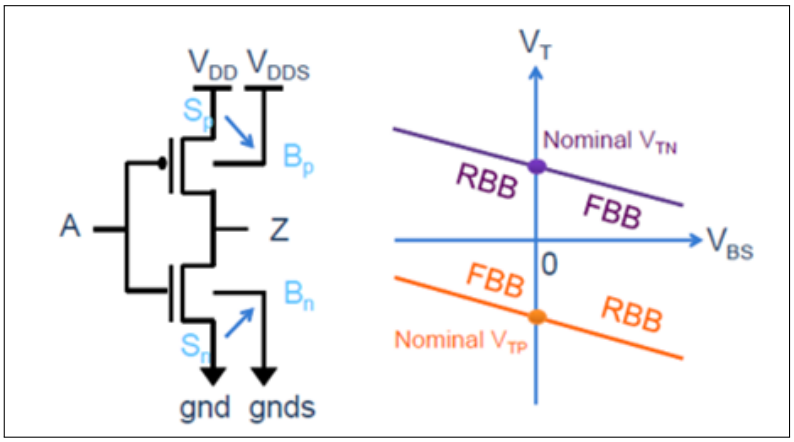

Figure 2.3.1: Effect of applying forward and reverse bias to substrate in FDSOI

Today's low power process technology provides more than one Vt device options typically High Vt, low Vt, and standard Vt for power optimization, these set of threshold voltages are called native threshold voltages. Body bias technique is used to shift the threshold voltage to values different than native offer. Back biasing can be implemented block level for chip level power management. In bulk CMOS technology the formation of P-N junction diode at source/drain to substrate puts limit on body bias range for -300mV to 300mV , otherwise the source and drain p-n junctions to substrate start to turn 'on' and too much leakage current starts to flow, there is no such problem in FD-SOI because source and drain are fully isolated from the substrate by the buried oxide. As a result it is possible to bias the N-well and P-well to much higher voltages enabling the extended body bias range from -3V to 3V with large performance boost factor. While the effectiveness of Body Bias tends to sharply degrade as transistor dimensions shrink and become relatively ineffective at the 20nm node, this is not the case for back-bias in FD-SOI.

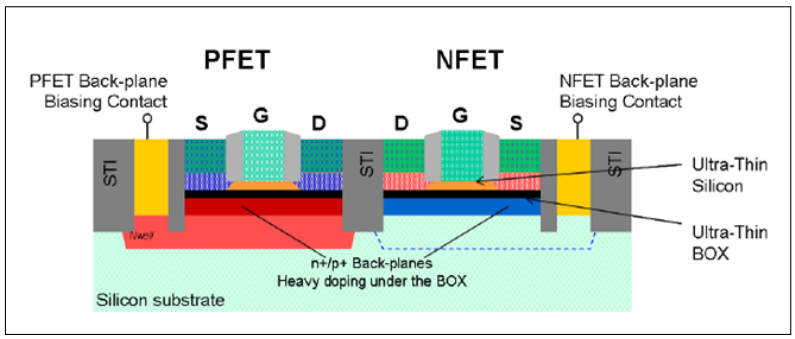

Figure 2.3.2: Back bias implementation in UTBB FDSOI

Back-bias requires bringing a bias voltage underneath the Box of transistors, as outlined in Figure 2.3.2. A contact is made between a biasing voltage source and the substrate, through the top silicon and the Box. Electrical continuity under the Box is ensured by an N-type or P-type well implanted under the Box. Obviously having a back-gate contact for each transistor would be penalizing in terms of area. However, owing to the electrical continuity ensured by the wells, multiple transistors sitting over the same well can be biased by a limited number of contacts the required as shown in Fig 2.3.2. Density of substrate ties will be defined by Design Rules of the technology. It is expected to be lower than the density required for Bulk substrate ties, as the primary factor that defines this density in Bulk is latch-up prevention – which is not a concern in FD-SOI owing to the presence of the buried oxide and resulting full device isolation.

2.3.2 Multi threshold voltage (vt) adoptation schemes

Multi-threshold voltage (VT) is widely used power management technique for speed/leakage optimization in today's SoC. High threshold voltage device offer reduced leakage with degraded performance used for power saving in non-timing critical paths, whereas Low VT device is used for high performance with increased leakage in timing critical paths. Multi-VT in planar bulk CMOS technology is achieved by multiple channel implants, this approach is normally not used in planar FDSOI, because it is an undoped channel technology. Regardless of this of this limitations planar UTBB FDSOI technology allows several methods for setting the threshold voltage VT, including engineering the gate stack work function, gate length-/poly biasing, body biasing, well implant type. UTBB FDSOI is capable of offering 2 native VTs Regular Threshold Voltage (RVT), Low Threshold Voltage (LVT).Various approaches to fabricate these devices are explained in this section. Using a doped back plane (BP) below ultra-thin buried oxide (BOX) allows setting up distinct VT options with a single metal gate through the application body biasing, in this approach the VT of the device is adjusted by the electrostatic control of the BOX/back plane interface. This back interface is shown as thick oxide/poly-Si back gate, of n/p type.

Literature provides bad process engineering techniques to give rise to multiple threshold voltage flavors with opposite well-plane architecture i.e is by using P-back plane with N-well and vice versa and similar well-plane for opposite device.Two native VT flavors are offered with no opposite implant doping by combining back plane and flip-well approach to save extra mask and avoid Vt process variability issue.booth the Vt flavour have same back-plane and well approach using flip-well as shown in Fig 2.3.3 and Fig 2.3.4. N back plane implant is not used with the P-well and N back plane implant is not used with the N-well to save mask cost[18].Keeping N-back plane with N-well and P-back plane with P-well two native

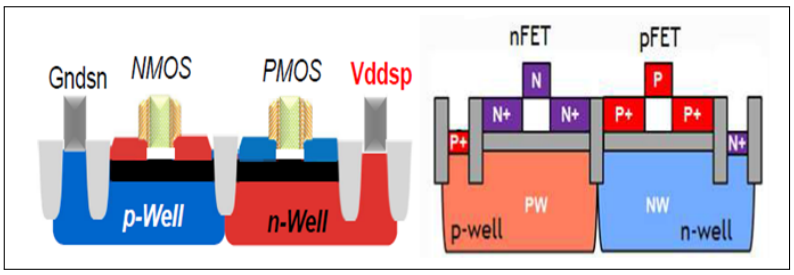

Figure 2.3.3: Regular threshold voltage device in standard well technology

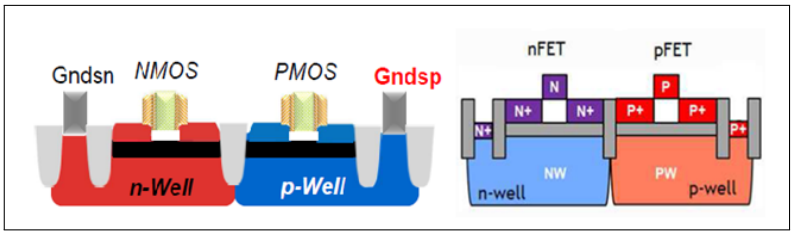

Figure 2.3.4: Low threshold voltage device in flip well technology

Vt flavors are generated through the use of body bias potential as shown in Fig 2.3.3 and 2.3.4.In regular threshold voltage device are constructed with same well-plane architecture for opposite device using conventional standard well techniques.n-type back plane along with n type well used for PMOS and vice versa given in Fig 2.3.3.The low threshold voltage device is build with flipped-well architecture, i.e n-back plane along with n-well is used for NMOS device and vice versa through the effective use of body bias as illustrated in the Fig 2.3.4. Apart form this native flavours extended body bias range allows furthe threshold voltage modulation.

If opposite well plane architecture is used than a floating P-N junction diode is formed underneath the buried oxide that impacts the polarization of ground plane making it unstable and thereby causing threshold variations with increased leakage current because of diode[18].With the flip well architecture this is issues is no more present but the bulk has to be kept at proper bias voltages for the flip well diode to work.Flip well technology is specific FDSOI because the wells have no impact on the electrical characteristics of the transistors and thanks to the buried oxide that ensures a total dielectric isolation of the device.[18]

Chapter 3

Design Methodology

This chapter gives the detailed methodology for the development of standard cell library development.

3.1 Creation of Standard Cell Library

Cell pins, with the exception of abutment pins (VDD and GND) must be placed on the intersections of the vertical and horizontal routing grids. Vertical and horizontal routing grids may be offset with respect to the cell's origin, provided that the offset distance is exactly one-half of the grid spacing. The cell height must be a multiple of the horizontal grid spacing; the cell width must be a multiple of the vertical grid spacing.

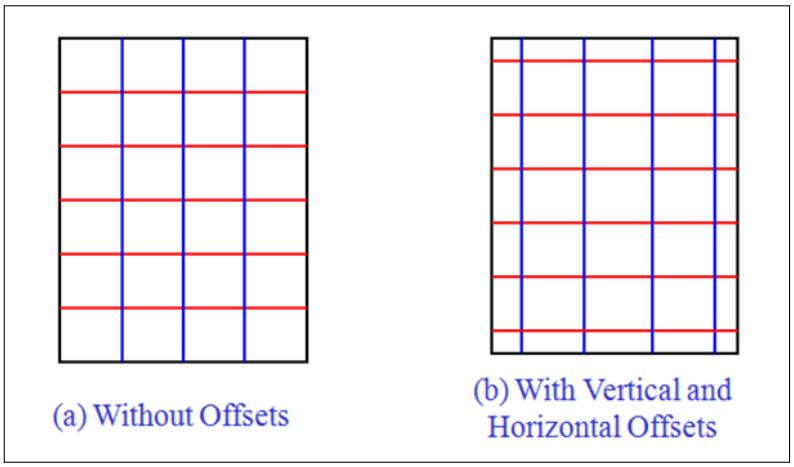

Figure 3.1.1: Routing grids in standard cell

The fig 3.1.1 shows the horizontal and vertical routing grids. Figure a represents grid with zero offset and figure b represents grids with some offsets. The grid highlighted in red color represents the horizontal routing grid and that in blue color shows vertical routing grid. The routing grids are where the over-the-cell metal routing will be routed. The pins of your standard cells should always lie on the intersections of the horizontal and vertical routing grids [7]. Although some CAD tools will route to off-grid pins, this may cause some other complications.

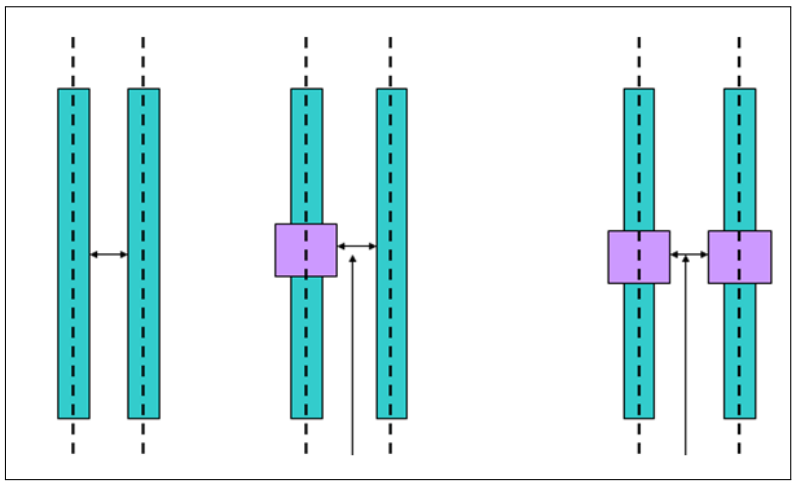

Figure 3.1.2: Via spacing

The fig 3.1.2 shows the spacing guidelines, the first figure shows the minimum spacing, grid spacing must be defined for each routing layer. The first figure in 3.1.2 indicates minimum spacing. The second figure indicates placement of via on routing grid and the minimum spacing for placement of via on neighboring grid. The spacing between two vias is shown in third figure in fig 3.1.2.

3.2 Standard Cell Library template

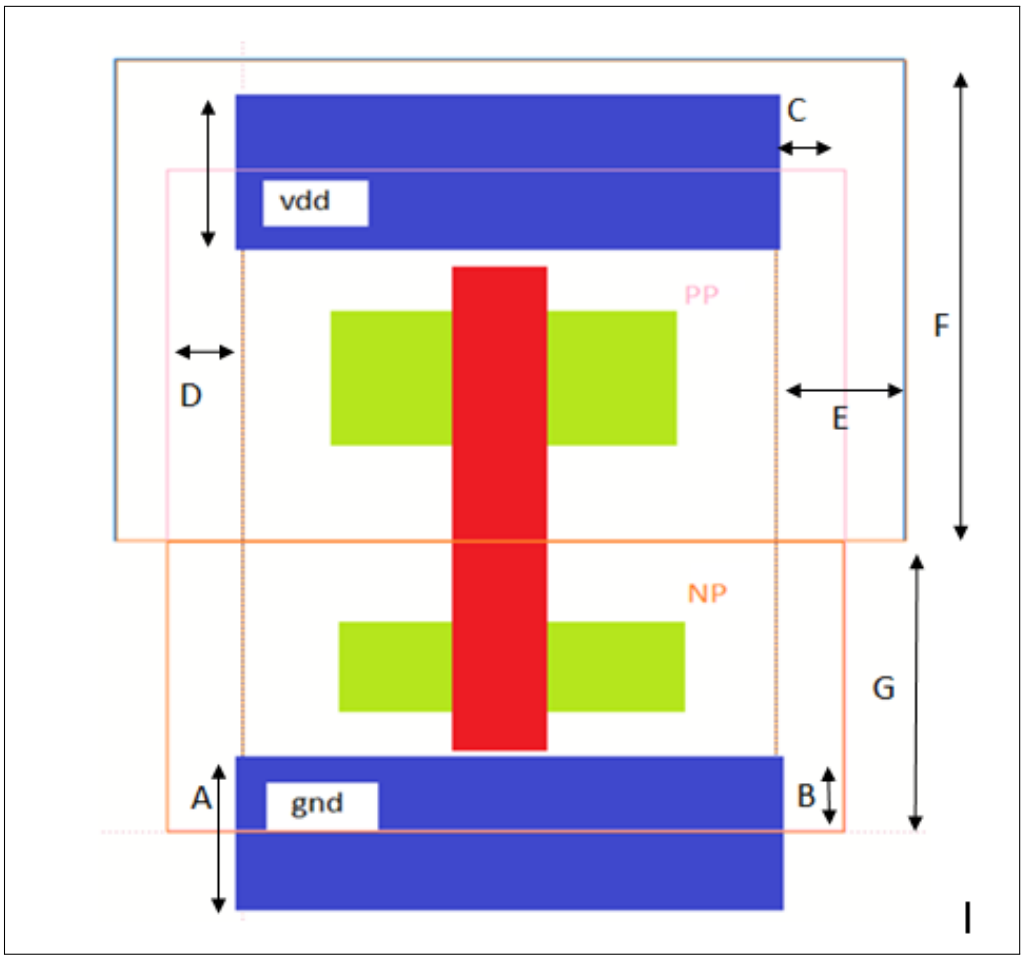

Figure 3.2.1: Standard Cell Library Template

The fig 3.2.1 shows the standard cell library template. The standardization for the template is mostly formed by keeping PR boundary as reference for mask layers, implant layers, etc. In the above figure 'A' represents the height of the power rail vdd and gnd which is fixed for a given library. 'B' represents the vertical offset of power rail from PR boundary. 'C' and 'D' represents the extension of the implant layers from PR boundary in x direction. 'E' represents the NWELL extension from the PR boundary in x direction and upward direction. 'F' represents P implant layer length and 'G' represents N implant layer length. The widths of metal layers are fixed and are generally greater than the widths of the metals routed. This is because to reduce the electromigration effect. Increasing the metal width reduces the effect of movement of ions in metal. Usually PMOS is connected to vdd and NMOS is connected to gnd, thus top region of layout is allotted to PMOS and bottom region to NMOS in layout.

3.3 Types of standard cell libraries

The libraries are classified mainly with respect to basic reference to the cell architecture, properties regarding to performance, specific cell and drive driven properties. The architecture of the libraries is divided into high density specific, high speed, data path architecture, etc [11]. The performance properties may include oxide thickness, threshold, optimization, symmetric design, etc. Oxide thickness mainly include for a particular process, the thickness of the oxide is 'X' nm and for another process, it may be 'Y' nm.

Threshold represents the devices mainly regular voltage threshold, high voltage threshold, low voltage threshold or ultra high threshold voltage devices. Libraries may be defined in terms of area optimization, speed optimization or power optimized manner. The power optimized libraries can be for design optimized for clock power dissipation or data power dissipation.

3.4 Functionality based Classification of libraries

Based according to the function of the particular cells, the libraries are grouped into mainly CORE libraries, Place and Route library, Engineering change order library, clock library, retention flop library, etc.

Clock library mainly contains of clock buffers, clock inverters or clock gating cells, all these required to meet the timing constraints like setup and hold optimization, etc.

The core library consists of basic gates like inverters, buffers, and gates, multiplexers, complex gates like AOI (And OR Inverter), flip flops, latches, etc. Majority of the cells are taken from this library.

Place and Route library consists of the cells using during backend physical design process i.e. place and route. The cells are mainly filler cells which may be used to increase the density of the cell [11], antenna protection cells, cells used for clearing layout versus schematic checks, etc.

3.5 Drive strength of library cells

Functions of library include cells like AND3, OR5, MUX2, etc. Standard cell library provides multiple cells with different drive strengths like X2, X4, etc. The consumption of power is more for cells with higher drives, but can be used to drive larger load. They can be used to improve the circuit speed. The granularity or quantization leads to over design.

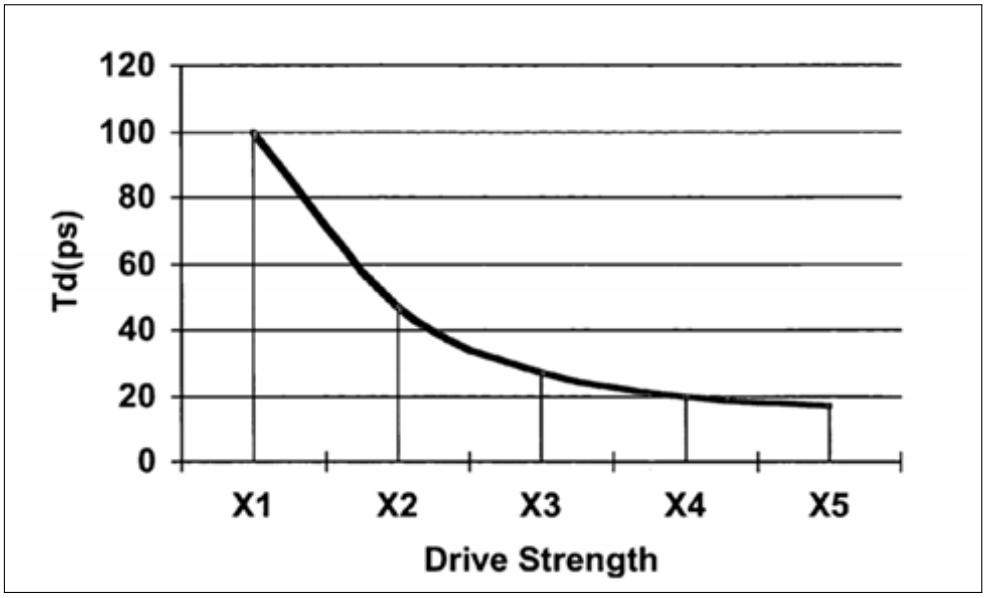

Figure 3.5.1: Delay Variation versus drive strength

The fig 3.5.1 shows the variation of delay versus the drive strength at the nominal load. Consider a case where cell needs drive strength of x1 and nest available drive strength is 1.2X, also 0.7X drive strength is available. In either case the power consumption is significantly reduced compared to cells having drive strengths X1, X2, etc [3].

The number of strength cells must be carefully choose as unnecessary addition of drives can lead to increase in the synthesis run time. The drive strengths, are generally referred to an active area, such that a 2X cell has twice the active area of an lX cell, and an l.2X cell has 1.2 times the active area of 1X cell, etc. However, cell active area and cell physical area do not necessarily scale together, [3] and so in practicing the invention, various choices can be made in relating cell physical size to cell drive strength.

Chapter 4

Development Flow

4.1 Library development flow

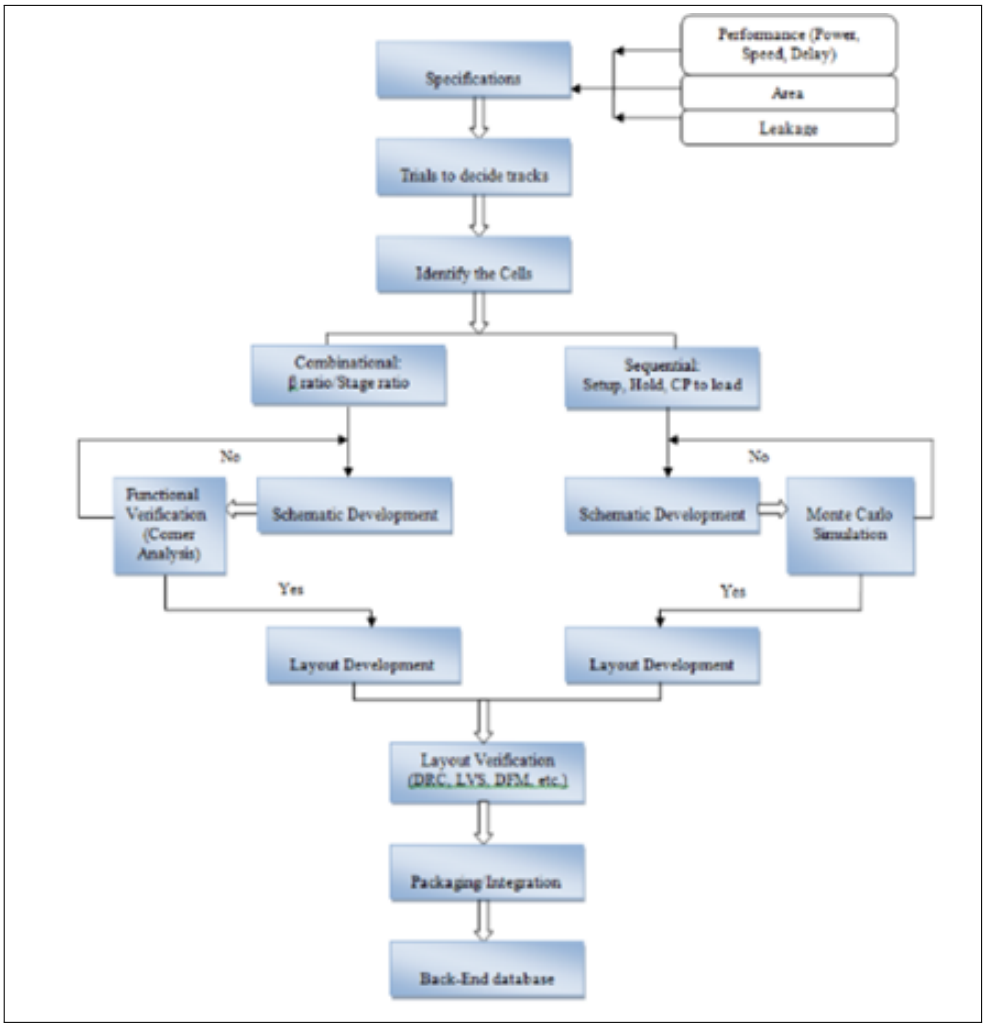

Figure 4.1.1: Standard cell Library Design Flow

Library is a collection of cells. It is the data used for system on chip design. It consists of different views used for designing of the chip. The initial phase involves use of device kits, tools required for the development. The tools required for development are sourced from a particular file. The appropriate design kits are chosen according to the requirement of the

customer. The next phase involves actual characterization, schematic, layout development, etc.

The fig 4.1.1 depicts the library development flow in elaborative manner. Based on the specifications in terms of area, timing or power, the number of tracks are decided for the design required. For combinational cells the beta ratio and widths are fixed by the front end development flow. For functionality validation characterization is performed at a particular PVT [4]. For sequential cells, timing checks are done which checks the setup and hold time failures of a cell.

After functional verification and Monte Carlo analysis design is staged for layout development. Once the cell level schematics are optimized back end team starts layout design. After the development of layout, verification checks like DRC, LVS, DFM, etc are performed. All the cells of library are then integrated and library is ready for packaging. After packaging of library backend database is developed which contains information about different views.

4.2 Standard Cell library format

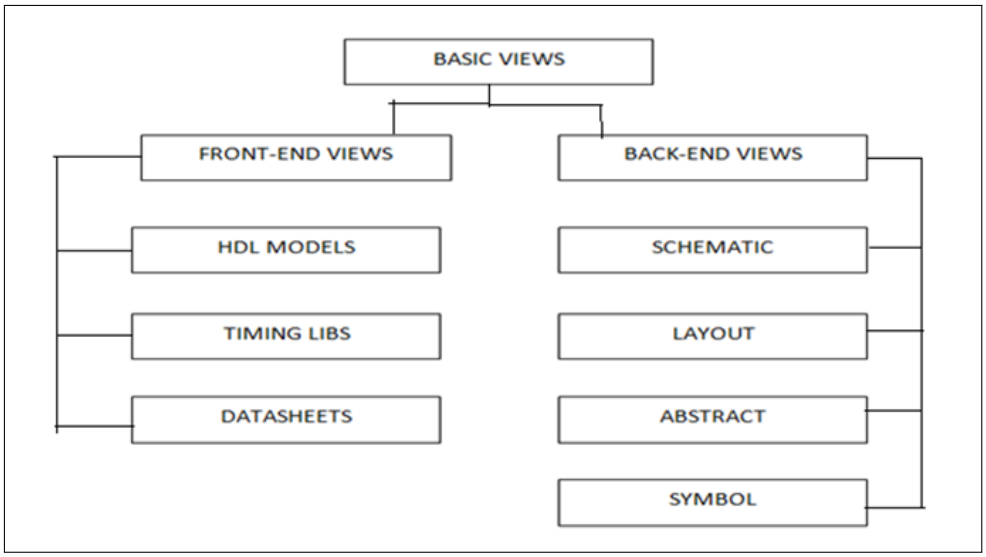

Figure 4.2.1: Structure of Standard cell library

There are two basic view front end and back end views. The information about timing and modeling of the cell is given by front end view. The physical design information is given by backend view.

4.2.1 Back end views

4.2.1.1 Layout view

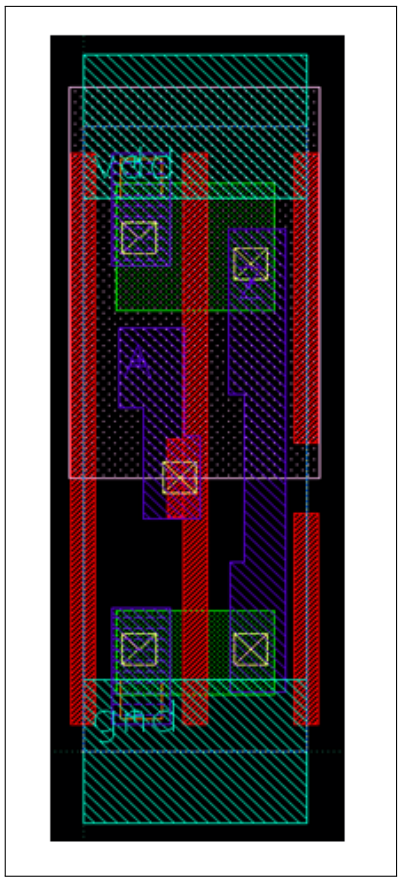

Figure 4.2.2: Layout view of standard cell

The layout view represents the actual physical implementation of the cell that is to be implemented on silicon. The representation comprises of different layers used in layouts . Above figure shows the layout of an inverter cell. The blue layer named metal M1 layer represents the metal layer used for terminal interconnections, routing . The light green layers named metal M2 layer labeled vdd and gnd are used for power rails . The light orange box layer signifies a via between M1 metal layer and M2 metal layer. The green layer called RX region defines active region for PMOS at top and NMOS at the bottom. The poly silicon layer shown in red color signifies the gate of both the transistors. The light pink highlighted color layer shows the BP layer which shows the area of P implant layer.

4.2.1.2 Symbol view

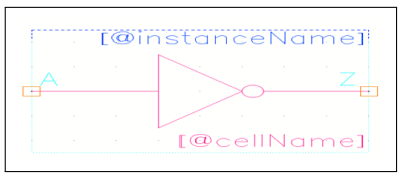

Figure 4.2.3: Symbol view of standard cell

The fig 4.2.3 shows the symbol view which gives the information about selection box, pin labels, symbol graphics. The shape of symbol in symbol view indicate the functionality of the cell.

4.2.1.3 Schematic view

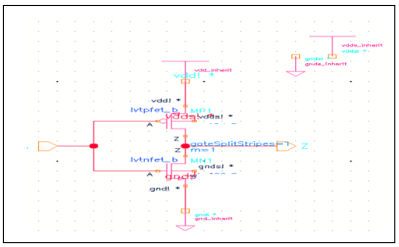

Figure 4.2.4: Schematic view of standard cell

In this view basically the instances, nets, wires, pins, supply pins of the device are shown. Pins are nothing but input and output of the schematics view. Schematic view is the transistor level implementation in which the transistors widths, number of fingers of transistor is also shown .

4.2.1.4 Abstract view

Figure 4.2.5: Abstract view of standard cell

In this view all the metal connections in the layout are shown.Apart from the metal connections the pins locations , rail connections , details about the PR boundary ie if there is offset in the PR boundary. This view is important for place and route tool as the Place and route tool doesn't require require other layers information while routing. This view is very useful in that scenario.

Chapter 5

Library validations and checks

5.1 Valication Checks

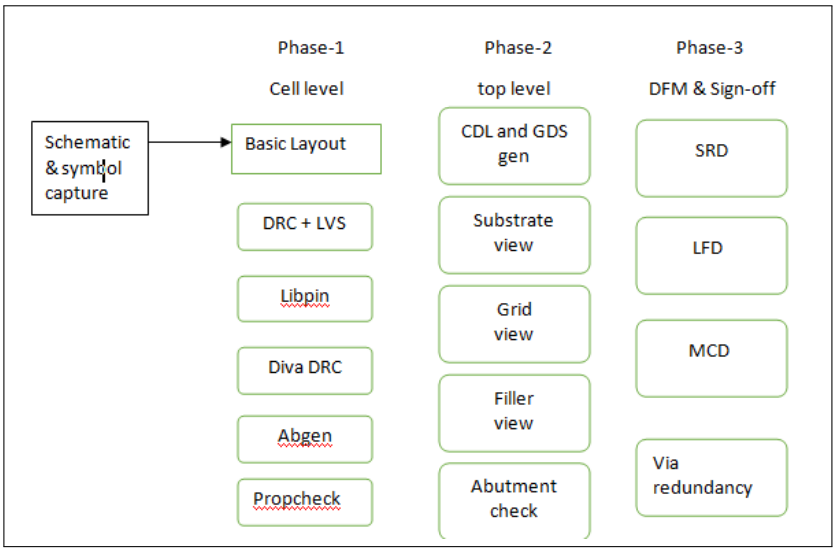

Figure 5.1.1: Validation flow

The fig 5.1.1 shows the validation flow. In the initial step layouts are drawn from schematic and consistency checks are performed to check whether the pins are on the grid crossing or not.After this check DRC check is performed.

DRC rules are different for different technologies. DRC rules are decided by the foundry people based on the process technology in the form of Design Rule manual (DRM). Some of the most common DRC errors are minimum width violation,minimum area violation, minimum spacing violation, contact and via coverage violation, etc.

LVS (layout Vs Schematic) is a tool that compares the connections in the schematic with the connections in the layout. If there is a mismatch between the two, it shows an LVS error. Some of the common LVS errors are like property errors, missing Instances, incorrect nets, missing ports.

Another phase in validation involves generation of substrate views, grid views, filler views, etc. After generation of these views, abutment design rule check is performed in which cells are abutted in a random way to check whether any design rule is violated after the placement of all the cells of library.

The next phase of validation involves design for manufacturing checks which include Optical Proximity Correction (OPC) checks, Smart Regular Design (SRD) checks, Manufacturing Check Desks (MCD), Litho Friendly Design (LFD) checks, etc. These checks are performed with intent of increasing the yield in the process by optimizing the layout .

5.2 Design rules and basic checks

The section gives brief idea about various types of design rules. The section also depicts how design rule check (DRC) is performed along with the results.

5.2.1 Design rules

Every foundry has its own set of silicon fabrication process rules for the given technology based on the manufacturing process methodology. The layout drawn must comply with these rules in order to get manufactured at the particular foundry. The rules are described along with their name and implications in a Design Rule Manual (DRM) supplied by the foundry along with the technology design kit.

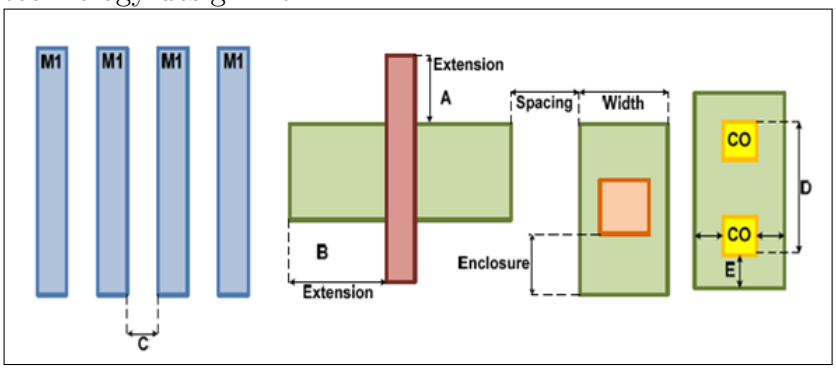

Figure 5.2.1: Basic design rules

As shown in Fig. 5.2.1, A is rule for the extension of the poly silicon in the direction other than source/drain side shows the active area extension past PC. This rule is associated with a layout dependent effect called length of OD(LOD),where change in threshold voltage is observed due to rounding of active region. C is a metal to metal spacing rule D is center to center separation between two contacts and E is the distance of contact form the active, if this rule is not followed than a bad contact is formed causing no connection.

There are three basic types of rules: Size rules are for example minimum width, minimum area of a shape, length of a particular shape etc. Separation rules describe minimum separation distance from two geometries on same or different layer. Overlap rules, where certain shapes have to be overlap by an amount due inaccurate mask alignment.

5.3 Basic checks

5.3.1 DRC checks

The DRC checks can be mainly categorised into minimum area/width rules , minimum spacing rules , minimum overlap rules. Minimum width violation: for each technology the

each layer has some fixed width. If we do not follow this DRC error will come. If we do not fallow the minimum width for the metal open will create between interconnections. Minimum area violation: every layer as some fixed minimum area in each technology, minimum area required is necessary for the manufacturing without error. Minimum spacing violation: minimum spacing between layers is required to avoid shorts between layers, some of the spacing rules occur between metal-metal, contact-contact, and via-via. Contact and via coverage violation: minimum contact coverage by metal should fallow to avoid contact punch through minimum via enclosure by metal to flow of current between to metal layers.

5.3.2 Layout vs Schematic checks

This check basically checks whether properties of the schematic are same as the the properties of layout. It checks for all the interconnects between the transistors and verifies whether the same connections are made in layout or not. If they are not same then an error is flaged. This check can only verify the connectivity,number of transistors , transistor widths ,input and output pins but it will not show if there is any functionality error in the design.

Some of the common LVS errors are like Property errors which are related to the width of the transistors. If the width of a transistor is not same in the layout and the schematic then it will show a property error. Missing Instances in which if some connection that is present in the schematic is missing in the layout or if any label present in the schematic is missing in the layout or if the number of transistors are not equal in the layout and the schematic, then it will gives the corresponding instance error. Incorrect nets problem arises due to mismatch in the interconnections between the schematic and the layout. Missing Ports because if the labels present in schematic are either missing or not on correct layer in the layout.

5.4 Other integration checks

Apart from the basic checks some checks are performed like abstract check, half DRC check, gds abutment check, etc for the validation of standard cell library. These checks contain information about process oxide, technology, library architecture, supply pins, etc.

5.4.1 Half-drc check

The rules in check are coded according to the template for the cells of the library. The standard cell template of the dimensions of different layers must be maintained uniform across the library. Fixed power rail and via template is coded in these checks. The distance of the metal from the PR boundary or the NWELL position template is fixed.

If the cells of the library need to be abutted, some specific distance has to be maintained between the abutted layers. For that purpose half DRC rules are coded which provides rules for metal and via spacing from the PR boundary. The rules regarding the pin accessibility are also coded in this check, to verify whether the pin has sufficient number of hit points or routing points as specified.

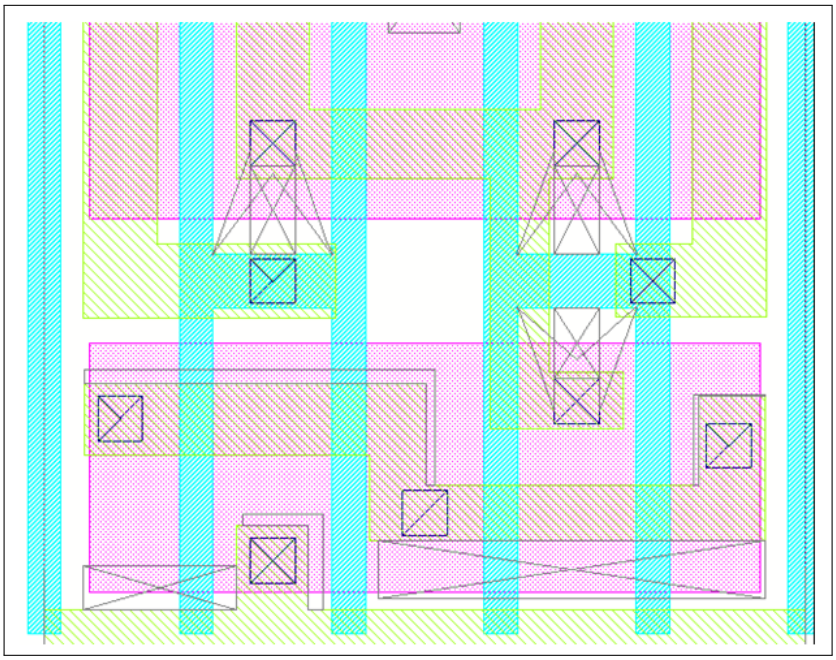

Figure 5.4.1: Half DRC examples

The fig 5.4.1 shows the half-DRC check performed on the layout. The cross boxes indicate the violations; one of the violations shows the distance of the metal from PR boundary. The other violation shows distance of contact from the corner of H-shaped poly.

5.4.2 Abstract generation checks

These checks include checks with respect to DFM (Design For Manufacturing) guidelines. They are broadly classified into two types mainly those checks are mandatory and the other which are tolerated under designer responsibility.

```
-- Abgen ---
## Check under the responsibility of : sagar

  %%% Decks %%%
eck     :  divaDRC_CMOS028SOI.rul_v1.111
b Cells :  1

>>File<<<>>>/data/cmos028lpg/BE/GROUP/SAGAR/VIRTUOSO/QUALIFICATION/MAT09/OPUS/ABGEN/absdeckupd.log<<<
ILE NOT FOUND
>>File<<<>>>/data/cmos028lpg/BE/GROUP/SAGAR/VIRTUOSO/QUALIFICATION/MAT09/OPUS/ABGEN/abs.log.opus<<< 10:02 Mon 11 Apr 2016
>>File<<<>>>/data/cmos028lpg/BE/GROUP/SAGAR/VIRTUOSO/QUALIFICATION/MAT09/OPUS/ABGEN/abs.log<<< 10:02 Mon 11 Apr 2016
>>File<<<>>>/data/cmos028lpg/BE/GROUP/SAGAR/VIRTUOSO/QUALIFICATION/MAT09/OPUS/ABGEN/C8T28SOI_LL_NAND2X8_P0/abgen<<< 10:02 Mon 11 Apr 2016
kOpusIAppendRegUserTriggers Warning : new registration of already registered userPostInstallTrigger maskLayout CreateAddonRef
       8  DFM.RBT.LT2CAonRX at least 2 CA in RX region are recommended for robustness
       2  DFM.SC.CA_GR_204b RX minimum overlap past CA in gate direction >= 0.013
       4  DFM.SC.M1_GRabut1 prBound minimum overlap past M1 >= 0.035
       3  MDT.SC.CA_GR_207bR1 CA over RX min space to PC inner vertex = 0.098
       3  MDT.SC.CA_GR_207bR2 CA over RX min space to PC = 0.092
      10  MDT.SC.M1OBS_R_1 M1 obs layer must be within M1 drawing layer
       4  MDT.SC.M1_GRabut1 prBound minimum overlap past M1 >= 0.025
       4  MDT.SC.M1_abut_504k2 (M1 span > 0.072 & runlength > 0.104) min space to prBound >=0.033
       4  MDT.SC.M1_abut_504l2 (M1 span > 0.156 & runlength > 0.104) min space to prBound >=0.034
       4  MDT.SC.M1_abut_504m2 (M1 span > 0.208 & runlength > 0.104) min space to prBound >=0.037
      46  Total errors found
-- End of File ---
```

Figure 5.4.2: Abstract generation log

The fig 5.4.2 indicates the abstract generated log with the errors categorized into mandatory errors indicated by MDT, errors tolerated under designer responsibility and DFM errors.

Mandatory errors shown include contact spacing on RX to poly, minimum RX enclosure of contact in gate direction, etc. DFM error shows requirement of 2 contacts on the RX region recommended for robustness.

5.4.3 DRC or GDS (graphic database system) abutment check

In these checks, the cells of the library are randomly abutted or placed in top, bottom, left, right position. This check ensures that at the time of placement of standard cells there should not be any DRC violations or half DRC violations. This database is commonly termed as co validation database. This abutment can be done either by encounter tool or by skill method. The encounter tool uses electronic digital implementation place (ediplace) or electronic digital implementation route (ediroute) methodology for development of abutment database.

5.5 Generation of views

There are some views generated at the time of integration of the library required for validation purpose. These views are as mentioned below.

5.5.1 Substrate view

In order to clean the LVS errors we run this check wherein substrate connection is given to the layout. In Fig 5.5.1 the cell which is in the left is called substrate tap cell and the cell in the right is a normal cell from the library. The black background is treated as p-substrate. Here both N-well and the power rails of 2 cells are connected.

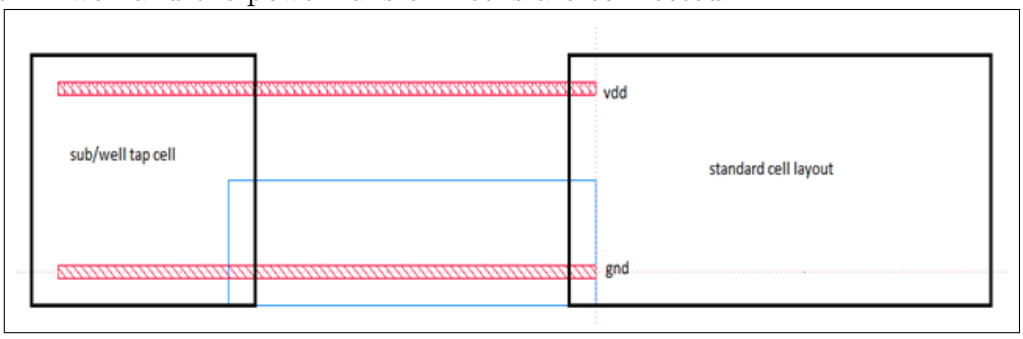

Figure 5.5.1: Substrate view

5.5.2 Grid view

The standard cells will be placed adjacent to each other like a wall of bricks. Here we have created grid view of layout wherein a standard cell is placed and its N-Well is extended as shown in fig.5.5.2 so that well-proximity effects are taken into account. Also M2 and M3 are placed on every grid so that parasitics are extracted considering the worst case as shown in Fig. 5.5.2. In implantation phase, Kinetic ions scattered and embedded near cell boundary edge resulting in Vt shift is called well proximity effect.

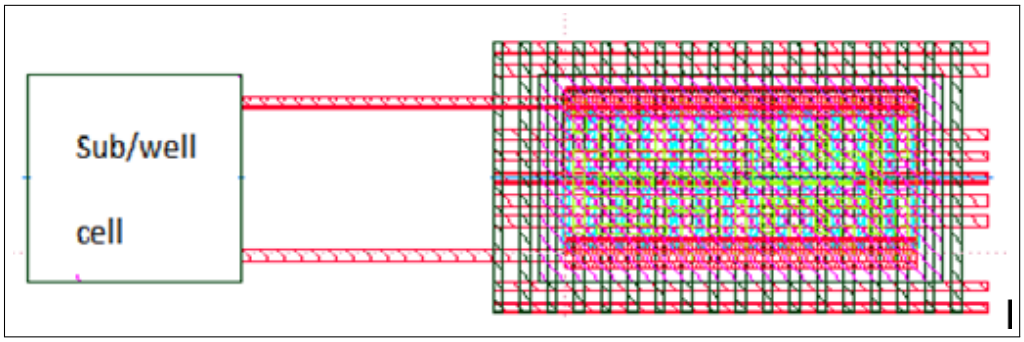

Figure 5.5.2: Grid view

This view adds grid to the layout for the calculation of parasitic. Grid is added to the above view as discussed. This view is required for parasitic extraction i.e. for extraction of the netlist. In this view NWELL is extended so that well proximity effect does not affect the performance of the layout.

5.5.3 Filler view

Filler cell does not contain any transistor, it only has well, power and ground connections using the same design rules and the template used for the library. The filler view places filler cell at all side of the cell to ensure that filler cell are being properly placed on all sides maintaining the continuity of rail and via. During place and route phase the CAD tool places filler cells with standard cell to meet the density requirement, to ensure whether tool will be able to put filler properly or not this check is performed in Fig. 5.5.3

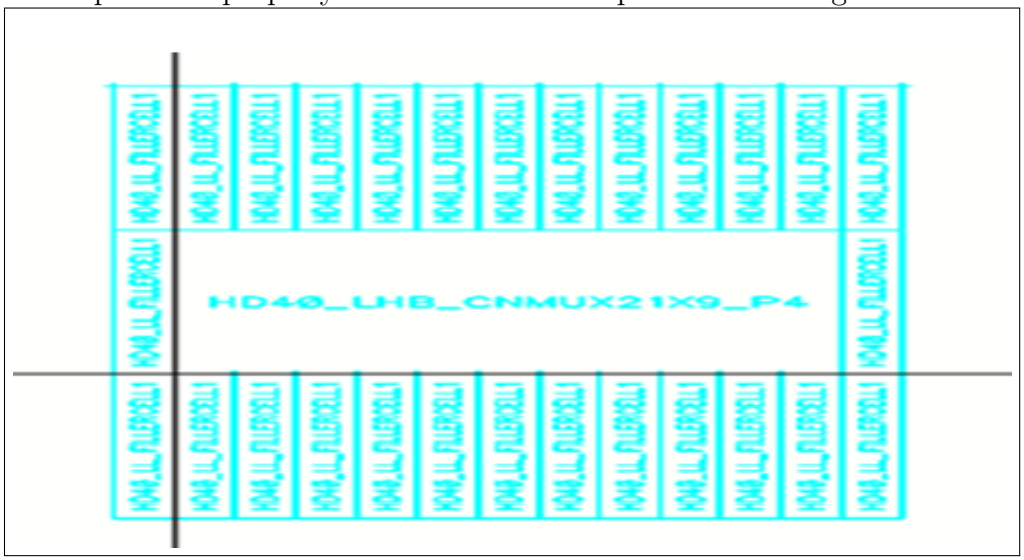

Figure 5.5.3: Filler cells surrounding a cell

5.6 Design for manufacturing checks

As we move towards deep submicron technology, the random variations in the lithographic, etching, mask generation, etc limits the catastrophic or parametric yield loss. Since the lithographic projections are highly non linear at different process conditions, it cannot be captured at the design rule level. There is a tradeoff in area if we try to relax DRC. Layout

Dependent Effect (LDE) variations can affect timing and performance. The stress and strain developed, well proximity effect can change the electrical characteristics of the transistor.

5.6.1 Dfm guidelines

In order to mitigate with the above effects, it is necessary to follow the guidelines like taking care of the critical signals, making use of the dummy poly, making maximum use if of contacts in source or drain region. Widening of the wires, addition of vias in layout are also probable solutions of increasing the yield with respect to Design for manufacturing requirements.

Chapter 6

Work Done in project

6.1 Schematic comparison for area ,power and speed in 28nm and 40nm

6.1.1 Introduction to the activity

The activity consist of following steps:

1. Analyze the 28nm and 40 nm libraries for a list of cells which consisted of AOI,OAI, NOR/NAND, OR/AND, XOR/XNOR, inverters, buffers .

2. First find all the combinational logics with same functionality but different architecture. For example : AND2B(AND gate with B inverted) NOR2A (NOR gate with A inverted).

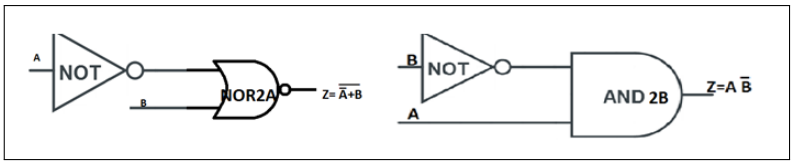

Figure 6.1.1: Gate level schematic of AND2B and NOR2A

3. The combinational logic with such different architectures are compared for speed ,area and power .

4. The tool used for this analysis is Eval Ring which is an internal ST tool . The tool uses the design under test ie. our combinational logic and creates a ring oscillator .

5. We apply the inputs to the DUT as given below and make it an inverter.

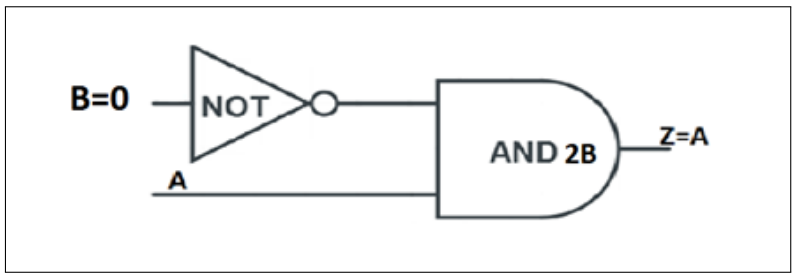

Figure 6.1.2: Inputs to AND2B

6. Using such type of inputs we can monitor the effect of each input of gate on the output.

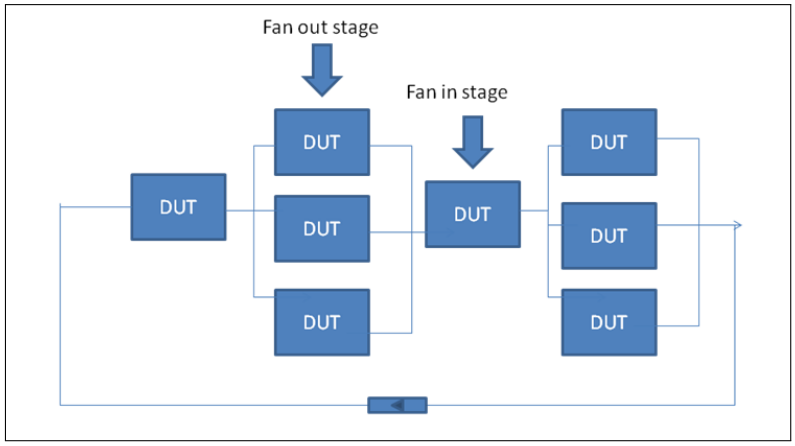

Figure 6.1.3: Block diagram of ring oscillator

7. Tool used to design the schematics and layouts of the combinational logic is Cadence Virtuoso.
8. The conditions used for :
   - Delay analysis:
     - NMOS and PMOS are the slowest
     - Temperature is -40c.
     - Voltage : VDD 0.9
   - Power analysis:
     - NMOS AND PMOS are the fastest
     - Temperature : 125c
     - Voltage : VDD 1.5v

6.1.2 Results of activity:

1. The three stage circuits are found to be faster than a two stage circuit.
   - Theory says the two stage circuits are faster than three stage circuits but the results of the above activity tend to differ from it. The reason for it could be the

output stage is a single stack for three stage circuits whereas it is a two stack for a 2 stage circuit.

2. Area is increased for three stage circuits.
3. Power dissipation has also increased for 3 stage circuits.

6.2 Design of a mux to improve the dynamic power dissipation and delay reduction

6.2.1 Introduction of activity

1. The below shown is 8:1 MUX is the reference of our analysis.

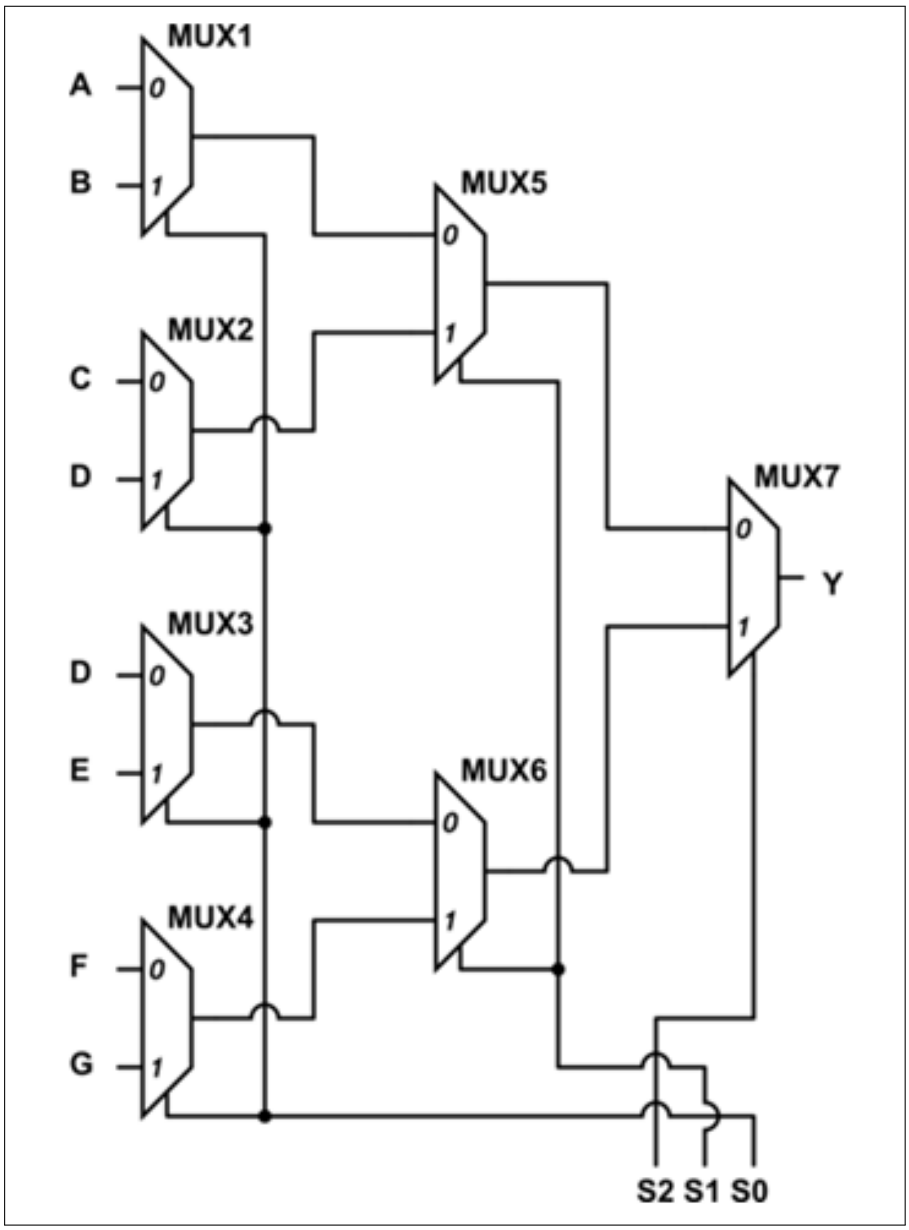

Figure 6.2.1: Conventional 8:1 mux

2. The drawbacks of the above MUX are:
    - EXCESS POWER DISSIPATION : If 8 clock signals are toggling but only one will be selected .So rest of the toggling clocks will add to unnecessary dynamic power dissipation .
    - EXCESS DELAY: Each clock will have to travel through 3 stages in this conventional mux .
3. The new mux design must be a design to reduce all the above draw backs .
4. The schematic proposed for this new mux is :

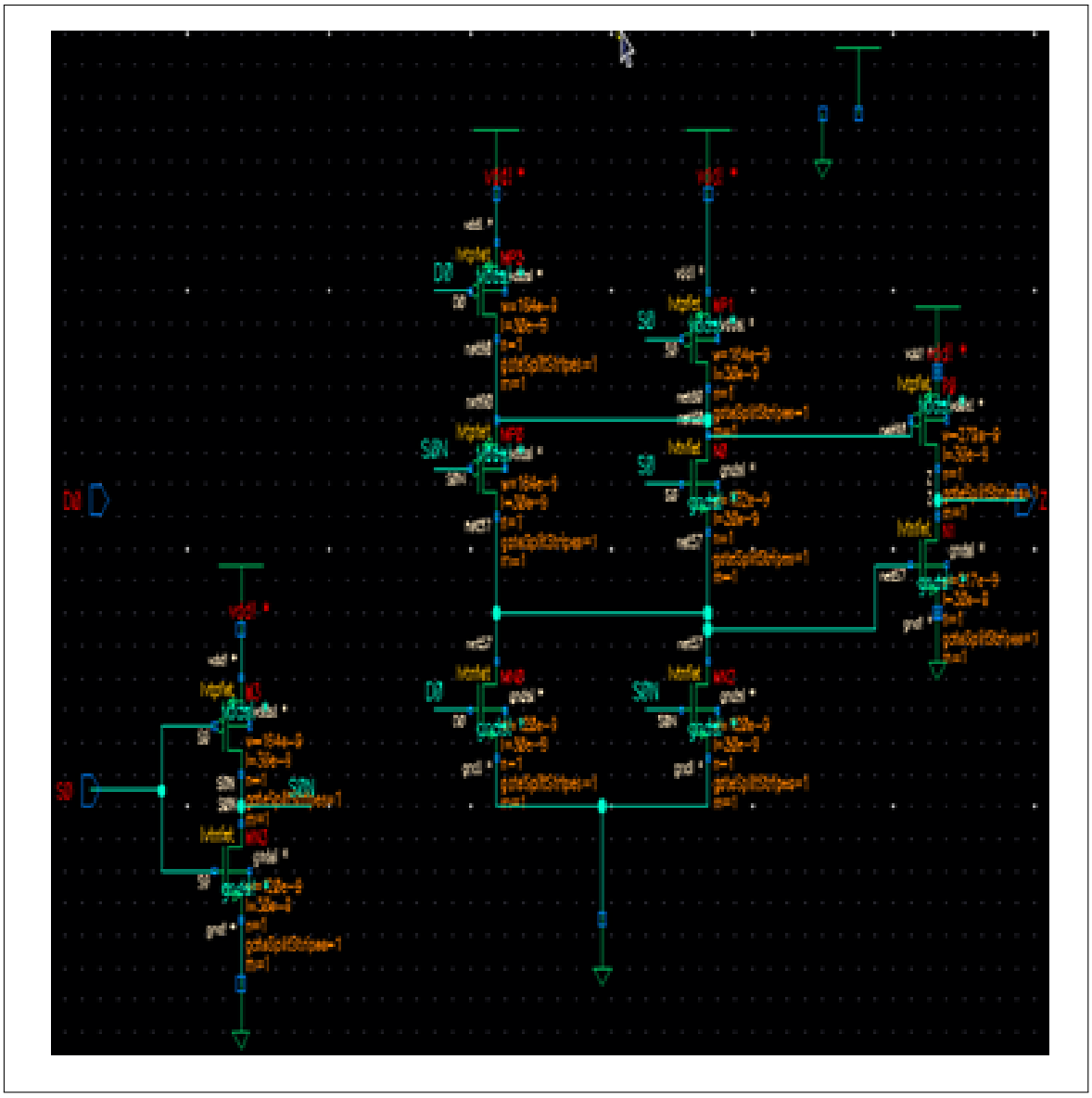

Figure 6.2.2: New mux design

5. Features of the new proposed design are:
    - This design acts like a switch . It has select line S0 for an input D0.
    - If the switch is on ie. S0 is 1, then only OUTPUT is D0 else high impedence
    - Such 8 modules are used to create 8:1 MUX as shown below:

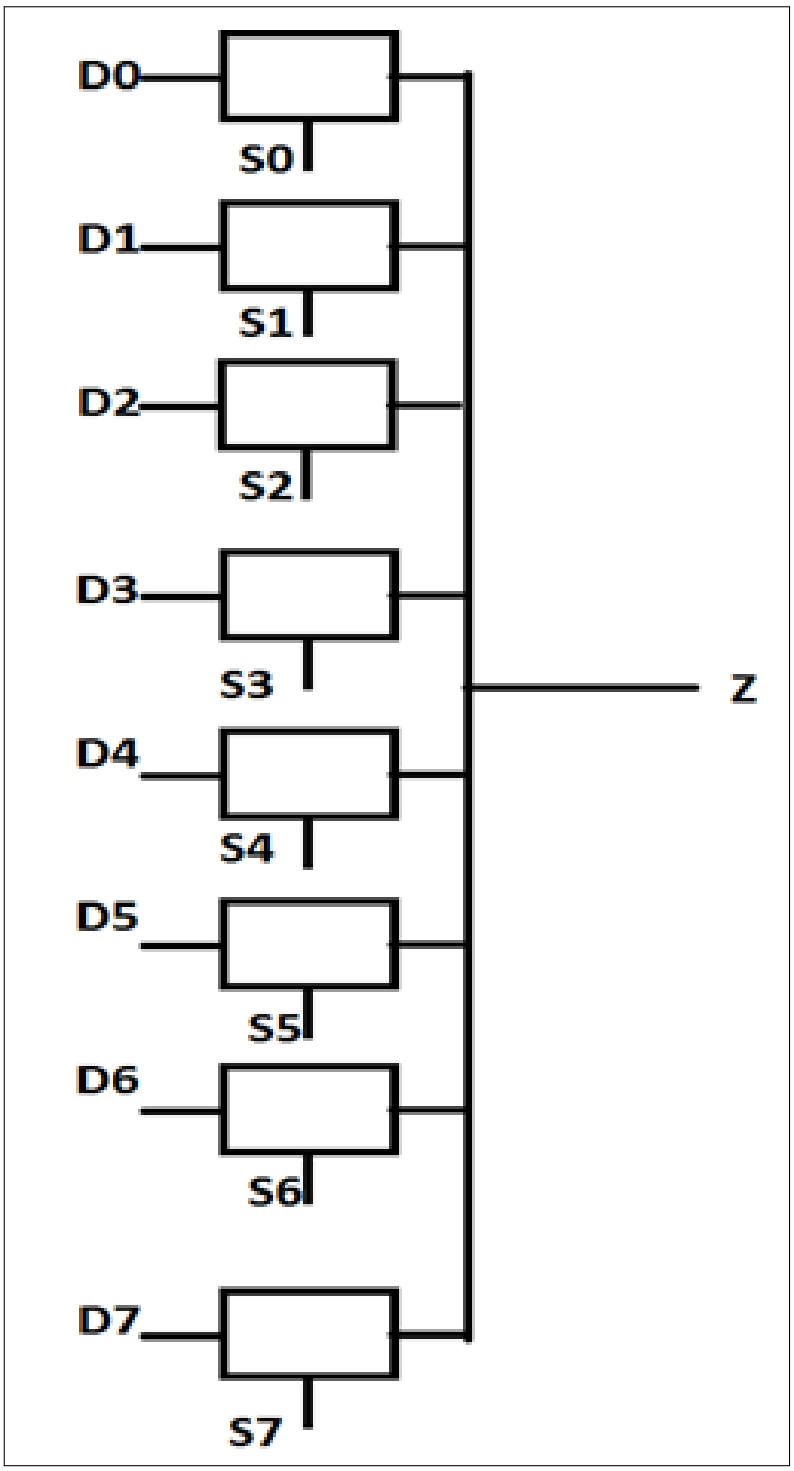

Figure 6.2.3: 8:1 One hot mux

6.2.2 Results

1. The proposed new mux design is faster as it has it has only a single stage per clock input. So delay has been reduced around 20 to 30
2. The new design is has lowest power dissipation. The power dissipation has been reduced by 50
3. There is an area overhead from the conventional multiplexer.

6.3 Measure the hold time of scan d flip flop and find out the transistors which are sensitive to hold time

6.3.1 Introduction

6.3.1.1 Basics

1. What is hold time?

   The time for which the input should be stable after the clock edge so as to get proper output.

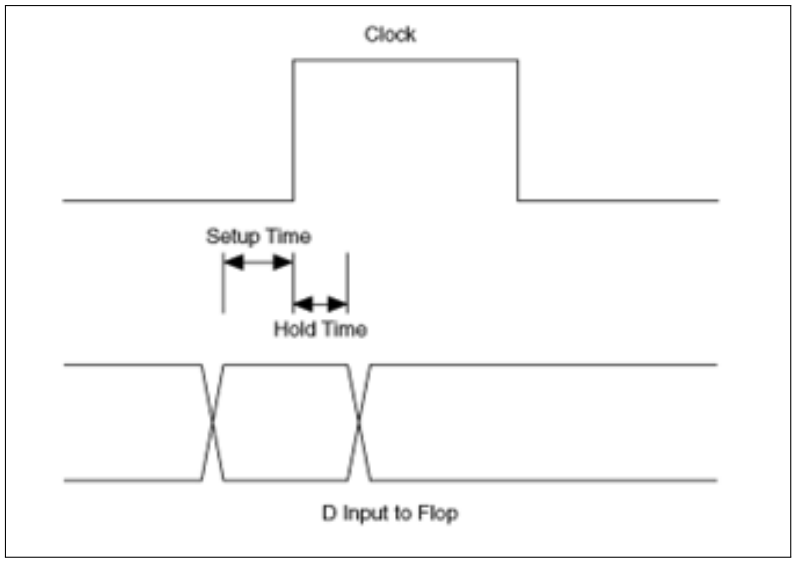

Figure 6.3.1: Hold time for and input

2. How to measure the exact hold time ?

   If we have an input D and a pulse clock as shown as above, and if we try to converge them towards each other and check for hold time violation the time there is hold violation the value just before it will be the minimum hold time.

6.3.1.2 Activity details

The Schematic diagram of the SCAN flip flop used is:

1. Most important point to remember is that hold time violation is highly prone to change in the data after the clock pulse. So we are mainly focusing on the transistors of Scan mux and master latch.
2. In this task we take each transistor and we make it the fast and slow and observe its impact on the hold time . The results of which will show the sensitivity of each transistor on hold time.
3. The transistors are made faster or slower by increasing or decreasing the widths of each transistors. • For example if we make the PMOS of scan mux slower, then the

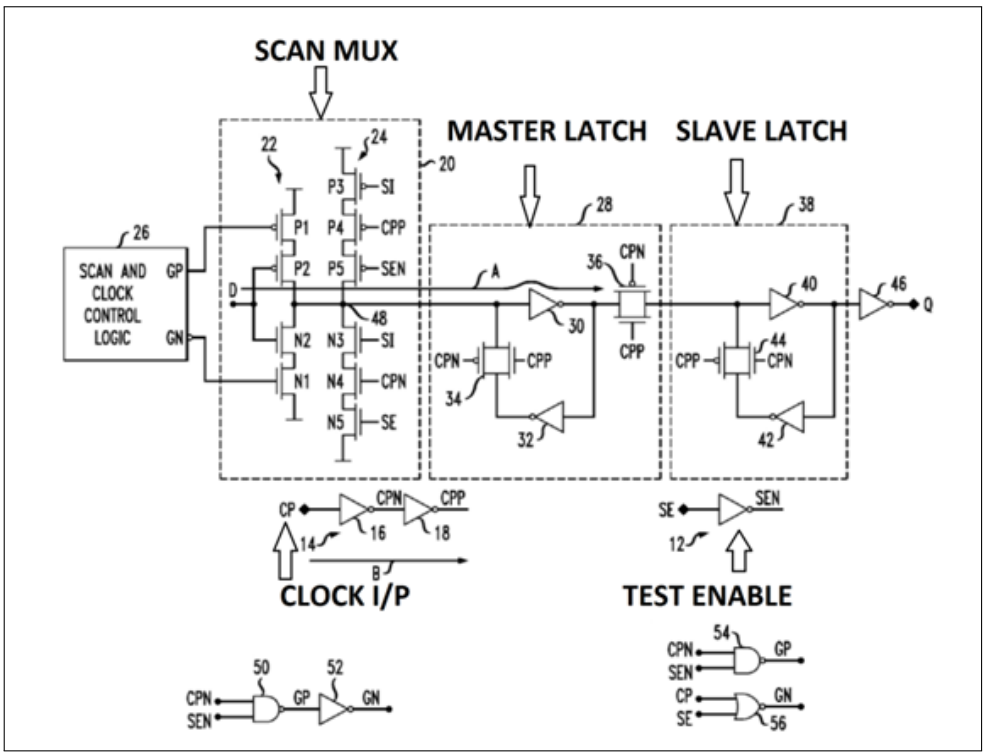

Figure 6.3.2: Scan d flip flop

incoming data will be slower and stable much before the clock pulse so we will get improved hold timings in such cases.

4. Benefits of the task are:
   - We can get the sensitivity of each transistor on the hold time.
   - So if there is a hold time violation then simply increase the delay of data path and it will be greater than the transmission gate so now when the transmission lines try to close to latch the data to output the data will not able to change it.
   - So only these transistors of the result can be changed if there is a hold violation.

6.3.2 Result

1. The hold time is thus computed by varying each and every transistor of Scan D flip flop and we found out that the transistors of the scan D flip flop are the most sensitive.
2. The clock path transistors can be made faster to switch off the transmission gate before the data arrives.

6.4 Delay variability in Ultra Low Voltage Designs

Today, SoC needs are mainly driven by applications such as Internet of Things (IoT), wearable and implantable biomedical devices. Since such devices are typically untethered, they must survive on a battery or on power harvested from their environment. Such devices typically require long lifetimes, further constraining power consumption. Thus key requirements of these applications are to achieve ultralow power and at the same time low cost

6.4.1 Major issues in Ultra Low Voltage designs

It is seen that as we decrease the supply voltage the impact of process variations starts to dominate such that the variability of delays increases beyond tolerance levels. The process variations are the variations which are due to inability of process technology to meet the accuracy required as per the device dimensions or fabrication issues in manufacturing short channel devices .

The process variations are due to three major reasons :

1. Variation of Gate length due to edges (H shapes and L shapes) in Poly gate.

   Standard Cell Layouts will have H shapes or L shapes in layouts as per the requirement of design or to get optimized layouts. The issue arises while fabricating the gate , the edges result into curves and is the reason of variation in gate lengths. If the gate length varies the current will vary which implies the change in delay.

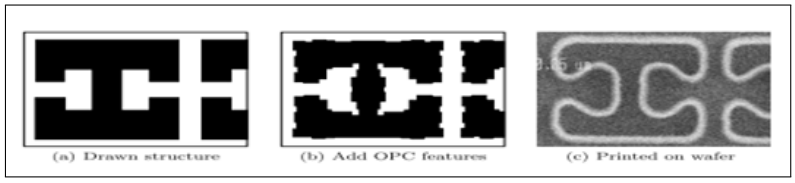

Figure 6.4.1: Lithography effects on Poly edges and OPC corrections

2. Variation of Dopant atoms in channel area

   In long channel devices we have 1000 dopant atoms / unit channel area (approx) but in short channel devices the number of dopant atoms per channel is approximately 10 . The problem here arises when there is variation while doping the channel, if doping varies the threshold voltage will vary which will in turn alter delay . This is the best reason for process variations being a reason for delay variability.

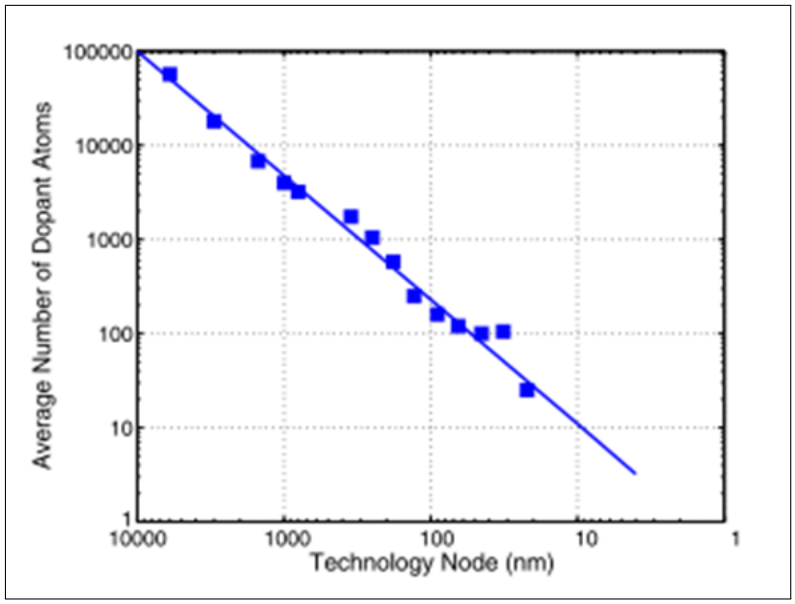

Figure 6.4.2: Doping concentration across various channel lengths

3. Variation in thickness of gate oxide

The thickness of oxide has been reduced to a very huge extent in deep sub micron technology. A slight variation in gate oxide thickness will impact on the gate control over channel. This will impact the variations in delay.

4. Voltage variations

   The impact of drop across the power rail and variation of voltage supply (VDD) changes the delay of a cell. This lead to fluctuations in delay of cells. So various power mesh stratergies are used to cope up with the voltage variations crisis. Also decap cells are used to give full vdd supply.

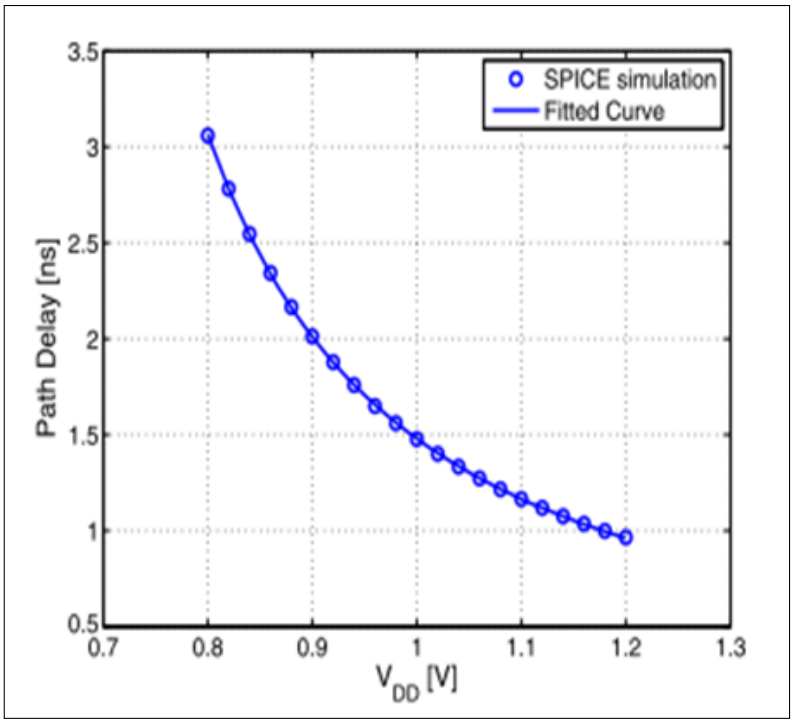

Figure 6.4.3: Voltage variations leads to delay variations

6.4.2 Method to analyze delay variability - Monte Carlo Analysis

As stated above we have listed some reasons which shows how process variations leads to delay variability . To analyze the delay variability for each cell we use Monte Carlo Analysis. This analysis is carried out in steps as shown below :

1. Take the model file which is derived from test chip .This model file consist of data that describes the varying mobility and Vt's across the test chip.
2. Keep the widths of transistors fixed .
3. For each combination of mobility and threshold voltage , evaluate the delay of each cell using Monte Carlo feature of ELDO for 100 iterations.
4. For all 100 delay values take the mean and standard deviation .
5. Check whether mean delay of each cell falls in the range -3sigma to 3sigma , if the mean lies in the range then the cell satisfies the criteria for lower variability else it signifies a larger delay variability.

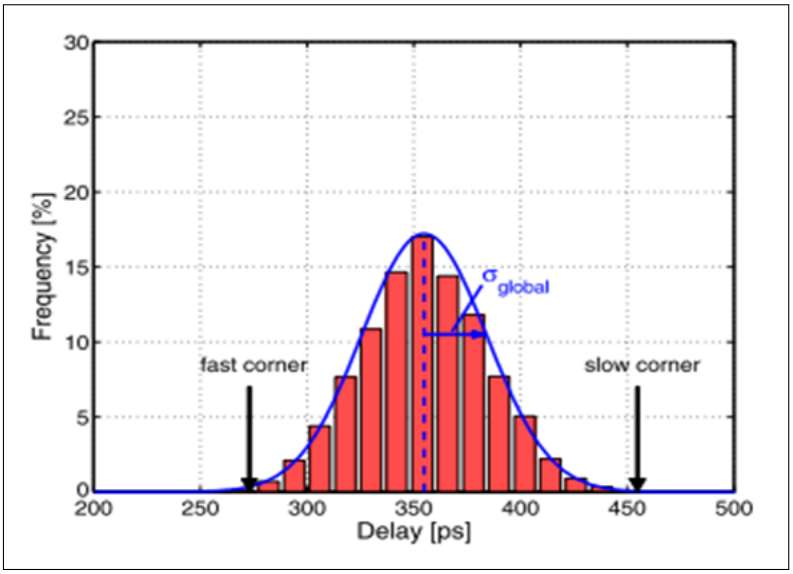

Figure 6.4.4: Monte carlo analysis using Gaussian Curve

6.5 Methods For Increased Routability

6.5.1 Modification of metal pin shapes

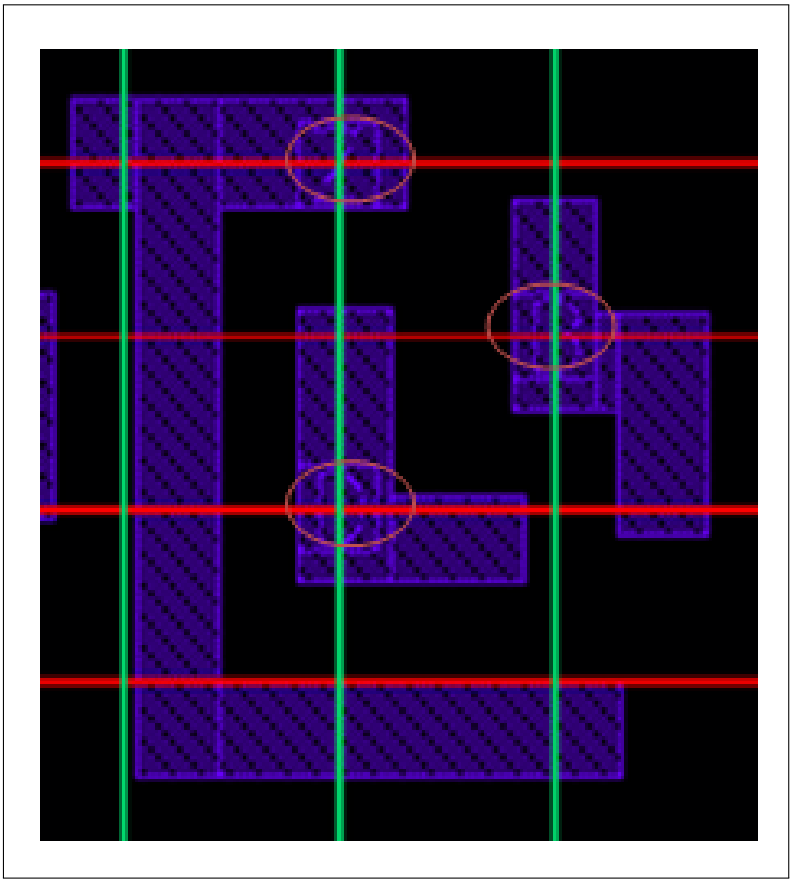

Figure 6.5.1: Initial Metal pin position

As discussed about the routing grids,they are defined for the efficient routing of the pins. To increase the number of routing points or hit points, the shape of the pins can be modified from the existing shapes. While modifying the shapes of the pins care is taken that newly developed layout should clear from DRC violations, LVS cleans and consistency check passed.

The above figure 6.5.1 shows accessibility of the pins B, D and Z with the routing points highlighted on the grid. The two adjacent horizontal routing points of pin Z are not simultaneously accessible. It is because M2 metal is horizontally routed, thus the second hit point is not accessible since it violates minimum via spacing rule.

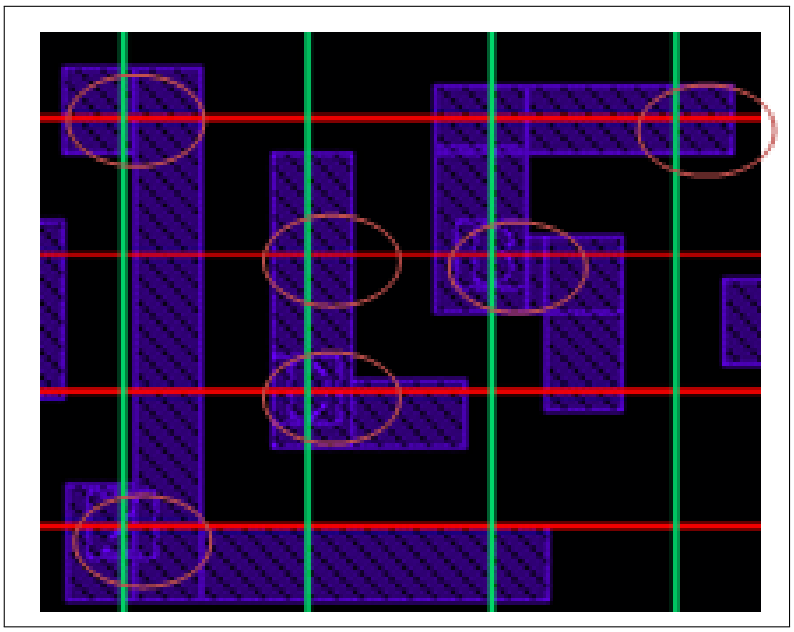

Figure 6.5.2: Modified Metal pin position

In figure 6.5.3 it is seen that Z and B pin shape is modified to U shape to get one access point more. Thus pins have increased routabilty for the signal.

6.5.2 Modification of power rail width and grid offset

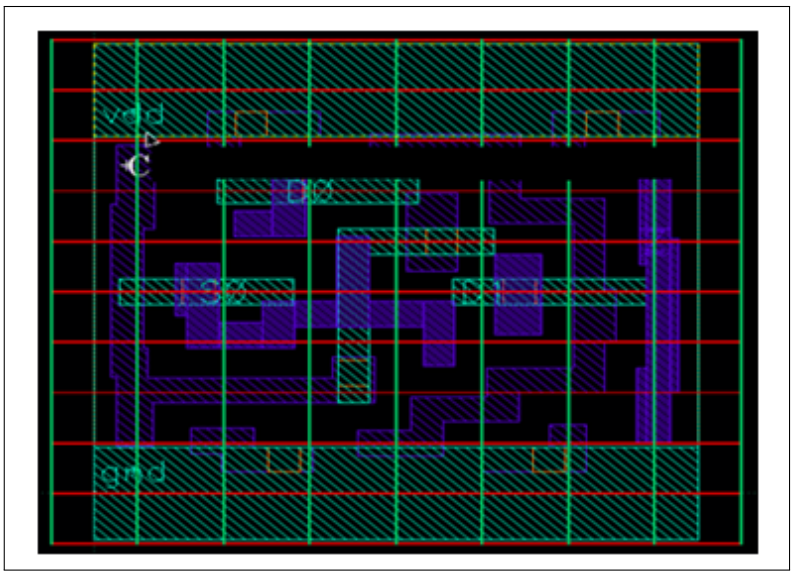

Figure 6.5.3: Initial layout M2 power rail

Generally in standard cell library for 28nm, the power rails are made of M2 metal layer. For increasing the number of routing tracks in the layout, the power rail width is decreased and replaced by M1 metal power rail.

From the fig 6.5.3 the power rails for vdd and gnd highlighted in light blue color has a fixed width and offset from the horizontal routing grid. The pins D0 and S0 have one each hit point on routing grid and that too with M2 metal highlighted in light blue color. Thus routing for the next level metal, we need to use M3 metal for D0 and S0.

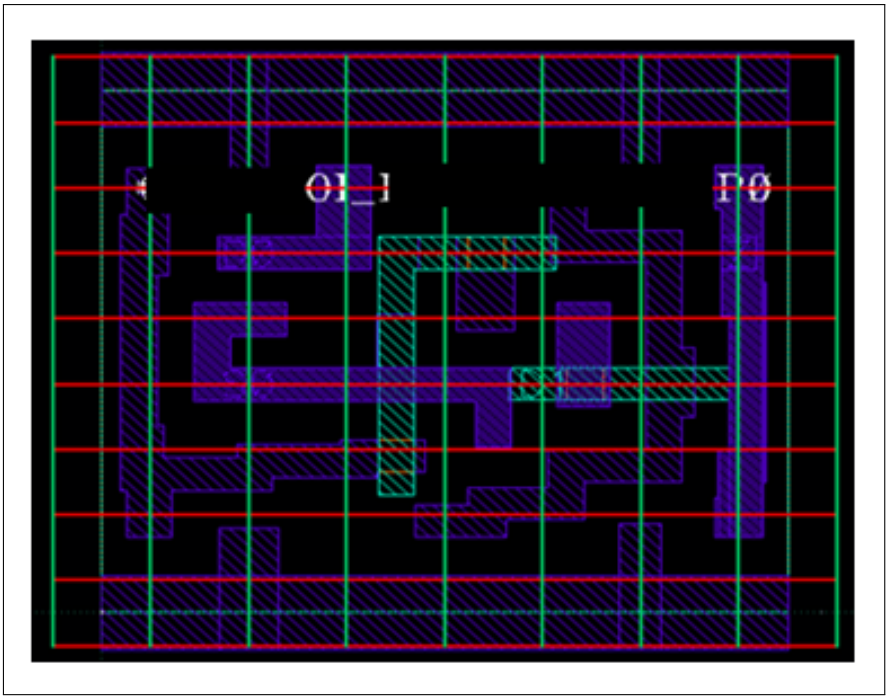

Figure 6.5.4: Modified layout with M1 power rail

The figure 6.5.4 shows the use of M1 metal power rail for vdd and gnd pins. The width of power rail is reduced by 'X' nm and the horizontal offset is changed by 'Y' nm. In initial layout 5 routing tracks were available for the routing of the pins, but in fig 6.4 6 routing tracks are available for routing. Also the pins S0 and D0 are replaced by metal M1 layer. Pin S0 has 3 hit points and D0 has 2 routing points. Thus the routing capability has increases for both pins from the previous version of the layout.

Conclusion

The Standard Cell libraries are designed for the benefit of the user end. They are provided with a wide range of cells with wide range of drive strengths. These libraries are characterized for thousands of PVT's and tested completely. All the above activities performed were to optimize the libraries for power, speed, area. But on the industry level there are three different libraries made for each category speed , area and power. These optimizations can be done on a schematic level for the setup and the hold timings. These libraries are completely designed by keeping the low power design in mind . The new techniques in low power design such as multi vdd etc requires a basic cell called as level shifter .The standard cell libraries include all the basic elements needed for a generic design .

Future Scope

Currently ST Microelectronics is working on FDSOI technology.Apart from the benefits of FDSOI technology , there can also be use of FinFET technology. The complexity in this technology and better control over channel than FDSOI brings in new challenges. The future scope of standard cells is solving design challenges while adapting FinFET as the base technology. The rules to design the layouts will increase and the checks may double.The efforts to increase the yield will surely double.This will surely decide the future of chips , future of VLSI, need of efficient standard cell libraries.

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