POWER AND SIGNAL INTEGRITY OF ASIC DESIGN

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

NISHANT PATHAK

(14MECV23)

Electronics & Communication Engineering Branch
Electrical Engineering Department
Institute of Technology
NIRMA University
Ahmedabad-382 481

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May 2016

Certificate

This is to certify that the Major Project entitled **"POWER AND SIGNAL INTEGRITY OF ASIC DESIGN "** submitted by **NISHANT PATHAK (14MECV23)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in VLSI Design , NIRMA University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this major project, to the best of our knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

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Certificate

This is to certify that the Project entitled "**Power and Signal Integrity of ASIC Design**" submitted by **NISHANT PATHAK(14MECV23)**, towards the submission of the Project for requirements for the degree of Master of Technology in VLSI Design, NIRMA University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

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Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at NIRMA University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- NISHANT PATHAK.

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- NISHANT PATHAK

14MECV23

Abstract

Physical Implementation of any ASIC design is process of converting Register Transfer Logic (RTL) design to routed gate level netlist considering provided constraints and targets for timing closures. Implemented design also has to meet power specifications and Design Rules. After successful implementation of the design, it can be fabricated on the silicon and ICs can be made.

Physical implementation of any design follows a flow which is called physical design flow or RTL to GDS-II flow. This flow divides implementation in small steps like floorplanning, placement, power planning, clock tree building, routing, etc.

Design closure in advanced designs requires a delicate balance of many complex issues. Timing remains critical, but power has become important toward achieving design success. Today, power management is a mainstream design challenge and a key concern for chip designers as it affects packaging decisions, cooling requirements, battery life, design performance, and chip reliability.

Power, timing, and signal integrity (SI) effects are all interdependent at 90- nanometers (nm) and below. To achieve the highest accuracy power analysis, an accurate timing engine is required to perform accurate timing and slew calculations. Since timing parameters affect power dissipation, designers require a solution that takes advantage of these inter dependencies. Due to large power densities, smaller voltage supplies, and higher frequencies, full- chip dynamic and static power integrity is one of the key challenges for designs. Dynamic power and peak voltage drop is difficult to analyze and correct, being a transient phenomenon and its impact on chip timing and yield is a growing concern.

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Chapter 1

Introduction

1.1 Motivation

In semiconductor devices, metal interconnect traces are typically used to make the between various portions of the circuitry to realize the design. As the process technology shrinks, these interconnect traces have been known to affect the performance of a design. Advances in process technology and in design styles are increasing with design node shrinking, the impact of electromigration (EM) and IR- drop effects on the performance and reliability of analog, mixed-signal, RF designs, memory and custom digital IP blocks. Excessive IR drop may result in functional failures and/or timing violations Electromigration mechanisms induces an irreversible failure of electrical discontinuities or short circuits due to ion migration.

1.2 IR Drop

In the latest deep submicron CMOS technologies, the problem of the voltage drop on the integrated circuit supply rails has become significant.The supply voltage has dropped from 5V common with 0.6Âţm technology down to 1.2V at 90nm technology. The power consumption has remained about the same, or is even higher than it used to be, because integrated circuits have more gates and run at higher fre-

quencies. This means, for the same power, that the currents flowing in the power supply are proportionately higher.The power distribution network distributes power and ground voltages from pad locations to all devices in a design. Shrinking device dimensions, faster switching frequencies and increasing power consumption in deep sub-micrometer technologies cause large switching currents to flow in the power and ground networks which degrade performance and reliability. A robust power distribution network is essential to ensure reliable operation of circuits on a chip. Power supply integrity verification is a critical concern in high-performance designs. Due to the resistance of the interconnect constituting the network, there is a voltage drop across the network, commonly referred to as the IR-drop. The package supplies currents to the pads of the power grid either by means of package leads in wire- bond chips or through C4 bump arrays in flip chip technology. Although the resistance of package is quite small, the inductance of package leads is significant which causes a voltage drop at the pad locations due to the time varying current drawn by the devices on die. This voltage drop is referred to as the di/dt-drop. Therefore the voltage seen at the devices is the supply voltage minus the IR-drop and di/dt-drop.

1.3 Electromigration

Electromigration is the gradual displacement of metal atoms occurring when the current density is high enough to cause the drift of metal ions in the direction of the electron flow producing

1. Voids when the outgoing ion flux exceeds the incoming ion flux resulting in an open circuit.

2. Hillocks when the incoming ion flux exceeds the outgoing ion flux resulting in a short circuit.

1.4 Effects

Excessive voltage drops in the power grid reduce switching speeds and noise margins of circuits, and inject noise which might lead to functional failures. High average current densities lead to undesirable wearing out of metal wires due to electromigration (EM).

1.5 Objective

The challenge in the design of a power distribution network is in achieving excellent voltage regulation at the consumption points notwithstanding the wide fluctuations in power demand across the chip, and to build such a network using minimum area of the metal layers. These issues are prominent in high performance chips such as microprocessors, since large amounts of power have to be distributed through a hierarchy of many metal layers. A robust power distribution network is vital in meeting performance guarantees and ensuring reliable operation. The crux of the problem in designing a power grid is that there are many unknowns until the very end of the design cycle. Nevertheless, decisions about the structure, size and layout of the power grid have to be made at very early stages when a large part of the chip design has not even begun. Unfortunately, most commercial tools focus on post-layout verification of the power grid when the entire chip design is complete and detailed information about the parasitic of the power and ground lines and the currents drawn by the transistors are known. Power grid problems revealed at this stage are usually very difficult or expensive to fix, so the preferred methodologies help to design an initial power grid and refine it progressively at various design stages.

Chapter 2

IR Verification Flow

2.1 Introduction

ANSYS RedHawk is an industry-standard sign-off platform for system-aware SoC power, noise and reliability. The power integrity platform enables power noise closure and sign-off for low-power, high-performance SoCs using 28 nm FDSOI and other advanced technologies. Its power integrity solution is a full-chip cell-based power/ground design and verification product with integrated SPICE, addressing static and dynamic power integrity from early in the design flow through verification and sign-off. Its advanced engines and simulation capabilities deliver significantly high capacity and improved turn-around times for full-chip IR voltage drop, power/signal electromigration (EM) It enables RTL-to-GDS power closure, SoC-level IP verification and chip-aware system analysis.

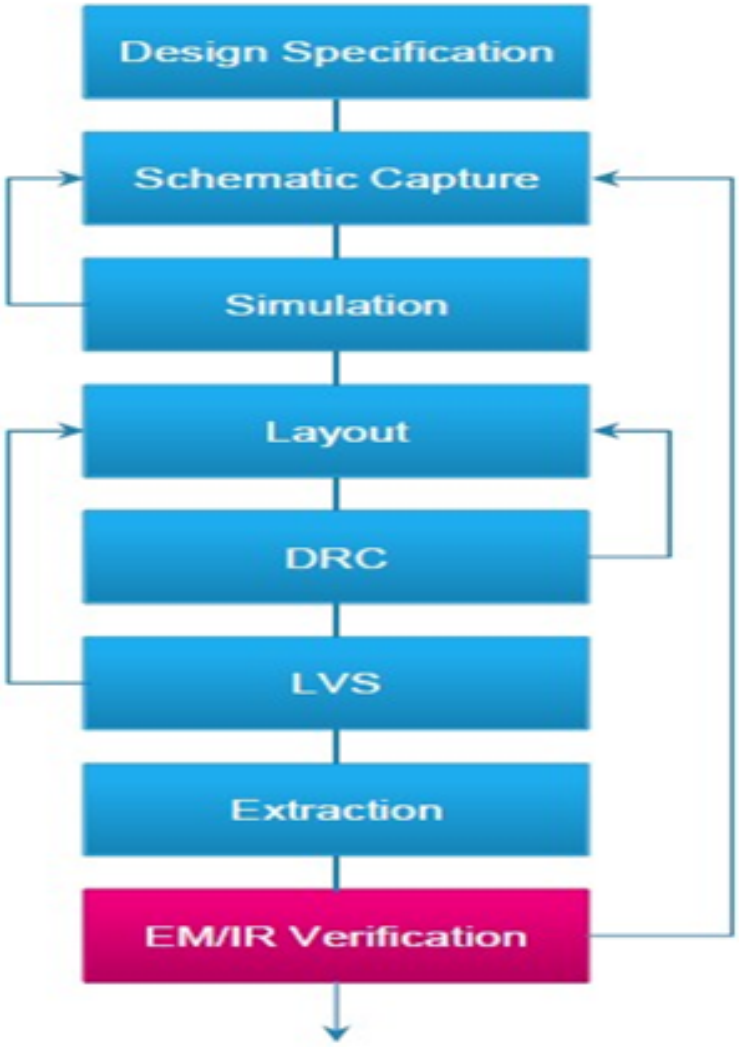

Figure 2.1: EM/IR Verification Flow

2.2 Types of Power Analysis

RedHawk performs several types of power analysis on a circuit:

1. Static (IR) voltage drop with average cycle currents.
2. Dynamic voltage drop with worst-case switching currents.
3. Electromigration analysis.
4. Critical path and clock tree impacts.

Each type of analysis can be run in different ways, depending on the input data available and the desired speed of analysis and accuracy of results. An overview of

the data flow for static IR and dynamic voltage drop analyses is presented in the following sections

2.2.1 Static Voltage Drop Analysis Flow

Figure 2-2 shows the design flow for running the static IR drop solution

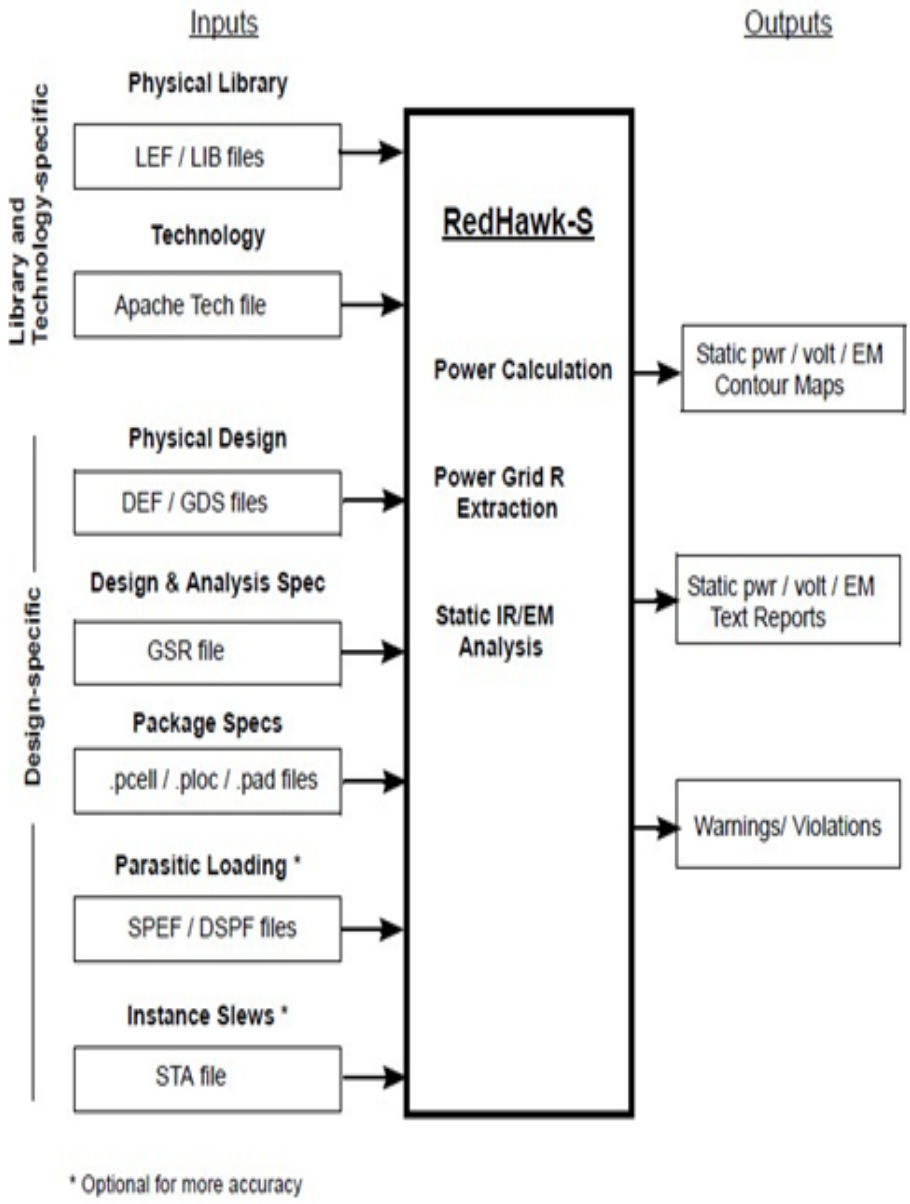

Figure 2.2: Design Flow for Static Analysis

2.2.2 INPUTs

The following are the key steps in the static voltage drop analysis flow:

1. Prepare design data files.

2. Import design data using the automated setup script or the GSR file.

3. Perform power calculation.

4. Perform power grid extraction for R network.

5. Evaluate power/ground grid weakness.

6. Define pad and package constraints.

7. Perform static IR voltage drop and EM analysis.

8. Review static IR/EM summary reports and evaluate what other information is needed from the analysis.

9. Explore solutions to reduce excessive static IR drop with the RedHawk power grid Fixing and Optimization tools.

After importing all design data, the full chip view should be displayed. Continue with the analysis procedure in the following sections:

a. Power calculation:-

Power calculation uses information from a number of design files to evaluate the average cycle power consumption of all cell instances for both flat and hierarchical designs. The calculated power is used for both static and dynamic analysis. Three methods are available for modeling chip activity and setting up power calculation:

1.Mixed-mode, when only some parts of the design have VCD data.

2.Vectorless, when no VCD file is available, and toggle-based state propagation methods are used.

3.Event-propagation, using full chip VCD file data.

An outline of how to select the power calculation method based on the input data available is presented in following figure:

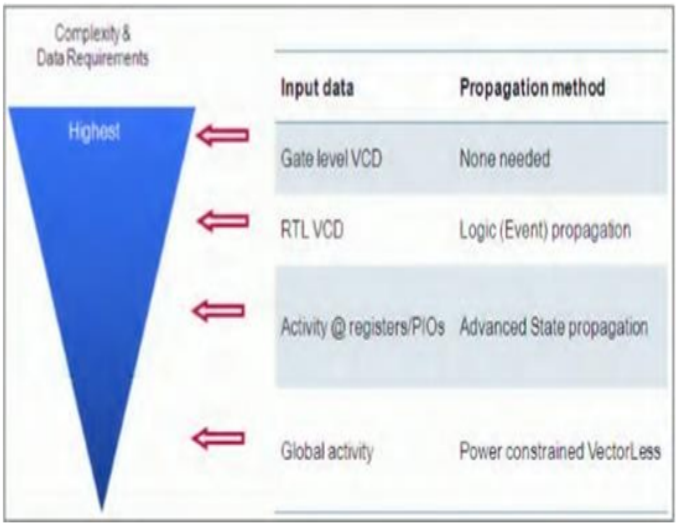

Figure 2.3: Power Calculation Selection Method

The two primary propagation flows are shown in figure:

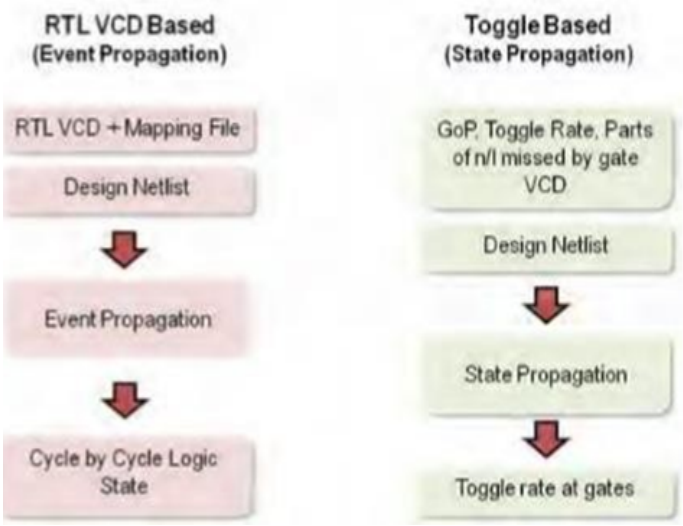

Figure 2.4: Event and State Propagation Flows

i. Setup for Vectorless power calculation

When no VCD file is available, an estimate of the toggle rate should be made, using values from a group of GSR keywords as follows:

- STA FILE

- FREQUENCY

- TOGGLE RATE

ii. Setting up for Event-Driven (VCD File) Power Calculation

If you have a VCD file for the design it is strongly recommended that you perform power calculation based on VCD data. The Value change dump (VCD) file contains information about any value changes on the selected variables. This file can be used for hierarchical monitoring of all signal changes within design modules.

b. Power Grid Resistance Extraction.

After power calculation, the next step is to perform network resistance extraction, using either TCL or GUI commands. At technology nodes now being used for design, very precise estimates of wire resistance, and therefore wire thickness, is necessary. To obtain very accurate resistance values for wire segments, both width and thickness values must be accurately determined. To achieve an accurate estimate of wire thickness, an accurate assessment of the metal density for all metal geometries in the region of the wire is needed, because of the effects of CMP on wire thickness.

c. Power/Ground Grid Weakness

Excessive voltage drop can occur due to weak power/ground grid structures. RedHawk can identify problems in P/G structures early in the design cycle after placement and CTS is completed, even without STA and SPEF files. P/G weakness analysis can report two different measures of grid weakness:

âĂć An estimate of the upper bound on grid resistance for all instances in the design, normalized to the highest instance grid resistance. For grid check, an instance that has a weakly connected Power or Ground network shows up as high impedance in the generated report.

âĂć The calculated effective grid resistance for a specified number of instances in the design.

Analysis based on STATIC IR drop

The following are some important issues that can be identified by the static voltage drop maps:

1. Number and location of hot spots (expected or not).

2. Unexpected color jumps may indicate missing straps or connections.

3. Any unexpected black areas (which could mean a black box element, missing data, a missing logical connection, or a missing physical connection.

4. If a color changes from source to hot spot make sense.

5. Electro-migration (EM) analysis.

6. Power grid weakness due to very high resistance of interconnects.

7. Relative distribution of power throughout the design.

2.2.3 Dynamic Voltage Drop Analysis Flow

Figure 2-3 shows the design flow for running the dynamic voltage drop solution.

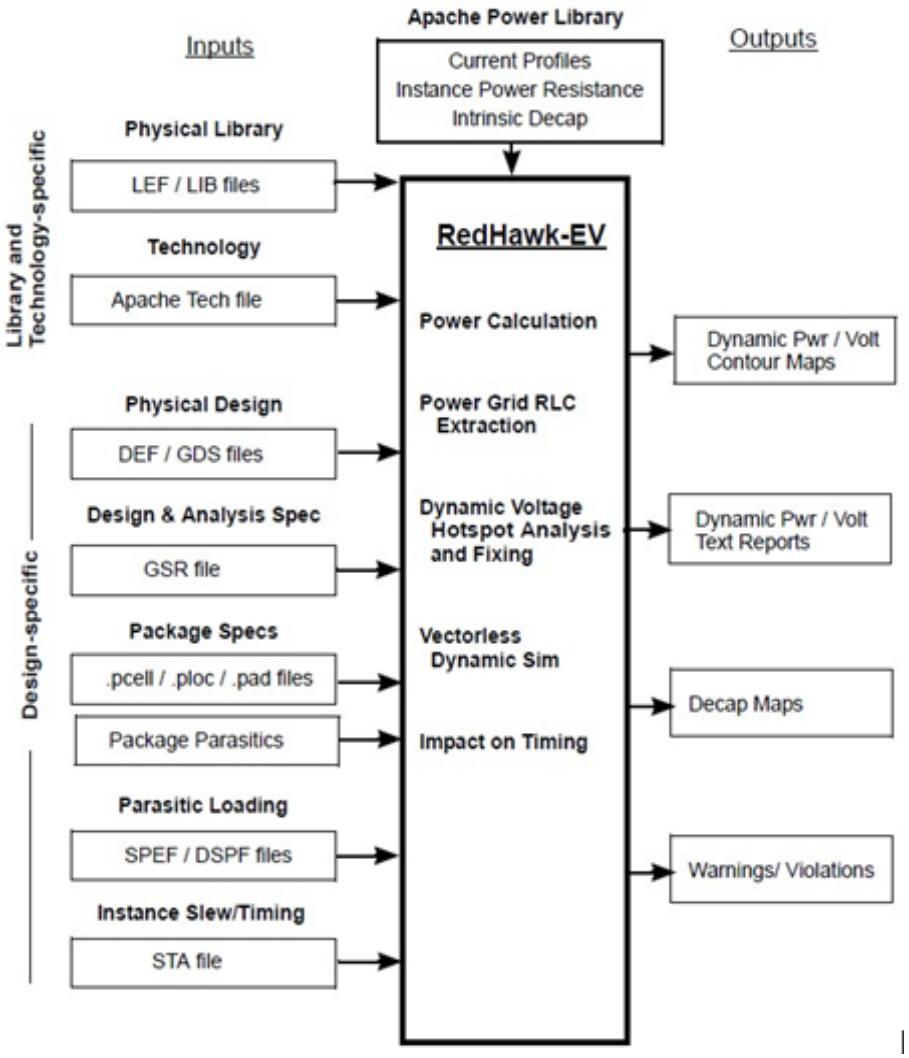

Figure 2.5: Design Flow for Dynamic Analysis

2.2.4 INPUTS

The key required inputs for running dynamic voltage drop analysis are:

1. LEF files for cell library, including standard cells, memories, and I/Os.
2. Flat or hierarchical DEF files.
3. .lib library files.
4. .tech technology file - conductor and via resistance, dielectric thick-

nesses and dielectric constants, EM current density limits.

5. Pad instance, pad cell, or pad location files.

6. Global System Requirements (GSR) file, containing information on toggle rates, frequency, clock roots, default slews, and block power.

7. Timing windows and slews from STA.

8. Extracted parasitics from SPEF or DSPF.

9. Pad, wirebond/bump, or package RLC information.

10. VCD vector file.

11. SPICE subcircuits for all memories, I/Os, and IP blocks (optional).

12. GDSII for memories, I/Os, and IP blocks (optional).

The following sections describe the dynamic voltage drop analysis methodology and procedures:

a. Perform Cell Characterization

To create the dynamic current profiles, effective power resistance, and decoupling capacitance for cells in your design, uses the Apache Power Library tool to perform characterization.

b. Power Calculation

If you have already performed power calculation, for example before performing static analysis, you can import the results or you can follow the procedure of setting up GSR file for power calculation describes for Static IR drop.

c. Network Extraction Perform network RLC extraction using the Dynamic Network Extraction command. Any combination of R, L and

C extraction can be selected, but use all three for best accuracy. If ECO changes have been made to decaps, vias, or pins, extraction must be performed again.

Methods of Dynamic Voltage Drop Analysis

There are several methods of vectorless and VCD-driven dynamic voltage drop analysis available. The chosen method of performing dynamic voltage drop analysis depends primarily on whether a VCD file is available, and if so, the quality of the VCD information. The goal is to use the best switching information available to construct a realistic switching scenario with the information available. Available methods for performing dynamic analysis are summarized in the Figure diagram following

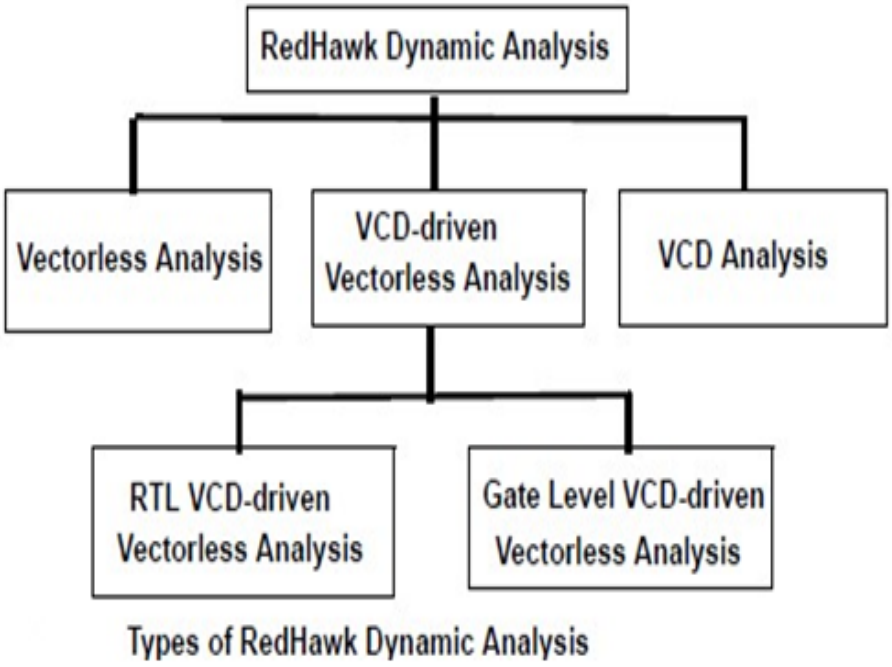

Figure 2.6: Types of Redhawk Dynamic Analysis

a. Characteristics of vectorless dynamic analysis

i. No VCD file available for design.

ii. Covers realistic worst case switching scenario.

iii. Uses GSR keywords and the timing file to define realistic toggle rate and switching times.

iv. Switching scenario is derived statistically and depends on several design-aware factors, such as:

- Areas with structural weaknesses.

- Instance timing windows.

- Logic/power/toggle rate of instances.

b. Characteristics of VCD-driven vectorless dynamic analysis.

i. VCD file is available, but may not represent the worst case.

ii. Helps drive vectorless switching scenario creation.

Two types of VCD files are available.

- RTL VCD

i. Available in early design stages.

ii. Requires mapping RTL names to DEF. Instance level name mapping, in addition to instance/pin and net level mapping, also can be performed.

iii. Switching activity at state points (PIs, FF, latches) is propagated through the logic using the state propagation algorithm.

iv. Clock gating is inherently supported in this flow.

v. For missing VCD coverage, a constraint file can be used to assign

toggle rates, in addition to available RTL VCD, to improve switching activity. vi. Realistic toggle rate distribution, which drives vectorless switching scenario creation.

- Gate-level VCD

i. Gate level VCD can be directly mapped to the design.

ii. Peak power cycle is identified by scanning through the entire VCD.

iii. Toggle rates are derived from VCD for all nets and used to guide vectorless witching scenario creation.

c. Characteristics of Event-driven VCD dynamic analysis.

i. Gate-level VCD with timing back annotation is used for a pure VCD analysis.

ii. VCD used for representing worst case and for measurement/correlation purposes.

iii. Peak power cycle(s) are identified by scanning through entire VCD.

iv. Specific cycle analysis with switching events and delays are derived from VCD.

Designs with gate level VCD files have a complete set of vectors available for accurate power analysis at the instance level.

Analysis of Dynamic IR drop

Gate level timing-annotated VCD with scan activity is usually available very late in design cycle. Therefore, evaluating potential scan clock network problems early in design by using this scan methodology, in which the scenario files are generated from constraint file specifications it can avoid many cases of chip failure and yield reduction.

i. This analysis renders the most accurate results for IR drop.

ii. Actual data of high power density area or nets is obtained.

iii.Nets or area which has value beyond the threshold value is also obtained.

iv. Absolute power distribution of power throughout the design.

v. Dynamic voltage drop color maps and power density color maps.

vi. Capacitance maps, including decap effects.

Chapter 3

Methodology

3.1 GSR File

The Global System Requirements (GSR) file contains the input design file specifications, operating conditions for chip for power calculation, static IR drop and EM analysis, and dynamic voltage drop analysis.

Keywords defined in GSR File for IPs

a. TECH FILE

Required to specify the RedHawk technology file (*.tech) to be used in the design.

Syntax: TECHFILE techFilePathName.tech

b. IGNORE LEF DEF MISMATCH

Defines the DEF import operation. When set to 0, the DEF import operation stops when a pin instance name in the NETS section of a DEF file is not defined for the corresponding cell in the LEF file.

Syntax: IGNORE LEF DEF MISMATCH [0 | 1]

c. LEF FILES

Required to specify the physical Library Exchange Files (*.lef) to be used in the design. Note that LEF files should be imported directly using this keyword.

Syntax:

LEF FILES

lef FilePathName-1.lef

...

File PathName-n.lef

where lefFilePathName-1.lef : specifies the path and name of the LEF file; the first .lef file should contain the technology information.

d. DEF FILES

Required keyword that specifies the Database Exchange Files (*.def) to be used for the design. The last file listed must be the âĂIJtopâĂİ file for the design.

Syntax:

DEF FILES

def FilePathName-1 .def block

...

def FilePathName-n .def top

Where $\text{def}_{F}ilePathName-1.def : specifiesthepathandfilenameforablock; thelast.d$
$levelDEFfile.$

e. LIB FILES

Required to specify library files (*.lib) or custom lib files to be used in the design. If a directory is specified, all files in the directory are selected.
Syntax:
LIBFILES
[lib filename | lib file dir] CUSTOM
...
Where lib filename: specifies library filename lib
file dir: specifies library directory
CUSTOM: specifies a custom library file. Only one may be specified. For example, this allows including or excluding particular states from power calculation using a custom LIB file. You can do this for a particular cell, or if one or more cells is not specified, it applies globally for all cells.

f. APL FILES

APL FILES can be used to specify multiple APL input files and directories at a time. The files are listed in a block in which the first column specifies a filename or directory and the second column specifies what type of file it is, such as current, device capacitance, pwcap, or avm.
Syntax:

APL FILES

inputfile [current | cdev | pwcap | avm | current avm | cap avm]

...

input dir [current | cdev | pwcap]

...

g. ENABLE ATE

The Apache Timing Engine (ATE) is integrated into RedHawk. Using DEF/LIB/SPEF files specified in the GSR, it obtains C1-R-C2 data via the STA file. If this keyword is set to 1, RedHawk launches ATE to generate signal load information, ignores the specified SPEF file. RedHawk loads ATE results at the stage at which it would normally load SPEF files, optionally, if you also specify SDC files using ATE CONSTRAINT FILES, the ATE-generated STA file is used for both C1-R-C2 and STA purposes.

Syntax:

ENABLE ATE [0 | 1]

h. ATE CONSTRAINT FILE

When this keyword is used and ENABLE$_ATEisset, ATEgeneratestheSTAfileduring$
$usesthisC1-R-C2information.$

Syntax:

ATE CONSTRAINT FILES

SDC file1

SDC file2

i. STA FILE

the keyword is defined, the power for each net is calculated from the transition times (âĂIJslewâĂİ) of each instanceâĂŹs input/output pins, using the clock frequency domain for all the instances that are specified in the STA output file.

Syntax:

STA FILE

top level block name sta output file

j. CELL RC FILE

Defines the SPEF/DSPF interconnect parasitics file for each cell in a flat or hierarchical design. When the EXTRACT RC option is set to 1 (default), RedHawk builds a c1-r-c2 equivalent circuit for each instance output RC network specified in the SPEF file. When set to 0, RedHawk uses the total output C for each instance output instead. For static IR-drop analysis, set EXTRACT RC to 0.

Note that you should specify at least one of the following keywords:

CELL RC FILE, INTERCONNECT GATE CAP RATIO, or STEINER TREE CAP. If all three keywords are specified, then the CELL$_R C_F ILEvalueisusedfort$

k. TEMPERATURE

Specifies operating temp for current profile generation.

l. VDD NETS

The syntax of the power net mapping section, using the VDD NETS keyword, is shown below:
VDD NETS

m. GND NETS

To define the ground net mapping section, use the GND NETS keyword, which has the following syntax:
GND NETS

n. PARA CALC POWER

When set, performs power calculation and extraction in parallel, which improves performance.
Syntax: PARA CALC POWER [0 | 1]

o. FREQUENCY

Defines the dominant operating frequency on the chip, or the lowest frequency that includes a majority of the power consumption on the chip.

Also this keyword provides a frequency for Cycle Selection when all instances in the design have zero frequency defined in the STA file. For a design in which several frequencies consume significant power, the frequency to be specified is the frequency at which less than 10 percent of the chip power is consumed at lower frequencies
Syntax:
FREQUENCY (value in hertz)

p. TOGGLE RATE

Defines the default signal toggle rate of the nets on the chip that are not otherwise specified. The rate is the product of the probability that the nets will toggle times the actual clock toggle rate. Toggle rate is defined as the sum of the state changes from 0 to 1 and 1 to 0 within a clock cycle with respect to the net's clock domain. For example, a clock net generally has a toggle rate of 2.0 with respect to its clock domain, since the net switches once from 0 to 1 and once 1 to 0 within a clock cycle.

q. DYNAMIC SIMULATION TIME

Dynamic simulation uses the specified start and end times. For backward compatibility, if only one number is specified, that number is interpreted as the end time, and the assumed start time is t=0.

Syntax:

DYNAMIC SIMULATION TIME (start time sec) (end time sec)

r. ADD PLOC FROM TOP DEF

If set to 1, the PINS section in the top level DEF is used as the power and ground pad locations, provided that power and ground pin geometries in the PINS section are well-defined with physical shapes for connection to top level. You can also select a single metal layer from which the plocs are created. This option is most useful in block level analysis, where block level pins are defined in DEF. If no metal layers are specified, plocs from all metal layers are created.

Syntax:

ADD PLOC FROM TOP DEF [0|1]

s. POWER MODE APL

Specifies the primary data source for internal/ switching power and leakage power calculation analysis.

Syntax:

POWER MODE [APL | LIB | MIXED | APL PEAK | APL PEAK1]

where.

APL: specifies primary use of APL power data for internal/switching and

leakage power. Where APL data are not available, .lib data are used.
LIB: specifies use of .lib power consumption data; cells without power data in .lib do not have internal power consumption data, but have switching power information from RedHawk.
MIXED: specifies primary use of .lib power data; for cells without power components (internal power consumption or leakage power) in .lib, APL data are used.
APL PEAK: uses the peak charge from APL in power calculation for every cell in the design, and the current is derived from the charge.
APL PEAK1: uses the APL peak current values for every cell in the in power calculation. Power for each instance is computed as Power = (peak current) *(supply voltage)*(toggle rate). Using peak current leads to a higher power value if a more conservative model is desired.

t. VCD FILE

The VCD FILE keyword reads in original VCD files directly for power calculation purposes. Note that instance switching specified in the GSC file overrides the VCD file.
Syntax:
VCD FILE
top block name (VCD filepath)
FILE TYPE [VCD | FSDB | RTL VCD | RTL FSDB]

DUMP SAIF FILE (filename)

VCD DRIVEN [0|1]

FRONT PATH (string)

SUBSTITUTE PATH (string)

SELECT RANGE (start time) (end time)

SELECT TYPE [WORST POWER CYCLE | WORST DPDT CYCLE]

START TIME (start)

END TIME (end)

TIME [0|1]

where

- Top block name: Specifies name of top block.

- VCD file path: Specifies path to VCD file.

- FILE TYPE [VCD | FSDB | RTL VCD | RTL FSDB]: Selects file type (default: VCD)

- DUMP SAIF FILE: Creates a specified SAIF file reflecting activities at all nets in the design, after Event Propagation. The SAIF file not only includes the instances covered in VCD/FSDB, but also includes the instances that are propagated.

- VCD DRIVEN: Turns VCD-driven state propagation based power calculation on and off. Default is off.

- FRONT PATH (redundant path string): Specifies the string describing the VCD file hierarchical path of the instance. This string is then re-

placed by the SUBSTITUTE PATH string in order to match the path of the instance in the DEF.

- SUBSTITUTE PATH (substitute path string): Specifies the string describing the DEF file hierarchical path of the instance. This is used internally to substitute the VCD path (specified by FRONT PATH) with the DEF path in order for RedHawk to properly identify the equivalent instances and nets in the VCD and DEF.

- SELECT RANGE: Specifies the start time and end time for performing automatic critical cycle selection during power calculation. If START TIME and END TIME values are set to -1, the full VCD period is included in cycle selection.

- SELECT TYPE: Default value WORST POWER CYCLE ranks cycles based on highest cycle power. Set to WORST DPDT CYCLE invokes DPDT (delta power/delta time) ranking of cycle selection, since large cycle-to-cycle changes in power level (high DPDT) may cause very high di/dt values, leading to large dynamic voltage drops.

- START TIME (time): Specifies VCD or FSDB file start time for power calculation. If both START TIME and SELECT RANGE are specified, SELECT RANGE is ignored, so cycle selection is skipped. Default start time = 0. If the specified START TIME is within the dump-off range (where activity is not considered), the START TIME is automatically reset to the start of the next dump-on time.

- END TIME (time): Specifies VCD or FSDB file end time for VCD-driven state propagation-based power calculation. For other flows, END TIME is ignored, and it is determined by START TIME + DYNAMIC SIMULATION TIME. Default end time is the end of the VCD/FSDB file.

- TRUE TIME: If set to 0, uses STA timing data and assumes no glitches; if set to 1, uses VCD switching and timing data; default = 0.

Chapter 4

Crosstalk Aware Static Timing Analysis

4.1 Introduction

Signals crosstalk due to coupling capacitances between adjacent interconnect lines is going to heavily affect the timing behaviour of the 0.18um (and below) CMOS digital designs. The design timing verification step has been addressed by enhancing the traditional STA approach in order to consider the delay shift (speed-up / slow-down) and the arrival times of aggressors/ victim signals.

In the todayâĂŹs high speed digital designs, the crosstalk effetcs due to the coupling capacitance between interconnection lines has become one of the main performance limiting factors. Infact, as the geometry of transistors and interconnects becomes smaller, the coupling capacitance tends

to be more of the 80 percent of the total wire capacitance. The interaction between signals on adjacent lines may cause both noise injection and signal timing deviation.

4.2 Methodology Description

The crosstalk effects impair the traditional STA approach, because it does not account for a relevant portion of the timing behaviour. Either the speed-up or the slow-down of the signals may cause a timing constraint violation, therefore a circuit failure.

The crosstalk timing effects depend on the dynamic characteristics of the signals, like the relative arrival times (signals overlap), phase and transition time, but the signal arrival times are themselves dependent on the delays in the fan-in cone.

Because of the dynamic nature of the effect, this cannot be addressed by a capacitance multiplying factor. Moreover, the main concern of a high performance design flow, is to avoid overlay pessimistic estimations, that may result from very conservative assumptions like the doubling-the-coupling approach and/or assuming that every signal may occur at any time.

4.3 Approach

Based on the considerations above, the verification approach is based on the following main 3 tasks:

TASK 1 Design setup and coupling capacitance filtering. Besides the usual setup of the clocks and the timing constraints, the user will possibly specify a set of thresholds that enable to filter the coupling capacitances during the loading of the SPEF files. Moreover, the designer may specify the set of nets that are not switching during the typical operation of the circuit (i.e. scan-chain, reset).

TASK 2 Full-chip xtalk analysis, assuming infinite arrival windows. Assuming that any signal may switch at any time, a fast yet conservative estimation is performed, for both worst- case speed-up and worst-case slow-down. Note that this step of the analysis may conclude the STA process, if no violations are detected.

TASK 3 Detailed analysis, accounting for the arrival windows computed at the previous step. This step is suitable to give a more accurate (less pessimistic) estimation of the delay values, by accounting for both arrival times and signals correlations. Although this is computationally more expensive, it is applied only to the subset of the nets that are relevant to the determination of the constraint violations, identified on the previous

step. By iteratively re-computing the delays, the min/max arrival windows will progressively shrink and the level of pessimism will reduce.

4.4 PrimeTime-SI implementation details

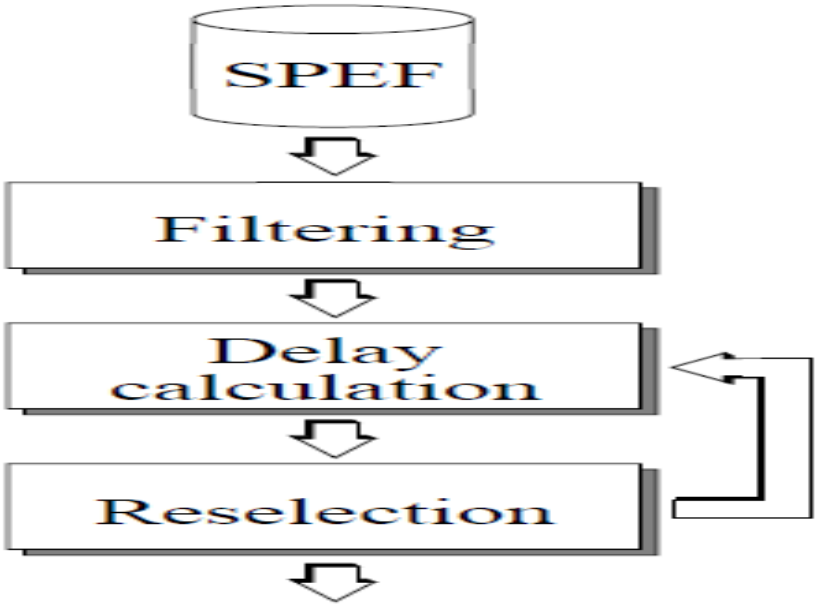

Figure 4.1: Crosstalk Flow

The PrimeTime-SI analysis consists in the following flow, as shown in Fig 1.

1. Filtering

During the SPEF reading phase, a coupling capacitance filtering process is performed (see TASK 1 above) . When a capacitance is filtered, it is splitted and connected to ground with a multiplier factor of one. The filtering mechanism is based on thresholds that can be modified by the

user. Several filtering criteria are available, based on the value of a single coupling capacitance, total net coupling capacitance and so on. A further filtering phase is performed when a âĂŸupdate-timingâĂŹ command is called. While the previous one is based just on the value of the coupling capacitances, this filtering mechanism takes into account the driver strength. For a given victim net, a potential aggressor net is considered effective if the amplitude of the peak injected on the victim net, evaluated with the modified VMS model and normalized to the power supply value, is greater than an user defined threshold.

2. Delay calculation The first time, called "phase 0" or "infinite window phase", the design is timed by using an Arnoldi based engine as delay calculator for all the design nets and the ECMF model to estimate the crosstalk extra-delay on the coupled nets. The evaluated crosstalk extra-slopes are propagated too. The ECMF model requires as an input the Thevenin representation of both victim and aggressors driving cells: they are computed during the effective capacitance iteration step, which is performed during the timing analysis.

3. Reselection

At this level, a set of nets that may need a further analysis is identified. A set of selection criteria is available to the user. For example, the user may specify that only the nets which lie on the top critical path (of each timing group), and the nets that are coupled with them, will be selected for the detailed phase. Furthermore, since the crosstalk analysis is an it-

erative refinement process, a set of exit criteria are provided to the user, in order to guarantee the iteration scheme convergence. The iterative loop will end either because one of the above mentioned criteria is met or because no more nets are reselected. The successive delays calculation will be performed by using the Arnoldi based engine both for calculation and for crosstalk extra- delay estimation. Moreover, the timing arrival window information will be taken into account, allowing to dramatically reduce the level of pessimism

4. Implementation Method

The only pre-requisite to run the PrimeTime- SI analysis, is that the SPEF file includes the net-to net coupling capacitances.
A typical script to run the crosstalk analysis looks like the one shown In order to activate the crosstalk analysis features, the variable: rc-activate-capacitive-crosstalk has to be set to âĂIJtrueâĂİ. The crosstalk analysis will begin when the update-timing, check-timing or report-timing commands are issued. A new option of the read- parasitics command (-keep-capacitive-coupling) has been added in order to load the coupling capacitances (by default, the coupling capacitances are splitted and lumped to ground).
As mentioned above, the user may have direct control over the number of cross-coupled capacitors to analyze, by filtering from the analysis the

capacitors that are small in value, therefore improving run time with negligible loss of accuracy. Moreover, a further filtering, based on the amplitude on the peak injected on the victim net, may be specified throughout the variable: rc-cc-vms-ratio-threshold. The user may control the subset of nets that will be reselected for the next iteration by specifying the value of threshold variables. For example, to reselect the nets belonging to the critical path, the following variable: xtalk-critical-path-reselection has to be set to âĂIJtrueâĂİ. Other variables may be specified by the user in order to exit from the iteration refinement process. After the analysis, the results regarding the crosstalk effects on timing are provided directly by using the report timing command with the following new option: -crosstalk-delta.

Moreover, a new set of attributes related the crosstalk info has been introduced in PrimeTime-SI. For example, the voltage peak amplitude ofthe noise bump injected by each effective aggressor on a victim net: victim can be obtained with the command: get-attribute -class net victim rc-xtalk$_b$*umps*

set rc-activate-capacitive-crosstalk TRUE

read-db ./ref-test.db

current-design ref-test

link

read-parasitics -keep-capacitive-coupling SPEF.spf

report-timing -input -crosstalk-delta

create-clock -period 10.0 clock

5. Performance

The new features introduced in PrimeTime-SI have been tested on two designs, D1 and D2. The first one is a 0.18m CMOS small block, while the second one is a 2.7 million gates design, based on a 0.25m CMOS technology. Regarding D2, the crosstalk analysis has been performed only on the top-level interconnects (about 11.000 nets over the about 1 million total nets). For both the designs, all the filtering variables have been set to 0, in order to load all the coupling capacitances. Regarding the reselection criteria, just the nets belonging to the critical paths have been reselected for the next phase. The results of the crosstalk aware timing analysis are summarized in Table 1.

By performing the same analysis without accounting for the crosstalk effects, the update timing phase would take 8âĂŹ and 44âĂŹ for the design D1 and D2 respectively. Note that the performances are heavily dependent on the filtering thresholds (not exploited in these experiments). The setting of the filtering variables is tightly related to the particular technology and even to the design style. A preliminary analysis of the impact of the filtering step is strongly recommended in order to identify the optimal trade-off between performance and accuracy.

Chapter 5

Results

5.1 Color Maps

Thermal Sensor (90nm)

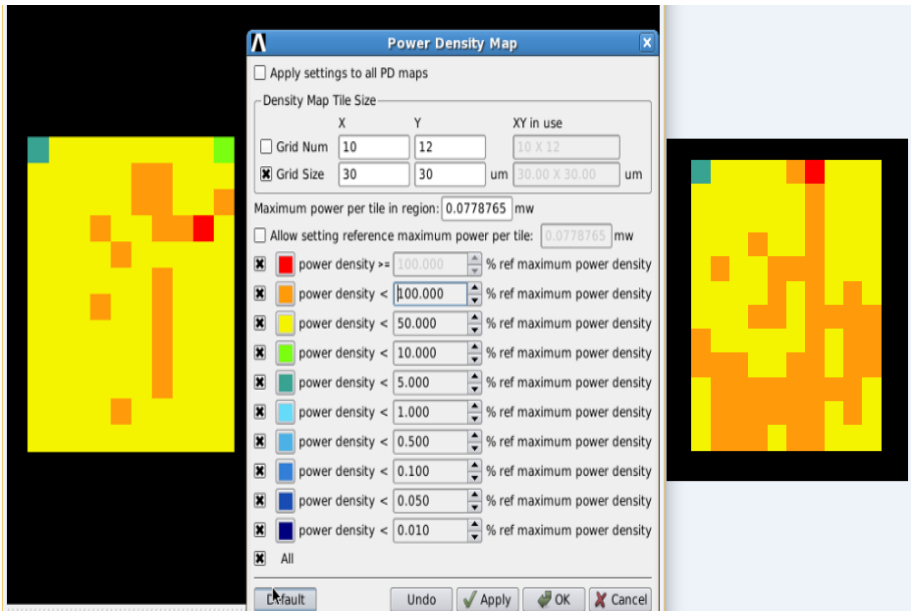

Figure 5.1: Static vs Dynamic Power Density Map

Thermal Sensor IR Drop Map (28nm)

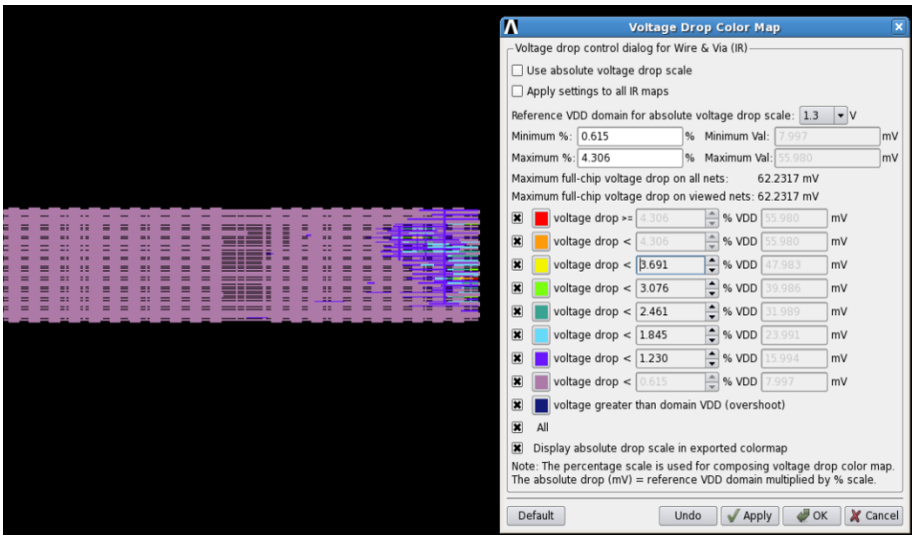

Figure 5.2: IR Drop Dynamic Analysis Color Map

Thermal Sensor Power Density Map (28nm)

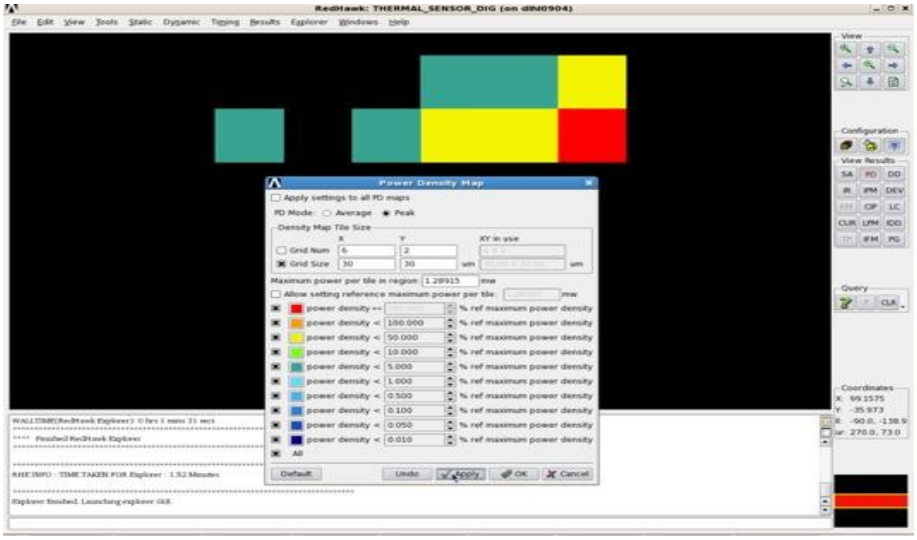

Figure 5.3: Power density Map

Thermal Sensor VCD Switching (28nm)

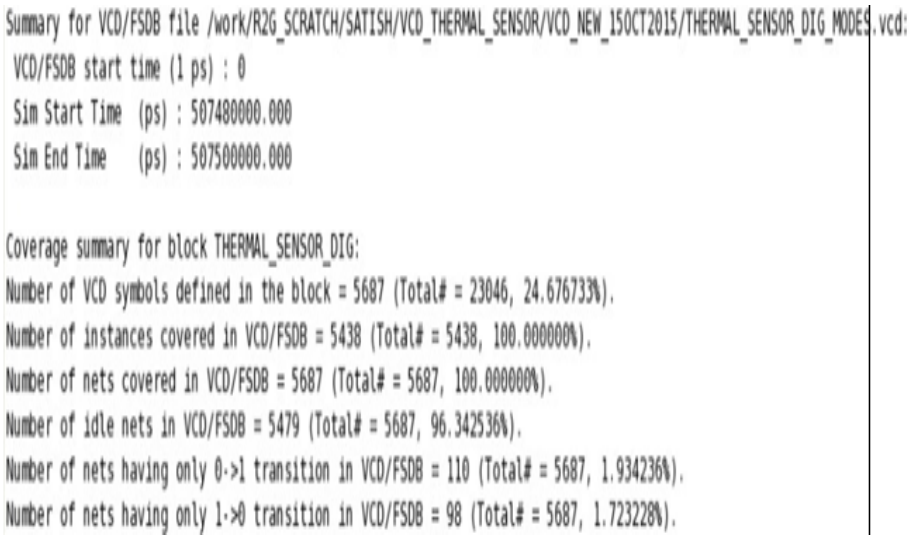

Figure 5.4: VCD Switching Report

5.2 Sign Off Smart Kit (Prime Rail)

5.2.1 Introduction

The SignOffSmartKit is a set of TCL procedures and GUI interfaces that simplify the parasitic extraction (PEX), Delay calculation Static Timing Analysis and IR-Drop Analysis during Digital SignOff addressing only âĂIJSmart Power High Voltage TechnologiesâĂİ (BCD).

5.2.2 Sign Off Smart Kit Flow

1. Technology and Design Setup for Parasitic Extraction.

2. STAR-RC command options setup for LEF DEF database extraction flow.

3. Analysis conditions setup to perform multiple parasitic extractions.

4. Environment and design setup for delay calculation. Analysis conditions setup to perform multi corner STA.

5. Technology and Design Setup for IR-Drop and EMI Analysis.

6. Power Analysis flow implementation thru Synopsys PrimeTime PX in batch mode.

7. Dynamic and Static IR-Drop and EMI Analysis flow for Multi Supply

8. Single Voltage designs using Synopsys PrimeRail GUI.

9. Analysis conditions setup to perform multiple IRdrop/EMI analyses.

Color Map vdd and gnd (130nm)

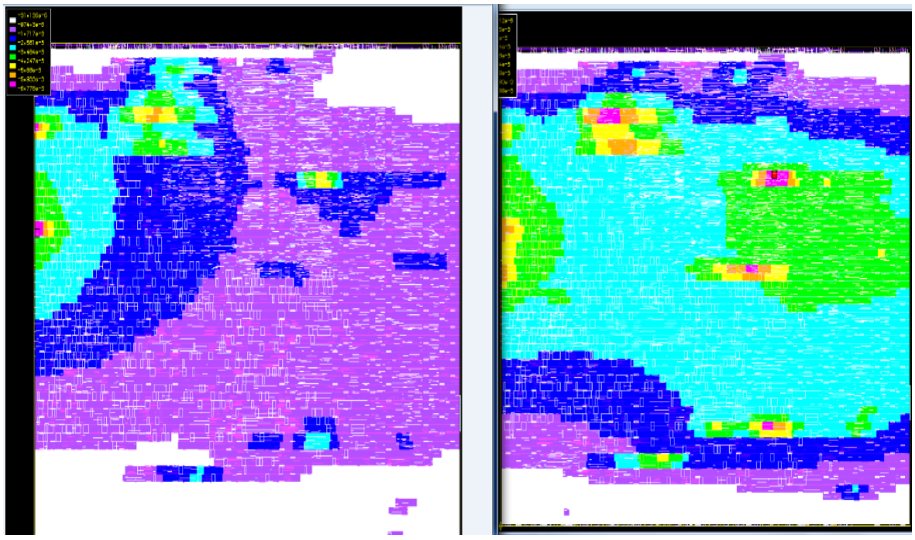

Figure 5.5: vdd and gnd Color Map

Hotspot Locations

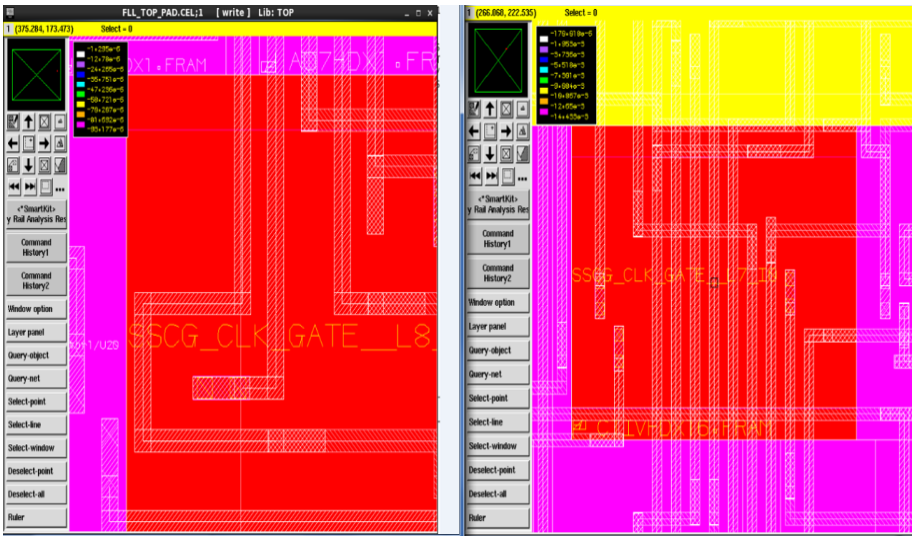

Figure 5.6: Different Hotspot Locations

Chapter 6

Conclusion

My work / responsibility was to analyze the IR(voltage) drop and Electromigration(EM) of the design and give feedback for the improvement of floor plan as a part of Place and Route(PNR) activity in design flow.
1. After working on several IPs and running simulations iteratively with the help of REDHAWK was able to establish that not only we can reduce the power and IR drop on the IPs with the above described techniques but also reduce the design cycle time.
2. Design cycle time can be reduce by pre estimating the IR drop with the help of developed methodology. For designs that are in early stages of design and do not have complete placement and routing information, RedHawk allows you to perform power grid verification early in the design process to ensure that the grid meets initial design guidelines. This can verify, at an early stage, the placement of power pads and check electromigration issues at the pad connections or at other key locations on

the grid.

3. Also to develop the methodology to reduce the effect of cross talk on IPs under process for performance enhancement.The new features in PrimeTime-SI enable the STA of the circuits in presence of timing deviations due to the crosstalk effects. The methodology and the main commands/attributes have been presented and the tool has been applied to two 90um / 28um high speed digital designs. Although some areas of enhancement, like performance and accuracy, will have to be addressed, to handle a problem that is expected to become dominant in the next future technologies.

Thus, as the technology is shrinking day by day power integrity and signal integrity has been the burning topic nowadays.

Chapter 7

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