Abstract

In the domain of deep submicron (DSM) and nanometer ASIC teclinologies (180 nm and below), the traditional separation between logical (synthesis) and physical (place and route) design methods often causes a problem—designs cannot meet their realistic timing objectives; creating the well known "timing closure problem". Timing closure is now considered the biggest area of difficulty for ASIC performance-oriented designs. The underlying reason is that circuit delays are dominated by net delays, which are influenced by the placement of the cells. The traditional fanout-based wireload models, for estimating interconnect delay during synthesis, are considered inaccurate and are the key factor causing the lack of timing predictability between post synthesis and post layout results. It is evident that synthesis and placement technologies must merge to create properly placed and routable designs that meet realistic performance goals.

Certification of standard cells libraries is defined as the process of certifying an Intellectual Property (LP.) through various design flows. The inputs to the process of certification process are the cell views available in the standard cell libraries. These cell views are schematic, layout, symbol and abstract of the various combinational and sequential logic blocks.

The process starts by generating a gate level netlist using the cells available in the library to be certified. The salient feature of the gate level netlist is that the entire design is only using the cells of the library.

Thus, in all, generation of this type of netlist makes the required platform for the certification flow to run on this netlist. Next, the place and route flow operations like floorplanning, placement, clock tree synthesis (CTS), post CTS optimization, routing and post-route optimization are performed on this netlist to generate the layout at each and every level of flow. Ultimately, the post-routed design is fed to the finish design flow, wherein, the gdscad file (GDS-II) is generated along with some other files which are useful for the signoff of the design. By Signoff, we do the operations like Formality Verification, DRC, LVS, Delay Calculation, Timing Analysis, Back-annotation and many more. The aim of certification is to verify that the standard cell library when used won't create violations regarding timing closure, area constraints, power dissipation. The thesis basically deals with this very domain of VLSI design, the Certification of Standard Cell Libraries.
Shared BIST Architecture for Embedded Memories