Abstract

Distributed Arithmetic (DA) is an important Algorithm for DSP Applications. It is based on a bit level rearrangement of the MAC "Multiply accumulate" operation to replace it with set of Look Up Table (LUT) addition and shifting operations. DA based computations are bit serial in nature. The advantage of a distributed arithmetic approach is its efficiency of mechanization. The basic operations required are a sequence of table look-ups, additions, subtractions and hifts of the input data sequence. All of the functions efficiently map to FPGAS.

In a conventional MAC based FIR realization, the sample throughput is coupled to the filter length with a DA architecture, the system sample rate is related to the bit precision of the input data samples.

As sample rate is decoupled from the filter length. The decoupled from the filter length.

The trade off introduced here is one of Silicon Area (or FPGA Real Estate) for time.

This report describes a theory of DA based FIR filter with various options and configurations and also methodology to implement DA based FIR filter on FPGA.Final aim of project is to develop IP for Custom Digital Signal Processor (CDSP)