

Abstract

The Dissertation work involves Designing Power grid, Static and Dynamic IR drop analysis at various stages (Floor planning, Place & Route and GDS), Effect of IR drop on Timing, Adding Decoupling Capacitance from the analysis result of Dynamic IR drop.

The design of efficient power distribution meshes is increasingly subject to worst case IR drop, and the effect that IR drop will have on circuit timing.

While power planning tools can optimize a power grid for a specified maximum IR drop, this level of detail omits two important factors from analysis.

The first is whether the maximum IR drop threshold is correctly chosen. For example, if a number of critical timing paths pass through the area of maximum IR drop, and the reduced supply voltage causes those timing paths to experience setup or hold failures, then the maximum IR drop threshold may need to be lower. Likewise, if the power grid is over-designed, we may be able to gain area by reducing P/G wire width without worsening peak IR drop, and thereby improve critical path timing by freeing routing channels for more direct signal routing. The goal of IR drop analysis is to analyze the power-grid in different stages of the physical design flow and finally to fix the power-grid based on the IR drop analysis result. The IR drop analysis result is also taken to the delay timing analysis. The IR drop analysis is a continual exercise from the floor planning to final layout stage.