Defect Characterization and Testing of QCA Devices and Circuits: A Survey

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Abstract*—QCA (Quantum-dot Cellular Automata) is the promising future nanotechnology for computing. In QCA, the cells must be aligned properly at nano scales for proper functioning. Defects may occur in synthesis and deposition phase. So the defect analyses and testing cannot be ignored. This paper presents a survey on QCA basics, defect characterization and various testing aspects of QCA.

***Index Terms*—quantum-dot, QCA, defect, testing.**

I. INTRODUCTION

Among emerging nanotechnologies like Single Electron Transistor (SET) [1], Quantum-dot Cellular Automata (QCA) [2] and Resonant Tunneling Diodes (RTD), QCA is most promising technology. Quantum-dot Cellular Automata is capable to implement dense, low power circuits and systems for high performance computing. Quantum-dot Cellular Automata is a mean of representing binary information in cells, through which no current flows, and achieving device performance by the coupling of those cells [3].

As the QCA is promising nanotechnology, the defect and faults should be analyzed. There should be development of testing method. One can think about the mapping of available conventional CMOS technology circuit testing to the QCA circuits. This paper presents a survey on QCA basics, defect characterization and various testing aspects of Quantum-dot Cellular Automata.

II. QCA BACKGROUND

Fig. 1. Shows the schematic of a four-dot QCA cell. The cell consists of four quantum dots positioned at the corners of a square. The cell contains two extra mobile electrons, which can tunnel between quantum dots of the cell [4].

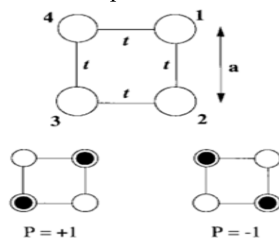

Fig. 1. A schematic of a four-dot QCA cell [4]

Electrons within the cells always occupy antipodal sites due to Coulombic repulsion. As per the positions of electrons shown in Fig. 1. , the cell polarizations are P=+1 and P= -1, which are encoded as binary '1' and '0' respectively.

The basic building blocks of QCA are majority voter, inverter and binary wire as shown in Fig. 2. (a), (b) and (c) respectively [5]. The Boolean function of the majority gate is given as F = AB + BC + AC. An AND gate and an OR gate can be easily built using a majority gate by fixing one of its input to either low or high respectively.

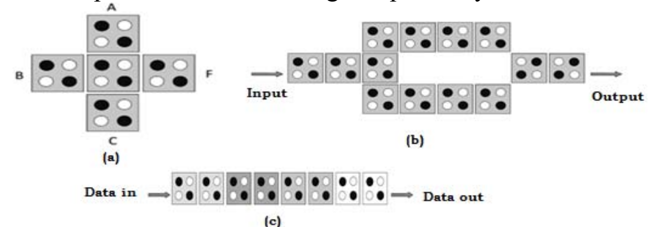

Fig. 2. QCA basic blocks (a) Majority gate (b) Inverter (c) Binary wire

Clocking is important in QCA circuit in which clock signal is given to each cell. QCA clocking mechanism consists of four clock signals with equal frequencies with phase difference of $\pi/2$ as shown in Fig. 3.

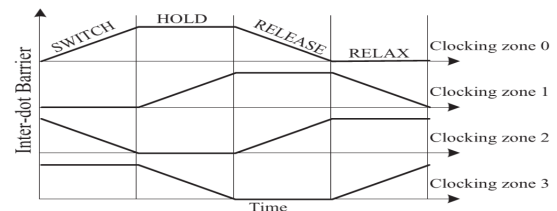

Fig. 3. Clocking scheme [6]

Each clock zone contains four phases like switch, hold, release and relax.

III. DEFECT CHARACTERIZATION

Defects during molecular QCA manufacturing can occur in two phases namely synthesis and deposition. In the synthesis phase, the individual cells (molecules) are manufactured and in the deposition phase the cells are placed in a specific location on the surface [7]. The defect classification is shown in Fig. 4.

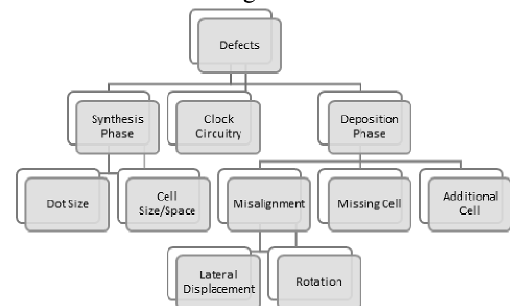

Fig. 4. Classification of defect characterization

In cell misalignment defect, defective cell is misplaced from its original direction. A cell of device or circuit is missing in a missing cell deposition defect. The cell without electron or missing electron defect can be model as missing cell deposition defect. Additional cell may get deposited on the substrate in additional cell defect.

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Tahoori *et al*. have simulated the various deposition defects in MV using QCADesigner1 v1.20 simulation tool [8] with a 5-nm dot size, a 20 nm 20 nm cell size, a 5-nm cell distance [9]. They have analyzed the cell displacement defects in MV like displace of cell A, B, all input cell and output cell, all input cell, A and B considering the defect free MV as shown in Fig. 2 (a). They also analyzed the misalignment defects for defect free MV shown in Fig. 2 (a) , like cell A misaligned toward the right and left, Cell C misaligned towards right and left, both the cells A and C misaligned towards right and left and cell B misaligned.

The have [9] concluded using these defect analyses that the input cell B is dominant in most of the cases. For misalignment, any single cell misalignment greater or equal to half a cell causes malfunction which causes the fault at logic level. The misalignment defects affects the functionality of an MV with the same defective distance as the displacement defect.

Momenzadeh *et al.* have analyzed the deposition defects in molecular QCA devices and circuits [7]. Unlike metal-based QCA, in molecular QCA implementation a defect may occur due to the erroneous deposition of cells on a substrate. This deposition may cause the missing cell or an additional cell which may get placed near to the layout or within the layout of a device. Extensive simulation and the impact of missing cell and additional cell defects were evaluated for in the devices like majority voter, inverter, different wire configurations like straight, L-shape, coplanar crossing and fanout. Input and output cells were considered as defect free. A single missing or additional cell deposition defect was injected in the original device or along the adjacency boundary. The coherence vector engine of QCADesigner v1.4.0 was used for simulation with cell size is $10\times10nm^2$, cell-to-cell distance and dot size of 2.5nm.

The functional effects of the deposition defects were observed which further permitted to define a fault set for each QCA device. It was observed that an extra cell deposition generates no functional fault for almost all devices except inverter and the coplanar wire crossing. Further QCA 2 inputs exor gate circuit was analyzed for the obtained fault set of each device, one by one, to generate the test vector.

IV. TESTING ASPECTS

The properties of MV has been investigated and proved by Tahoori *et al*. The effectiveness of different stuck-at test sets for detection of QCA defects were studied in [10]. They also presented the design for testability scheme based on a change in the structure of the design.

The first comprehensive test generation methodology for combinational QCA circuits has been proposed by Gupta *et al.* [11] [12]. SSF is not guaranteed to detect all the simulated QCA defects using QCADesigner in the majority gates sothat further test generation is required for additional test vectors. Based on the QCA defect characterization results from [7] and [10], [11] [12] have provided the additional test vectors other than SSF test set, to detect defect in the QCA circuit. Based on the fault list derived from fault collapsing theorems, [11] [12] have generated an SSF test set using a Boolean satisfiability (SAT) based approach. Fault simulation on the logic-level circuit was performed using the generated test set.

The bridging faults were also targeted for QCA interconnects in [11]. The proposed Automatic Test Pattern Generator (ATPG) were tested for MCNC and ISCAS'85 benchmark circuits.

F. Karim *et al.* have considered the probability-based testability analysis technique and presented an extension to the existing PODEM algorithm to include the ability to generate test patterns for majority and minority networks, specifically targeting quantum-dot cellular automata (QCA) [13]. Further the unspecified bits in the test patterns generated by ATPG were filled using genetic algorithm to achieve compaction on the final test set size. The modified PODEM algorithm was tested on a set of MCNC benchmark circuits.

V. CONCLUSION

We have covered state of art of the available defect characterization and testing aspects of QCA devices and circuits in this survey paper. Survey suggests that there is a wide scope in research of new fault model and testing algorithm for QCA devices and circuits.

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