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DEFECT ANALYSIS OF QUANTUM-DOT CELLULAR AUTOMATA COMBINATIONAL CIRCUIT USING HDLQ

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ABSTRACT

CMOS technology has achieved the device dimension in the nanometer range. Beyond this CMOS technology is the QCA (Quantum-dot Cellular Automata). Due to nanoscale defects may occur in this technology so in the consequences of it the faults will occur. This paper presents the defect analysis of QCA basic devices like Majority Voter (MV), inverter. The defect analysis and its effects on the output of combinational circuit using Hardware Description Language for QCA (HDLQ) is presented in this paper.

Index Terms: Quantum-Dot, QCA, Defect, HDLQ

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1. INTRODUCTION

CMOS technology has achieved the device dimension in the nanometer range. Further if this technology scale down the effects like doping fluctuations, short channel effects, and ultra-thin gate oxides may occur. Nanotechnologies that can be substitute to CMOS technology are Single Electron Transistor (SET) [1], Quantum-dot Cellular Automata (QCA) [2] and Resonant Tunneling Diodes (RTD) [3]. Researchers claimed that Quantum-dot Cellular Automata is best solution to the replacement of conventional CMOS technology [2]. It is also predicted that QCA will implement the digital circuits with no current conduction so the power dissipation will be extremely

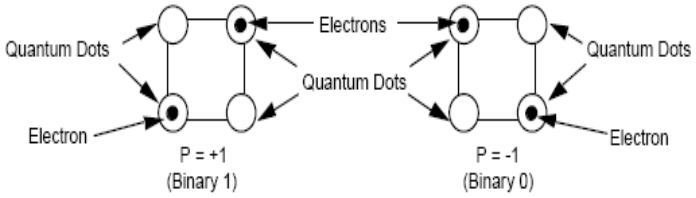
low. Since the information flow due to the interaction of cells, the speed can be achieved up to THz. The dimensions of QCA cells will be very less, in nanometer so higher device density can be achieved. [4]. Basically QCA consists of the array of cells in which information hold and transfer from source to destination with the help of the Coulombic interaction between cell to cell [5].

Due to the nanostructure of the cells of QCA, there is possibility of the occurrence of defects in the QCA devices and circuits. At nanoscale, there are chances of defects in QCA devices and systems. The survey on various defects is carried out in [6]. It is discussed in section III. So it important to analyzed the defects in the QCA devices and circuits. This analysis will helpful to decide fault model and testing of QCA circuits. In this paper the QCA combinational circuit is implemented using Hardware Description Language for QCA (HDLQ) [7]. Also the defects and fault effects on the output of the QCA combinational circuit is analyzed using HDLQ.

The sections of paper is arranged as follows, section II contents the background of the concepts of QCA. The defect classification and earlier work done is carried out in section III. About the HDLQ and its features given in section IV. Defect analysis of QCA combinational circuit is discussed in section V. Paper is concluded in section VI.

2. BACKGROUND

QCA consists of array of cells in which each cell contains four, five or six quantum dots depending upon the types. Two electrons are free to tunnel between the quantum dots. The arrangement of quantum dot cell is shown in. Fig. 1. [8]. Four quantum dot cell is shown in Fig.1. All four dots are positioned at the corners of a square cell.



(a) (b)

Figure 1 Four-dot QCA cell

Because of the Coulombic repulsion the electrons in the cell occupy antipodal sites as shown in Fig. 1. Polarization of shown configuration is calculated using equation 1 given below

$$P = \frac{(\rho 1 + \rho 3) - (\rho 2 + \rho 4)}{\rho 1 + \rho 2 + \rho 3 + \rho 4} \quad (1)$$

According equation 1, the polarization for Fig.1. (a) is P=+1 and for Fig.1. (b) is P=-1. Polarizations P=+1 and P=-1 are encoded as binary '1' and '0' respectively.

According to the material used for quantum dot to make QCA cell the types of QCA are decided. The available types of QCA are magnetic, metal-islands, molecular and semiconductor [8] [9] [10] [11]. Molecular QCA is the most capable type in which single molecular can act as a cell. Small size molecular QCA cells are fabricated using self-assembly process [12]. Magnetic and metal-island QCA can

achieve the speed up to MHz while semiconductor and molecular QCA can achieve the speed up to THz.

The basic building blocks of QCA are majority voter, inverter, binary wire, 450 inverter chain [13]. A majority gate is basic element which works as a logic gate in QCA. It consists of three inputs and one output, as shown in Fig. 2. The Boolean function of the majority gate is given as F = AB + BC + AC. The output of the majority gate, as indicated by the name, is determined by the majority of its three inputs. For example, if two of the inputs are low, the output will be a low. If two of the inputs are high, then output will be a high. Here high refers to the polarization state P = +1, and low refers to the polarization state P = -1. The truth table of a majority gate covering all possible combination of inputs and corresponding output is shown in Table 1.

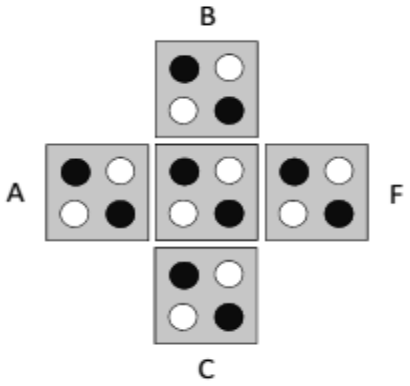


Figure 2 QCA Majority Gate

Table 1 Truth table of majority gate

C	B	A	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

QCA inverter is shown in Fig.3, is another fundamental logic gate in QCA with one input and one output. It takes the input logic and produces its inverse logic on output. The truth table of it is given in Table 2. If the input is logic High, the output will be Low. If the input is logic Low, the output will be high. So many implementations are possible for inverter but the given one is robust implementation.

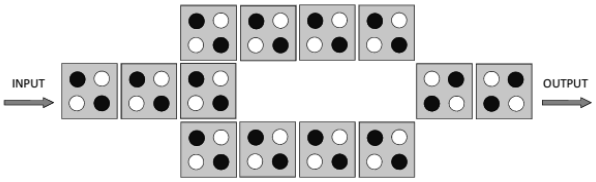


Figure 3 QCA Inverter

Table 2 Truth table for QCA inverter

Input	Output
0	1
1	0

One can have conventional logic gates such as AND and OR gate using majority gate. An AND gate and an OR gate can be easily built using a majority gate by fixing one of its input to either low or high respectively. Fig. 4(a) shows a QCA design of a two-input AND gate and Fig. 4(b) shows a QCA design of a two-input OR gate. The truth tables of AND gate and OR gate are shown in Table 3(a) and (b) respectively.

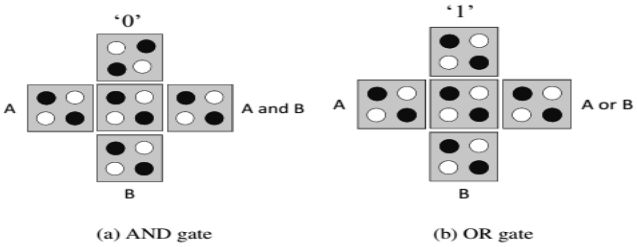


Figure 4 QCA (a) AND gate (b) OR gate

Table 3 Truth table for AND and OR gate

C	B	A	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

$C = 0$: $F = A \wedge B$
(a)

C	B	A	F
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$C = 1$: $F = A \vee B$
(b)

A binary wire is used to transfer information from one part of the circuit to another. In a QCA circuit, a wire not only helps in information transfer, it actually can performs some computational operation on the information to be transferred. The two basic types of wire in QCA are the normal wire and the inverter chain.

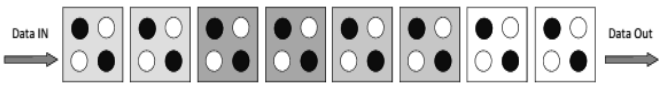


Figure 5 Binary QCA Wire

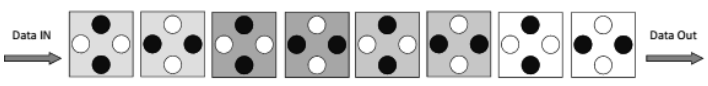


Figure 6 An Inverter 45^o chain

Coplanar wire crossing is possible in QCA unlike conventional CMOS. It enables the QCA wire to cross in the plane without changing the value being transmitted on

either wires. Coplanar wire crossing needs wires to be of different orientation, i.e., one of them should be of 90-degree orientation and other of 45-degree orientation. Fig. 7. shows an example of coplanar wire crossing, where value of Input1 flows towards Output1 and Output 2 determines the value of Input2.

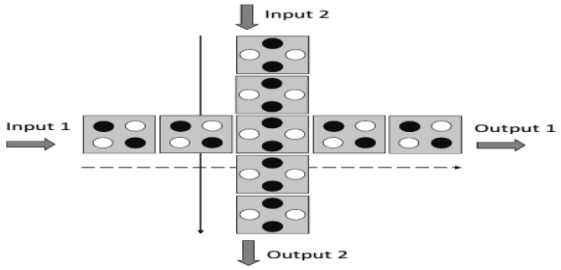


Figure 7 Coplanar QCA wire crossing

Clocking in QCA provides the power gain. It is important in QCA circuit. In clocking of QCA, clock signal is given to each cell [14]. Two types of clocking schemes are possible for QCA one is abrupt clocking scheme and another is adiabatic clocking scheme.

QCA has a clocking mechanism that consists of four clock signals with equal frequencies. One of the clock signals can be considered the reference (phase = 0) and the others are delayed one (phase = $\pi/2$), two (phase = π) and three (phase = $3\pi/2$) quarters of a period as shown in Fig. 8.

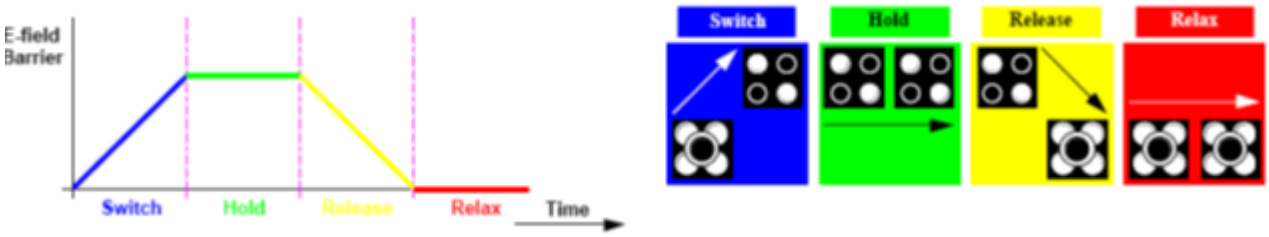


Figure 8 Clocking scheme

3. DEFECTS IN QCA

The defect classification is shown in Fig. 9. There are possibility of defect during synthesis and deposition phase. In synthesis phase single cell is fabricated while in deposition phase the cells are placed on substrate at desired location [15].

In synthesis phase dot size variation can occur. Also there is change in size of cell in the synthesis phase. In the deposition phase cell misalignment, missing cell and additional cell deposition defects can occur. In the cell misalignment deposition defect, the cell can be misplaced from its defect free structure. In this defect cell can be displaced from its original location in the QCA basic devices discussed in the section II.

In the missing cell deposition defect the single or multiple cell can be missed in the QCA device. In the additional cell deposition defects the extra cell is going to be deposited nearer to the QCA device.

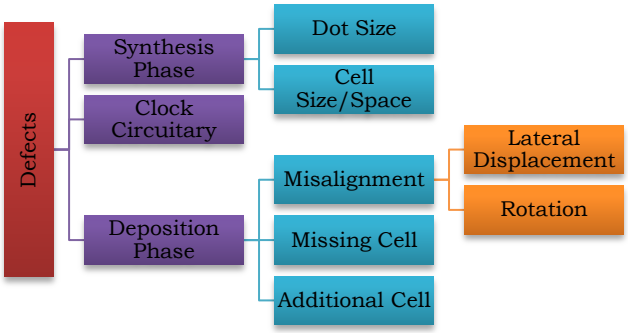


Figure 9 Types of defect

The deposition defects are analyzed in molecular QCA devices and circuits in [15]. This deposition may cause the missing cell or an additional cell which are nearer to the layout or placed within the layout of a device. Extensive simulation and the impact of missing cell and additional cell defects were evaluated for in the devices like majority voter, inverter, different wire types like straight, L-shape, coplanar crossing and fanout.

The misalignment and displacement defects are analyzed in [16, 17].

4. HARDWARE DESCRIPTION LANGUAGE FOR QCA

The layout design and simulator tool is available to observe the response of QCA circuits named QCADesigner [18, 19]. The single missing cell defects can be analysed using QCADesigner. To support and describe the logical behavior of the circuit and system, hardware description language must be available. VHDL and Verilog are two widely used HDLs. Synthesis using these languages consists basic, universal gates since they are available as primitives. In QCA circuit and system the basic elements are MV, inverter. QCA circuit is basically network of MVs and inverters. So primitives of MV must be available. The hardware description language for this kind of primitives of QCA is developed in [7]. This is known as HDLQ.

Apart from the QCA logical circuit synthesis which gives the combinations of MVs and inverter using HDLQ, there has to be provision of analysis of defects or faults discussed in section III. The developed HDLQ [7] also support this feature. HDLQ allows the designer to verify the logic characteristics of a QCA system and the unique features of QCA such as bidirectionality and timing/clocking partitioning as well.

As given in [20] fault-injection involves the deliberate insertion of faults or errors into a computer system to determine its response. Fault injection using HDLQ would be done at the logical level.

1. Majority Voter primitive in HDLQ with fault injection capability Consider the majority voter shown in Fig. 10.

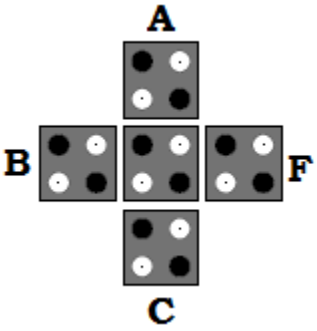


Figure 10 Majority voter

MV implements the function F (A, B, C) = AB+BC+AC. The single missing cell and additional cell deposition defects carried in [15], MV has faults stuck_ at_ B (s_a_B) and F (A', B, C'). Two auxiliary inputs *fault*0 and fault1 are available in the HDLQ MV primitive as shown in Fig. 11.

Fig.11. shows the synthesis result of HDLQ MV using Xillinx ISE tool. If *fault*0 = 0, fault1 = 0 then it is considered as the fault-free configuration. If *fault0 = 0*, *fault*1 = 1 then it is considered as the stuck-at-B fault. If *fault*0 = 1 and *fault1 = 0* then it is considered as the fault F (A', B, C').

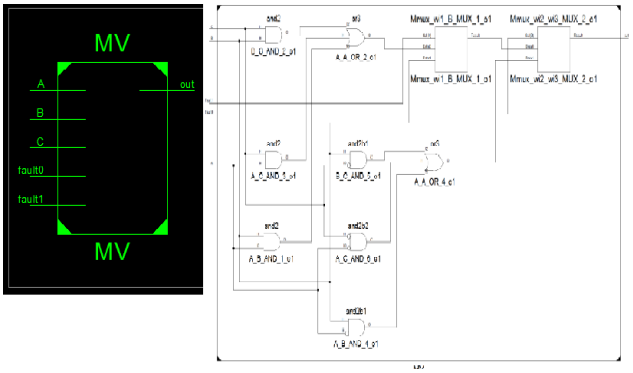


Figure 11 Majority voter primitive synthesis using HDLQ

Simulation can be done by setting the values of auxiliary inputs *fault0* and *fault1* for the corresponding fault injection. Simulation results for fault S_a_B is shown in Fig.12. Here the value of auxiliary inputs are, fault0=*0* and *fault1=1*.

When input A=0, B=1 and C=0 the out (F) which is the majority of these must be logic 0. Since the presence of S_a_B fault the out (F) is at logic 1.

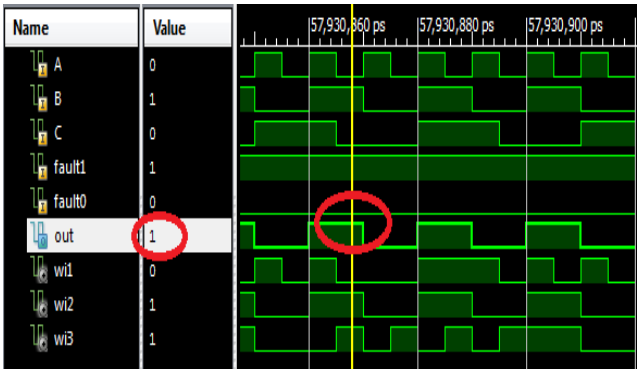


Figure 12 Simulation result for MV at S_a_B fault

The Table 4 shows the effect of output due to S_a_B fault for the various combinations of input.

Table 4 Effect of S_a_B fault

A	B	C	F Fault Free	F Faulty
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

HDLQ supports the fault injection capabilities for all basic building blocks. Using this feature of HDLQ, effects of faults can be analyzed in QCA circuits and systems.

In this way the defect analysis and fault effects could be carried out for QCA basic building blocks MV, inverter, binary wire, L-Shaped wire and fanout.

5. DEFECT ANALYSIS OF QCA COMBINATIONAL CIRCUITS

The given combinational circuit or its Boolean function must be synthesis into QCA MV and inverter network. Synthesis tools reported in [21] are used to convert the given Boolean function into QCA MV and inverter network.

In this paper 2X1 multiplexer, adder are implemented using HDLQ. Single missing cell defect analysis and fault effects are carried out using HDLQ. This analysis will further helpful for the development of testing methods for QCA circuits and systems.

The single missing cell deposition defect analysis also possible using QCADesigner [18] at the layout level. The single missing cell deposition defect analysis are carried out in [16] using QCADesigner. Also in [22] the defect analysis of adder is carried out layout level using QCADesigner and at logic level using HDLQ. Both the results are compared and found equivalent.

The Fig.13. shows QCA 2x1 multiplexer using MVs and inverter. Here AND and OR gates are implemented by keeping one of the inputs of MV at logic 0 and logic 1 respectively.

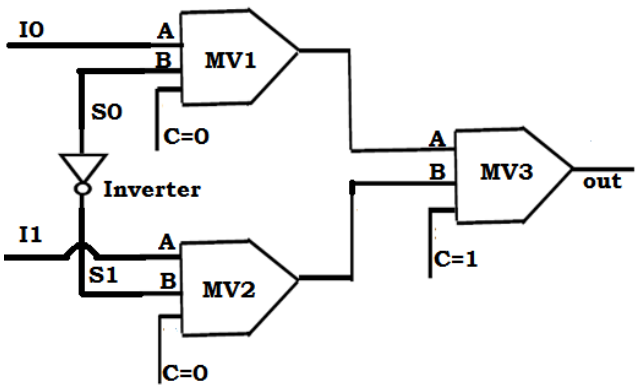


Figure 13 QCA 2X1 Multiplexer

MV1out = I0S0

MV2out = I1S1

Where S1=S0’

MV3out = out = I0S0+ I1S1

The 2X1 multiplexer shown in Fig. 13. is implemented in HDLQ for the defect and fault analysis. The instantiations of all HDLQ modules for MV and inverter are taken. The testbench is also developed. Xillinx 13.1 ISE tool is used.

Here one by one fault is injected in the HDLQ to observe the response of the QCA 2X1 multiplexer.

For Example

Consider the Majority Voter 1 (MV1). As discuss in section IV, the S_a_B fault is injected by setting the values of fault0 and fault 1 as logic 0 and logic 1 respectively. The snap shot of HDLQ simulation of 2X1 multiplexer for MV1 at s_a_B is shown in Fig. 14.

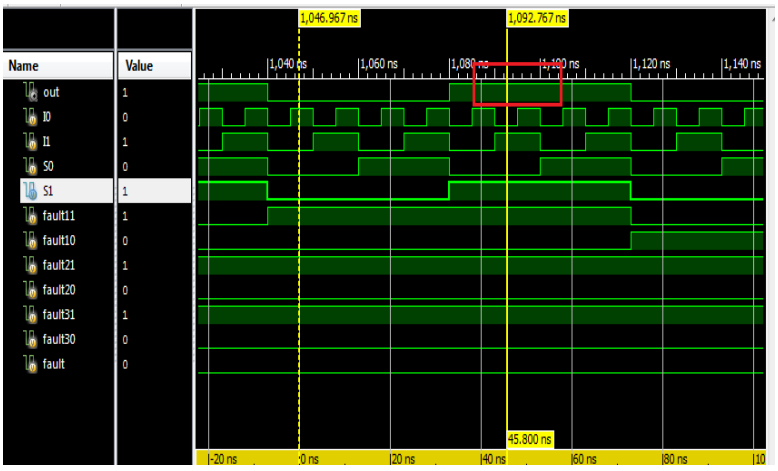


Figure 14 Simulation of 2X1 multiplexer for MV1 at s_a_B

For fault free condition, if I0=0 and I1=1 the output must be logic 0. In case of presence of S_a_B fault, the out=1. This is because MV1 S_a_B means the output of MV1 is S0 instead of I0S0.

MV1out = S0 (due to S_a_B)

MV2out = I1S1

Where S1=S0’

MV3out = out = S0+ I1S1

If I0=0 and I1=1 out will be logic 1 instead of 0.

The all possible defects and faults are analysed for QCA 2X1 multiplexer in all basic devices like MV and inverter.

The fault caused by the defects and its effects on output is summarized in Table 5.

Table 5 Analysis of defects and faults on 2X1 multiplexer

Input				**Fault Free output**	**MV1**		**MV2**		**MV3**		**Inverter**
I0	I1	S0	S1	out	S_a_B	F(A'BC')	S_a_B	F(A'BC')	S_a_B	F(A'BC')	S_a_A
					out						
0	0	0	1	0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	0	0	0	0	0
0	1	0	1	0	1	1	1	1	1	0	0
0	1	1	0	1	1	1	0	1	0	0	1
1	0	0	1	1	1	1	1	1	0	0	0
1	0	1	0	0	1	1	1	1	0	0	1
1	1	0	1	1	1	1	1	1	1	0	0
1	1	1	0	1	1	1	1	1	0	0	1

6. CONCLUSION

The defects in the future nanotechnology is more likely to occur. The defect analysis for deposition missing cell and additional cell in the QCA circuit can be done using Hardware Description Language for QCA, HDLQ. In this paper the analysis of defect and faults are done for 2X1 multiplexer using HDLQ. The fault free and faulty outputs are observed which will be useful for the test generation and the testing.

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