

Abstract

The major objective of this work is to design low noise amplifier (LNA) and phase locked loop (PLL) for the receiver front end. The receiver front end is designed for an RF application to transfer the data in the range of 100 meters. The specifications used are similar to the bluetooth specifications.

The design is implemented in 0.8 μm CMOS technology. The major constraints are power consumption, area and noise. The noise and gain analysis of the LNA is covered in this work. The noise analysis is done using IIP3 (Third Order Intermediation Product) concept. The IIP3 and gain of the LNA is 10.79 dBm and 10.78 dB respectively. For the design of the LNA, on chip inductors are used. The values of the on chip inductors are up to 10 nH. The layout of the design is also completed.

The PLL frequency synthesizer is used for the channel selection in receiver front end. The simulation of the PLL is done in the work.

The PLL comprises phase frequency detector (PFD), Charge pump, Loop Filter and Voltage Controlled Oscillator (VCO). The reference frequency is 5 MHz. In the designing of PLL, digital phase frequency detector is used. Passive 2nd order filter is used as a loop filter. The architecture to implement the voltage controlled oscillator is LC based. Low value on chip inductors is used in the design of VCO.