Abstract

The Dissertation work involves removing the antenna violations, producing a layout satisfying the DRC rules and calculation of IR Drop for each memory block on a test chip at the floorpalnning stage.

The 'antenna' is an interconnect, i.e., a conductor like polysilicon or metal, that is not electrically connected to silicon, i.e., not 'grounded', during the processing steps of the wafer.

The connection to silicon would normally provide an electrical path to bleed-off any accumulated charges. If the connection to silicon does not exist, charges may build up on the interconnect to the point at which rapid discharge does take place and permanent physical damage results, e.g., to MOSFET gate oxides.

This destructive phenomenon is known as the 'antenna effect'. The 'antenna ratio' of an interconnect is used to predict if the antenna effect will occur. To remove the antenna effect the antenna ratio is calculated and as per the ratio either the reverse biased diode is connected between the gate of the transistor and Vdd or Vss or jogging of the different metal layers is performed. DRC (design rules) can be considered as a prescription for preparing the photo masks used in the fabrication of integrated circuits. Design rule specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs.

To make the layout satisfying all the DRC rules the errors like space, enclosure and end of line is corrected as per the availability of space on the chip area. The power dissipation of the chip, and thus, the temperature, increases with the increasing clock frequency. Since the dissipated heat must be removed effectively to keep the chip temperature at an acceptable level, the cost of packaging, cooling, and heat removal becomes a significant factor in these circuits. Finally, IR Drop for each memory block is calculated by using the ASTRO rail flow.