Abstract

In this major project we designed a floating point coprocessor that operates in double precision mode. The floating point co-processor is IEEE 754 compliant. Floating point co-processor is important in many high performance signal processing applications. This floating point co-processor design is implemented for our VHDL double precision floating point library. This design is implemented in VHDL and is designed to make efficient use of FPGA hardware and speed of 1MHz. The implementation of addition, subtraction, multiplication and division are algorithm based. These algorithms are particularly well-suited for implementation on FPGA. The addition, subtraction, multiplication and division components have been incorporated into the framework of our double precision floating-point library.

The completed Floating Point Unit can be attached to a CPU through an AHB bus enabling faster calculation.
In the proposed design, interface of floating point coprocessor is established through master slave bus approach of AMBA-bus.

This particular design is verified using test bench for various algorithms of add / subtract, multiplication and division. The exception mechanism is introduced using Flags This RTL design of 64-bit floating point arithmetic co-processor can be used as IP core.