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Model based robust Peak Detection algorithm of Radiation Pulse Shape using limited samples

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Abstract: Impulses coming from radiation detector are amplified / enhanced using charge sensitive low noise preamplifier which modifies the original pulse shape retaining the measurable properties of input. One of the important parameter of such pulse shape is the pulse height which in most cases is proportional to the energy of in-coming impulses. In application of high resolution measurement like Multi Channel Analyzer, the accuracy of pulse height measurement is an important issue for resolution of energy peak between two adjacent channels.

In this paper, we propose a method to estimate the accurate peak using model based computation of radiation pulse shape profile with limited digitized samples on pulse profile to achieve higher energy resolution. Use of limited digitized samples allow us to use low sampling ADC instead of fast flash ADC having sampling speed of 100 to 400 Ms/s. The model is built using multi-layer Feed Forward type Neural Network (FFNN) along with back propagation learning algorithm. It uses 4 to 5 normalized random samples as input to fit the detector and amplifier shape characteristic and provides output indicating its peak. It assumes, shape characteristic remains constant with respect to pulse height variation.

To test the model, we have generated simulated pulses similar to the output of CR-RC shaper circuit with pattern signature database for FFNN instead of radiation detector and front end analog signal processing circuits. In training phase, Neural Network is trained using known peak value and 4 samples taken at fixed intervals. The trained FFNN weights are used in operating phase. In operating phase, random 4 sample points are acquired on pulse profile and applied to a trained FFNN model to estimate the peak value using trained FFNN weights. Result obtained with simulated data set is very encouraging. Percentage accuracy of correct prediction of peak height is more than 99.95% which is equivalent to 2 channel shift error in 4096 channel Multi Channel Analyzer (MCA).

I. Introduction:

The most widely used radiation detectors are devices that respond to ionizing radiation by producing electrical impulses and will be used by the signal processing circuits to extract the useful information from these impulses. In order to extract such information from the narrow width and low amplitude detector pulses, a number of analog and digital signal processing steps are required. Broadly speaking the signal can be either processed entirely through a chain of analog circuitry or it can be converted to digital form for analysis.

The figure 1 and 2 shows the various stages of Analog and Digital Pulse Processing techniques respectively. The impulse produced by the detector output has a very narrow width and amplitude and therefore cannot be directly processed. Whether the processing is analog or digital, the detector pulse always be first pre-amplified using charge sensitive pre-amplifier. The subsequent processing steps highly depend on which signal processing method is used. If Analog Signal Processing technique is used then as shown in Figure1, the pulse is further shaped using widely used CR-RC shaping amplifier circuit, Digitized using Peak Sensing Analog to Digital Convertor (ADC) and stored into histogram memory for further analysis.

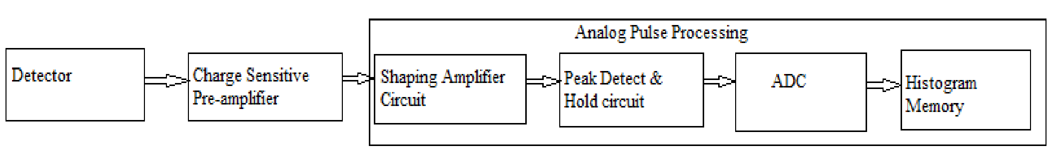


Figure 1: Schematic diagram of Analog Pulse Processing Architecture

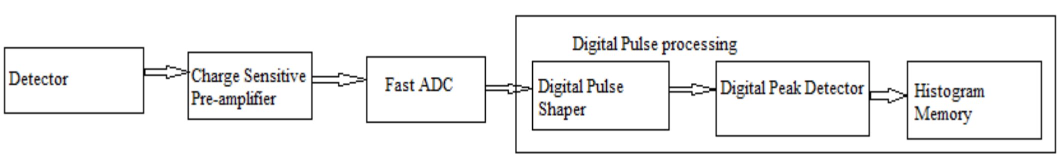


Figure 2: Schematic diagram of Digital Pulse Processing (DPP) Architecture

On the other hand, Figure 2 shows the schematic diagram if Digital Pulse Processing technique is desired. Output of the Charge sensitive pre-amplifier circuit is directly digitized using fast ADC and processed digitally as shown in Figure 2. In this technique, the Charge sensitive preamplifier output pulse is digitized directly using a fast flash ADC having sampling rate in the order of 100 to 400 Ms/S. Pulse is digitally shaped and digital peak detector will detect the peak and it will be stored in histogram memory for further analysis. This is possible due to the development of improved and high speed front end devices for data acquisition (high speed ADCs) and ultra high speed programmable logic devices like FPGAs. Various advantages of DPP over standard analog processing have been already reported in many publications[3,4,5] .

One of the important parameter of charge sensitive pre-amplifier output pulse shape is the pulse height which in most cases is proportional to the energy of in-coming impulses. In application of high resolution measurement like Multi Channel Pulse Height Analyzer, the accuracy of pulse height is an important issue for resolution of energy peak between two adjacent channels. Many DPP methods have been proposed to measure the pulse height of the output of the charge sensitive pre-amplifier circuit. These methods use flash ADC having sampling rate of more than 100 Ms/S to digitize the full pulse profile. Then various algorithms like simple peak search, digital shaping followed by peak search, polynomial fitting , deconvolution etc[6,7] are applied to measure the pulse height. Algorithms mostly depends on the number of digitized samples (to obtain complete pulse profile) which demands higher and higher sampling rate ADCs (sampling rate > 100 Ms/S). Most of the algorithms involves complex mathematical calculations which demands off-line processing in many cases. Also in all DPP methods, it is reported that "accuracy claimed" can be further improved if higher sampling rate ADCs are available.

In our work, we have proposed hybrid Pulse Processing Architecture. Pulse output of charge sensitive pre-amplifier will have the characteristic of fast peak and long exponential tail. CR-RC shaping circuit receives the signal from the charge sensitive preamplifier output and provides a quasi Gaussian output whose width can be changed selecting different shaping time constant. The height is still proportional to the energy released by the detected particle. It digitizes output of the CR-RC shaper circuit instead of output of the Charge sensitive pre-amplifier circuit as shown in figure 3.

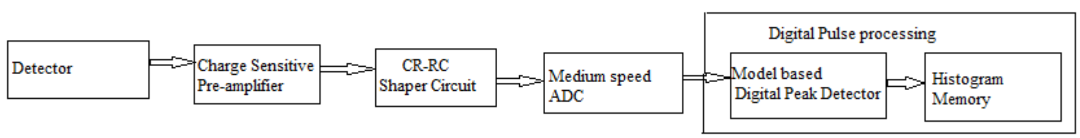


Figure 3 : Schematic diagram of Proposed Hybrid Pulse Processing Architecture

Our model does not require the complete digitized pulse profile, instead it uses only few sampled value on the pulse profile at fixed intervals. This allows us to use slow sampling ADC instead of flash ADC based board having sampling rate of 100 Ms/S or more. Many researchers have reported a flash ADC based board in their DPP based spectroscopy systems[8,9,10] due to requirement of many digitized sample values on pulse profile of the pulse shape in their algorithms. Analog shaping will add the error of pulse pile up in the measurement, if the Pulse Repetition Frequency (PRF) is high. The work is in progress to detect the pulse pile up and correction with the neural net model and will be reported during the subsequent publications.

II. Materials and Methods:

We have built the neural net model on the basis of step pulse response of CR-RC pulse shaper circuit. CR-RC pulse shaping technique is simplest and widely used method of pulse shaping the output of charge sensitive pre-amplifier. If we assume that the output of the charge sensitive pre-amplifier is a step function with a step voltage of amplitude V0 at t = 0 then the pulse profile after passing through subsequent CR and RC stages can be approximated by[1,2]

$$V_{out} = \frac{V_0\ \tau_d}{(\tau_d - \tau_i)}\left(e^{t/\tau_d} - e^{t/\tau_i}\right) \qquad \text{---} \quad \text{Eq.1}$$

Where τd and τi are time constant of CR (differentiator) and RC (integrator) circuits respectively. Figure 4 shows a simple CR-RC shaper circuit and its response to step input pulse.

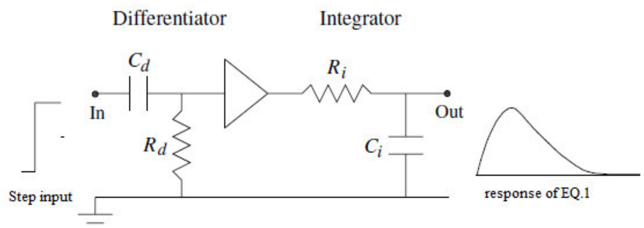


Figure 4 : A simple CR-RC shaper circuit and its output response to a step input

According to EQ.1, the rise and decay times of the shaped pulse depends on the time constants of the CR and RC shapers. In nuclear pulse amplifiers, CR-RC shaping is most often carried out using equal differentiation and integration time constants. In that event, Eq.1 becomes indeterminant, and a particular solution for this case is[1] :

$$V_{out} = V_0 \, (t/_{\tau}) \, e^{-t/\tau} \qquad \text{Eq.2}$$

The choice of time constant of a CR-RC shaper depends on the particular requirements of the detection system. The measurement of high resolution and high throughput capability are two contradicting factors that must be considered to find an optimized solution. Good resolution demands that the time constant be large enough to ensure complete integration of the detector signal. However long pulse duration might be problematic in high pulse rate situations which will create pulse pile up. In such a case the time constant is shortened at the expense of resolution.

We have generated simulated pulses similar to the output of CR-RC shaper circuit to test our model. To obtain the semi Gaussian shape, one more stage of integrator is added which will follow the Eq.3 (assuming differentiation and integration time constants having equal value τ)[1]:

$$V_{out} = V_0 \, [(t/_{\tau})]^2 \, e^{-t/\tau} \qquad \text{Eq.3}$$

Simulated pulses were generated based on the Eq.3 with pattern signature database and used for training as well testing our neural net based model. System will be further validated in real radiation spectroscopy system with commercial detector, charge sensitive pre-amplifier and CR-RC shaping amplifier pulse profile.

III. Implementation:

A Simulator which emulates the radiation detector pulse at the output of CR-RC2 shaping circuit which follows mathematical model based on Eq.3, is designed. The data obtained from this simulator is used to train and test the FFNN model.

i) Simulated Data Generator:

Simulated data generator is designed to emulate the detector and shaper circuit and shown in Figure 5 which replaces nuclear pulse generator or actual experimental set up[11]. It assumes shape characteristics of the shaping circuit remains constant with respect to pulse height variation.

We have assumed 4096 energy channel analyzer which is normally being used for scientific investigations to measure the energy profile of the radiation. Simulator described above, produces normalized energy level between 0 to 1 in real values but to match the resolution, 0 to 1.0 range is quantized to 0 to 4096 levels to simulate the output of 12-bit ADC, which is used in 4096 channel analyser. This makes 4096 possible pulse profiles of different heights.

It can generate infinite sequences of pulses of random amplitude and frequency which is limited by storage space for analysis. It also generates Peak Pile up and Tail Pile up events which will be useful later for testing of pile up detection and correction algorithms. For present reported work, the training and test data set excludes Pile up events.

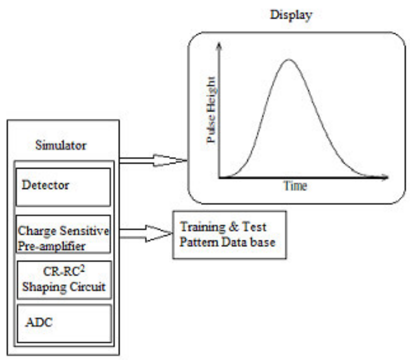
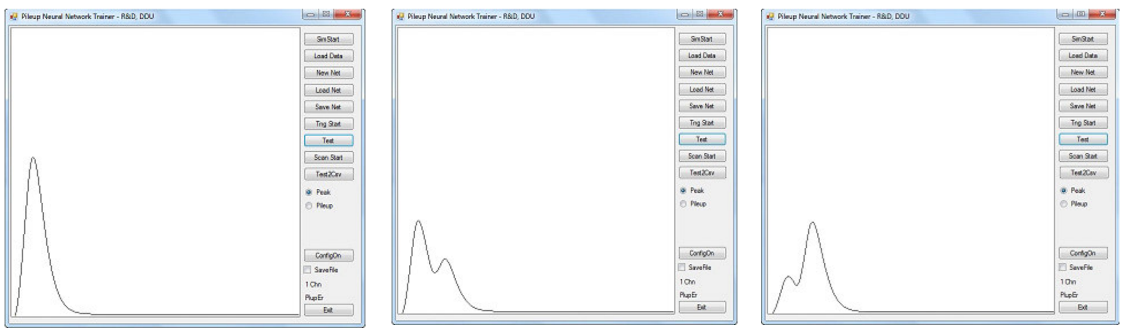


Figure 5: Simulator which emulates detector, amplifier and CR-RC2 shaping circuit

Figure 6(a), 6(b) and 6(c) shows no pileup, tail pileup and Peak pileup events respectively.



(a) (b) (c)

Figure 6: Simulated shaper output for (a) No Pile up (b)Tail Pile up (c) Peak Pile up (time vs amplitude profile)

One most important advantage of simulator is to avoid expensive detector and radiation source which is a source of health hazard also. It also generates pattern signature database as shown in table 1 and used for training and testing the FFNN model.

The figure 7 shows the simulated pulse profile generated by the simulator. It also shows the 4 sample points on pulse profile which are used during training phase and testing phase. The first point P1 is the threshold point. Remaining 3 points P2, P3, P4 are at a fixed time interval from the threshold point P1. Simulator reflects these 4 sample points in pattern database as shown in table 1. It also reflects the Pulse Peak point which is used during training phase and validation phase

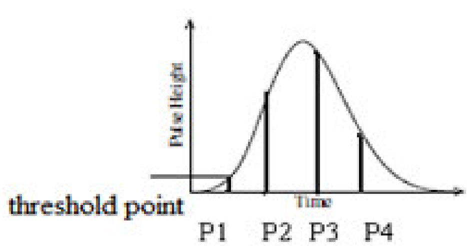


Figure 7: 4 digitized sample points on simulated pulse profile

The entry in the pattern data base generated for a pulse profile by the simulator is shown in Table 1 below :

H1	H2	H3	H4	H5	H6	D0	--	D499
H1 is PileUp / no pileup	H2 is Peak Value Index	H3 is P1 point Index (Threshold)	H4 is P2 point Index	H5 is P3 point Index	H6 is P4 point Index	D0 is the first 12-bit simulated ADC value in array	--	D499 is the last simulated 12-bit ADC value in array

Table 1: Pattern signature database for FFNN

Column 1(H1) in Table1 indicates presence of pileup. If it is "1", it is a pileup event and is not used by the present work for training or test data set. If it is "0", it is without pileup event and is used by the model as training data or test data set. Column 2 (H2) indicates the index of peak position in D0 to D499 array and is used during training phase as expected output during error calculation. During operating phase, this value is used for validation. Column 3(H3) is the index of threshold point and column 4 to 6 are the index of three sample points at fixed intervals after threshold point. Remaining columns are the 12-bit simulated pulse profile values.

ii) System Architecture to test the neural net model with simulated data set:

In this paper, we propose a method to estimate the accurate peak using model based computation of radiation pulse shape profile with limited digitized samples on pulse profile to achieve higher energy resolution. Use of limited digitized samples on pulse profile allow us to use low sampling ADC (without the use of sample and hold circuit) instead of fast flash ADC in our hardware set up. Due to low sampling ADC, even if we miss the digitized peak value on the pulse profile, model will estimate the correct peak. Simulated pulse profile shown in figure 7 and pattern database generated by the simulator shown in table 1, are used to train and test the model. From these samples, a numeric model of the CR-RC2 shaper circuit is built to estimate the energy level (peak value).

Figure 8 shows the simplified software architectural experimental setup for training phase and operating phase of the FFNN model to estimate accurate Peak (pulse height) of the simulated radiation Pulse Profile.

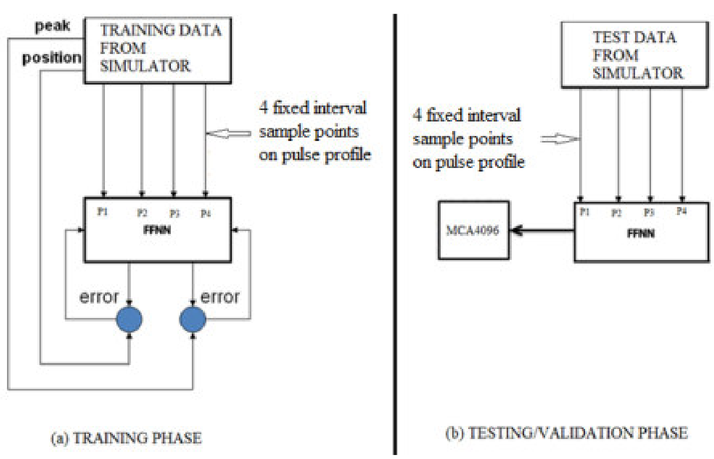


Figure 8: System Architecture to test FFNN model with simulated data (a) Training Phase: simulated training data is collected with known pulse peak value and peak time to train FFNN using back propagation algorithm. The trained FFNN weights are used in testing/validation phase.(b) Testing / Validation Phase : A set of four samples on pulse profile are applied to a trained FFNN model to estimate the peak value for multi-channel analyzer MCA4096.

The model is built using multi-layer Feed Forward type Neural Network (Figure 9) along with back propagation learning algorithm. In first phase, Neural Network will be trained using known simulated peak value and 4 samples taken at fixed intervals. The network architecture used is four input neurons for normalized four input sample points on pulse profile. There are two outputs - peak position and peak height. The peak position is used only for validation of predicted profile display. Time is not used for actual analysis. The predicted output from the system is shown in figure 10.

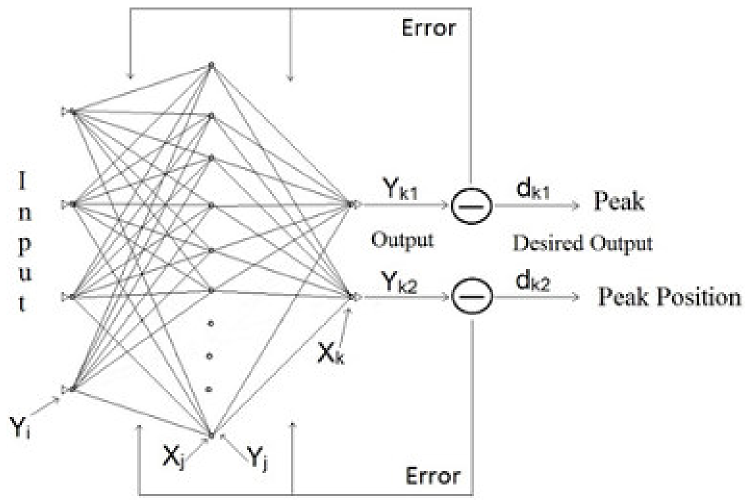


Figure 9: A multilayer Feed Forward Neural Network with Y_i as inputs and Y_k as outputs for pulse peak prediction application

Equation 4, 5, 6, 7 shows the forward pass computation to update all neural nodes	
$X_j = \sum_{i=0}^{imax} W_{ij} * Y_i$ -------------------------------- Eq.4	$Y_j = \frac{1}{1+e^{-X_j}}$ --- Eq.5
$X_k = \sum_{j=0}^{jmax} W_{jk} * Y_j$ ------------------------------- Eq.6	$Y_k = \frac{1}{1+e^{-X_k}}$ --------------------------------------- Eq.7
$W_{kj} = W_{kj} + \eta * (Y_k - d_k) * Y_k * (1 - Y_k) * Y_j$ -- Eq.8 Equation 8 - Update of Output Layer's Connection Weight's using Back Propagation	
$W_{ji} = W_{ji} + \eta * \sum\{(Y_k - d_k) * Y_k * (1 - Y_k)\} * Y_j * \left(1 - Y_j\right) * Y_i$ --- Eq.9 Equation 9 - Update of Hidden Layer's Connection Weight's using Back Propagation	

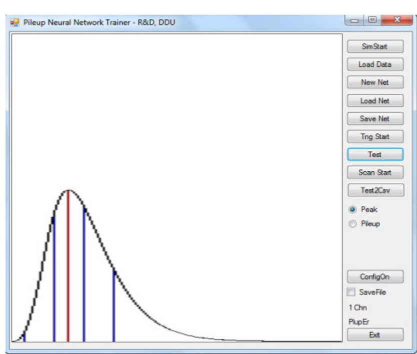


Figure 10: Output showing the 4 sample points input (blue) to NN and correctly predicted peak output (red) (time vs amplitude profile)

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IV. Proposed Implementation:

Model has been tested with emulated pulses whose characteristics are similar to CR-RC2 shaper circuit. Figure 11 shows the simplified software/hardware architectural experimental setup for training phase and operating phase of the FFNN model to estimate accurate Peak (pulse height) of the radiation Pulse Profile.

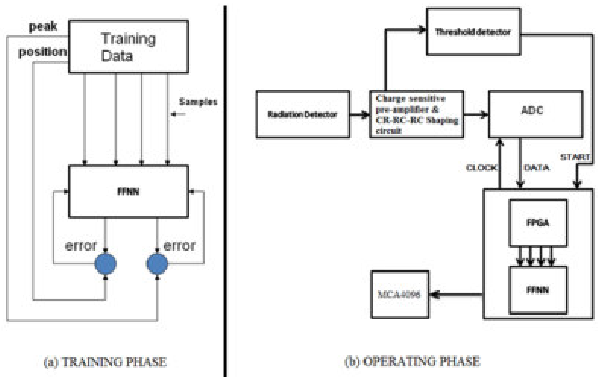

Figure 11: System Architecture with hardware set (a) Training Phase: simulated training data is collected with known pulse peak value and peak time to train FFNN using back propagation algorithm. The trained FFNN weights are used in operating phase. (b) Operating Phase: Leading edge of pulse profile and threshold set value decides the START event that triggers ADC conversion process and collects four samples at fixed intervals. A set of four 12bit samples are applied to a trained FFNN model to estimate the peak value for multi-channel analyzer MCA4096.

V. Measurement Result:

The predicted output after training is tested (validated) using a different non exclusive data set of 10000. The predicted accuracy for the given data set is shown in table 2. More than 2 channel shift error is zero. Hence Percentage accuracy of correct prediction of peak height is more than 99.95% which is equivalent to 2 channel shift error in 4096 channel Multi Channel Analyzer (MCA).

Table 2: Pulse Peak detection Accuracy

Test data set per test (pulses)	Zero Channel shift pulses	*One Channel shift error	**Two Channels shift error	More than Two Channels shift error	% accuracy of correct prediction
10000	9056	920	24	0	99.76
10000	9073	908	19	0	99.81
10000	9143	830	27	0	99.73
10000	9092	875	33	0	99.47
10000	9133	848	19	0	99.81
10000	9090	889	21	0	99.79
10000	9113	865	22	0	99.78
10000	9140	833	27	0	99.73
10000	9129	847	24	0	99.76
10000	9151	832	17	0	99.83

* One channel shift detected pulses are quantizing error of the system, hence could be considered no error.

VI. Conclusion:

A method is described to estimate the accurate pulse peak using model based computation of radiation pulse shape profile with limited digitized samples on pulse profile to achieve higher energy resolution. Accuracy is tested with simulated pulse profile. Use of limited digitized samples on pulse profile allow us to use low sampling ADC (without the use of sample and hold circuit) instead of fast flash ADC in our hardware set up. Field Programmable Gate Array (FPGA) is used for real time data acquisition and processing. This knowhow will be used for implementation of FPGA based MCA for space payloads.

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