Abstract
In this thesis architecture for a sigma-delta over-sampling analog-to-digital converter (ADC) is described. In this architecture the first order modulator is realized using an integrator and a comparator at the input stage.

The 1-bit digital-to-analog converter used as feedback stage. The first order modulation is designed using an 4 MHz sampling clock frequency and implemented in a standard 0.35um n-\vell CMOS process.
The decimator is an on-chip sine-filter. In this thesis decimator filter design has been implemented in 0.35um n-well CMOS process for integration with an above designed modulator to form a sigma-delta digital-to-analog converter. The decimator is implemented using cascaded Integrator Comb (CIC) filter. The input to decimator is provided from a first order modulator. ADC can be operated with an oversampling clock frequency of up to 4MHz. The ADC is designed to provide an output resolution of 8-bit. An in-built clock divider circuit has been designed which generates two output clocks whose frequency are equal to the input clock frequency and input clock frequency divided by over-sampling ratio 4.The layout of complete sigma-delta ADC,1 bit modulator along with decimator filter is carried out in Microwind version 3.0 . The complete design also includes ESD protection circuits along with the pads for connecting core logic with external world.