Simulation, Design, and Analysis of Three-Level Shunt Active Harmonic Filter using T-Type NPC Topology

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***Abstract*—Power quality at the source side deteriorates due to current harmonics which are introduced in the power system by non-linear loads, originating a vital difficulty. Rectifiers, variable speed drive, switched mode power supply, etc. types of non-linear loads create such harmonics. Conventional technique to eliminate such harmonics is use of passive filters but this technique has the disadvantage of series and parallel resonance within the network impedance, overcompensation of reactive power at fundamental frequency and poor flexibility. Shunt Active Harmonic Filters (SAHF) are generally used to reduce current harmonics. The active harmonic filters introduce remunerating currents into the source to neutralize the harmonics possessed by the load current. The compensating currents will be derived by sensing three-phase voltages at the Point of Common Coupling (PCC) and load currents. Efforts are made in this study to analyze Fast Fourier Transform (FFT) algorithm, Instantaneous Reactive Power (IRP) technique, and Synchronous Reference Frame (SRF) technique used to derive the reference compensating currents. These compensating currents act as reference currents for the fixed switching based current controllers which generate control signals for the SAHF employing three-level T-type Neutral Point Clamped (TNPC) topology of converter.**

Keywords*— *Fixed Switching based Current Controller; Reference Compensating Current Generation Techniques; Shunt Active Harmonic Filter; Three-Level T-type Neutral Point Clamped (TNPC) Topology of Converter.

I. INTRODUCTION

The design of transformers, transmission lines have been made easier by using ac supply which is sinusoidal in nature with fixed frequency. It also provided feasibility of long distance power transmission during nineteenth century ending. If the phase angle between load current and source voltage was zero then the electrical power system could be formed more systematic or such that achieving maximum productivity due to appearance of sinusoidal voltage sources. From this the concept of Reactive Power, Apparent Power and Power Factor had been come in existence. The circuit has been utilized by higher the power factor and it is economical also because the state electrical power distributor companies have identified clearly bottom line restriction for power factor & load utilized at poor power factor is penalized for not using available power with maximum productivity. Conventional techniques for power factor correction use capacitor banks & reactors. The concept of reactive & apparent power loses its usefulness in non-sinusoidal cases after 1920's. At that time Budeanu [1, 2] and Fryze [3] give power definitions under non- sinusoidal conditions. Budeanu defined power in the frequency domain while Fryze defined power in time domain in the year 1927 & 1932, respectively. In late 1960's power electronics emerged hence increasing the penetration of non-linear loads that consume non-sinusoidal current. The conventional incandescent lamps and induction motor in steady state are linear loads but electronically controlled fluorescent lamps and induction motor drive equipped with rectifier-inverter for achieving adjustable speed control are non-linear loads. Power converters may take reactive power with harmonic current from power system, but they offer rapid control in governing their voltages/currents. The evolution & increased growth of active harmonic filters for reactive power compensation & harmonic compensation is inevitable because the standard power hypothesis constructed on average/rms values of voltages & currents are not relevant to the investigation & blueprint of power converters & power system. As we know "Necessity is the mother of invention", the pioneer papers considered for a fundamental concept of controlled reactive power remuneration had been published by the authors Erlicki & Emanuel-Eigeles [4], Sasaki & Machida [5], Fukao, Iida & Miyari [6] during the period between the end of 1960's to the beginning of 1970's. The term "Instantaneous Reactive Power for a single phase circuit" has been introduced in 1976 by Harashima, Inaba & Tsuboi [7] for the first time and in the same year the term "active ac power filter" has also been introduced for the first time by Gyugyi & Strycula [8]. In 1996, the article published by H. Akagi reports status of active harmonic filters based on state of the art power electronics technology and their future prospects [9]. The study about a DSP implemented hardware execution of current error space phasor constructed hysteresis controller for shunt active harmonic filter is published in 2014 [10]. The study about a multipurpose single phase SAHF for domestic purpose is published in 2015 [11]. The study about the modification in the classical model predictive control method and its application to active harmonic filter is published in 2017 [12]. Multi-level inverters have been applied for active power filters [13]-[18]. Various techniques for harmonic extraction like instantaneous

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reactive power theory (IRP) and synchronous reference frame theory (SRF) have been developed [19]-[23]. This paper presents the investigation of 3 phase shunt active harmonic filter using three-level T-type Neutral Point Clamped topology, utilizing fixed switching frequency based current control with various reference compensating current generation schemes for compensating load harmonic currents as shown in Figure 1.

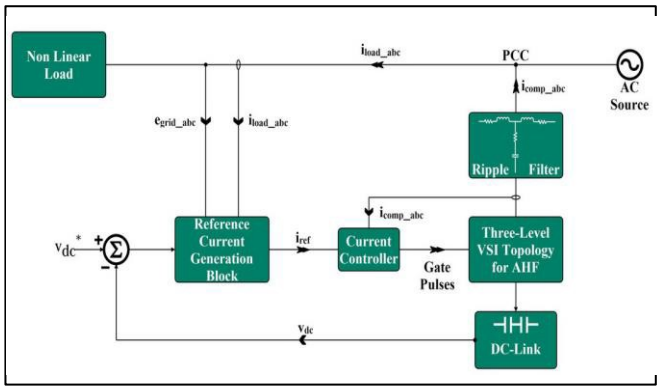

Fig. 1: System Block Diagram

II. Need of Active Harmonic Filter

Focus on power quality issues have increased due to enhanced use of non-linear loads, as a result of which are rising the rising incidents of harmonic complications on the power network. The rising issues of power network distortion is due to number of factors like:

- Rising implementation of power electronic type devices which have non-linear V -I characteristics are cause rise in production of harmonics on the power network. These devices include rectifiers, inverters, etc., used for such things as medium voltage drives and converters for electro-mechanical loads.
- Rising implementation of shunt capacitor banks for power factor correction & voltage regulation consequences in a raised potential for resonant states which can magnified existing harmonic margins.
- The equipment is more susceptible to harmonic voltages and currents due to decreased margins in equipment design.

III. Inverter Topology

Three phase two-level voltage source inverter is used for medium & high power traction as well as industrial power drives. The power circuit of the high power two-level voltage source inverter (V SI) is shown in Figure 2. The expression multi-level initiates with the three-level inverter launched by Nabae [13]. The harmonic distortion has been reduced in output voltages with more steps creating a staircase waveform by raising the number of levels in the inverter. Today, multi-level inverters are widely applied in medium voltage high power applications. Following are the multi-level topologies:

- Cascaded H Bridge (CHB) Topology
- Flying Capacitor (FC) Topology
- Neutral Point Clamped (NPC) Topology
- T-Type Neutral Point Clamped (TNPC) Topology

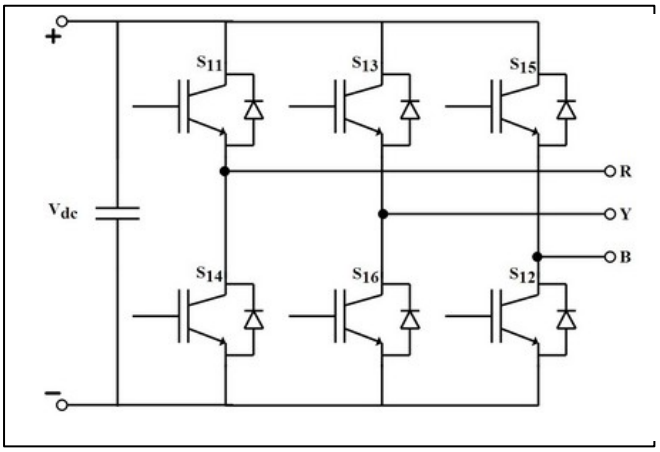

Fig. 2: Three-Phase Two-Level Inverter Topology

In 1975, the cascaded H-Bridge inverter was primarily proposed with a design that combines separately dc sourced full bridge cells in series to analyze a staircase ac output voltage [14]. It eases reactive power compensation since no complex multi-pulse input transformer is required and also used for very high-power applications, since the series interconnection allows a rise of the power level of the converter. The basic Symmetric five-Level CHB multi-level inverter (CHB-MLI) is shown in Figure 3.

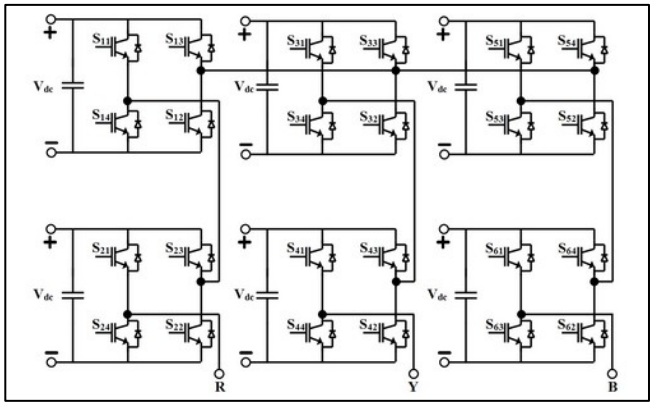

Fig.3: Three-Phase Symmetric Five-Level Cascaded H-Bridge Inverter Topology

The flying capacitor (FC) V SI topology was proposed nearly 25 years ago. It was presented by Hochgraf [15] in 1994 and Lai [16] in 1996. In FC multi-level inverter (FC-MLI) topology, clamping capacitors or floating capacitors are used to clamp the voltages and hence this topology is also known as capacitor clamped inverter topology. The additional expense of flying capacitors, particularly at low carrier frequencies and a increased capacitor voltage balancing requirement are the main disadvantages of the FC topology. The FC topology is used in high bandwidth implementations, such as medium voltage traction drives. The basic Three Level FC MLI topology is shown in Figure 4.

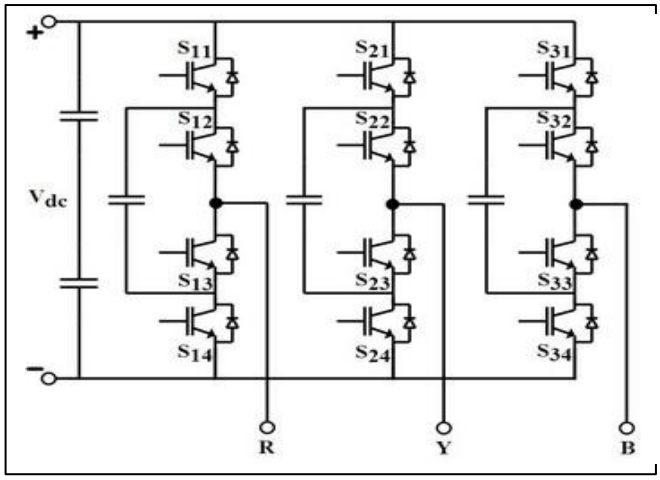

Fig. 4: Three-Phase Three-Level Flying Capacitor Inverter Topology

The neutral point clamped (NPC) is also known as diode clamped inverter. It was primarily proposed as a three-level inverter where in dc-link is halved and the centre point is the dc-link is identified as the neutral point. The neutral point clamped MLI topology is effectively able to develop voltage levels twice the device voltage level without needing accurate voltage matching. It was proposed in 1980s [17]. The basic three-level NPC MLI topology is shown in Figure 5.

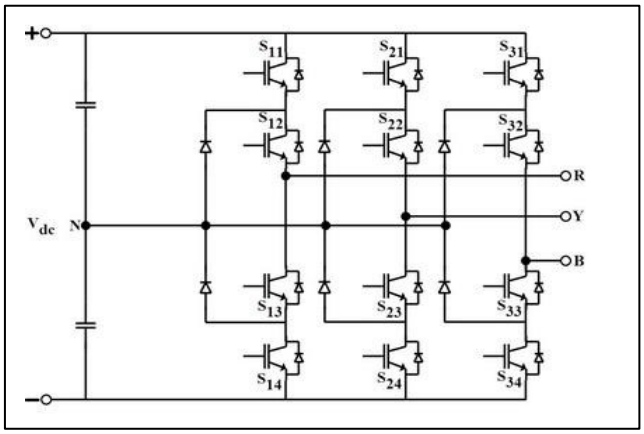

Fig. 5: Three-Phase Three-Level Neutral Point Clamped Inverter Topology

For low voltage implementation, the accessible gadgets have enough voltage grading and rapid switching rates. A raised output power is obtained with raised phase current & conduction loss are a key ingredient for restricting the power span and should be kept as minimum as feasible. So, the TNPC MLI topology [18] is the prime selection for low voltage implementations formed on bipolar gadgets. The basic three-level TNPC MLI topology is shown in Figure 6. Maximum productive energy transformation in the low voltage span has acquired more & more awareness towards implementations such as photo voltaic grid inverters, power factor correction rectifiers, automotive inverters and active harmonic filter systems, which urged for a marvelous efficiency at low costs.

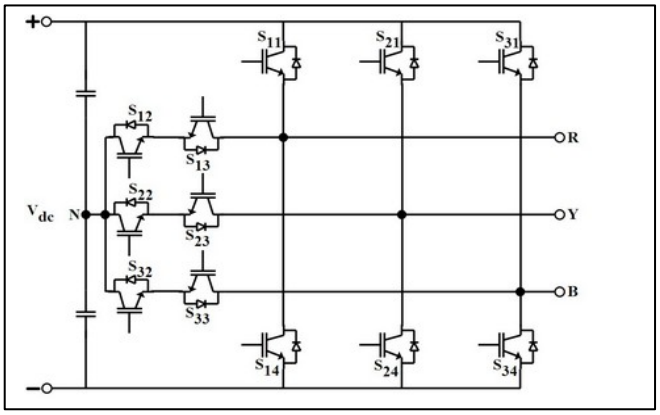

Fig.: 6 Three-Phase Three-Level T-Type NPC Inverter Topology

The switching frequency is often raised to medium magnitudes of 10-35 kHz which tends to higher switching loss & lower system productivity in order to have small and cheap passive components. The IGBT formed two-level V SI topology is regardless the typical industry requirement to fulfill the needs of the implementations mentioned. A nother solution has troubles to acquire market share due to their raised complication & costs. Potential energy savings realized with a distinct inverter topology can only assure the customer if the inceptive costs are not too high and the speculation may give good revenue. Multi-level inverter topologies have a dependence on the inverter efficiency & the switching frequency. If a typical two-level V SI with 1200 V IGBTs is compared to a three-level NPC inverter with 600 V power semiconductor devices, the productivity of the three-level inverter can be superior if the switching frequency is higher to 35 kHz. Below 5 kHz switching frequency, Selecting Three Level topology of V SI is no question because conduction losses are more than Two Level topology. Definitely greater than 35 kHz, NPC is the best solution but if switching frequency is less than or equal to 20 kHz than the switching losses are less in TNPC topology still between 20 kHz and 35 kHz which NPC or TNPC topology is better that issue is still debatable.

IV. . Reference Generation Technique

The power quality at the source side deteriorates due to current harmonics which are introduced in the power system by non-linear loads, cause major difficulty. Shunt active harmonic filters (SA HF) are generally used to reduce current harmonics. The active harmonic filters introduce compensating currents into the source to neutralize the harmonics hold in the load current. The compensating currents will be derived by sensing three phase voltages at the point of common coupling and the load currents. Using one of the various techniques like FFT algorithm, instantaneous reactive power technique and synchronous reference frame technique, the reference compensating currents will be derived using appropriate mathematical derivations and calculations. These compensating currents act as reference currents for the current controller which

generates control signals for the SA HF. Following are the techniques for reference current generation:

- Fast Fourier Transform (FFT) Algorithm
- Instantaneous Reactive Power (IRP) Technique
- Synchronous Reference Frame (SRF) Technique

J. W. Cooley & J. W. Tukey issued a paper based on some works of the premature 20th century which again launched the technique in 1965 which is now known as the Fast Fourier Transform (FFT) [19]. The FFT is a method or algorithm for computing the DFT with reduced number of calculations. The FFT is widely used in power electronics harmonic analysis applications because of its ease of implementation into embedded systems. This technique is favored in most of DSP implementations if the waveform is exercised online using microprocessors with more clock frequency. The fundamental working principle of a SA HF needs excerpting harmonics to be removing or reduced from the load current waveform. So, the FFT is a strong implement for harmonic investigation in active harmonic filter. The course of action time of the technique applied in processor is the disadvantage of this exercise because it wants sampled data over one cycle to judge the spectrum of harmonics. If the load current differs in every few cycles of time, the FFT technique may not issue ample statistics online to follow the load harmonics.

Takahashi, Fujiwara & Nabae issued two papers informing a concept of the appearance of the IRP theory in 1981 [20, 21]. As shown in the block diagram of Figure 7, the harmonic current constituents can be discovered by IRP technique of reference compensating current generation in three phase system. The dc & ac constituents in these instantaneous active & reactive powers are due to fundamental & harmonics parts of load currents, respectively. The high pass filter (HPF) is used to filter out the power values of the dc constituents. Thus, the still existing part is excerpted as active & reactive powers sourced by the load harmonic currents. Here, the hindrance of response is due to filter's performance. The reference compensating current for each phase of the SA HF has been generated in stationary coordinates and then finally in a, b & c phases using inverse Clarke's transformation. This technique does not carry zero sequence constituents & hence the outcome of unbalanced voltages & currents into account, due to this limitation the IRP theory is widely used for three phase balanced non-linear loads, such as rectifiers. The block diagram of synchronous reference frame (SRF) technique [22] is shown in Figure 8. This technique primarily formed on Clarke's & Park's Transformation. The

+V e & -V e sequence controller blocks are mainly implemented. The +V e sequence constituent of load current is converted to rotating axis by creating +V e sequence phase statistics $+\theta_e$ from PLL Circuit. The description of mathematical execution of PLL software in the synchronization of three-phase network is given in [23]. Three-level flying capacitor based filter is proposed in [24].

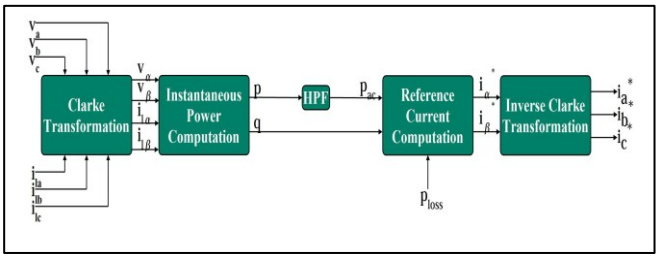

Fig. 7: Block diagram of IRP based reference current generation scheme

The dc & ac constituents in +V e sequence waveform include fundamental & harmonic parts of load current, respectively. The –V e sequence constituent of load current is also converted to rotating axis by creating –V e sequence phase statistics - θ_e from the PLL circuit. For the balanced three phase voltages & currents, the output of –V e sequence controller will be zero. The –V e sequence current constituents are eliminated from the reference compensating current waveform & the active harmonic filter only compensates the load current harmonics because here the aim is not to mitigate current imbalance in the load currents.

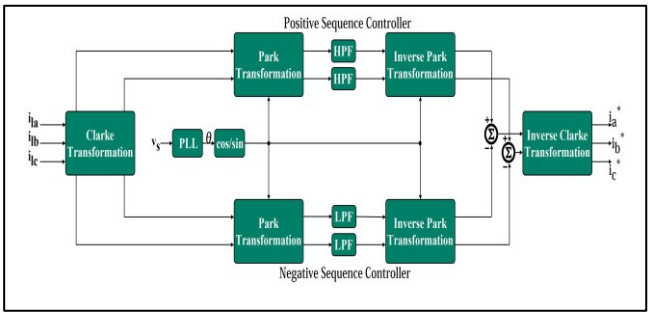

Fig. 8: Block Diagram of SRF based reference current generation scheme

V. . Simulation Results & Discussion

Here, simulation results of shunt active harmonic filter using different reference generation techniques have been shown with appropriate analysis. Simulation block diagram has been shown in Figure 9. Simulation system parameters for source, rectifier load, ripple filter and DC Link have been shown in Table I.

TABLE I. Simulation System Parameters

	Parameter	Value
Source Parameters	v_{sourc}	415 V
	f_{source}	50
Rectifier Load Parameters	L_{load}	2 mH
	C_{load}	1000
	R_{load}	10 Ω
Ripple Filter Parameters	L_{grid}	80 µH
	C_{filter}	3 µF
	$L_{decoupling}$	280 µH
DC-Link Parameters	$C_{dc1} = C_{dc2}$	(4700 * 2.5) µF
	*	700 V

v_{dc}

Figure 10 shows reference compensating currents, which contains only harmonics available in load current. Actual compensating currents track reference compensating current and are generated using continuously comparing reference compensating current & actual compensating current and error between this is given to the PI current controller and limiter (saturater) which generates sinusoidal reference signal which is compared with the two triangular carrier signals with 7 kHz switching frequency hence switching signals for switches have been generated. The frequency spectrum and three-level voltage results are shown in Figure 11 & 12, respectively. While results for IRP technique are shown in Figure 13 & Figure 14, respectively. Analysis of FFT algorithm results & IRP algorithm results are shown in Table II & Table III, respectively. As shown in Figure 12 & 15, three-level has been obtained in inverter line voltage and dc bus voltage regulation has been also obtained using dc PI controller for both techniques. As shown in Table IV, the source current THD has been reduced in SAHF using FFT algorithm and IRP algorithm compared to without using SAHF.

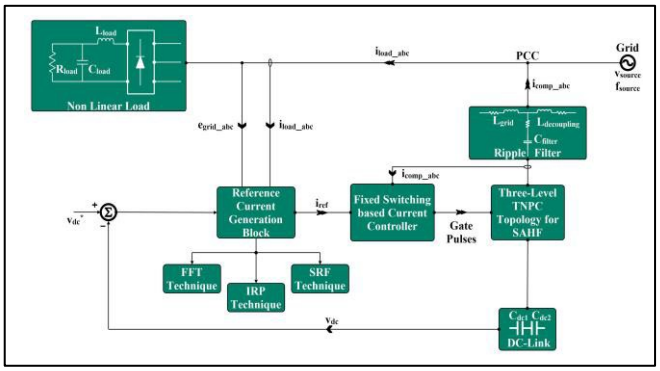

Fig. 9 Simulation Block Diagram

TABLE II. Analysis of FFT Algorithm Results

Harmonic Order	Load Current (A)	Source Current (A)
5th	13.9040	0.808
7th	4.667	0.402
11th	4.292	0.590
13th	2.079	0.525
17th	1.497	0.362
19th	1.308	0.158

TABLE III. Analysis of IRP Algorithm Results

Harmonic Order	Load Current (A)	Source Current (A)
5th	19.2600	3.500
7th	6.204	0.416
11th	4.350	0.320
13th	2.321	0.559
17th	2.341	0.227
19th	1.421	0.175

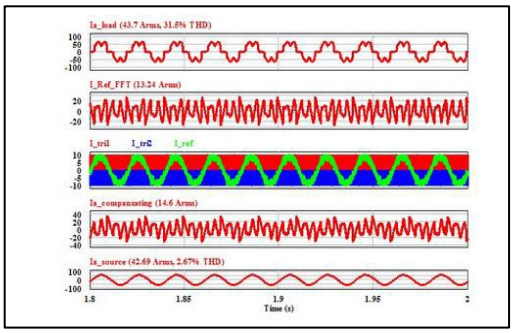

Fig. 10: FFT results for phase A–load current (Ia_load) [Y-axis: 50 A/div]; reference compensating current (I_Ref_FFT) [Y-axis: 20 A/div]; sinusoidal reference & carrier signals for switches (I_ref, I_tri1 & I_tri2) [Y-axis: 05 A/div]; actual compensating current (Ia_compensating) [Y-axis: 20 A/div]; source current (Ia_source) [Y-axis: 50 A/div]; [X-axis: 0.05 s/div]

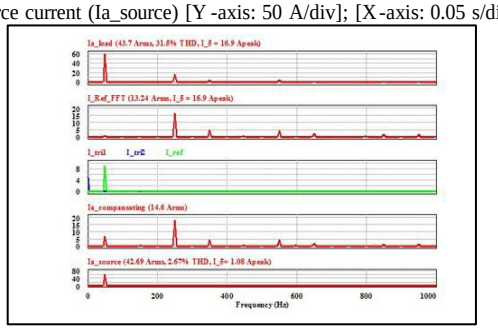

Fig. 11: Frequency spectrum of FFT results for phase A–load current (Ia_load) [Y-axis: 10 A/div]; reference compensating current (I_Ref_FFT) [Y-axis: 05 A/div]; sinusoidal reference & carrier signals for switches (I_ref, I_tri1 & I_tri2) [Y-axis: 02 A/div]; actual compensating current (Ia_compensating) [Y-axis: 05 A/div]; source current (Ia_source) [Y-axis: 20 A/div]; [X-axis: 200 Hz/div]

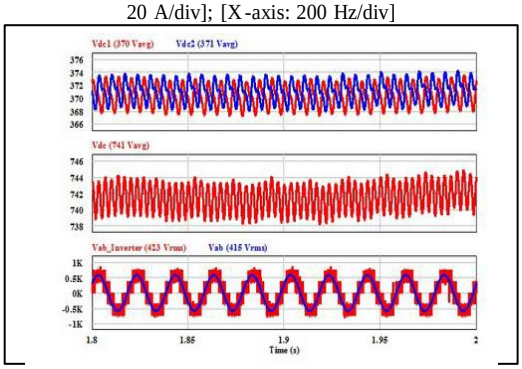

Fig. 12: FFT results–half dc-link voltages (V_{dc1} & V_{dc2}) [Y-axis: 02 V/div]; full dc-link voltage (V_{dc}) [Y-axis: 02 V/div]; inverter line voltage ($V_{ab\_Inverter}$) & source line voltage (V_{ab}) [Y-axis: 500 V/div]; [X-axis: 0.05 s/div]

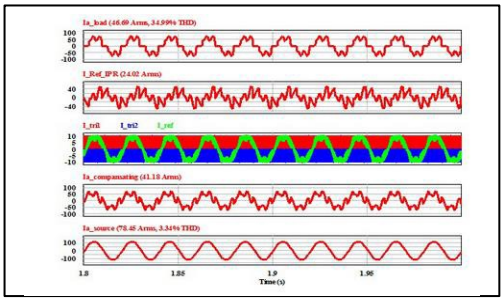

Fig. 13: IRP results for phase A–load current (Ia_load) [Y-axis: 50 A/div]; reference compensating current (I_Ref_IRP) [Y-axis: 20 A/div]; sinusoidal reference & carrier signals for switches (I_ref, I_tri1 & I_tri2) [Y-axis: 05 A/div]; actual compensating current (Ia_compensating) [Y-axis: 50 A/div]; source current (Ia_source) [Y-axis: 50 A/div]; [X-axis: 0.05 s/div]

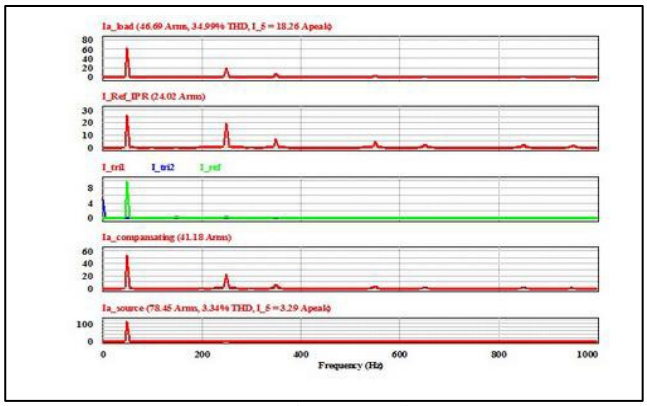

Fig. 14: Frequency spectrum of IRP results for phase A–load current (Ia_load) [Y-axis: 20 A/div]; reference compensating current (I_Ref_IRP) [Y-axis: 05 A/div]; sinusoidal reference & carrier signals for switches (I_ref, I_tri1 & I_tri2) [Y-axis: 02 A/div]; actual compensating current (Ia_compensating) [Y-axis: 10 A/div]; source current (Ia_source) [Y-axis: 20 A/div]; [X-axis: 200 Hz/div]

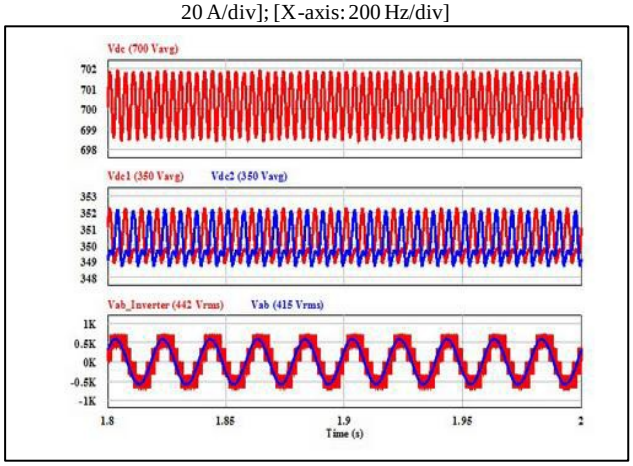

Fig. 15: IRP results – half dc- link voltages (Vdc1 & Vdc2) [Y-axis: 01 V/div]; full dc-link voltage (Vdc) [Y-axis: 01 V/div]; inverter line voltage (Vab_Inverter) & source line voltage (Vab) [Y-axis: 500 V/div]; [X-axis: 0.05 s/div]

TABLE IV. Comparative Analysis of Reference Generation Techniques

Parameter	Load Current %THD	Source Current %THD
Without using SAHF	33.5600	33.5600
SAHF using FFT Algorithm	33.5600	2.8770
SAHF using IRP Algorithm	33.5600	3.3380

VI. CONCLUSION

The source current harmonic compensation using SA HF is studied and demonstrated in the proposed work for FFT algorithm and IRP algorithm of reference compensating current generation techniques. It is clearly depicted from the results presented that the source current THD is improved through SA HF using FFT algorithm and SA HF using IRP algorithm compared to without using SA HF. Simulation of three-level SA HF using TNPC topology is done by using FFT algorithm and IRP theory based reference current generation techniques.

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