Abstract

The input/output circuits (I/O) are essential to VLSI chip design. The design quality of these circuits is a critical factor that determines the reliability, signal integrity and interchip communication speed of the chip in today's systems environment. If the package is considered a protection layer of the silicon chip, then the i/o frame containing input and output circuits can be considered as a second protection layer. Any external hazards such as a electrostatic discharge and noise should be filtered out before propagating to the external circuits for their protection. Also, some chips have to communicate with the transistor-transistor logic (TTL) or emitter-coupled logic (ECU bipolar chips, and in such cases, the input or output circuit must provide proper level shifting so that the transmitted signal contents can be correctly received or sent by the CMOS chip.

This project deals with the front end package development of IO libraries for Non Volatile Memories for different technologies. It involves understanding of IO cells specification, timing and power characterization of IO cells, threshold analysis, and generation of UNIDATA, SYNOPSYS_DC, SYNOPSYS_DP and other views. The work also involves validation of these views and final packaging of these views.