Abstract

Recently the Wavelet Transform has gained a lot of popularity in the field of signal processing. This is due to its capability of providing both time and frequency information simultaneously, hence giving a time-frequency representation of the signal. The traditional Fourier Transform can only provide spectral information about a signal. Moreover, the Fourier method only works for stationary signals. In many real world applications, the signals are non-stationary. One solution for processing non-stationary signals is the Wavelet Transform.

Currently, there is a tremendous focus on the application of wavelet Transforms, and in particular, on Discrete Wavelet Transform (DWT) for real time signal processing. This leads to the demand for efficient architectures for the implementation of DWT. These architectures are targeted for portable devices and their real-time applications, with very low power consumption and a high throughput.

The DWT can be viewed as a case of sub-band coding.

The basic building block of DWT consists of a high-pass and low-pass, followed by decimation of two. The incoming data stream is passed through the low pass and high pass filters and decimated by a factor of two. The low pass output is further passed through the similar basic building block, and the process continues until required numbers of levels have been obtained.

One of the possible VLSI architectures for the implementation of DWT is the "folded architecture". In folded architecture, the same basic building block is utilized to implement DWT with time-multiplexing. In this project work, the "folded architecture" has been used for the design of DWT. Also, the multipliers used in the architecture are based on Distributed Arithmetic, instead of the lumped ones.