Abstract

To Design high speed and low voltage analog circuits, now a days designers have started using current mode approach. It means that the individual circuit elements should interact by means of current, not voltages.

Due to this change in signal definition, Analog signal processing circuits must also be change from voltage to current mode .in this regard there is need of several ranges of current amplifier architectures with high speed and low voltage for various application.

The major advantage of current feedback amplifier is, its gain-bandwidth product which is not constant. Because of these characteristics, at present current mode approach is used for high speed amplifier design without sacrificing the gain.

The architecture implemented in this thesis is based on current conveyer. The current conveyer is basic building block used to convey current. It consists of two input terminal (High and low impedance), and two output terminals (High and low impedance). Thus it is hybrid analog building block used for all possible signal conversion, i.e.(voltage i/p-voltage o/p, current i/p-current-o/p, voltage i/p-current o/p, current i/p-voltage o/p).

Part-1 of the thesis, describes a design of low- voltage current feedback amplifiers (CFAs) by employing a second generation positive current conveyer(CCII+) followed by an operational amplifier. It provides high driving current capabilities .The current Feedback operational amplifier operates at supply voltages of ±1.8V. The Circuits exhibits a bandwidth of 40 MHz.

Part-2 of the thesis, describes a design using a negative current conveyer (CCII-The current Feedback operational amplifier operates at supply voltages of ±1.8V The Circuits exhibits a bandwidth of 10 MHz.
Part-3 of the thesis, describes a low-voltage CMOS current feedback operational amplifier (CFOA) which allows rail-to rail input/output operation. Also, it provides high driving current capabilities. The current feedback amplifier operates at supply voltages of ± 0.75V. The circuit exhibits a bandwidth of 120 MHz and a current drive capability of ±1 mA.