Design and Simulation of Different architectures of analog multiplier using sub-micron technology

By

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07MEC002

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

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Major Project

Submitted in partial fulfillment of the requirements

For the degree of

Master of Technology in Electronics and communication

By

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Institute of Technology,

Nirma University of Science and Technology,

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Certificate

This is to certify that the Major Project entitled "Design and Simulation of Different architectures of analog multiplier using sub-micron technology" submitted by Ami Patel(07mec002), towards the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and communication Engineering of Nirma University of Science and Technology, Ahmedabad is the record of work carried out by her under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Abstract

The four-quadrant multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase locked loop, modulation, detection, frequency translation, square rooting of signals, neural networks and fuzzy integrated systems.It performs linear product of two continuous signals x and y, yielding an output z = Kxy, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main metrics of performance.At present, the power consumption is a key parameter in the designing of high performance mixed-signal integrated circuit.

The main objective of this project is to analyze different architectures of analog multipliers. In this report basic types of analog multiplier architectures such as wide range analog multiplier,multiplier based on nMOS transistor,multiplier working in triode region are presented, which is widely used, and a new architecture is proposed and their performances are compared by ac analysis, dc analysis, and transient analysis,linearity error. All multiplier circuits are implemented with 0.35-μm CMOS technology with power supply voltage of 1.5V and simulated using BSIM3 modeling parameter in T-Spice(Tanner EDA) and Eldo (Menter Graphics).

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- Ami Patel

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Chapter 1

Introduction

Analog multipliers are important circuit blocks for many applications such as frequency mixers, variable frequency oscillators, adaptive filters, etc[2]. It performs linear product of two continuous signals x and y, yielding an output z = Kxy, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main metrics of performance.At present, the power consumption is a key parameter in the designing of high performance mixed-signal integrated circuit.Therefore it is necessary that analog multiplier to be used must be able to operate under a reduced supply voltage and consume low current.[6]

A Gilbert multiplier cell is first introduced Analog multiplier,which was in bipolar technology[1]. Conventional design technique for a CMOS analog multiplier circuit is based on the square-law characteristics of an MOS transistor[3].There are many analog multiplier structures already proposed using CMOS technology[2]-[6],[8]-[10]. Analog Multiplier is linear device. According to operating frequency ranges, MOS analog multiplier realization method can be classified into three categories in accordance with the operation regions of the MOS devices. For the case of low frequency applications, weak-inverted MOSFET is preferred. Triode-biased MOSFET is the best choice for the intermediate frequency applications. Finally, in the hundred of kilohertz up to megahertz frequency range, strong inversion saturated MOSFET is usually employed.

1.1 Types of multiplier

1.1.1 Digital Multiplier

Digital multiplier takes digital quantity as inputs and gives digital output bits according to input bits. As go on higher frequency performance of digital multipliers degraded as compared to analog one. So in telecommunication such as mixer, Balance modulator analog multiplier is preferred, whereas digital multipliers are preferred in digital computer or digital arithmetic systems.

1.1.2 Analog Multiplier

In electronics, an Analog multiplier is a device which takes two analog signals and produces an output which is their product. Such circuits can be used to implement related functions such as squares (apply same signal to both inputs), and square roots.

Although analog multiplier circuits are very similar to operational amplifiers, they are far more susceptible to noise and offset voltage-related problems as these errors may become multiplied. When dealing with high frequency signals, phase-related problems may be quite complex. For this reason, manufacturing wide-range general-purpose analog multipliers is far more difficult than ordinary operational amplifiers.

In most cases the functions performed by an analog multiplier may be performed better and at lower cost using Digital Signal Processing techniques. At low frequencies a digital solution is cheaper and more effective, and allows the circuit function to be modified in firmware. As frequencies rise, the cost of implementing digital solutions increases much more steeply than for analog solutions. As digital technology advances, the use of analog multipliers tends to be ever more marginalises towards higher-frequency circuits or very specialist applications.

1.2 Types of Analog multiplier

1.2.1 One Quadrant Multiplier

Inputs and Outputs both are Having one polarity. For example either both the inputs are positive or both the inputs are negative, and output will have polarity accordingly.

1.2.2 Two Quadrant Multiplier

One input have only one polarity and another input can be positive or negative and output will have polarity accordingly.

1.2.3 Four Quadrant Multiplier

Here both the inputs can be positive or negative and output will have polarity accordingly. Here two four quadrant analog multiplier's responses are simulated.

1.3 Performance Metrics of Analog Multiplier

The linearity, supply voltage, power dissipation and noise are the main metrics of performance. So, aim is to design some specific structures or topologies for the analog multiplier that have low power dissipation while at the same time keeping good linearity, low supply voltage and low noise.

Linearity error is the maximum output voltage deviated from an ideal straight line of transfer function. It is expressed in terms of error in percentage of a full scale.

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the Fundamental frequency.

power that is converted to heat and then conducted or radiated away from the device termed as Power dissipation.

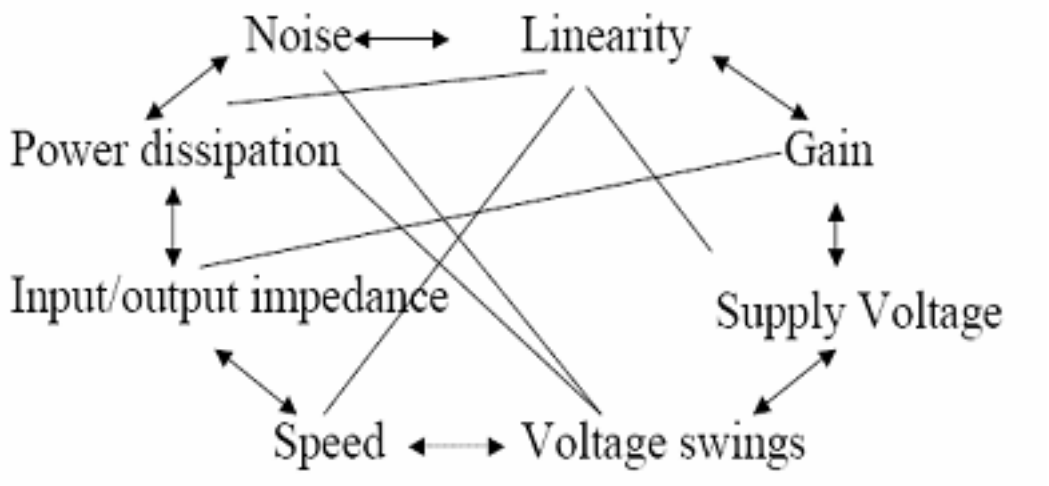

Figure 1.1: Performance matrix of analog multiplier.

Chapter 2

Different Architectures of Analog Multiplier

Analog multiplier does linear operation. Multipliers are implemented using nonlinear devices,so Depending on different nonlinearity cancelation schemes different Architectures are developed. Here four different architectures of Analog multipliers are presented. Since a single-ended configuration cannot achieve complete cancelation of nonlinearity and has poor power supply rejection ratio (PSRR), a fully differential configuration is necessary in a sound multiplier topology.

2.1 FQAM using single quadrant multiplier

The multiplier has two inputs, therefore there are four combinations of two differential signals, i.e. (x,y), (x,-y),(-x,y), (-x,-y). The topology of Fig. 2.1 is based on single-quadrant multipliers.

For Fig.2.1

$$[(X+x)(Y+y)+(X-x)(Y-y)]-[(X-x)(Y+y)+(X+x)(Y-y)]=4xy \quad (2.1)$$

2.2 FQAM using square devices

Fig. 2.2 is based on square law devices. These topologies achieve multiplication and simultaneously cancel out all the higher order and common-mode components (X and Y) based on the following equalities:

For Fig.2.2

$$[(X+x)(Y+y)^2+(X-x)(Y-y)^2-(X-x)(Y+y)^2+(X+x)(Y-y)^2]=8xy \tag{2.2}$$

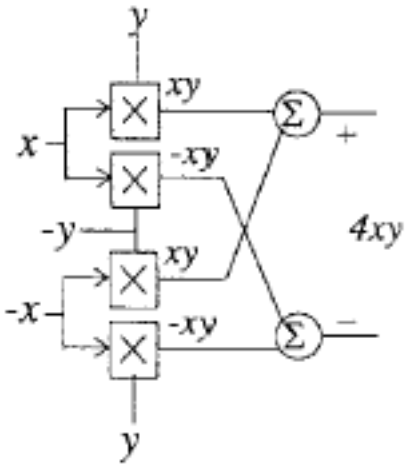

Figure 2.1: FQAM using single quadrant multiplier[2]

2.3 FQAM using Quarter-Square Algebraic Identity technique

The Quarter-Square Algebraic Identity is famous method for a multiplier implementation. There is 3 steps as shown in Fig. 2.3 and can be described below: 1. Sum and

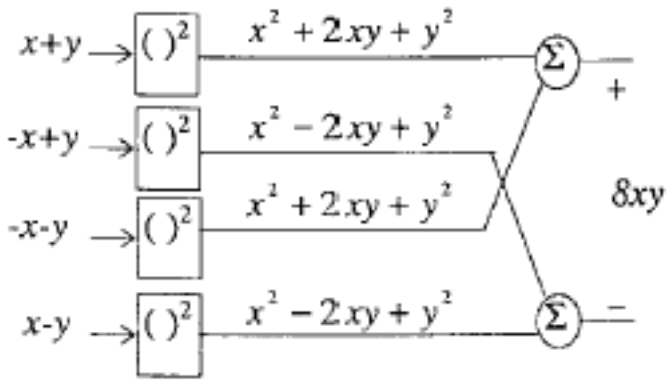

Figure 2.2: FQAM Using square devices[2]

Subtraction both inputs. 2. Taketheir results of 1st step to squaring. 3. Subtraction of 2nd step with each other that output can be express as

$$Vo = \frac{1}{4}[(V1 + V2)^2 - (V1 - V2)^2] = V1V2 \tag{2.3}$$

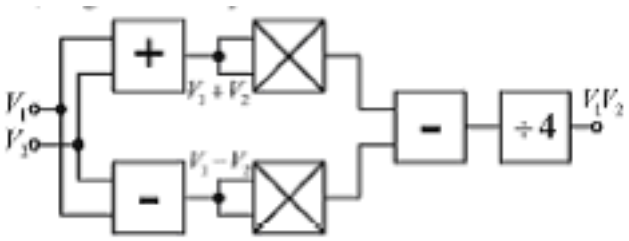

Figure 2.3: The Quarter-Square Algebraic Identity Technique[5]

2.4 Block diagram of proposed architecture

A CMOS four-quadrant multiplier can be used to multiply two bipolar signals, x and y. This type of multiplier has been used to build many analog circuits, such as modulators and adaptive filters.

The block diagram of the proposed multiplier is shown in Fig.2.4. The first stage

consists of four identical adders producing the sum of their respective input signals. These outputs are then combined in the second stage to form the multiplication function.

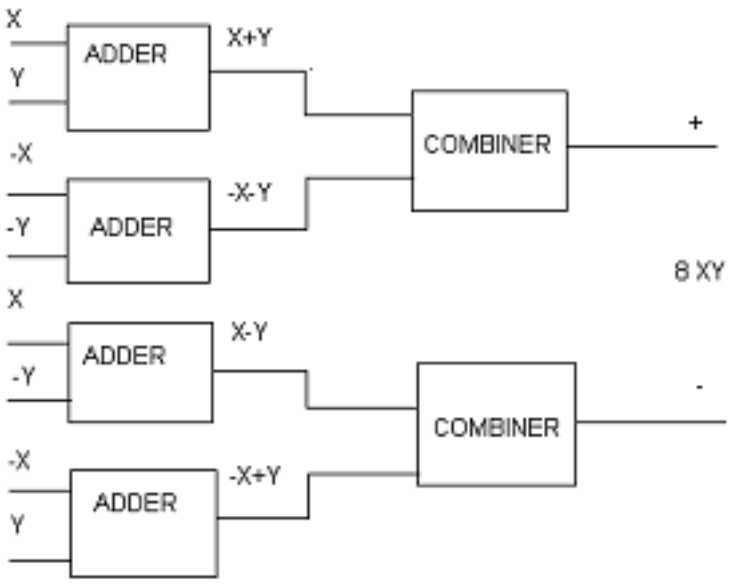

Figure 2.4: Block diagram of proposed multiplier

2.5 Specifications of Analog Multiplier

Analog Multiplier specification includes supply voltage, technology, input voltage range, bandwidth, linearity error and total harmonics distortion.

Power Supply	±1V - ±1.5V
technology	0.35µm
Input voltage range	±1V - ±1.5V
Bandwidth	10-MHz - 150MHz
Linearity Error	<2%
Total Harmonics Distortion	<0.7%

Table I: Specifications

Chapter 3

Analog Multiplier based on Architecture 1

An Analog multiplier is an important sub circuit for many applications such as adaptive filters and frequency modulators. A variety of multipliers have been designed for different optimization objectives A general idea behind these designs is to use electronic devices to process the input signals, followed by a cancellation/minimization of errors caused by nonlinearity of the devices. Due to the popularity of advanced CMOS technology, MOS transistors are a natural choice for the devices, while differential circuit structure is widely used for nonlinearity cancelation.

3.1 Four quadrant analog multiplier

For CMOS analog multiplier design, most transistors are biased to operate in the saturation region where the drain current Id of the device is given by

$$Id = \frac{1}{2}[K(Vgs - Vth)^2(1 + \lambda Vds)] \tag{3.1}$$

where K=μ0C0xW/L is the transconductance parameter, Vth is the threshold voltage of the device, and λ the channel- length modulation effect for long channel devices.

It can be seen that in the saturation region, low power consumption requires a small value of VGS which leads to a reduced input range. By biasing the transistors to operate in the linear region instead, one can reduce the drain current while keeping a relatively large input range. The drain current in linear region is given by

$$Id = K[(Vgs - Vth)Vds - \frac{1}{2}Vds^2], (Vgs - Vth) > Vds \tag{3.2}$$

The drain current can remain a proper value by decreasing VDS , keeping the power dissipation at same level. Considering the fact that pMOS transistors need less drain current with larger overdrive voltage (VGS- VTH) compared with nMOS transistors, pMOS transistors are preferably chosen in the input terminals for operations in either saturation or linear region.

Multiplier structure is shown in Fig.3.1. Here most transistors are working into linear region and use pMOS devices to operate in saturation region to provide low power. Multiplier consist of 4 pMOS transistors (P1- P4) operating in saturation region and 8 nMOS transistors (N1-N4 and M1-M4) operating in linear region.

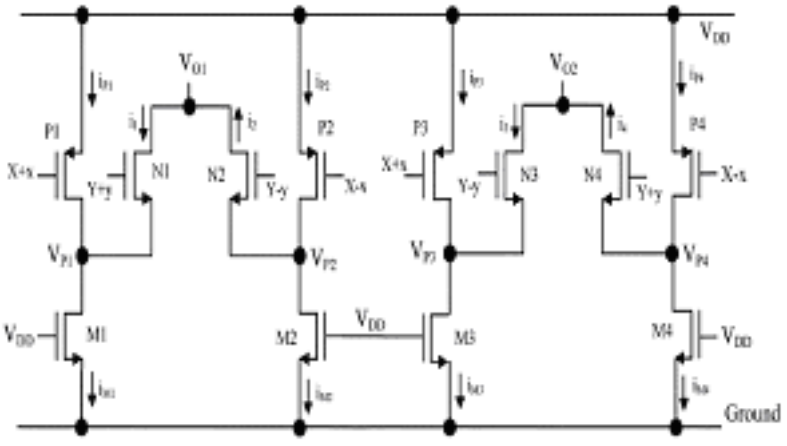

Figure 3.1: wide bandwidth FQAM[4].

Here the upper case letters, X and Y, represent common-mode (dc bias) components, while the lower case letters, x and y , represent small (input) signals. Assuming that all transistors in Fig. 3.1 are biased to operate in proper (linear or saturation) region, we can prove that this topology achieves multiplication, i.e.,

$$V_{01} - V_{02}\alpha \ fracK_P K_N K_M xy \tag{3.3}$$

A potential advantage of this structure is that a larger input range can be obtained with only pMOS transistors in their saturation region. In other words, for the same input range, a lower supply voltage can be used. The transistors P1-P2 in saturation region reduce VP1-VP4, pushing up the input range for signal y. For a given DC bias, the output range of the multiplier also depends on KP/(KN KM) which has a maximum value in order to keep M1-M4 and N1-N4 in linear region. While exhibiting the ability of canceling nonlinearity, the circuit still has a linearity error due to temperature, body effect of transistors N1-N4, and possible device mismatches. The required bias conditions for Fig. 3.1 can be written as

$$V_P - |V_{THP}| \leq X + x \leq V_{DD} - |V_{THP}|, For P1 - P4. \tag{3.4}$$

$$Y \pm y \geq V_o + V_{THN}, For N1 - N4. \tag{3.5}$$

The bias voltage of M1-M4 is chosen to be VDD in order to keep VP as low as possible, allowing P1-P4 for a larger input range. Typical values to be used are: VDD=1.5V,X=0.5V,Y=1.5V, VTHP=0.75V,and VTHN=0.6V. For instance, when all transistors have same size of W/L=0.8 μm/0.35 μ m with, both and turn out to be 16.1 mV.

MOSFETs	*W/L(μm)*
M1-M4	0.8/0.35
P1-P4	0.8/0.35
N1-N4	0.8/0.35

Table I: Aspect Ratio of Analog Multiplier in Fig. 3.1

3.2 Simulation Results

The multiplier circuits of Fig. 3.1 has been simulated using TSPICE with model parameters for a 0.35μm CMOS process (Vtn 0.5V and Vtp - 0.6V) under the same single supply voltage of 1.5V. Transistor channel widths (W) and channel lengths (L) of the multiplier circuit in Fig. 3.1 were set as listed in Table I.DC characteristics of multiplier is shown in Fig. 3.2, here Vx is varied from -1 to 1 in step of 0.1V and Vy from 1.3 to 1.7 in step of 0.1V. Linearity error of the multiplier comes out to be 3.23

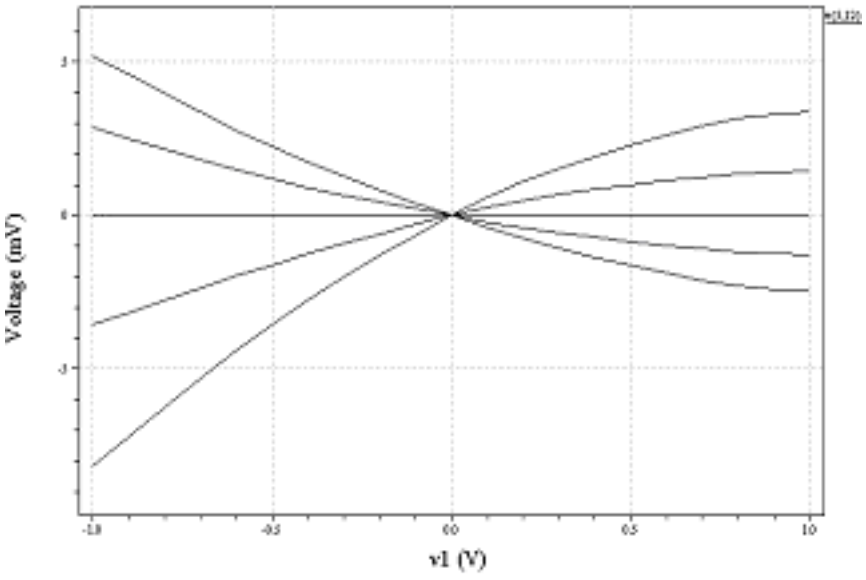

Figure 3.2: DC Characteristics of multiplier.

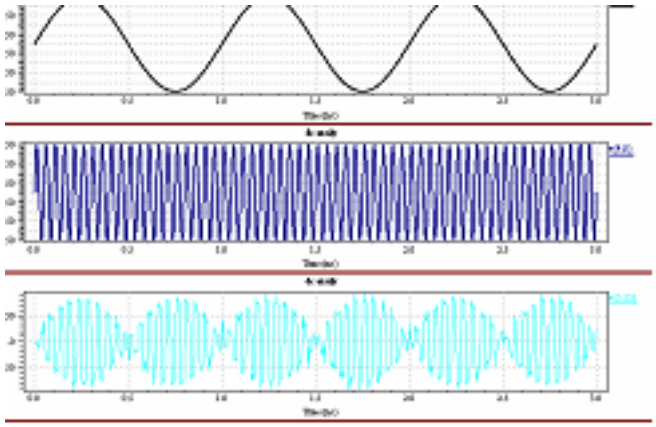

Figure 3.3: Transient response of multiplier.

Transient characteristic of the multiplier is shown in Fig. 3.3 with one signal of 1kHz and another signal of 20kHz and we get the modulated output. An AC characteristic of the multiplier is shown in Fig. 3.4 and Band width of the multiplier is 1.9GHz.

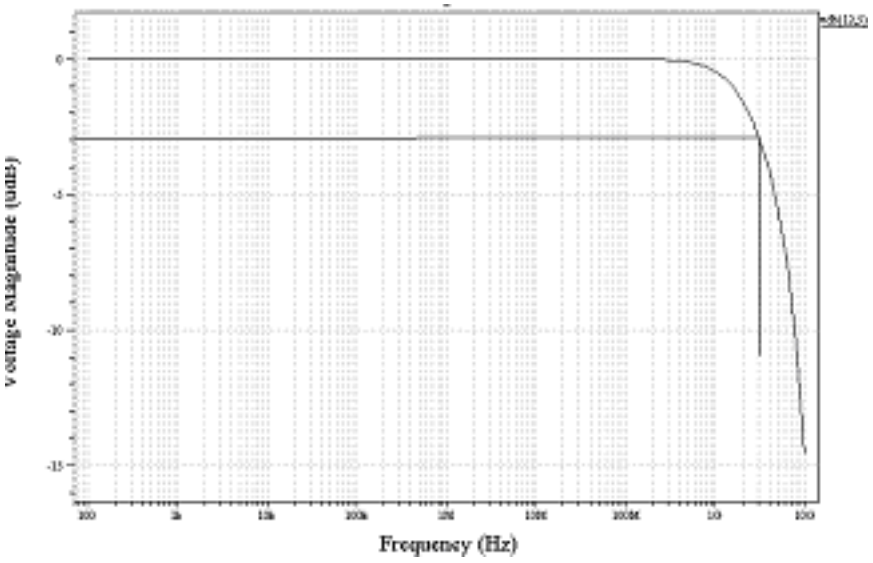

Figure 3.4: Frequency response of multiplier.

Chapter 4

Analog Multiplier based on Architecture 2

Different Architectures of Analog Multipliers are shown in chapter 2. Here in this chapter Analog Multiplier based on Square devices are shown. Once again Square based four quadrants Analog Multiplier block diagram is shown in Fig 4.1.

4.1 Block Diagram

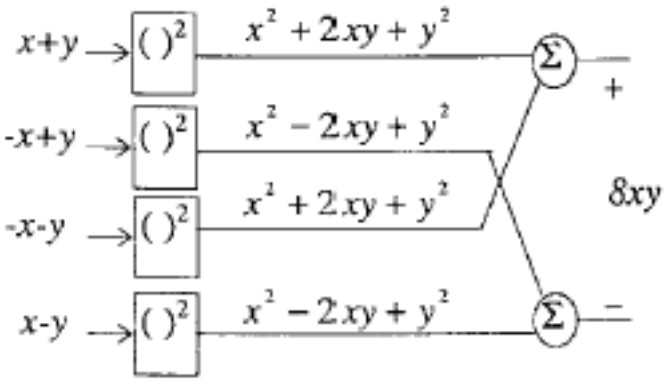

Figure 4.1: FQAM using square devices[2].

4.2 Circuit Realization

According to operating frequency ranges, MOS analog multiplier realization method can be classified into three categories in accordance with the operation regions of the MOS devices. For the case of low frequency applications, weak-inverted MOSFET is preferred. Triode-biased MOSFET is the best choice for the intermediate frequency applications. Finally, in the hundred of kilohertz up to megahertz frequency range, strong inversion saturated MOSFET is usually employed although caution should be taken on several second - order effect such as channel length modulation and mobility degradation.

four-quadrant analog multiplier is described in Fig 4.2. It is composed of compact simple CMOS circuits, including common source, common drain and differential pair circuits, which can be operated under a low-voltage supply. The squarer-based four quadrant analog multiplier topology is exploited and modified to be able to reject signal dependent offsets and can be simply constituted by the above simple sub-circuits in compact structure. Moreover, unlike the FVF-based multipliers, feedback path and the threshold related limitation are not encountered in this circuit. Therefore, the proposed multiplier can be operated by consuming low power and provides high linearity and bandwidth.

we will consider first the case where M1 - M12 are saturated in strong inversion and M1-M8 are identical, by using SPICE level 49 model, it is straightforward to show that

$$I_{01} = K_{9-12}[(V_{X1} - V_{Y1} + V_B)^2 + (V_{X2} - V_{Y2} + V_B)^2] \tag{4.1}$$

and

$$I_{01} = K_{9-12}[(V_{X1} - V_{Y2} + V_B)^2 + (V_{X2} - V_{Y1} + V_B)^2] \tag{4.2}$$

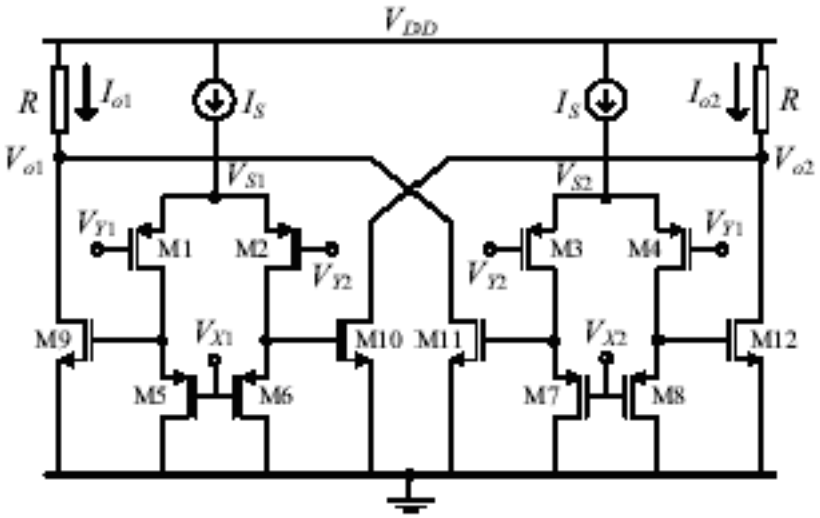

Figure 4.2: Analog Multiplier based on Architecture-2[6].

MOSFET	W [µm]	L [µm]
M1-M4	0.7	2
M5-M8	3	0.7
M9-M12	2	0.5

Table I: MOSFETs dimentions of Fig. 4.2

Where K9-12 is the transconductance parameters of M9 - M12. VB = Vs - Vtn in which Vs = Vs1 = Vs2 and Vtn is the threshold voltages of M9 - M12. Substituting above equations in to Vod = (Io1 - Io2) R, we have

$$V_{od} = 2K_{9-12}(V_{X1} - V_{X2})(V_{Y1} - V_{Y2}) = 2K_{9-12}V_{xd}V_{yd} \tag{4.3}$$

It can be shown that in the case where M1 - M4 are not identical to M5 - M8, above equation will become

$$V_{od} = 2\sqrt{\frac{K_{1-4}}{K_{5-8}}}K_n R V_{xd} V_{yd} \tag{4.4}$$

Now we obtain a multiplication function from this circuit and its conversion gain can be adjusted via transistor geometries and the load resistor.

4.2.1 Simulation Results

Fig. 4.3 shows the simulated DC transfer characteristics of the multiplier when Vyd is continuously swept from -0.4V to 0.4V while Vxd was step from -0.4V to 0.4V with 0.1V step size. This graph illustrates the circuit allows four-quadrant operation and 0.4V signal amplitude can be applied for both input.

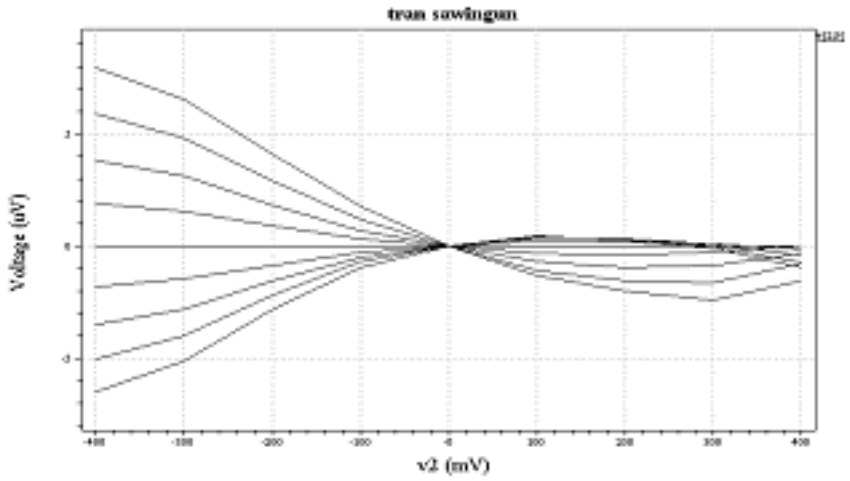

Figure 4.3: DC Characteristics of multiplier in Fig. 4.2

To demonstrate the application of the multiplier as a balance modulator, two sinusoidal voltages were applied to the circuit where by Vyd was a 200-kHz carrier signal with peak amplitude of 0.4V and Vxd was a 2-kHz modulating signal with the same amplitude. The simulated output waveform is shown in Fig. 4.4.

Fig. 4.5 shows the simulated AC response of the multiplier. It can be seen that pass-band response of the multiplier about 100 MHz.

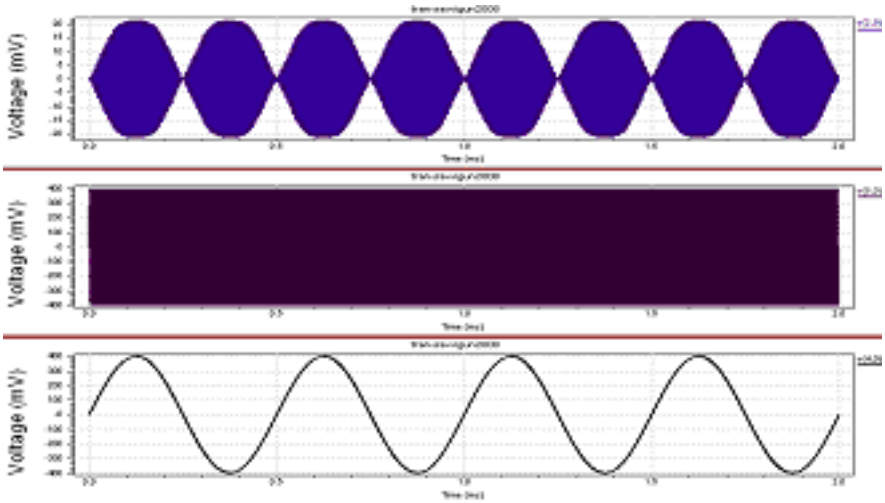

Figure 4.4: Transient response of multiplier in Fig. 4.2

4.3 Four-Quadrant Analog Multiplier Using Triode-MOSFETs

Using MOSFET in triode region is considered as a good candidate for realizing the analog multiplier due to high linearity and low level of bias voltage. Therefore several architectures of the triode-multiplier have been proposed [2], [8]. The multiplier circuit provides wide input linear range but unfortunately a threshold mismatch problem is occurred. To eliminate mismatched problem, the triode multiplier using regulated cascade circuits [4] is developed, but it uses higher power supply, which is not suitable for Low power applications.

Analog multiplier realized by using low voltage cell called "flipped voltage follower"which has been employed in [9] and can be operated under 1.5V supply, to coupling input signal into the low impedance node of the multiplier core for avoiding loading effect. Then obtain a four quadrant analog multiplier without any mismatched problem and can be properly operated under low voltage supply.

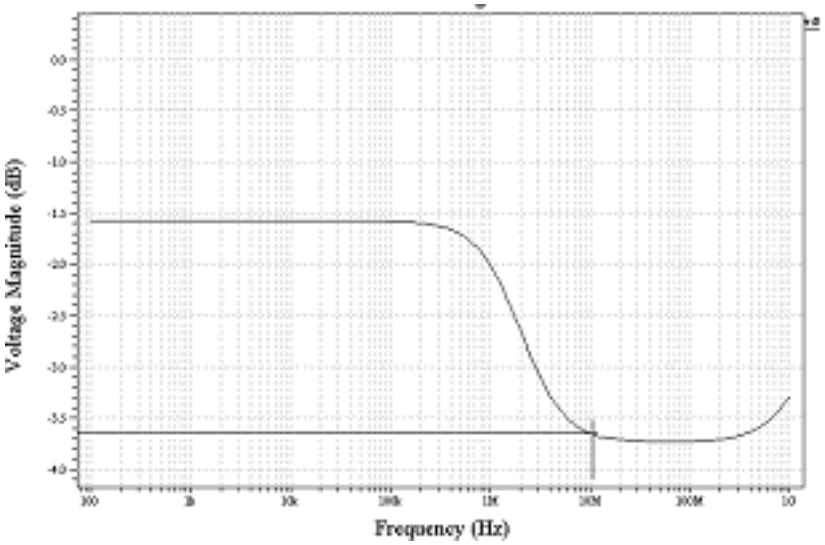

Figure 4.5: Frequency response of multiplier in Fig. 4.2

4.3.1 PMOS Transistor operated in Triode region

The main circuit which is used for realizing a four quadrant analog multiplier is shown in Fig. 4.6. It comprises a pair of PMOS transistors (MX and MY). Their body terminals are connected to VDD results in balanced physical structure. Thus, the drain current can flow in bi-direction either from drain to source or from source to drain terminals. Usually the directions of the current depend on a potential of voltage between each terminal. Considering the circuit in Fig. 4.6, under the condition that

$$V_{sg} > |V_{tp}| \tag{4.5}$$

and

$$V_{sd} < V_{sg} - |V_{tp}| \tag{4.6}$$

, where Vtp is the threshold voltage of PMOS transistor, Vsg the different voltage between source and gate terminals Vsd is the different voltage between source and drain terminals.

Referring to Fig. 4.6, it is obvious that VSD= V3 - V4 ,Vsgx = V3 - V1 and Vsgy

= V3-V2. Then drain current of each transistor can be expressed as

$$I_{Dx} = \beta_x(2V_{31}V_{34} - 2|V_{tp}|V_{34} - V_{34}^2) \tag{4.7}$$

and

$$I_{Dx} = \beta_y(2V_{32}V_{34} - 2|V_{tp}|V_{34} - V_{34}^2) \tag{4.8}$$

,where β= 0.5μpCox (W/L) is the process Tranconductance parameter.

Realizing multiplication function can be done by setting dimension of each transistor to satisfy the condition that βx= βy= β and subtracting the drain currents in above equations yields

$$I_{out} = I_{DX} - I_{DY} = 2\beta V_{12}V_{34} \tag{4.9}$$

It can be seen that the output current appeared in above equation is in form of a multiplication function between V12 and V34.

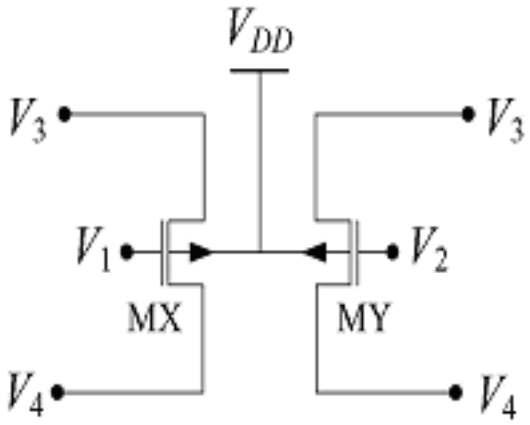

Figure 4.6: A pair of PMOS transistor biased in triode region[15].

4.3.2 Flipped Voltage Follower

However, since the currents are conducting impedances at the source-drain terminals become low, the signals V3 and V4 cannot be directly applied. For avoiding loading effect and trying to reduce voltage supply, a Flipped Voltage Follower (FVF) is employed for buffering. The operating principle of FVF will be briefly described as follows.

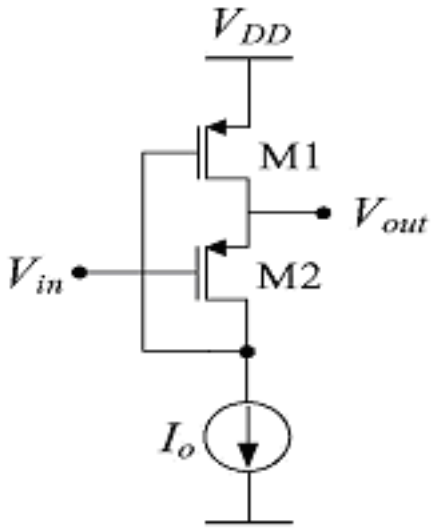

Figure 4.7: Flipped voltage follower[15].

A circuit cell which is known as Flipped Voltage Follower (FVF) is shown in Fig. 4.7. It consists of PMOS transistors M1 and M2 which are biased by a constant current source IO. From the circuit arrangement, it is evident that this circuit can be operated under a supply voltage of Vsg + Vsd(Sat) such that it is popularly used in low voltage applications. Since an inherent feedback loop contained in the circuit structure, output impedance of this circuit is forced to be very low as 1 / gm1gm2r02, typically is in the order of ten ohms.

4.3.3 Four quadrant Analog multiplier

Fig. 4.8 shows the four quadrant analog multiplier circuit which is constituted by connecting a pair of PMOS in Fig. 4.6 to the FVF cell (M1-M6) in Fig. 4.7. The FVFs are used here for two functions, first for buffering voltages V3 and V4 to the source and drain terminals of MX and MY, respectively. Second, sensing the drain current IDX and IDY and copying them to be output currents pass through unity gain current mirrors M1, M7 and M5, M8. Both drain currents are converted to be a differential output voltage by load resistors R in form of the relation that

$$V_{out} = V_{01} - V_{02} = R(I_{DX} - I_{DY}) \tag{4.10}$$

substituting value of IDX-IDY

$$V_{out} = 2\beta R V_{12} V_{34} \tag{4.11}$$

Here, an offset-free four quadrant analog multiplier is obtained. Its gain of the circuit can be adjusted by the load resistor R and the dimensions of each MOS via the process transconductance parameter β.

The multiplier circuit in Fig. 4.8 was designed and simulated using TSPICE for 0.13 μm CMOS process parameter with main parameters of Vtn=0.02 and Vtp = -0.22V. The constant current sources Io, are replaced by simple current mirrors circuits and set to be 5A for biasing all FVF circuits. The load resistors were set to be 50 kΩ. Supply voltage VDD and an input common mode voltage were set to be, 1.2V, and 0.1V, respectively. Quiescent power consumption of an overall multiplier circuit is 46.4 μW.

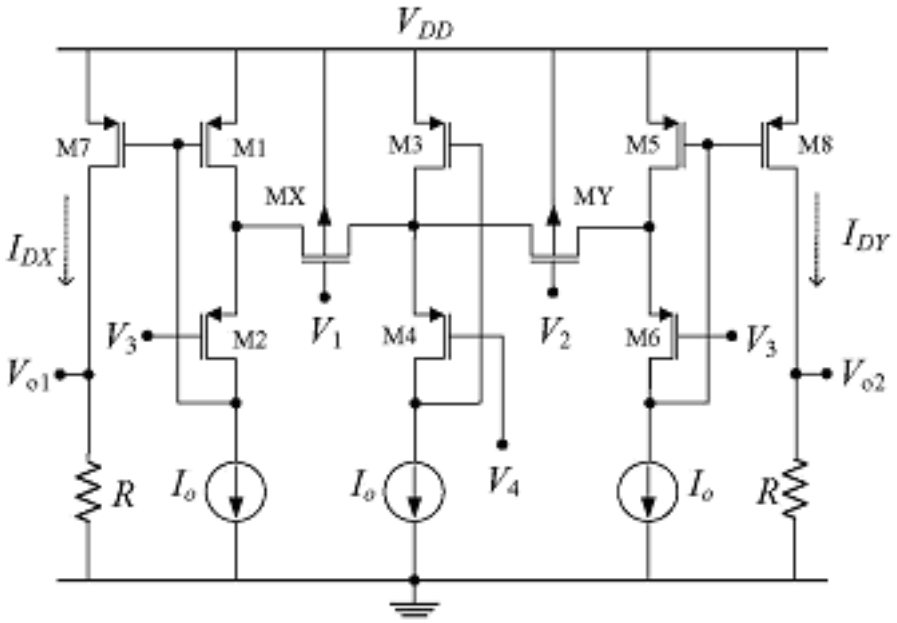

Figure 4.8: Four quadrant analog multiplier circuit[15].

MOSFETs	W/L(μm/μm)
MX,MY	0.4/1.2
M1-M6	3/0.2
M7,M8	2/0.2

Table II: Dimensions of MOSFETs in Fig. 4.8

4.3.4 Simulation Results

Fig. 4.9 shows simulated DC transfer characteristics of the proposed multiplier, where V34 was varied from -400 mV to 400 mV by sweeping V12 from -400 mV to 400 mV with 100 mV step size. Similar results were obtained by interchanging V12 and V34.Simulation is carried out in T-Spice Tanner EDA tool.

Fig. 4.10 shows simulated AC responses of the multiplier for various gains set by sweeping V12 from 100 mV to 400 mV with 100 mV step size. It can be seen that the bandwidth is higher than 50 MHz for all gains.

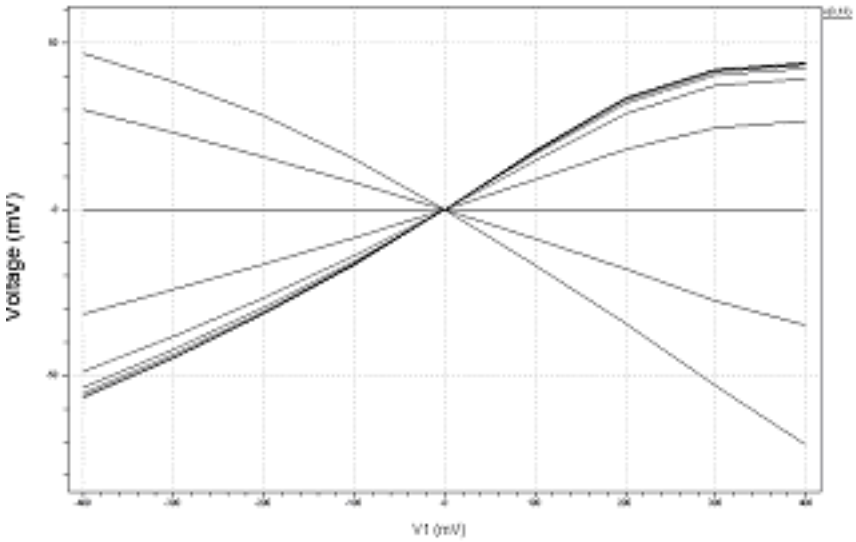

Figure 4.9: DC characteristics of analog multiplier in Fig. 4.8

Time domain representations of the multiplier which was applied as frequency doublers and amplitude modulator are shown in Fig. 4.11 and Fig. 4.12.

For the frequency doublers, both input were applied by 400mV, 1 kHz-sinusoidal signal and the result has shown in Fig. 4.11.

For amplitude modulation, a 400mV, 1 kHz-sinusoidal modulating V12 and 400mV, 25 kHz-sinusoidal carrier signal V34 were applied at the inputs, the result shows in Fig. 4.12.

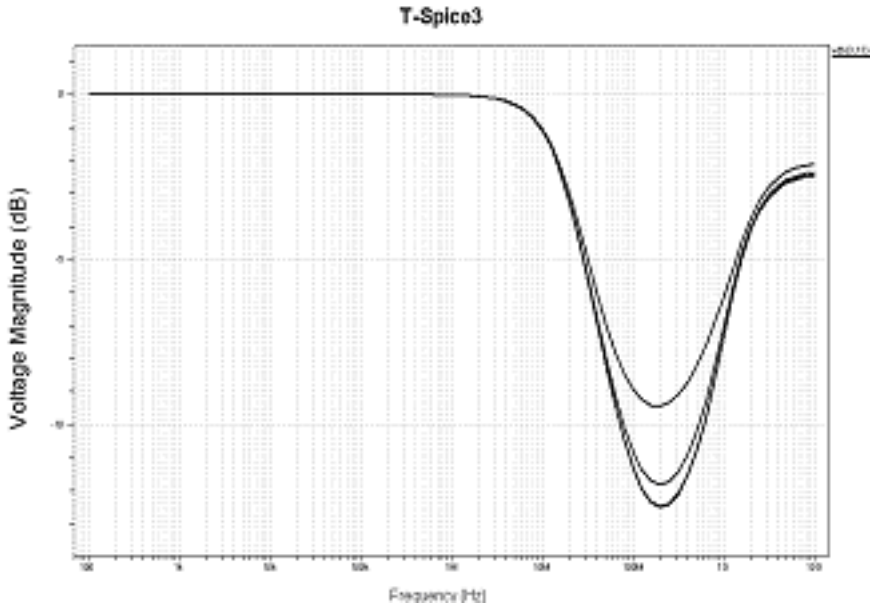

Figure 4.10: AC characteristics of analog multiplier in Fig. 4.8

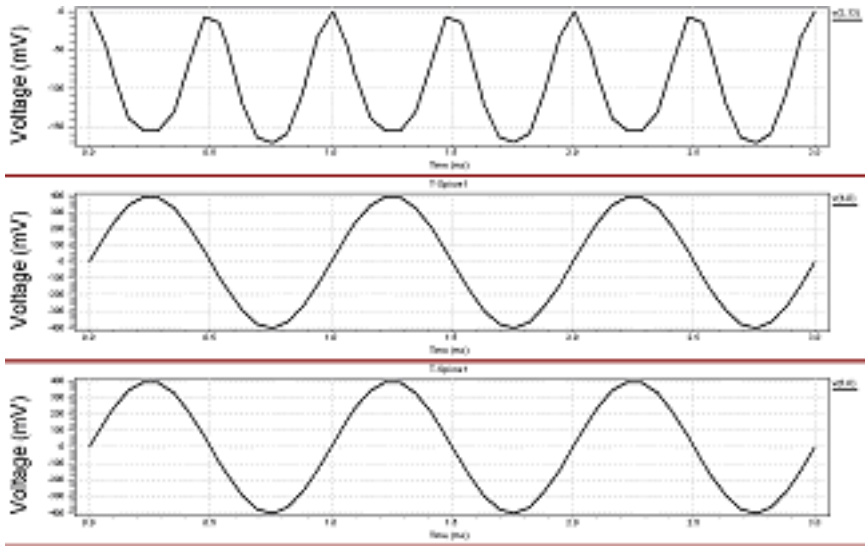

Figure 4.11: analog multiplier working as frequency doublers.

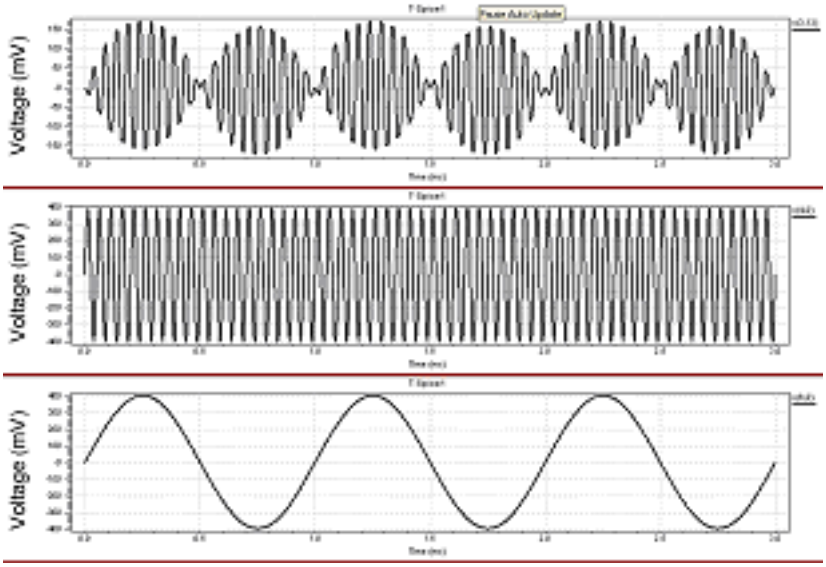

Figure 4.12: analog multiplier working as amplitude modulator.

Chapter 5

Analog Multiplier based on Architecture 3

The multiplier circuit is very useful and can be applied to any analog signal processing building blocks as well as analog filter, frequency doublers, modulator etc. Multiplier circuit shown in this chapter uses a Quarter-Square Algebraic Identity technique. It consists of 2 shunt-feedback buffer circuits for bias to their squaring transistors and 2 voltage attenuator circuits. The achieved dynamic range is reaching power supply about +1.5V. The good performances are obtained such as high band-width, high linearity and low THD.

5.1 Block Diagram

Block Diagram of Quarter-Square Algebraic Identity Technique based multiplier is shown in Fig. 5.1.

The Quarter-Square Algebraic Identity is famous method for a multiplier implementation. There are 3 steps as shown in Fig. 5.1 and can be described below:

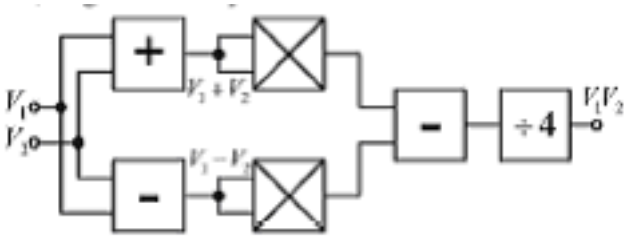

Figure 5.1: The Quarter-Square Algebraic Identity Technique[5].

1. Sum and Subtraction both inputs. 2. Take their results of 1st step to squaring. 3. Subtraction of 2nd step with each other that out can be express as

$$Vo = \frac{1}{4}[(V1 + V2)^2 - (V1 - V2)^2] = V1V2 \tag{5.1}$$

5.2 Wide range Analog Multiplier Circuit

5.2.1 The Active Attenuator circuit

The voltage attenuator circuit is shown in Fig. 5.2. The transistors M1 and M2 are operated in ohmic and saturation region, respectively. The output voltage equation can be written

$$V_o = [1 - \sqrt{\frac{(W/L)_1}{(W/L)_1 + (W/L)_2}}](V_i + |V_{TP}| - V_{DD}) + V_{DD} \tag{5.2}$$

Suppose that, the aspect ratio of M1 and M2 are defined to ((W/L)2 = 3(W/L)1), output voltage can be written as

$$V_o = \frac{(V_i + |V_{TP}| - V_{DD})}{2} \tag{5.3}$$

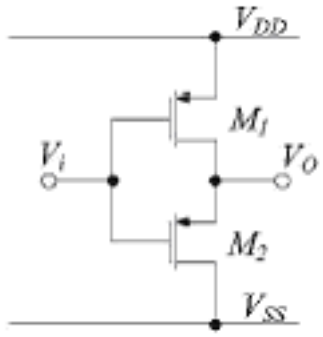

Figure 5.2: The PMOS voltage attenuator circuit[5].

Shunt -Feedback Buffer Circuit

The Fig. 5.3 shows shunt-feedback buffer circuit. It contains the 2 current sources and 3 transistors. The transistor M1 is using for supply its source voltage, M2 using for supply current at node Vo. The transistors are operated in saturation region. The current of both transistors can be written as

$$I_{D1} = k_{N1}(V_X - V_o - V_{TH})^2 \tag{5.4}$$

$$I_{s2} = k_P(V_{SG} - |V_{TP}|)^2 \tag{5.5}$$

where

$$k_P = \frac{\mu_N C_{OX}}{2}(W/L), \tag{5.6}$$

$$k_N = \frac{\mu_N C_{OX}}{2}(W/L) \tag{5.7}$$

VTN and VTP are threshold PMOS transistors, respectively.

Consider transistor M1, the current source I1 is drain current while Vx is applied

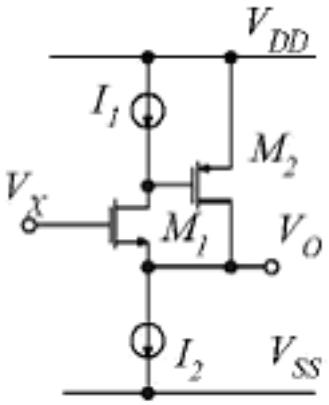

Figure 5.3: The Shunt-Feedback Buffer Circuit[5]

for gate voltage. The output voltage can be obtained by source of M1. The positive and negative load-current are done by M2 and I2, respectively in order to regulated output voltage. The achieved output voltage can be express as

$$V_o = V_X - \sqrt{\frac{I_1}{k_N}} - V_{TH} \tag{5.8}$$

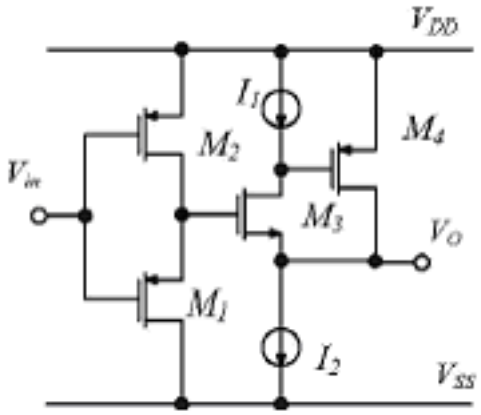

Figure 5.4: Developed shunt-feedback buffer circuit[5].

Suppose that, the active-attenuator gain is 0.5 and connected to shunt-feedback buffer circuit as shown in Fig. 5.4. The output voltage of developed shunt-feedback

buffer circuit can be obtained to

$$V_o = ((V_i + |V_{TP}| + V_{DD}) \div 2) - \sqrt{(I_1) \div k_N} - V_{TN} \tag{5.9}$$

5.2.2 Multiplier Circuit

The differential squaring circuit is described as in Fig. 5.5.

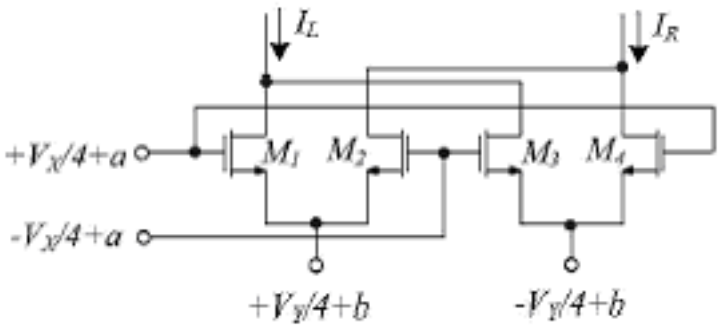

Figure 5.5: The multiplier using Differential Squaring Circuit[5].

The input voltage is applied at gate and source of each transistor that operated in saturation region. From principles above, the output of shunt-feedback buffer in Fig. 5.4 and active attenuator in Fig. 5.2 are used to applied as input of differential squaring circuit.The drain current of each transistors can be written as

$$I_{D1} = \frac{\mu C_{OX}}{2}(W/L)[((V_x \div 4) + a) - ((V_y \div 4) + b) - V_{TH}]^2 \tag{5.10}$$

$$I_{D2} = \frac{\mu C_{OX}}{2}(W/L)[((-V_x \div 4) + a) - ((V_y \div 4) + b) - V_{TH}]^2 \tag{5.11}$$

$$I_{D3} = \frac{\mu C_{OX}}{2}(W/L)[((-V_x \div 4) + a) - ((-V_y \div 4) + b) - V_{TH}]^2 \tag{5.12}$$

$$I_{D4} = \frac{\mu C_{OX}}{2}(W/L)[((V_x \div 4) + a) - ((-V_y \div 4) + b) - V_{TH}]^2 \tag{5.13}$$

Where

$$a = (|V_{TP}| + V_{DD}) \div 2 \tag{5.14}$$

and

$$b = (|V_{TP}| + V_{DD} \div 2) - \sqrt{I_1 \div k_N} - V_{TN} \tag{5.15}$$

The differential output of differential squaring circuit can be realized in order to a multiplier function. The differential output current is obtained as

$$I_o = (I_{D1} + I_{D3}) - (I_{D2} + I_{D4}) = \frac{\mu C_{ox}}{8}(W/L)V_X V_Y \tag{5.16}$$

A complete wide-range analog multiplier can be constructed by above principle as shown in Fig. 5.6.

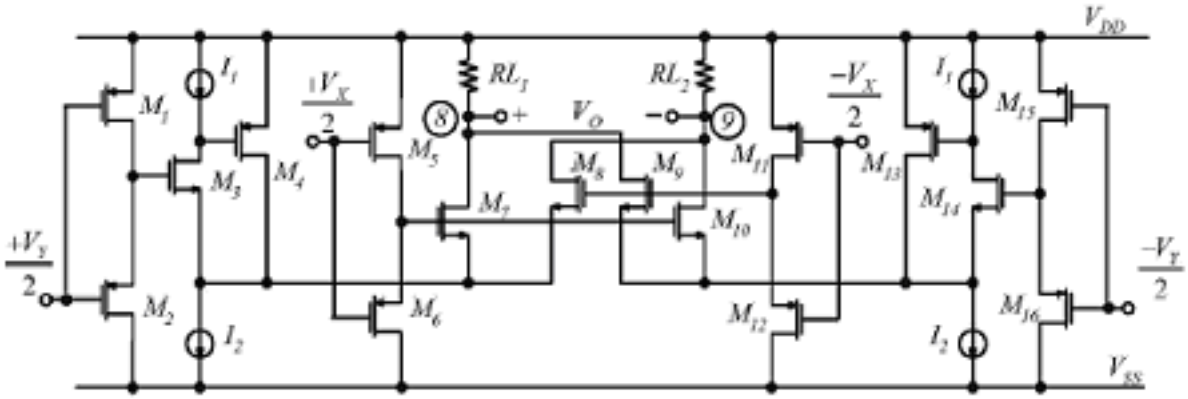

Figure 5.6: The complete of wide-range analog multiplier circuit[5].

Transistor	Aspect Ratio
M1, M3, M5, M11, M14, M15	1μm/1μm
M2, M6, M12, M16	3μm/1μm
M4, M13	70μm/1μm
M7, M8, M9, M10	1μm/2μm

Table I: Transistor Dimentions for Fig. 5.6

5.2.3 Simulation Results

The transistors aspect ratios for multiplier in Fig. 5.6 have shown in table I. The current sources I1 and I2 are 70μA and 210μ A, respectively. The power supply of given circuit is +1.5V and 5kΩ load connected as resistance. The dc characteristic of the multiplier is shown in Fig.5.7.

Amplitude modulated signal is shown for information signal of 1k-Hz and carrier of 50kHz, in Fig. 5.7. An AC characteristic of the multiplier is shown in Fig. 5.10 and Bandwidth comes out to be 20 MHz.

Dc characteristics is shown in Fig. 5.8 with one input varied in range -1V to 1V in step of 0.5V and another input varied in range -1.5V to +1.5V.

5.3 Four-Quadrant Analog Multiplier Using NMOS Transistor

An analog multiplier is an importance basic building block for the design of analog nonlinear function circuits. Usually, the variable transconductance technique which

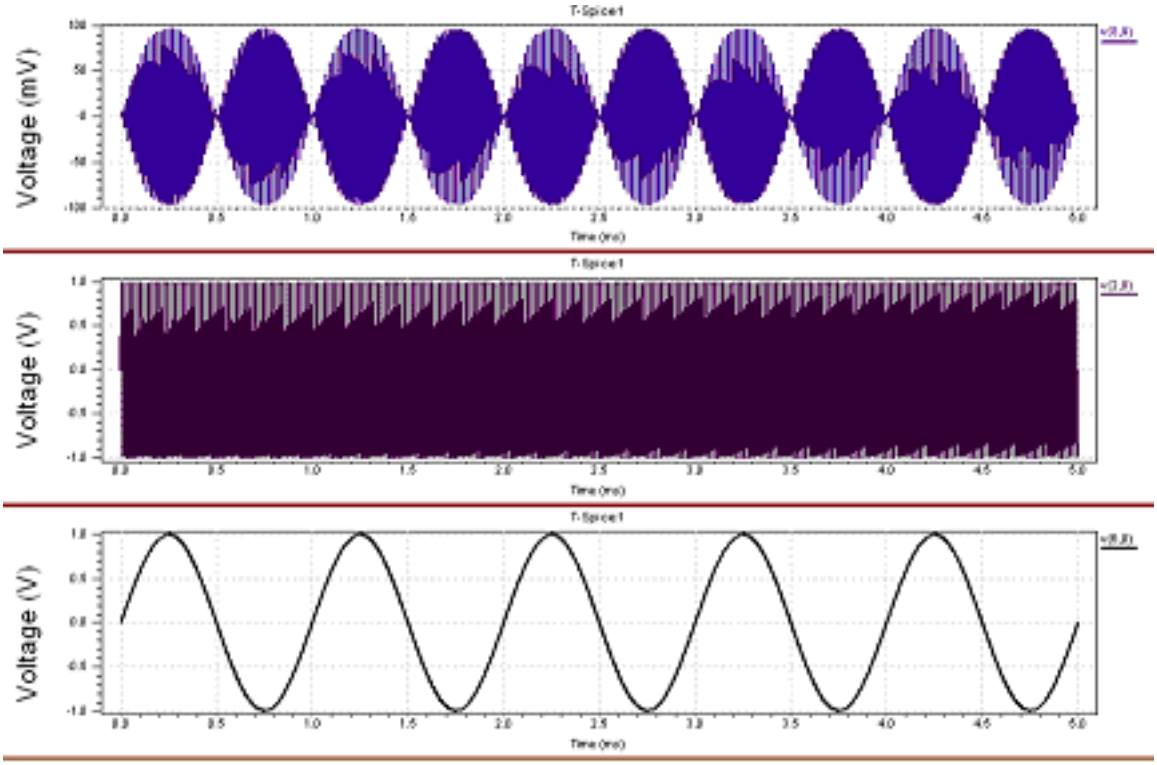

Figure 5.7: Amplitude Modulation.

operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies [1], [3]. The other approaches in CMOS technology are that based on square-law characteristics of MOS transistor which are biased in saturation region [11], [12], and that based on the current voltage characteristics of MOS transistor in the non saturation region [13]. Unfortunately, all the mentioned techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, or occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation. Only few types of the multipliers that can produce the output voltage without the use of resistors [14]. The multiplier described here uses the non-linear characteristic of the NMOS differential amplifier based upon the quarter square algebraic identity. But, however, the circuit also does not require resistors to obtain the output signal in voltage form.

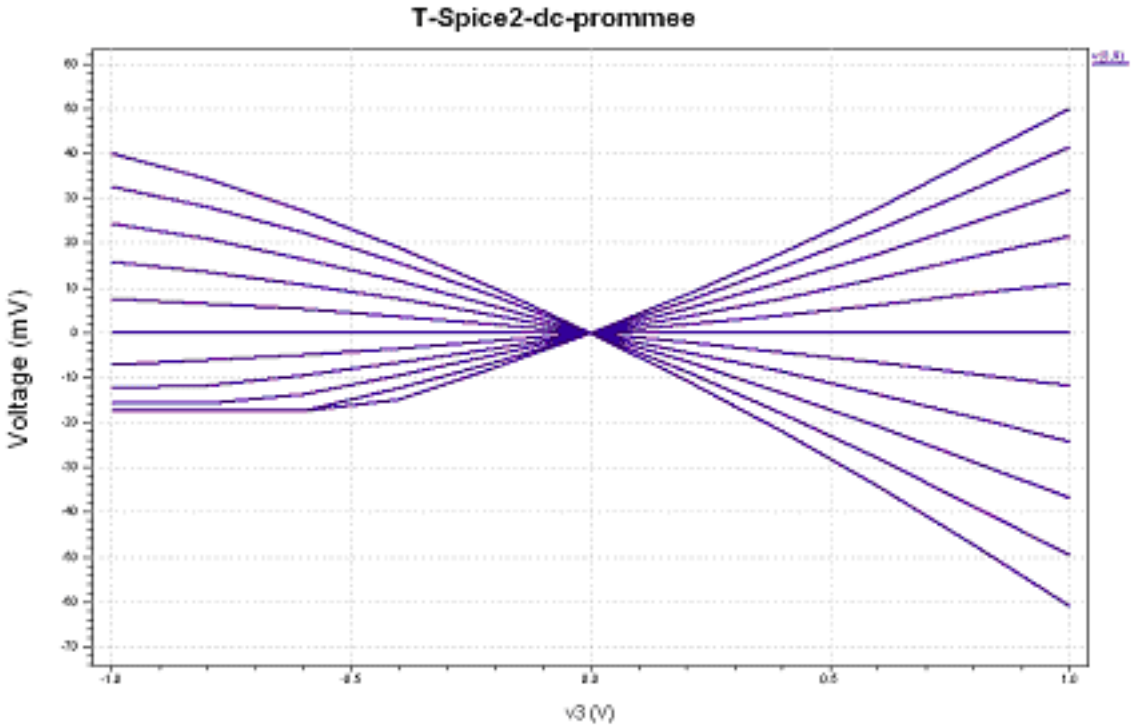

Figure 5.8: DC characteristics for input Vx.

5.3.1 Summing circuit

Fig. 5.11 shows the fully differential summing circuit that based on basic MOS differential pairs M1-M4 and the active loads M5-M6. Assuming that transistors M1-M4 are matched with transconductance parameter K1 and transistors M5-M6 are matched with K5. If all devices operate in saturation region, applying the differential input voltages V1 and V2, the loop equations of the gate-to-source voltages of the two differential amplifiers M1-M2 and M3-M4 can be written as

$$((V_1 \div 2) + (V_2 \div 2)) = V_{gs1} - V_{gs2} \tag{5.17}$$

$$-((V_1 \div 2) + (V_2 \div 2)) = V_{gs3} - V_{gs4} \tag{5.18}$$

where Vgs1 to Vgs4 are the gate-to-source voltage of the transistors M1-M4. By

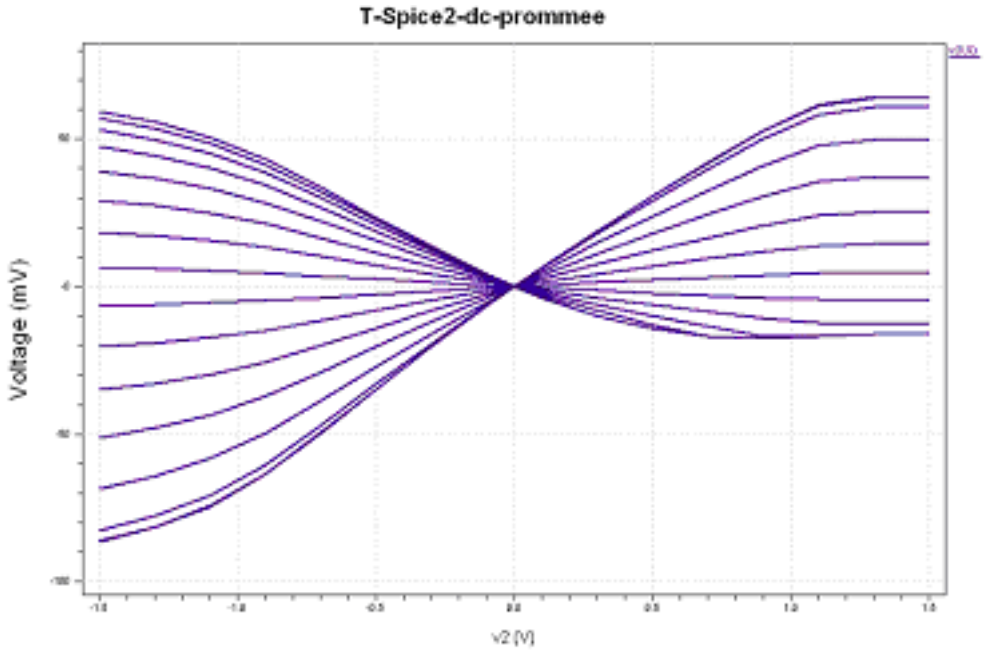

Figure 5.9: DC characteristics for input Vy.

replacing into above equations, we can write

$$((V_1 \div 2) + (V_2 \div 2)) = \sqrt{I_{d1}/K_1} - \sqrt{I_{d2}/K_1} \tag{5.19}$$

$$((V_1 \div 2) + (V_2 \div 2)) = \sqrt{I_{d3}/K_1} - \sqrt{I_{d4}/K_1} \tag{5.20}$$

Subtracting above equations

$$(V_1 + V_2) = (\sqrt{1 \div K_1})\{(\sqrt{I_{d1} + I_{d4}}) - (\sqrt{I_{d2} + I_{d3}})\} \tag{5.21}$$

Considering from the two differential amplifiers M1-M2 and M3-M4 in Fig. 5.11, we can see that Id1=Id4 and Id2=Id3. Then, above equation can be rearranged and rewritten in the form of

$$\sqrt{I_{d4}} + \sqrt{I_{d2}} = \sqrt{K_1}((V_1 \div 2) + (V_2 \div 2)) \tag{5.22}$$

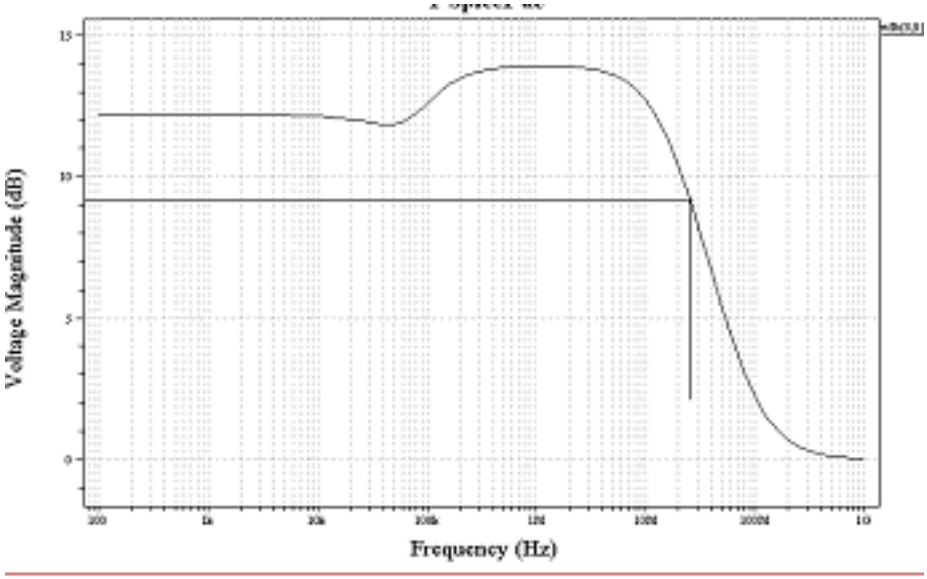

Figure 5.10: AC characteristics

From the output loop equation Vsum=Vgs5-Vgs6, the drain current Id5=Id4 and Id6=Id2 the output voltage Vsum is given by

$$V_{sum} = [(\sqrt{I_{d4} + I_{d2}}) \div \sqrt{K_5}] \tag{5.23}$$

From above two equations

$$V_{sum} = \sqrt{K_1 \div (4 \times K_5)}(V_1 + V_2) \tag{5.24}$$

and the maximum input voltage range of the circuit is

$$|V_1 \div 2 + V_2 \div 2| \leq \sqrt{I_{ss} \div K_1} \tag{5.25}$$

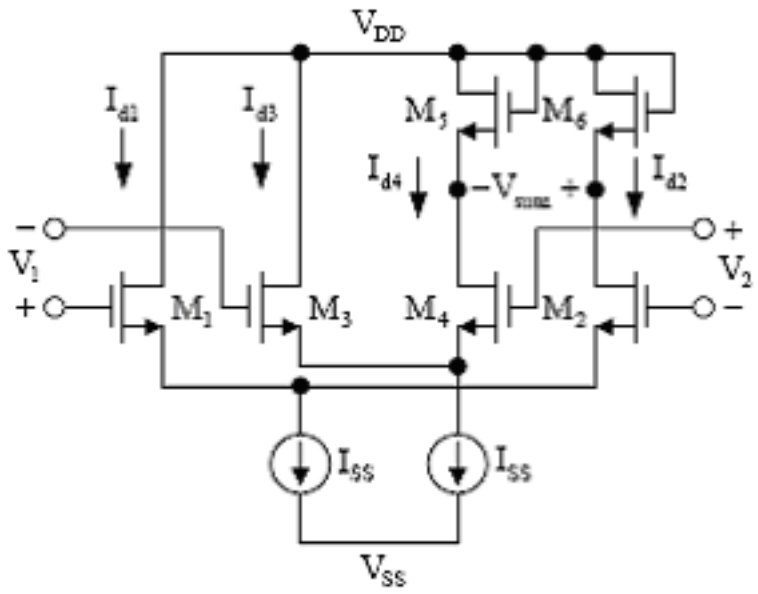

Figure 5.11: Fully differential summing circuit[10]

5.3.2 Squaring Circuit

Fig. 5.12 shows the configuration of the differential-input voltage squaring circuit that modified from a basic NMOS differential pair, where the transistors M7-M9 are bias in saturation region with individual wells connected to their sources to eliminate the body effect. If the differential input voltage Vd with the same common-mode Vc is applied, the drain currents of the transistors can be given by

$$I_{d7} = K_7(V_c + (V_d \div 2) - V_{sq} - V_{TH})^2 \tag{5.26}$$

$$I_{d8} = K_8(V_c + (V_d \div 2) - V_{sq} - V_{TH})^2 \tag{5.27}$$

$$I_{d9} = K_9(V_{G9} - V_{ss} - V_{TH})^2 \tag{5.28}$$

$$I_{d7} + I_{d8} = I_{d9} \tag{5.29}$$

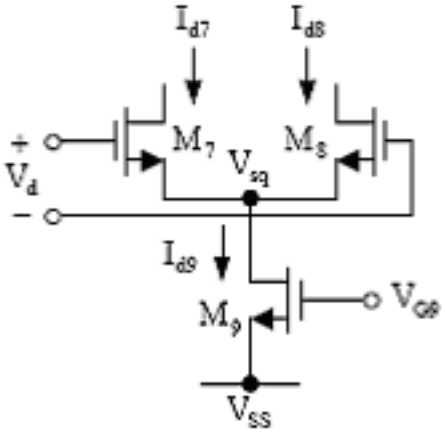

Figure 5.12: Squaring circuit based on differential pair[10]

where K7, K8 and K9 are transconductance parameter of the transistors M7-M9, and VTH is the threshold voltage of the transistors, respectively. Let M7 and M8 are identical, and the aspect ratio of M9 is twice that of M7 and M8.Output voltage of squaring circuit is given by

$$V_{sq} = V_c - V_{TH} - \sqrt{(V_{G9} - V_{ss} - V_{TH})^2 - (V_d \div 2)^2} \tag{5.30}$$

$$V_{sq} = V_c - V_{G9} + V_{ss} + (V_d^2 \div (8(V_{G9} - V_{ss} - V_{TH}))) \tag{5.31}$$

above equation indicate that the output voltage Vsq is related to the square of the differential input voltage Vd. Therefore, the source-coupled pair circuit as shown in Fig. 3 can be used as a squaring circuit for quarter-square multiplier. However, this relation is valid for the case that all transistors are operated in the saturation region.

5.3.3 Fully Differential Multiplier

By employing the squaring circuit of Fig. 5.12 and the summing circuit of Fig. 5.11, the fully differential all NMOS four-quadrant analog multiplier can be realized.The

output voltage Vo of the multiplier can be expressed as

$$V_o = (K_1 \div 4K_5) \div (8(V_{G9} - V_{ss} - V_{TH}))[(V_1 + V_2)^2 - (V_1 - V_2)^2] \tag{5.32}$$

$$V_o = (K_1 \div K_5) \div (8(V_{G9} - V_{ss} - V_{TH}))V_1V_2 \tag{5.33}$$

From above equation, the gain factor of multiplier can be controlled by the transconductance parameters K1, K5 and the gate voltage VG9. For example, when (W/L)1=(W/L)5, VTH=0.55V, VSS=-1.5V and VG9=-0.47V, the gain factor is calculated to be 0.091. For increasing the gain factor, the NMOS voltage amplifier circuit that shown in Fig. 4 has been introduced.

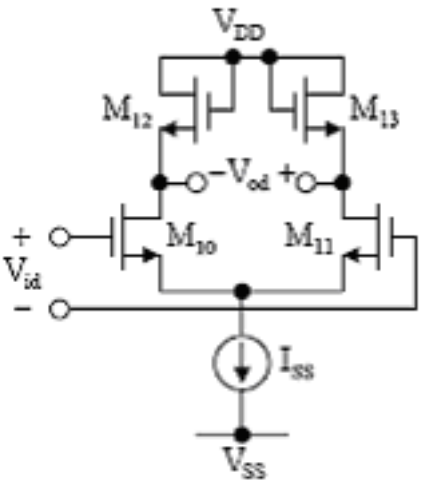

Figure 5.13: NMOS voltage amplifier[10].

For increasing the gain factor, the NMOS voltage amplifier circuit that shown in Fig. 5.13 has been introduced. Assuming that transistors M10=M11, M12=M13 and all devices are biased in the saturation, the voltage gain is given by Vod/Vid=K10/K12.

Fig. 5.14 shows the complete voltage-mode multiplier circuit. Transistors M1- M12 forms the summing circuits that produce the output voltage in term of the sum and difference of input signals. The sum and difference outputs from these stages are applied to the squarer circuits formed by M13-M18 and M24- M27 form NMOS voltage amplifier, where the transistors M19-M23 provide bias currents ISS for summing stages and amplifier circuit. Finally, the output voltage of the multiplier can be written as

$$V_{out} = [\{(K_1 \times K_{24}) \div (K_9 \times K_{26})\} \div (8(V_{G9} - V_{ss} - V_{TH}))]V_1V_2 \tag{5.34}$$

where VGG is the bias voltage at the gate of transistors M17- M23. above equation is valid for all transistors that are biased in their saturation-mode of operation.

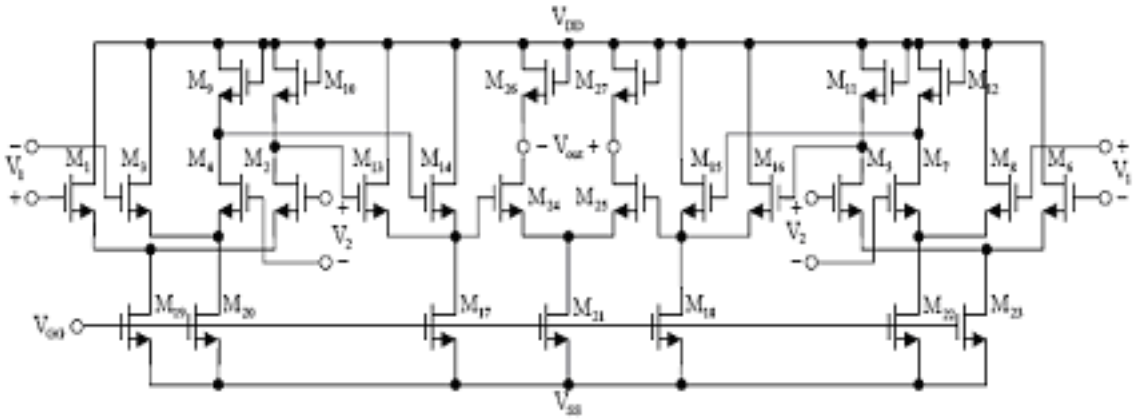

Figure 5.14: NMOS voltage-mode multiplier[10].

5.3.4 Simulation Results

The multiplier circuit described in Fig. 5.14 is simulated using TSPICE 0.35μm CMOS technology. The aspect ratios of the transisters are M1- M16 is 2.8μm /2.8μm, M17-M25 is 5.6μm /2.8μm, and M26-M27 is 2.8μm /2.8μm. The power supply voltage

is 1.5V, the bias gate voltage VGG = -0.47V. The dc characteristics of the multiplier are shown in Fig. 5.15. V1 and V2 varied from -1.2V to +1.2V voltage range in step of 0.2V. Power consumption of the multiplier is 64 W.

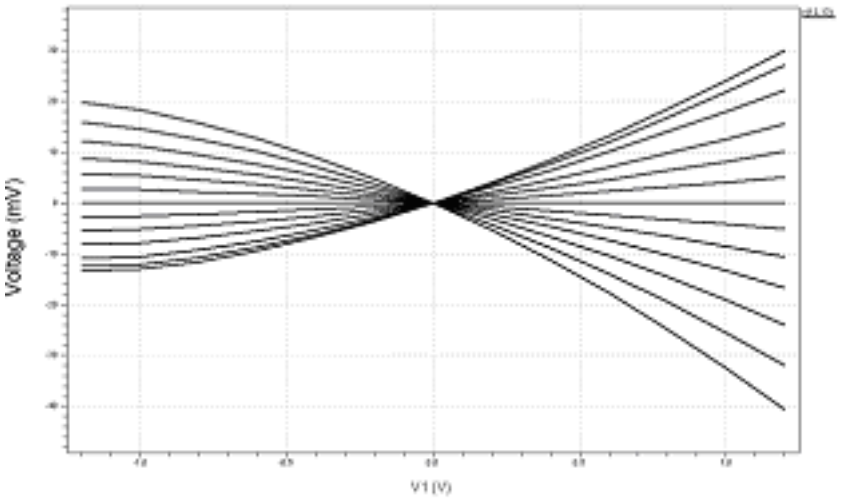

Figure 5.15: DC Characteristrics .

Fig. 5.16 shows analog multiplier working as modulator with modulation signal of 1kHz and carrier of 25kHz with peak amplitude of 0.25V. Fig. 5.17 shows analog multiplier working as frequency doublers with both the inputs of 1 kHz and 0.25V Peak to Peak.

Fig. 5.18 shows ac characteristics of analog multiplier, -3 db down Bandwidth is 140MHz. Fig. 5.19 shows simulated total harmonics distortion.

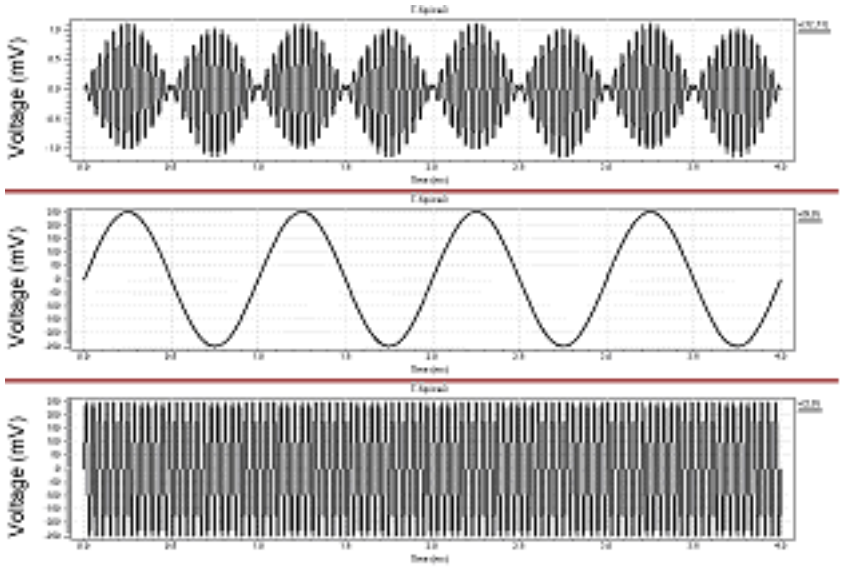

Figure 5.16: Amplitude modulation of sinusoidal signal .

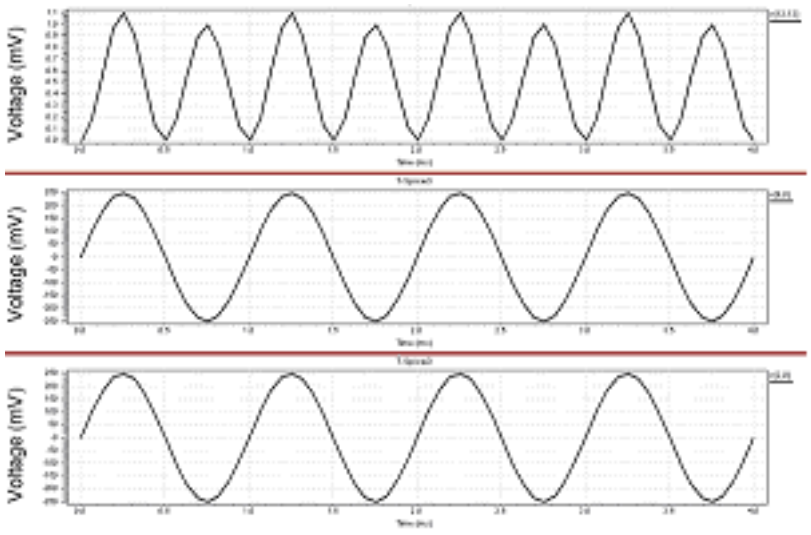

Figure 5.17: Analog multiplier as frequency doublers.

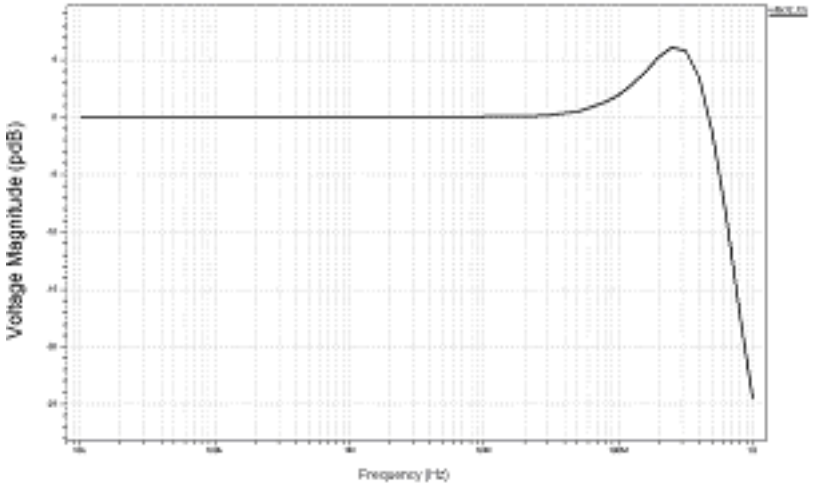

Figure 5.18: AC Characteristics and bandwidth is 140MHz.

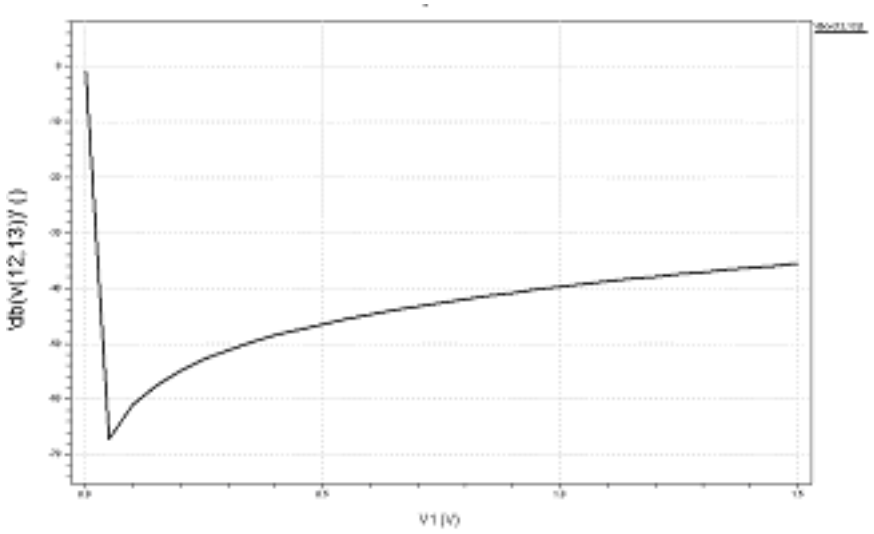

Figure 5.19: Total Harmonics Distortion.

Chapter 6

Proposed Architecture

A CMOS four-quadrant multiplier can be used to multiply two bipolar signals, (+/-)x and (+/-)y. This type of multiplier has been used to build many analog circuits, such as modulators and adaptive filters.

6.1 Block Diagram

The block diagram of the proposed multiplier is shown in Fig.6.1. The first stage consists of four identical adders producing the sum of their respective input signals. These outputs are then combined in the second stage to form the multiplication function.

6.1.1 Adder Circuit

Fig. 6.2, the voltage at node c is Vdd - V1. Now, since M3 and M4 are PMOS transistors, the source to gate voltage of these two transistors is Vdd - (Vdd - V1), or V1. Thus Vo is equal to V1 + V2.

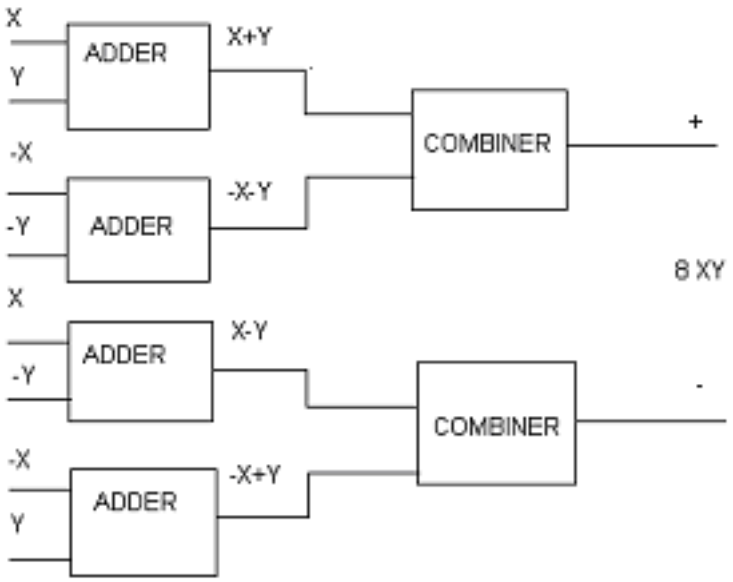

Figure 6.1: block diagram of Proposed architecture

6.1.2 Combiner cell

Fig. 6.3 is the 2-input combiner cell described in [6]. Referring to Fig. 6.3, it can be seen that the drain and source terminals of the n-channel devices M17 and M18 are connected to each other, the input voltages Vy and -Vy control the drain currents and these are summed in the load. Assuming matched devices and operation in the saturation region, the output voltage of the combiner may be expressed as

$$V_o = V_{DD} - k_n R[(V_y - V_{tn})^2 + (-V_y - V_{tn})^2] \tag{6.1}$$

Combiner cell with pmos load is used in the multiplier circuit.

6.1.3 Circuit realization

Proposed structure using four adder circuit and two combiner circuit is shown in fig.6.4. Four combinations of two inputs V1 and V2 i.e. ((V1,V2),(-V1,-V2),(V1,-

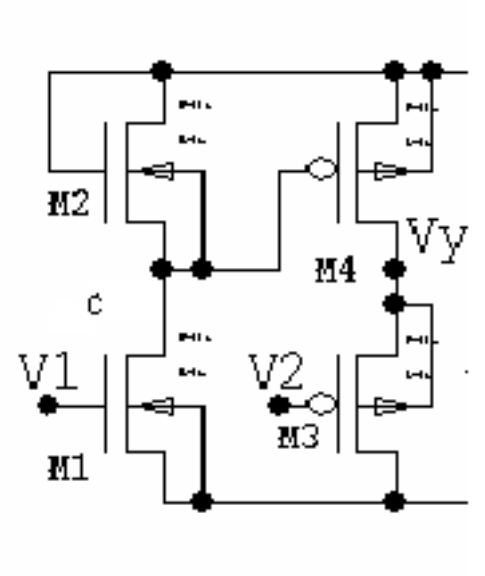

Figure 6.2: Adder circuit

V2),(-V1,V2))are applied to four different adders. And their outputs are applied to the combiner cell. Transistor M17 and M18 forms the one combiner cell and transistor M19 and M20 forms the other combiner cell. The sum (V1,V2),(-V1,-V2),(V1,-V2)and (-V1,V2) are applied to the gate terminal of M17,M18,M19and M20 as shown below.

$$V_{GS17} - V_{th} = v1 + v2 \tag{6.2}$$

$$V_{GS18} - V_{th} = -v1 - v2 \tag{6.3}$$

$$V_{GS19} - V_{th} = v1 - v2 \tag{6.4}$$

$$V_{GS20} - V_{th} = -v1 + v2 \tag{6.5}$$

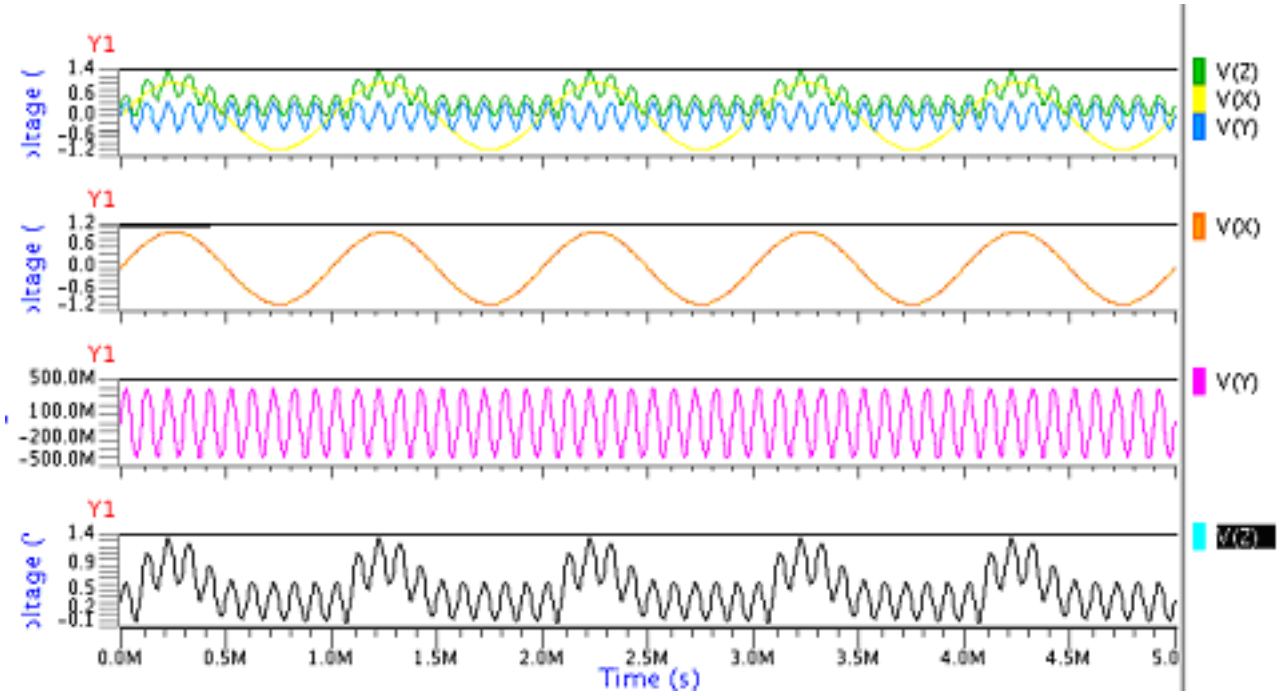

Figure 6.3: Transient analysis of an Adder circuit.

Drain current of these four transistor is shown below.

$$I_{D17} = K_n(W/L)[(V_{GS17} - V_{th})^2] = K_n(W/L)[V_1^2 + V_2^2 + 2V_1V_2] \tag{6.6}$$

$$I_{D18} = K_n(W/L)[(V_{GS18} - V_{th})^2] = K_n(W/L)[V_1^2 + V_2^2 + 2V_1V_2] \tag{6.7}$$

$$I_{D19} = K_n(W/L)[(V_{GS19} - V_{th})^2] = K_n(W/L)[V_1^2 + V_2^2 - 2V_1V_2] \tag{6.8}$$

$$I_{D20} = K_n(W/L)[(V_{GS20} - V_{th})^2] = K_n(W/L)[V_1^2 + V_2^2 - 2V_1V_2] \tag{6.9}$$

Output is taken between V01 and V02 and is given by

$$V_{out} = K[(I_{D17} + I_{D18}) - (I_{D19} + I_{D20})] = 8K_n(W/L)V_1V_2 \tag{6.10}$$

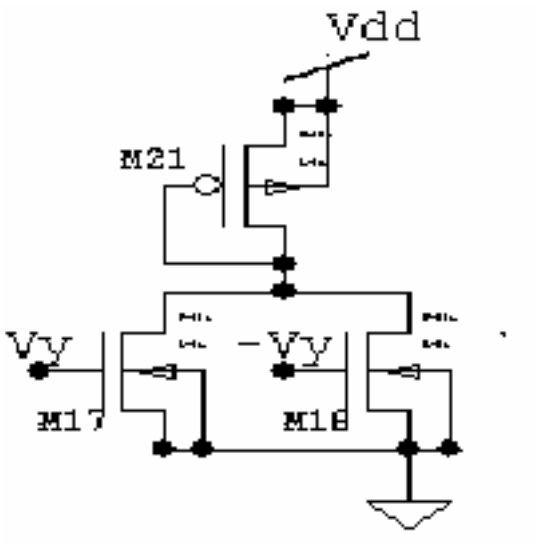

Figure 6.4: combiner cell.

6.1.4 Simulation Results

Analog multiplier is simulated using 0.35 μm CMOS technology with power supply of 1.5V.Thresold voltages for nMOS and pMOS transister are Vtn=0.55V and Vtp=-0.44V. Transient response of analog multiplier is shown in Fig.6.5 for modulating signal of 1kHz and carrier of 25kHz.Multiplier can be used as modulator is shown in Fig 6.5,this simulation is carried out in T-Spice using Tanner Tool.Transient analysis in Eldo(Mentor Graphics)simulator is shown in Fig. 6.6. Analog multiplier working as frequency doublers is shown in Fig. 6.7 with both the input keeping 1kHz.

Fig. 6.8 shows the DC characteristics of analog multiplier with V1 varied from 0 to 400mV and V2 from -400mV to 400mV. Fig. 6.9 shows the AC characteristics of analog multiplier and bandwidth comes out to be 10.5 MHz. Power dissipation is 67μW.

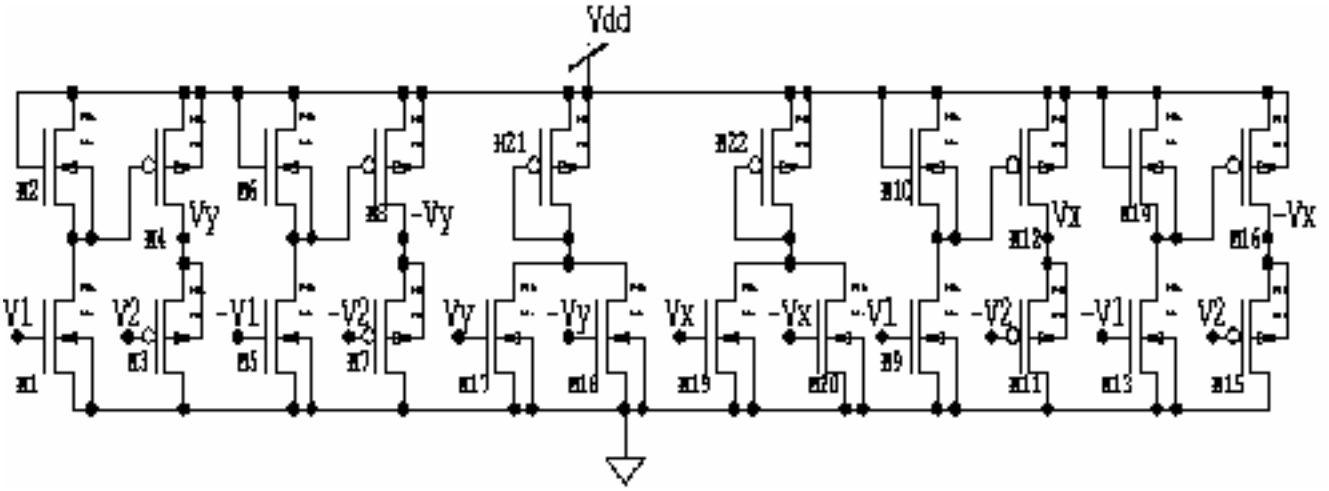

Figure 6.5: proposed analog multiplier.

6.2 Analog Multiplier Applications

Analog multiplier find many application in the telecommunication, as it can go up to higher frequency with less cost, such as mixer, analog computer, automatic gain control, product detector, squelch.

6.2.1 Frequency mixer

In telecommunication, a mixer is a nonlinear circuit or device that accepts as its input two different frequencies and presents at its output a mixture of signals at several frequencies:

1. the sum of the frequencies of the input signals 2. the difference between the frequencies of the input signals 3. Both original input frequencies these are often considered parasitic and are filtered out.

MOSFET AREA	W/L ratios(μm)
M1,M2,M5,M6,M9,M10,M13,M14	2/0.5
M3,M4,M7,M8,M11,M12,M15,M16	10/0.8
M17,M18,M19,M20	0.4/0.4
M21,M22	10/2

Table I: Aspect ratio of proposed structure.

The manipulations of frequency performed by a mixer can be used to move signals between bands, or to encode and decode them. One other application of a mixer is as a product detector.

The input signals are, in the simplest case, sinusoidal voltage waves, representable

$$V_i(t) = A_i \sin 2\pi f_i t \tag{6.11}$$

Where each A is amplitude, each f is a frequency, and t represents time. (In reality even such simple waves can have various phases, but that does not enter here.) One common approach for adding and subtracting the frequencies is to multiply the two signals; using the trigonometric identity

$$\sin(A) \times \sin(B) = (1 \div 2)[\cos(A - B) - \cos(A + B)] \tag{6.12}$$

we have

$$V_1(t)V_2(t) = (A_1A_2 \div 2)[\cos 2\pi(f_1 - f_2)t - \cos 2\pi(f_1 - f_2)t] \tag{6.13}$$

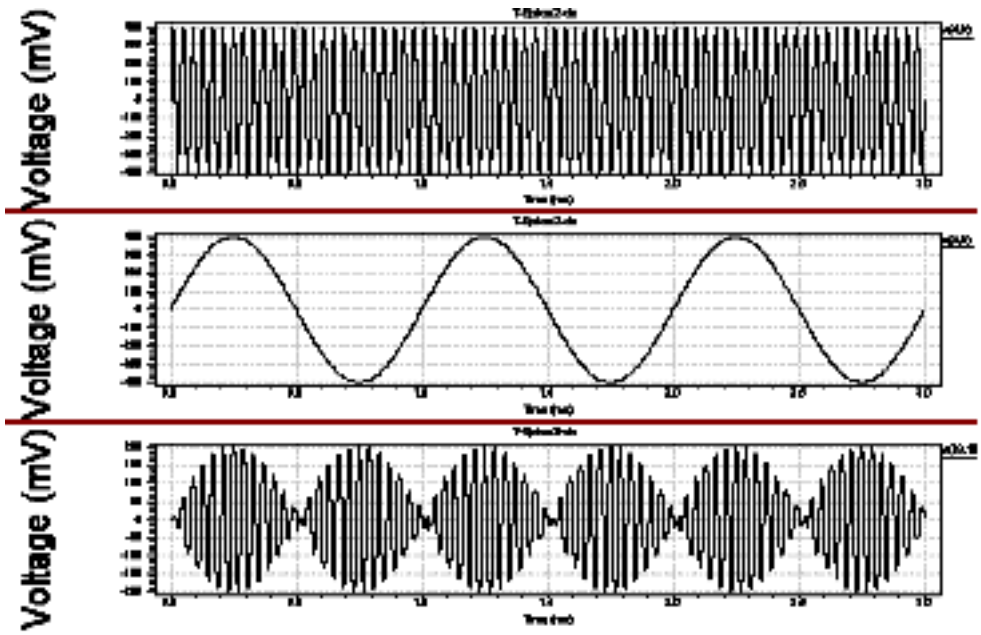

Figure 6.6: Transient Analysis in T-spice(Tanner EDA Tool).

Where the sum (f1 + f2) and difference (f1 - f2) frequencies appear. This is the inverse of the production of acoustic beats.

6.2.2 Product detector

A product detector is a type of demodulator used for AM and SSB signals. Rather than converting the envelope of the signal into the decoded waveform like an envelope detector, the product detector takes the product of the modulated signal and a local oscillator, hence the name. A product detector is a frequency mixer.

Product detectors can be designed to accept either IF or RF frequency inputs. A product detector which accepts an IF signal would be used as a demodulator block in a super heterodyne receiver, and a detector designed for RF can be combined with an RF amplifier and a low-pass filter into a direct-conversion receiver.

The simplest form of product detector multiplies an incoming signal by its carrier to produce a copy of the original message and another AM signal at twice the original carrier frequency. This high-frequency component can then be filtered out leaving the

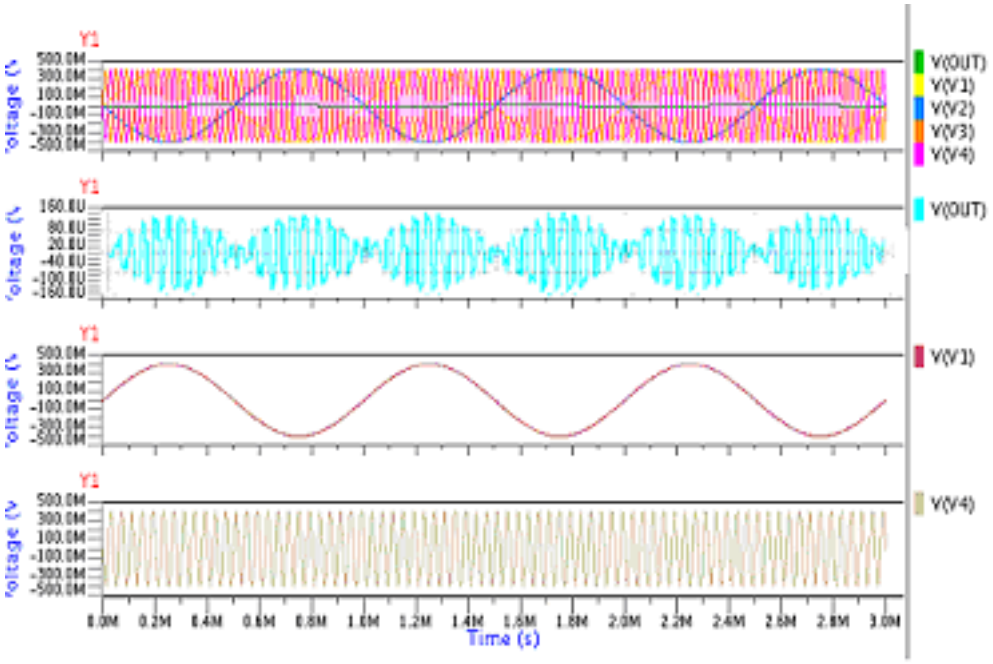

Figure 6.7: Transient analysis in eldo(mentor graphics).

original signal.

If m(t) is the original message, the AM signal can be shown by

x(t) = (C + m(t))cos(Wot).

Multiplying the AM signal x(t) by an oscillator at the same frequency as and in phase with the carrier yields

y(t) = (C + m(t)) cos(Wot) cos(Wot),

this can be re-written as

y(t) = (C + m(t))(1 / 2 + 1 / 2cos(2Wot)).

After filtering out the high-frequency component based around cos(2Wot) and the DC component C, the original message will be recovered.

6.2.3 Analog computer

A computer in which numerical data are represented by measurable physical variables, such as electrical voltage. A computer or computational device in which the

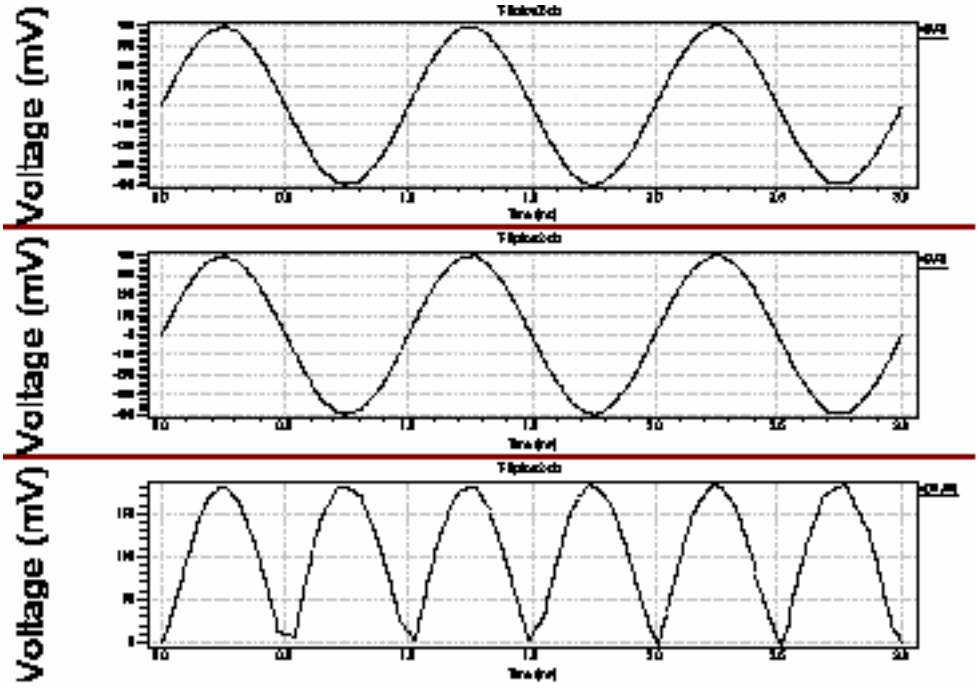

Figure 6.8: frequency doublers

problem variables are represented as continuous, varying physical quantities. An analog computer implements a model of the system being studied. The physical form of the analog may be functionally similar to that of the system, but more often the analogy is based solely upon the mathematical equivalence of the interdependence of the computer variables and the variables in the physical system.

6.2.4 Voltage-controlled amplifier versus analog multiplier

If one input of an analog multiplier is held at a steady state voltage, a signal at the second input will be scaled in proportion to the level on the fixed input. In this case the analog multiplier may be considered to be a voltage controlled amplifier. Obvious applications would be for electronic volume control and automatic gain control. Although analog multipliers are often used for such applications, voltage-controlled amplifiers are not necessarily true analog multipliers. For example, an integrated circuit designed to be used as a volume control may have a signal input designed for

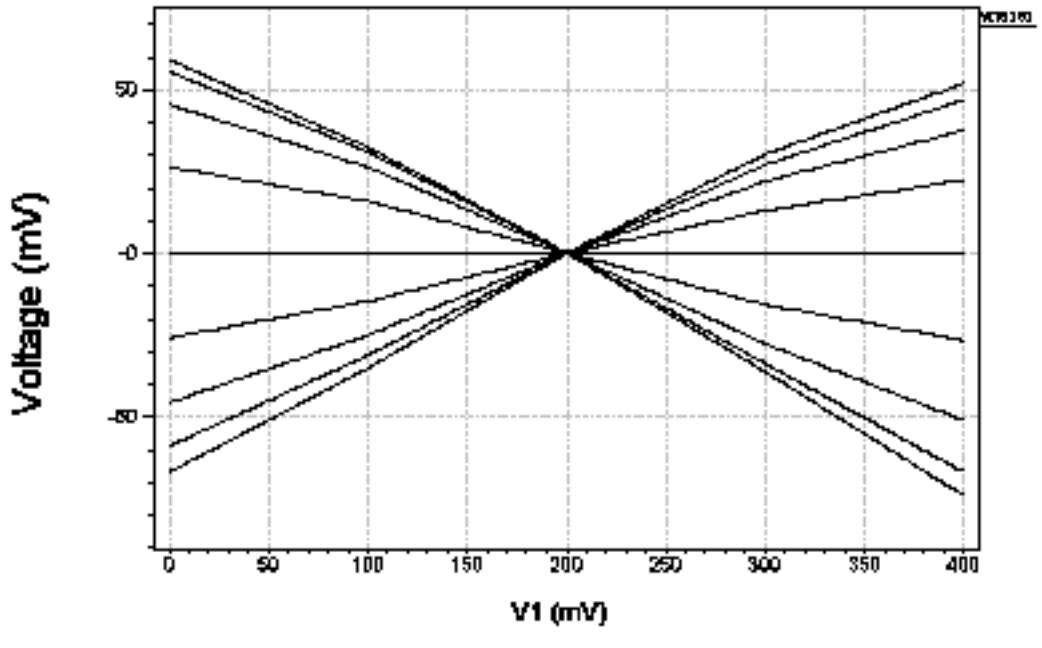

Figure 6.9: DC characteristics of analog multiplier

1 Vp-p, and a control input designed for 0-5 V dc; that is, the two inputs are not symmetrical and the control input will have a limited bandwidth.

By contrast, in what is generally considered to be a true analog multiplier, the two signal inputs have identical characteristics. Applications specific to a true analog multiplier are those where both inputs are signals, for example in a frequency mixer or an analog circuit to implement a discrete Fourier transform.

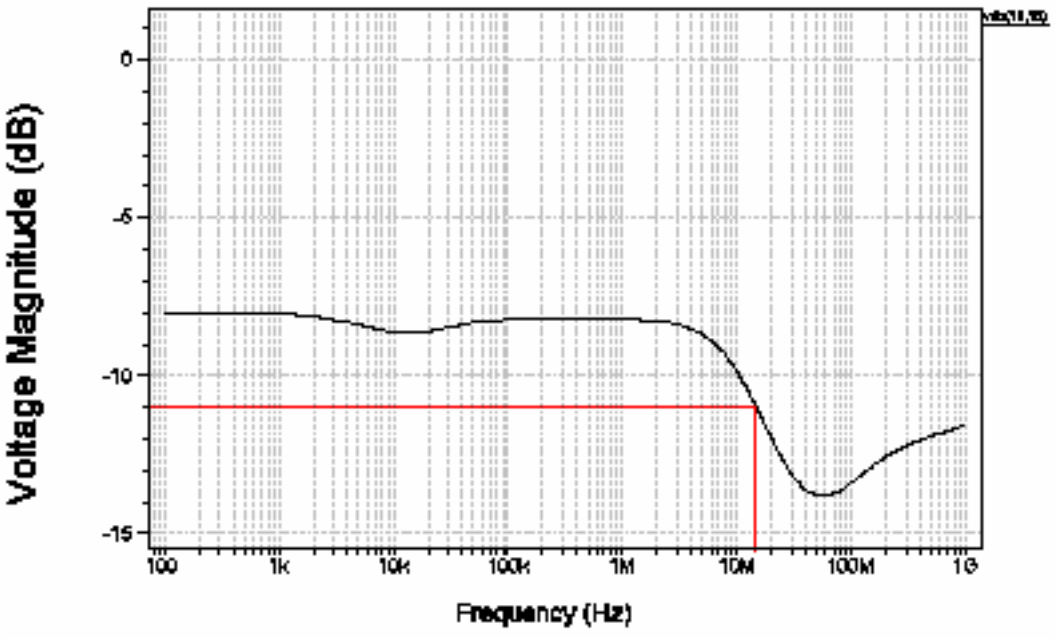

Figure 6.10: AC characteristics of analog multiplier

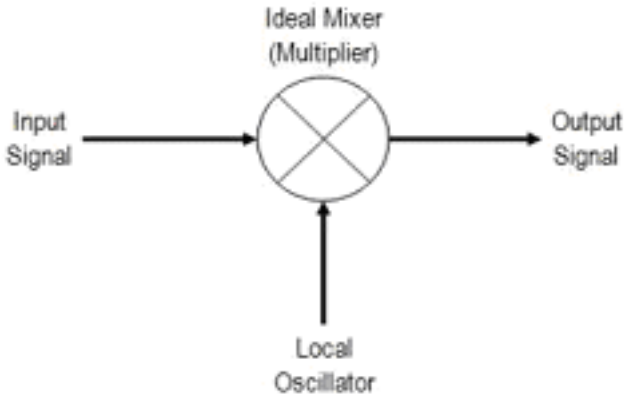

Figure 6.11: Frequency Mixer Symbol.

Chapter 7

Conclusion

Here Different Architecture of analog multiplier is shown which is widely used as modulator, frequency filter, and Frequency doublers.

All Four quadrant analog multipliers are simulated using 0.35μm CMOS process with power supply voltage of 1.5V.All multipliers are compared for there performance metrics such as power consumption, linearity error, input voltage range etc, which is shown below. Here some multiplier architectures use resistors and so their power consumption is high. Proposed structure does not use any resistor so its power consumption is less and linearity error is also less for the proposed structure. If input voltage range is considered then it is higher in multiplier proposed by chen and promme.Bandwidth is higher for multiplier proposed by chen.Number of active elements are less for multiplier architecture by chen.

From this study it is concluded that all multipliers are suitable for low power applications and proposed structure is having lower linearity error.

	FQAM by chen	FQAM by Sawigun	FQAM by prommee	FQAM by Boonchu	FQAM by Kiatwarin	Proposed structure
Power supply	±1.5V	1.5V	1.5V	±1.5V	1.2V	1.5V
Technology	0.35µm	0.35µm	0.35µm	0.35µm	0.13µm	0.35µm
Input voltage range	±1.5V	±0.4V	±1.5V	±1.2V	±0.4V	±0.4V
No. of active element	12	12	16	27	10	22
No. of passive element	0	2	2	0	2	0
Bandwidth	1.9 GHz	10MHz	25MHz	140MHz	50MHz	10.5MHz
Linearity error	3.23%	4.2%	1.5%	2.3%	3.1%	1.4%
Power consumption	40µW	290µW	460µW	64 µW	86.4 µW	67µW

Table I: Comparison of different analog multipliers

Appendix A

Codes in T-Spice using Tanner EDA Tool

Model parameters for 0.35µm technology:

```
.MODEL MOSN NMOS (                          LEVEL   = 49
+VERSION = 3.1            TNOM    = 27              TOX     = 8.1E-9
+XJ      = 1.5E-7         NCH     = 1.7E17          VTH0    = 0.5
+K1      = 0.6025239      K2      = 0.0263517       K3      = -3
+K3B     = 1.8485697      W0      = 1E-8            NLX     = 1.019602E-
7
+DVT0W   = 0              DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.7763827      DVT1    = 0.3833529       DVT2    = -0.1687347
+U0      = 469.1651318    UA      = 1E-13           UB      = 2.278136E-
18
+UC      = 7.195199E-11   VSAT    = 1.252153E5      A0      = 1.4356852
+AGS     = 0.1959745      B0      = -9.483581E-8    B1      = -1E-7
+KETA    = -1.697162E-3   A1      = 4.072094E-4     A2      = 0.8441967
+RDSW    = 923.6850076    PRWG    = -8.44494E-13    PRWB    = -0.0402781
+WR      = 1              WINT    = 7.029572E-8     LINT    = 8.189158E-
8
+DWG     = -5.6847E-10    DWB     = -1.231007E-9    VOFF    = -0.15
+NFACTOR = 2.5            CIT     = 0               CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0               ETA0    = 0.2789152
+ETAB    = -0.115313      DSUB    = 1.1935601       PCLM    = 0.6382926
+PDIBLC1 = 5.033446E-3    PDIBLC2 = 2.649708E-3     PDIBLCB = 0.0674678
+DROUT   = 0.0749558      PSCBE1  = 4.437569E8      PSCBE2  = 1.861992E-
5
+PVAG    = 0.0892561      DELTA   = 0.01            RSH     = 4.3
+MOBMOD  = 1              PRT     = 0               UTE     = -1.5
+KT1     = -0.11          KT1L    = 0               KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18       UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0               WLN     = 1
+WW      = 0              WWN     = 1               WWL     = 0
+LL      = 0              LLN     = 1               LW      = 0
+LWN     = 1              LWL     = 0               CAPMOD  = 2
+XPART   = 0.5            CGDO    = 3.6E-10         CGSO    = 3.6E-10
+CGBO    = 1E-10          CJ      = 1.028316E-3     PB      = 0.8
+MJ      = 0.3460467      CJSW    = 1.379724E-10    PBSW    = 0.9110771
+MJSW    = 0.1115064      CJSWG   = 1.64E-10        PBSWG   = 0.9110771
+MJSWG   = 0.1115064      CF      = 0               PVTH0   = -9.25355E-
3
+PRDSW   = -29.2484805    PK2     = -1.171165E-3    WKETA   = 1.804978E-
3
+LKETA   = -0.0130345      )
*
.MODEL MOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27              TOX     = 8.1E-9
+XJ      = 1.5E-7         NCH     = 1.7E17          VTH0    = -0.6
+K1      = 0.9589471      K2      = -0.0307189      K3      = 0
+K3B     = 4.92906        W0      = 1.491667E-8     NLX     = 1E-9
```

```
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.3126878      DVT1    = 0.5272331      DVT2    = -0.3
+U0      = 121.7426275    UA      = 1.471306E-9    UB      = 2.709433E-
21
+UC      = -1E-10         VSAT    = 8.735471E4     A0      = 0.7878688
+AGS     = 0.1283139      B0      = 1.58628E-6     B1      = 5E-6
+KETA    = 6.658718E-3    A1      = 0.0717648      A2      = 0.3
+RDSW    = 3E3            PRWG    = -0.1103537     PRWB    = -0.2132337
+WR      = 1              WINT    = 7.958254E-8    LINT    = 6.669867E-
8
+DWG     = -2.403925E-8   DWB     = 2.178152E-9    VOFF    = -0.0361606
+NFACTOR = 0.8753188      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0    = 0.3135357
+ETAB    = -0.1029206     DSUB    = 1              PCLM    = 1.2171081
+PDIBLC1 = 4.519703E-3    PDIBLC2 = 1.04969E-3     PDIBLCB = 0.1571044
+DROUT   = 0.0809132      PSCBE1  = 8E10           PSCBE2  = 8.437353E-
10
+PVAG    = 0.0150041      DELTA   = 0.01           RSH     = 3.1
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 3.58E-10       CGSO    = 3.58E-10
+CGBO    = 1E-10          CJ      = 8.546229E-4    PB      = 0.7409523
+MJ      = 0.3421975      CJSW    = 8E-13          PBSW    = 0.75
+MJSW    = 0.9098666      CJSWG   = 6.4E-11        PBSWG   = 0.75
+MJSWG   = 0.9098666      CF      = 0              PVTH0   = 5.98016E-3
+PRDSW   = 14.8598424     PK2     = 3.73981E-3     WKETA   = -
6.996779E-3
+LKETA   = -0.0316055      )
```

Model parameters for 0.13µm technology:

```
.MODEL NMOS1 NMOS (                        LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 3.2E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = vthn
+K1      = 0.3116278      K2      = -0.0242369     K3      = 1E-3
+K3B     = 4.0718988      W0      = 1E-7           NLX     = 1E-6
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.1328505      DVT1    = 0.156363       DVT2    = 0.2649006
+U0      = 444.7034216    UA      = -4.48287E-10   UB      = 3.424358E-
18
+UC      = 4.01122E-10    VSAT    = 1.969433E5     A0      = 0.2867655
+AGS     = 0.5216555      B0      = 6.476654E-6    B1      = 5E-6
+KETA    = 0.0304889      A1      = 2.743235E-3    A2      = 0.3
+RDSW    = 150            PRWG    = 0.3528522      PRWB    = 0.1083682
+WR      = 1              WINT    = 1.370437E-8    LINT    = 1.037662E-
8
+DWG     = 5.33378E-9     DWB     = 1.379031E-8    VOFF    = -0.0369443
+NFACTOR = 2.5            CIT     = 0              CDSC    = 2.4E-4
```

```
+CDSCD   = 0              CDSCB   = 0              ETA0    = 2.768114E-
6
+ETAB    = 0.4474854      DSUB    = 4.086007E-6    PCLM    = 0.9644002
+PDIBLC1 = 0.993971       PDIBLC2 = 0.01           PDIBLCB = 0.1
+DROUT   = 0.9978969      PSCBE1  = 7.955523E10    PSCBE2  = 5.002785E-
10
+PVAG    = 0.5006861      DELTA   = 0.01           RSH     = 7.3
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 4E-10          CGSO    = 4E-10
+CGBO    = 1E-12          CJ      = 8.383543E-4    PB      = 0.8911869
+MJ      = 0.5522633      CJSW    = 2.463297E-10   PBSW    = 0.8
+MJSW    = 0.3086109      CJSWG   = 3.3E-10        PBSWG   = 0.8
+MJSWG   = 0.3086109      CF      = 0              PVTH0   = 2.009264E-
4
+PRDSW   = 0              PK2     = 1.30501E-3     WKETA   = -
5.422862E-3
+LKETA   = 2.841924E-3    PU0     = 4.4729531      PUA     = 1.66833E-
11
+PUB     = 0              PVSAT   = 653.2294237    PETA0   = 1E-4
+PKETA   = -0.0345219      )
*
.MODEL PMOS1 PMOS (                               LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 3.2E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.45
+K1      = 0.3027543      K2      = 1.864222E-3    K3      = 0.0987453
+K3B     = 6.5023601      W0      = 1E-6           NLX     = 2.054634E-
7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.0282865      DVT1    = 0.7930904      DVT2    = 0.1
+U0      = 107.3068088    UA      = 1.328602E-9    UB      = 1.081735E-
21
+UC      = -4.07757E-11   VSAT    = 2E5            A0      = 1.1329332
+AGS     = 0.6150824      B0      = 8.195389E-6    B1      = 3.845906E-
6
+KETA    = 0.0360256      A1      = 1.14384E-3     A2      = 0.4014422
+RDSW    = 105.1225715    PRWG    = -0.4995805     PRWB    = 0.5
+WR      = 1              WINT    = 0              LINT    = 8.799136E-
9
+DWG     = 1.619181E-9    DWB     = -2.158446E-8   VOFF    = -0.1022829
+NFACTOR = 1.5332272      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0    = 2.490791E-
3
+ETAB    = -5.929764E-3   DSUB    = 1.156764E-3    PCLM    = 1.0382822
+PDIBLC1 = 0.0287408      PDIBLC2 = -1.66203E-12   PDIBLCB = -1E-3
+DROUT   = 0.7            PSCBE1  = 7.772908E9     PSCBE2  = 2.375114E-
9
+PVAG    = 3.350466E-5    DELTA   = 0.01           RSH     = 6.6
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
```

```
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 3E-10          CGSO    = 3E-10
+CGBO    = 1E-12          CJ      = 1.174314E-3    PB      = 0.8213848
+MJ      = 0.4093691      CJSW    = 1.315954E-10   PBSW    = 0.893802
+MJSW    = 0.1            CJSWG   = 4.22E-10       PBSWG   = 0.893802
+MJSWG   = 0.1            CF      = 0              PVTH0   = 9.239E-4
+PRDSW   = 57.2461714     PK2     = 1.85451E-3     WKETA   = 0.0353179
+LKETA   = 0.0141288      PU0     = -1.2495067     PUA     = -5.00288E-
11
+PUB     = 1.417348E-23   PVSAT   = 50             PETA0   = 1E-4
+PKETA   = -7.528316E-3    )
*
```

Net list for Analog multiplier architecture 1:

```
M1 3 1 0 0 MOSN W=0.8u L=.35u ps=1.05u pd=1.05u
M2 7 1 0 0 MOSN W=0.8u L=.35u ps=1.05u pd=1.05u
M3 10 1 0 0 MOSN W=0.8u L=.35u ps=1.05u pd=1.05u
M4 14 1 0 0 MOSN W=0.8u L=.35u ps=1.05u pd=1.05u
M5 3 2 1 1 MOSP W=0.8u L=.35u ps=1.05u pd=1.05u
M6 7 8 1 1 MOSP W=0.8u L=.35u ps=1.05u pd=1.05u
M7 10 2 1 1 MOSP W=0.8u L=.35u ps=1.05u pd=1.05u
M8 14 8 1 1 MOSP W=0.8u L=.35u ps=1.25u pd=1.25u
M9 5 4 3 3 MOSN W=0.8u L=.35u ps=1.25u pd=1.25u
M10 5 6 7 7 MOSN W=0.8u L=.35u ps=1.25u pd=1.25u
M11 12 6 10 10 MOSN W=0.8u L=.35u ps=1.25u pd=1.25u
M12 12 4 14 14 MOSN W=0.8u L=.35u ps=1.25u pd=1.25u


VDD 1 0 DC 1.5 V

v1 2 0 dc 0.5
v2 4 0  dc 1.5
v3 8 0 dc 0.5
v4 6 0 dc 1.5
.op
.dc v1 300mv 700mv 50mV v2 -0.2 0.2 0.1
.print dc v (5,12)

.end
```

Net list for Analog multiplier architecture 2

```
M1  3 8 7 7 MOSP W=0.7u L=2u PD=2.1 PS=2.1
M2  5 6 7 7 MOSP W=0.7u L=2u PD=2.1 PS=2.1
M3  10 6 12 12 MOSP W=0.7u L=2u PD=2.1 PS=2.1
M4  14 8 12 12 MOSP W=0.7u L=2u PD=2.1 PS=2.1
M5  0 4 3 3 MOSP W=3u L=0.7u PD=6.1 PS=6.1
M6  0 4 5 5 MOSP W=3u L=0.7u PD=6.1 PS=6.1
M7  0 15 10 10 MOSP W=3u L=0.7u PD=6.1 PS=6.1
M8  0 15 14 14 MOSP W=3u L=0.7u PD=6.1 PS=6.1
M9  2 3 0 0 MOSN W=2u L=0.5u PD=4.1 PS=4.1
M10 9 5 0 0 MOSN W=2u L=0.5u PD=4.1 PS=4.1
M11 2 10 0 0 MOSN W=2u L=0.5u PD=4.1 PS=4.1
M12 9 14 0 0 MOSN W=2u L=0.5u PD=4.1 PS=4.1
```

```
I1 1 7 10u
I2 1 12 10u


R1 1 2  5k
R2 1 9  5k
VDD 1 0 DC 1.2 V

v1 4 0 SIN (0 0.4 1k)
v2 15 0 SIN (0 -0.4 1k)
v3 8 0 SIN (0 0.4 5M)
v4 6 0 SIN (0 -0.4 5M)

.op

v1 4 0 DC 0.4 AC 1
v2 15 0 DC 0
*v3 8 0 DC 0.3
*v4 6 0 DC 0
*.print ac {v(11)-v(6)}
.tran 0.1m 3m start=0
.four 5M 10 interpolate=1

*.print tran v(4,0) v(8,0) v(2,9)
*.dc v2 -0.4 0.4 0.1 v3 -0.4 0.4 0.1
*.print dc v(2,9)
.end
```

Net list for Analog multiplier using Triode MOSFETs

```
M1 5 2 1 1 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M2 2 4 5 5 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M3 7 8 1 1 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M4 8 9 7 7 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M5 11 12 1 1 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M6 12 4 11 11 MOSP W=3u L=0.2u ps=32.5u pd=32.5u
M7 3 2 1 1 MOSP W=2u L=0.2u ps=22.2u pd=22.2u
M8 13 12 1 1 MOSP W=2u L=0.2u ps=22.2u pd=22.2u
Mx 5 6 7 1 MOSP W=0.4u L=1.2u ps=16.05u pd=16.05u
My 7 10 11 1 MOSP W=0.4u L=1.2u ps=16.05u pd=16.05u



R1 3 0 50k
R2 13 0 50k

I1 2 0 5uA
I2 8 0 5uA
I3 12 0 5uA

vdd 1 0 1.2V


V1 6 0 dc 0.2 sin(0 0.4 10k)
V2 10 0 dc 0 sin(0 -0.4 10k)
```

```
V3 4 0 dc 0.2 sin(0 0.4 2k)
V4 9 0 dc 0.2 sin(0 -0.4 2k)

.op
.dc V1 -400mV 400mV 100mV  V3 -400mV 400mV 100mV
.print dc v(3,13)

*.tran 0.1m 3m start=0
*.print tran v(6,0) v(4,0) v(3,13)
.probe
.end
```

Net list for Analog multiplier architecture 3

```
M1  3 2 1 1 MOSP W=1u L=1u PD=2.1 PS=2.1
M2  0 2 3 3 MOSP W=3u L=1u PD=6.1 PS=6.1
M3  4 3 5 5 MOSN W=1u L=1u PD=2.1 PS=2.1
M4  5 4 1 1 MOSP W=70u L=1u PD=140.1 PS=140.1
M5  7 6 1 1 MOSP W=1u L=1u PD=2.1 PS=2.1
M6  0 6 7 7 MOSP W=3u L=1u PD=6.1 PS=6.1
M7  8 7 5 5 MOSN W=1u L=2u PD=2.1 PS=2.1
M8  9 10 5 5 MOSN W=1u L=2u PD=2.1 PS=2.1
M9  8 10 11 11 MOSN W=1u L=2u PD=2.1 PS=2.1
M10 9 7 11 11 MOSN W=1u L=2u PD=2.1 PS=2.1
M11 10 12 1 1 MOSP W=1u L=1u PD=2.1 PS=2.1
M12 0 12 10 10 MOSP W=3u L=1u PD=6.1 PS=6.1
M13 11 13 1 1 MOSP W=70u L=1u PD=140.1 PS=140.1
M14 13 14 11 11 MOSN W=1u L=1u PD=2.1 PS=2.1
M15 14 15 1 1 MOSP W=1u L=1u PD=2.1 PS=2.1
M16 0 15 14 14 MOSP W=3u L=1u PD=6.1 PS=6.1

I1 1 4 70u
I2 5 0 210u
I3 1 13 70u
I4 11 0 210u

R1 1 8 5k
R2 1 9 5k
VDD 1 0 DC 1.5 V

v1 6 0 SIN (0 1.0 1k)
v2 12 0 SIN (0 -1.0 1k)
v3 2 0 SIN (0 1.0 50k)
v4 15 0 SIN (0 -1.0 50k)
*.ac dec 20 100 100g
.op

*.print ac {v(11)-v(6)}
.tran 0.1m 5m start=0
.print tran v (6,0) v(2,0) v(8,9)
.end
```

Net list for Analog multiplier using nMOS transistor

```
M1 1 2 3 3 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M2 8 9 3 3 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
```

```
M3 1 0 5 5 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M4 7 0 5 5 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M5 16 9 18 18 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M6 1 0 18 18 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M7 15 0 17 17 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M8 1 2 17 17 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M9 1 1 7 7 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M10 1 1 8 8 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M11 1 1 16 16 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M12 1 1 15 15 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M13 1 8 10 10 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M14 1 7 10 10 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M15 1 15 14 14 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M16 1 16 14 14 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u

M17 10 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M18 14 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M19 3 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M20 5 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M21 11 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M22 17 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M23 18 19 20 20 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M24 12 10 11 11 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u
M25 13 14 11 11 MOSN W=5.6u L=2.8u ps=15.5u pd=15.5u

M26 1 1 12 12 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u
M27 1 1 13 13 MOSN W=2.8u L=2.8u ps=6.5u pd=6.5u

vdd 1 0 1.8V
Vb 19 0 1V
vss 20 0 -1.8V

V1 2 0 DC 1 SIN(0 0.25 25k)
V2 9 0 DC 1 SIN(0 0.25 1k)

.dc V1 -1.2 1.2 0.2 V2 -1.2 1.2 0.2
.print dc v(12,13)

*.tran 0.1m 4m start=0
*.PRINT v(2,0),v(9,0),v(12,13)
*.ac dec 10
.op
.end
```

Net list for proposed Analog multiplier:

```
M1 2 3 0 0 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M2 1 1 2 2 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M3 5 4 0 0 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M4 1 2 5 5 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M5 6 7 0 0 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M6 1 1 6 6 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M7 9 8 0 0 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M8 1 6 9 9 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M9 10 3 0 0 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M10 1 1 10 10 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
```

```
M11 13 8 0 0 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M12 1 10 13 13 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M13 14 7 0 0 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M14 1 1 14 14 MOSN W=20u L=0.2u ps=400.5u pd=400.5u
M15 17 4 0 0 MOSP W=25u L=0.2u ps=400.5u pd=400.5u
M16 1 14 17 17 MOSP W=25u L=0.2u ps=400.5u pd=400.5u

M17 18 5 0 0 MOSN W=0.4u L=0.3u ps=5.5u pd=10.5u
M18 18 9 0 0 MOSN W=0.4u L=0.3u ps=5.5u pd=10.5u
M19 19 13 0 0 MOSN W=0.4u L=0.3u ps=5.5u pd=10.5u
M20 19 17 0 0 MOSN W=0.4u L=0.3u ps=5.5u pd=10.5u
M21 1 1 18 18 MOSN W=25u L=5u ps=5.5u pd=10.5u
M22 1 1 19 19 MOSN W=25u L=5u ps=5.5u pd=10.5u

vdd 1 0 1.5V

*V1 3 0 DC 0 SIN (0 0.4 1k)
*V2 7 0 DC 0 SIN (0 -0.4 1k)
*V3 4 0 DC 0 SIN (0 0.4 25k)
*V4 8 0 DC 0 SIN (0 -0.4 25k)

V1 3 0 DC 1
V2 7 0 DC 0
V3 4 0 DC -1
V4 8 0 DC 0.2

.dc V1 -400mV 400mV 100mV V3 -400mV 400mV 100mV
.PRINT DC V (19,18)
.op

*.tran 0.1m 3m start=0
*.print tran v (19,18)
.probe
.end
```

Appendix B

Codes in Eldo using Mentor Graphics

Proposed Adder Using Eldo:

```
   17          v3 n$5 ground DC 1.5V
   18          v2 y ground SIN ( 0 0.4v 10k 0 0 )
   19          v1 x ground SIN ( 0 1v 1k 0 0 )
   20          M4 GROUND Y Z Z P L=0.8U W=10U M=1
   21          M3 Z N$4 N$5 N$5 P L=0.8U W=10U M=1
   22          M2 N$4 X GROUND GROUND N L=0.5U W=2U M=1
   23          M1 N$5 N$5 N$4 N$4 N L=0.5U W=2U M=1
   24  *
   25  *end
    2
    3  .LIB $ADK/technology/accusim/ami05.mod
    4  ** INCLUDING LIBRARY
/home/software/FOUNDRY/adk3_0/technology/accusim/ami05.mod
    1  * DATE: Jan 25/99
    2  * LOT: n8bn                  WAF: 03
    3  * Temperature_parameters=Default
    4  * ***temp fix*** .lib NOM
    5  .MODEL NOTCHEDROW C
    6  .MODEL HR R
    7  .MODEL N NMOS (           LEVEL   = 53
    8  +VERSION = 3.1            TNOM    = 27            TOX     =
1.41E-8
    9  +XJ      = 1.5E-7         NCH     = 1.7E17        VTH0    =
0.7086
   10  +K1      = 0.8354582      K2      = -0.088431     K3      =
41.4403818
   11  +K3B     = -14            W0      = 6.480766E-7   NLX     = 1E-
10
   12  +DVT0W   = 0              DVT1W   = 5.3E6         DVT2W   = -
0.032
   13  +DVT0    = 3.6139113      DVT1    = 0.3795745     DVT2    = -
0.1399976
   14  +U0      = 533.6953445    UA      = 7.558023E-10  UB      =
1.181167E-18
   15  +UC      = 2.582756E-11   VSAT    = 1.300981E5    A0      =
0.5292985
   16  +AGS     = 0.1463715      B0      = 1.283336E-6   B1      =
1.408099E-6
   17  +KETA    = -0.0173166     A1      = 0             A2      = 1
   18  +RDSW    = 2.268366E3     PRWG    = -1E-3         PRWB    =
6.320549E-5
   19  +WR      = 1              WINT    = 2.043512E-7   LINT    =
3.034496E-8
   20  +XL      = 0              XW      = 0             DWG     = -
1.446149E-8
```

```
   21  +DWB     = 2.077539E-8    VOFF    = -0.1137226     NFACTOR =
1.2880596
   22  +CIT     = 0              CDSC    = 1.506004E-4    CDSCD   = 0
   23  +CDSCB   = 0              ETA0    = 3.815372E-4    ETAB    = -
1.029178E-3
   24  +DSUB    = 2.173055E-4    PCLM    = 0.6171774      PDIBLC1 =
0.185986
   25  +PDIBLC2 = 3.473187E-3    PDIBLCB = -1E-3          DROUT   =
0.4037723
   26  +PSCBE1  = 5.998012E9     PSCBE2  = 3.788068E-8    PVAG    =
0.012927
   27  +DELTA   = 0.01           MOBMOD  = 1              PRT     = 0
   28  +UTE     = -1.5           KT1     = -0.11          KT1L    = 0
   29  +KT2     = 0.022          UA1     = 4.31E-9        UB1     = -
7.61E-18
   30  +UC1     = -5.6E-11       AT      = 3.3E4          WL      = 0
   31  +WLN     = 1              WW      = 0              WWN     = 1
   32  +WWL     = 0              LL      = 0              LLN     = 1
   33  +LW      = 0              LWN     = 1              LWL     = 0
   34  +CAPMOD  = 2              XPART   = 0.4            CGDO    =
1.99E-10
   35  +CGSO    = 1.99E-10       CGBO    = 0              CJ      =
4.233802E-4
   36  +PB      = 0.9899238      MJ      = 0.4495859      CJSW    =
3.825632E-10
   37  +PBSW    = 0.1082556      MJSW    = 0.1083618      PVTH0   =
0.0212852
   38  +PRDSW   = -16.1546703    PK2     = 0.0253069      WKETA   =
0.0188633
   39  +LKETA   = 0.0204965       )
   40  *
   41  .MODEL P PMOS (                                LEVEL   = 53
   42  +VERSION = 3.1            TNOM    = 27             TOX     =
1.41E-8
   43  +XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -
0.9179952
   44  +K1      = 0.5575604      K2      = 0.010265       K3      =
14.0655075
   45  +K3B     = -2.3032921     W0      = 1.147829E-6    NLX     =
1.114768E-10
   46  +DVT0W   = 0              DVT1W   = 5.3E6          DVT2W   = -
0.032
   47  +DVT0    = 2.2896412      DVT1    = 0.5213085      DVT2    = -
0.1337987
   48  +U0      = 202.4540953    UA      = 2.290194E-9    UB      =
9.779742E-19
   49  +UC      = -3.69771E-11   VSAT    = 1.307891E5     A0      =
0.8356881
   50  +AGS     = 0.1568774      B0      = 2.365956E-6    B1      = 5E-
6
   51  +KETA    = -5.769328E-3   A1      = 0              A2      = 1
   52  +RDSW    = 2.746814E3     PRWG    = 2.34865E-3     PRWB    =
0.0172298
   53  +WR      = 1              WINT    = 2.586255E-7    LINT    =
7.205014E-8
   54  +XL      = 0              XW      = 0              DWG     = -
2.133054E-8
```

```
   55  +DWB     = 9.857534E-9    VOFF    = -0.0837499     NFACTOR =
1.2415529
   56  +CIT     = 0              CDSC    = 4.363744E-4    CDSCD   = 0
   57  +CDSCB   = 0              ETA0    = 0.11276        ETAB    = -
2.9484E-3
   58  +DSUB    = 0.3389402      PCLM    = 4.9847806      PDIBLC1 =
2.481735E-5
   59  +PDIBLC2 = 0.01           PDIBLCB = 0              DROUT   =
0.9975107
   60  +PSCBE1  = 3.497872E9     PSCBE2  = 4.974352E-9    PVAG    =
10.9914549
   61  +DELTA   = 0.01           MOBMOD  = 1              PRT     = 0
   62  +UTE     = -1.5           KT1     = -0.11          KT1L    = 0
   63  +KT2     = 0.022          UA1     = 4.31E-9        UB1     = -
7.61E-18
   64  +UC1     = -5.6E-11       AT      = 3.3E4          WL      = 0
   65  +WLN     = 1              WW      = 0              WWN     = 1
   66  +WWL     = 0              LL      = 0              LLN     = 1
   67  +LW      = 0              LWN     = 1              LWL     = 0
   68  +CAPMOD  = 2              XPART   = 0.4            CGDO    =
2.4E-10
   69  +CGSO    = 2.4E-10        CGBO    = 0              CJ      =
7.273568E-4
   70  +PB      = 0.9665597      MJ      = 0.4959837      CJSW    =
3.114708E-10
   71  +PBSW    = 0.99           MJSW    = 0.2653654      PVTH0   =
9.420541E-3
   72  +PRDSW   = -231.2571566   PK2     = 1.396684E-3    WKETA   =
1.862966E-3
   73  +LKETA   = 5.728589E-3     )
   74  * ***temp fix*** .ENDL
   75  *END
    4  ** END OF LIBRARY
/home/software/FOUNDRY/adk3_0/technology/accusim/ami05.mod
    4  .PLOT TRAN  V(Z)  V(X)  V(Y)
    5
    6
    7  .OPTION NOASCII
    8  .OPTION MODWL
    9  .OPTION ENGNOT
   10  .OPTION AEX
   11  .OPTION LIMPROBE = 10000
   12  .TRAN  0 5m 0
   13  .END

End of file


***** 0  error(s).
***** 0  warning(s).
INFORMATION ABOUT COMPILATION


Memory space allocated (bytes): 3518713
7 elements
5 nodes
3 input signals
```

```
Detail about objects and nodes found in the design...
Number of nodes                     5
Number of intrinsic nodes           0
Number of input signals             3
Number of resistors                 0
Number of floating capacitors       0
Number of grounded capacitors       0
Number of inductors                 0
Number of voltage sources           3
Number of current sources           0
Number of dependent sources         0
Number of diodes                    0
Number of BJT                       0
Number of JFET                      0
Number of MOS                       4
Number of SWITCHES                  0
Number of transmission lines        0
Total number of elements            7

Eldo VERSION : ELDO 2008.1 Production Mon Jun 30 08:51:48 GMT 2008


TEMPERATURE : 27.000000 degrees C

1***************23-Apr-2009 **********************  ELDO 2008.1
Production  (v6.11_1.1)
**********************14:01:45*****************

0* Component: /home/neeti/labs/ami/add  V
0****                  MODELS PARAMETERS
TEMPERATURE =   27.000 DEG C

0*********************************************************************
************************************************
 DEVICE          MOS
 MODEL: N
 TYPE            N
 LEVEL 53 : Bsim3v3 version 3.1

  names    values    units     names    values    units     names
values    units
  -----    ------    -----     -----    ------    -----     -----    --
----    -----
VER     = 3.1000E+00 -       MOBMOD  = 1          -       CAPMOD  = 2
-
VFBFLAG = 0          -       NQSMOD  = 0          -       NOIMOD  = 1
-
DERIV   = 1          -       BINFLAG = 0          -       PARAMCHK= 0
-
IIMOD   = 0          -       FNLEV   = 0          -

 * Threshold voltage related model parameters *
   ----------------------------------------
VTH0    = 7.0860E-01 V       DELVTO  = 0.0        V       K1      =
8.3546E-01 V^1/2
K2      =-8.8431E-02 -       NCH     = 1.7000E+17 At/cm^3 K3      =
4.1440E+01 -
```

```
K3B     =-1.4000E+01 1/V     DVT0    = 3.6139E+00 -       DVT1    =
3.7957E-01 -
DVT2    =-1.4000E-01 1/V     DVT0W   = 0.0        -       DVT1W   =
5.3000E+06 1/m
DVT2W   =-3.2000E-02 1/V     DSUB    = 2.1731E-04 -       ETA0    =
3.8154E-04 -
ETAB    =-1.0292E-03 1/V

 * Subthreshold related parameters *
   -------------------------------
NFACTOR = 1.2881E+00 -       CDSC    = 1.5060E-04 F/m^2   CDSCB   = 0.0
F/Vm^2
CDSCD   = 0.0        F/Vm^2  VOFF    =-1.1372E-01 V       CIT     = 0.0
F/m^2

 * Mobility related model parameters *
   ---------------------------------
UA      = 7.5580E-10 m/V     UB      = 1.1812E-18 (m/V)^2 UC      =
2.5828E-11 m/V^2
U0      = 5.3370E-02 unit1

 * Saturation related parameters *
   -----------------------------
PCLM    = 6.1718E-01 -       KETA    =-1.7317E-02 1/V     DELTA   =
1.0000E-02 V
A0      = 5.2930E-01 -       A1      = 0.0        1/V     A2      =
1.0000E+00 -
B0      = 1.2833E-06 m       B1      = 1.4081E-06 m       PVAG    =
1.2927E-02 -
PDIBLC1 = 1.8599E-01 -       PDIBLC2 = 3.4732E-03 -       PDIBLCB =-
1.0000E-03 1/V
DROUT   = 4.0377E-01 -       VSAT    = 1.3010E+05 m/s     PSCBE1  =
5.9980E+09 V/m
PSCBE2  = 3.7881E-08 m/V     PRWB    = 6.3205E-05 V^-1/2  PRWG    =-
1.0000E-03 1/V
RDSW    = 2.2684E+03 Ohm.um  AGS     = 1.4637E-01 1/V

 * Geometry modulation related parameters *
   --------------------------------------
LREF    = 0.0        m       WREF    = 0.0        m       LINT    =
3.0345E-08 m
DLC     = 3.0345E-08 m       LL      = 0.0        m       LW      = 0.0
m
LWL     = 0.0        m       LLN     = 1.0000E+00 -       LWN     =
1.0000E+00 -
WINT    = 2.0435E-07 m       DWC     = 2.0435E-07 m       WL      = 0.0
m
WW      = 0.0        m       WWL     = 0.0        m       WLN     =
1.0000E+00 -
WWN     = 1.0000E+00 -       WR      = 1.0000E+00 -       W0      =
6.4808E-07 m
DWG     =-1.4461E-08 m/V     DWB     = 2.0775E-08 m/V^1/2

 * Temperature effect parameters *
   -----------------------------
UPDATEPHI= 0          -       AT      = 3.3000E+04 m/sec   UTE     =-
1.5000E+00 -
```

```
KT1     =-1.1000E-01 V       KT2     = 2.2000E-02 -       KT1L    = 0.0
mV
UA1     = 4.3100E-09 m/V     UB1     =-7.6100E-18 (m/V)^2 UC1     =-
5.6000E-11 m/V^2
PRT     = 0.0        Ohm.um  RDSWTPOS= 1          -

 * Overlap capacitance related and dynamic model parameters *
   ---------------------------------------------------------
XPART   = 4.0000E-01 -       CLC     = 1.0000E-07 m       CLE     =
6.0000E-01 -
CGDO    = 1.9900E-10 F/m     CGDL    = 0.0        F/m     CGSO    =
1.9900E-10 F/m
CGSL    = 0.0        F/m     CGBO    = 0.0        F/m     CKAPPA  =
6.0000E-01 V
CF      = 7.4302E-11 F/m     ELM     = 5.0000E+00 -       VFBCV   =-
1.0000E+00 -

 * Substrate current related model parameters *
   -------------------------------------------
ALPHA0  = 0.0        m/V     BETA0   = 3.0000E+01 V

 * Process and parameters extraction related model parameters *
   -------------------------------------------------------------
TOX     = 1.4100E-08 m       DTOXCV  = 0.0        m       NGATE   = 0.0
At/cm^3
NLX     = 1.0000E-10 m       XL      = 0.0        m       XW      = 0.0
m
ND      = 1.0000E+20 At/cm^3

 * Noise effect related model parameters *
   --------------------------------------
THMLEV  = 0          -       FLKLEV  = 0          -       AF      =
1.0000E+00 -
KF      = 0.0        -       EF      = 1.0000E+00 -       NSTAR   =
2.0000E+14 -
FLKFLAG = 0.0        -       NOIFLAG = 0.0        -       NOIA    =
1.0000E+20 unit2
NOIB    = 5.0000E+04 1/V     NOIC    =-1.4000E-12 unit3   EM      =
4.1000E+07 V/m

 * Sidewall parasitic capacitances at gate side *
   ---------------------------------------------
MJSWG   = 1.0836E-01 -       PBSWG   = 1.0826E-01 V       CJSWG   =
3.8256E-10 F/m
WPEMOD  = 0.0        -       SCREF   = 1.0000E-06 m       KVTH0WE = 0.0
V
K2WE    = 0.0        -       KU0WE   = 0.0        -       WEB     = 0.0
-
WEC     = 0.0        -

 * Binning Parameters *
   -------------------
BINUNIT = 1.0000E+00 -
* Display only non null Binning Parameters *
PK2     = 2.5307E-02 -       LKETA   = 2.0497E-02 -       WKETA   =
1.8863E-02 -
PRDSW   =-1.6155E+01 -       PVTH0   = 2.1285E-02 -
```

```
   ----------------------------------------------------------------------
----

 *** Common extrinsic model parameters ***
OPTACM  = 0          -       ALEV    = 0          -       RLEV    = 4
-
 * Access resistances related parameters *
RD      = 0.0        Ohm     RS      = 0.0        Ohm     RSH     = 0.0
Ohm/Sq.
RDC     = 0.0        Ohm     RSC     = 0.0        Ohm
 * Geometry related parameters *
LD      = 3.0345E-08 m       WD      = 2.0435E-07 m       DL      = 0.0
m
DW      = 0.0        m       LDIF    = 0.0        m       HDIF    = 0.0
m
WMLT    = 1.0000E+00 -       LMLT    = 1.0000E+00 -       DEL     = 0.0
m
XJ      = 1.5000E-07 m
 * Static bulk-diode related parameters *
DIOLEV  = 6          -       JS      = 1.0000E-04 A/m^2   JSW     = 0.0
A/m
IS      = 1.0000E-14 A       NJ      = 1.0000E+00 -       NDS     =
1.0000E+00 -
VNDS    =-1.0000E+00 V       VDLIN   = 5.0000E-01 -
 * Dynamic bulk-diode related parameters *
DCAPLEV = 4          -       CJGATE  = 0.0                CBD     = 0.0
F
CBS     = 0.0        F       CJ      = 4.2338E-04 F/m^2   CJSW    =
3.8256E-10 F/m
FC      = 0.0        -       MJ      = 4.4959E-01 -       MJSW    =
1.0836E-01 -
TT      = 0.0        s       PB      = 9.8992E-01 V       PBSW    =
1.0826E-01 V
 * Temperature related Parameters
EG      = 1.1100E+00 eV      GAP1    = 7.0200E-04 eV/degK GAP2    =
1.1080E+03 degK
TNOM    = 2.7000E+01 degC    TLEV    = 0          -       TLEVC   = 0
-
TLEVI   = 3          -       XTI     = 3.0000E+00 -
 * Temperature Access Resistance related parameters * TLEVR = 1
TRD1    = 0.0        1/degK  TRS1    = 0.0        1/degK  TRSH1   = 0.0
1/degK
TRD2    = 0.0        unit4   TRS2    = 0.0        unit4   TRSH2   = 0.0
unit4

unit1 represents m^2/V/sec
unit2 represents V^-1.m^-2
unit3 represents V^-1.m^2
unit4 represents 1/degK^2

 DEVICE          MOS
 MODEL: P
 TYPE            P
 LEVEL 53 : Bsim3v3 version 3.1

  names    values    units     names    values    units     names
values    units
```

```
  -----    ------    -----     -----    ------    -----     -----    --
----    -----
VER     = 3.1000E+00 -       MOBMOD  = 1          -       CAPMOD  = 2
-
VFBFLAG = 0          -       NQSMOD  = 0          -       NOIMOD  = 1
-
DERIV   = 1          -       BINFLAG = 0          -       PARAMCHK= 0
-
IIMOD   = 0          -       FNLEV   = 0          -

 * Threshold voltage related model parameters *
   ----------------------------------------
VTH0    =-9.1800E-01 V       DELVTO  = 0.0        V       K1      =
5.5756E-01 V^1/2
K2      = 1.0265E-02 -       NCH     = 1.7000E+17 At/cm^3 K3      =
1.4066E+01 -
K3B     =-2.3033E+00 1/V     DVT0    = 2.2896E+00 -       DVT1    =
5.2131E-01 -
DVT2    =-1.3380E-01 1/V     DVT0W   = 0.0        -       DVT1W   =
5.3000E+06 1/m
DVT2W   =-3.2000E-02 1/V     DSUB    = 3.3894E-01 -       ETA0    =
1.1276E-01 -
ETAB    =-2.9484E-03 1/V

 * Subthreshold related parameters *
   -------------------------------
NFACTOR = 1.2416E+00 -       CDSC    = 4.3637E-04 F/m^2   CDSCB   = 0.0
F/Vm^2
CDSCD   = 0.0        F/Vm^2  VOFF    =-8.3750E-02 V       CIT     = 0.0
F/m^2

 * Mobility related model parameters *
   ---------------------------------
UA      = 2.2902E-09 m/V     UB      = 9.7797E-19 (m/V)^2 UC      =-
3.6977E-11 m/V^2
U0      = 2.0245E-02 unit1

 * Saturation related parameters *
   -----------------------------
PCLM    = 4.9848E+00 -       KETA    =-5.7693E-03 1/V     DELTA   =
1.0000E-02 V
A0      = 8.3569E-01 -       A1      = 0.0        1/V     A2      =
1.0000E+00 -
B0      = 2.3660E-06 m       B1      = 5.0000E-06 m       PVAG    =
1.0991E+01 -
PDIBLC1 = 2.4817E-05 -       PDIBLC2 = 1.0000E-02 -       PDIBLCB = 0.0
1/V
DROUT   = 9.9751E-01 -       VSAT    = 1.3079E+05 m/s     PSCBE1  =
3.4979E+09 V/m
PSCBE2  = 4.9744E-09 m/V     PRWB    = 1.7230E-02 V^-1/2  PRWG    =
2.3486E-03 1/V
RDSW    = 2.7468E+03 Ohm.um  AGS     = 1.5688E-01 1/V

 * Geometry modulation related parameters *
   --------------------------------------
LREF    = 0.0        m       WREF    = 0.0        m       LINT    =
7.2050E-08 m
```

```
DLC     = 7.2050E-08 m       LL      = 0.0        m       LW      = 0.0
m
LWL     = 0.0        m       LLN     = 1.0000E+00 -       LWN     =
1.0000E+00 -
WINT    = 2.5863E-07 m       DWC     = 2.5863E-07 m       WL      = 0.0
m
WW      = 0.0        m       WWL     = 0.0        m       WLN     =
1.0000E+00 -
WWN     = 1.0000E+00 -       WR      = 1.0000E+00 -       W0      =
1.1478E-06 m
DWG     =-2.1331E-08 m/V     DWB     = 9.8575E-09 m/V^1/2

 * Temperature effect parameters *
   ----------------------------
UPDATEPHI= 0          -       AT      = 3.3000E+04 m/sec   UTE     =-
1.5000E+00 -
KT1     =-1.1000E-01 V       KT2     = 2.2000E-02 -       KT1L    = 0.0
mV
UA1     = 4.3100E-09 m/V     UB1     =-7.6100E-18 (m/V)^2 UC1     =-
5.6000E-11 m/V^2
PRT     = 0.0        Ohm.um  RDSWTPOS= 1          -

 * Overlap capacitance related and dynamic model parameters *
   ---------------------------------------------------------
XPART   = 4.0000E-01 -       CLC     = 1.0000E-07 m       CLE     =
6.0000E-01 -
CGDO    = 2.4000E-10 F/m     CGDL    = 0.0        F/m     CGSO    =
2.4000E-10 F/m
CGSL    = 0.0        F/m     CGBO    = 0.0        F/m     CKAPPA  =
6.0000E-01 V
CF      = 7.4302E-11 F/m     ELM     = 5.0000E+00 -       VFBCV   =-
1.0000E+00 -

 * Substrate current related model parameters *
   -------------------------------------------
ALPHA0  = 0.0        m/V     BETA0   = 3.0000E+01 V

 * Process and parameters extraction related model parameters *
   -----------------------------------------------------------
TOX     = 1.4100E-08 m       DTOXCV  = 0.0        m       NGATE   = 0.0
At/cm^3
NLX     = 1.1148E-10 m       XL      = 0.0        m       XW      = 0.0
m
ND      = 1.0000E+20 At/cm^3

 * Noise effect related model parameters *
   --------------------------------------
THMLEV  = 0          -       FLKLEV  = 0          -       AF      =
1.0000E+00 -
KF      = 0.0        -       EF      = 1.0000E+00 -       NSTAR   =
2.0000E+14 -
FLKFLAG = 0.0        -       NOIFLAG = 0.0        -       NOIA    =
9.9000E+18 unit2
NOIB    = 2.4000E+03 1/V     NOIC    = 1.4000E-12 unit3   EM      =
4.1000E+07 V/m

 * Sidewall parasitic capacitances at gate side *
```

```
   ------------------------------------------
MJSWG   = 2.6537E-01 -       PBSWG   = 9.9000E-01 V       CJSWG   =
3.1147E-10 F/m
WPEMOD  = 0.0        -       SCREF   = 1.0000E-06 m       KVTH0WE = 0.0
V
K2WE    = 0.0        -       KU0WE   = 0.0        -       WEB     = 0.0
-
WEC     = 0.0        -

 * Binning Parameters *
   -------------------
BINUNIT = 1.0000E+00 -
* Display only non null Binning Parameters *
PK2     = 1.3967E-03 -       LKETA   = 5.7286E-03 -       WKETA   =
1.8630E-03 -
PRDSW   =-2.3126E+02 -       PVTH0   = 9.4205E-03 -
   ---------------------------------------------------------------------
----

 *** Common extrinsic model parameters ***
OPTACM  = 0          -       ALEV    = 0          -       RLEV    = 4
-
 * Access resistances related parameters *
RD      = 0.0        Ohm     RS      = 0.0        Ohm     RSH     = 0.0
Ohm/Sq.
RDC     = 0.0        Ohm     RSC     = 0.0        Ohm
 * Geometry related parameters *
LD      = 7.2050E-08 m       WD      = 2.5863E-07 m       DL      = 0.0
m
DW      = 0.0        m       LDIF    = 0.0        m       HDIF    = 0.0
m
WMLT    = 1.0000E+00 -       LMLT    = 1.0000E+00 -       DEL     = 0.0
m
XJ      = 1.5000E-07 m
 * Static bulk-diode related parameters *
DIOLEV  = 6          -       JS      = 1.0000E-04 A/m^2   JSW     = 0.0
A/m
IS      = 1.0000E-14 A       NJ      = 1.0000E+00 -       NDS     =
1.0000E+00 -
VNDS    =-1.0000E+00 V       VDLIN   = 5.0000E-01 -
 * Dynamic bulk-diode related parameters *
DCAPLEV = 4          -       CJGATE  = 0.0                CBD     = 0.0
F
CBS     = 0.0        F       CJ      = 7.2736E-04 F/m^2   CJSW    =
3.1147E-10 F/m
FC      = 0.0        -       MJ      = 4.9598E-01 -       MJSW    =
2.6537E-01 -
TT      = 0.0        s       PB      = 9.6656E-01 V       PBSW    =
9.9000E-01 V
 * Temperature related Parameters
EG      = 1.1100E+00 eV      GAP1    = 7.0200E-04 eV/degK GAP2    =
1.1080E+03 degK
TNOM    = 2.7000E+01 degC    TLEV    = 0          -       TLEVC   = 0
-
TLEVI   = 3          -       XTI     = 3.0000E+00 -
 * Temperature Access Resistance related parameters * TLEVR = 1
```

```
TRD1    = 0.0        1/degK  TRS1    = 0.0        1/degK  TRSH1   = 0.0
1/degK
TRD2    = 0.0        unit4   TRS2    = 0.0        unit4   TRSH2   = 0.0
unit4

unit1 represents m^2/V/sec
unit2 represents V^-1.m^-2
unit3 represents V^-1.m^2
unit4 represents 1/degK^2

*** DC Control Options :

GMIN           = 1.00e-12 NMAXSIZE       = 60000    ITL1           =
100
GRAMP          = 0        NETSIZE        = 100      VMIN           =
UNDEF
VMAX           = UNDEF

*** Initial Accuracy Control Options (May be adjusted during
simulation):

ITOL           = 1.00e-06 EPS            = 5.00e-03 VNTOL          =
1.00e-06
RELTOL         = 1.00e-03 RELERR         = 5.00e-02 PIVREL         =
1.00e-03
PIVTOL         = 1.00e-16 ABSTOL         = 1.00e-12 FLXTOL         =
1.00e-11
MAXORD         = 2.00e+00

*** Time-step Control Options :

ZOOMTIME       = 1.00e+00 STEP           = 0.00e+00 STARTSMP       =
0.00e+00
FREQSMP        = 0.00e+00 COURESOL       = 0.00e+00 TRTOL          =
7.00e+00
HMIN           = 1.00e-12 ITL3           = 3        ITL4           = 13
FT             = 1.25e-01 DCLOG          = 1.00e+00 LVLTIM         = 2
LVLCNV         = 2        DVDT           = -1       RELVAR         =
1.50e-01
ABSVAR         = 2.00e-01 SAMPLE         = 0.00e+00 HMAX           =
UNDEF


*** MosFet default Options :

SCALE          = 1.00e+00 SCALM          = 1.00e+00 SCALEBSIM      =
1.00e+00
DEFAD          = UNDEF    DEFAS          = UNDEF    DEFPD          =
UNDEF
DEFPS          = UNDEF    DEFW           = 1.00e-04 DEFL           =
1.00e-04
DEFNRD         = UNDEF    DEFNRS         = UNDEF    XA             =
6.00e-06
LIMRMOS        = UNDEF    SHRINK         = 1.00e+00

*** General Information Options :
```

```
SDA             = 0         CPTIME          = UNDEF     STAT            = 0
TIMEDIV         = 0         SIMUDIV         = 10        SAVETIME        = 0
MAXTRAN         = 1000      MAXNODES        = 10000     MAXV            =
1.00e+13
LIMPROBE        = 10000     FLICKER_NOISE   = 0         THERMAL_NOISE   = 0
TNOM            = 2.70e+01  TMAX            = UNDEF
SPICDC          = 0         SPIOUT          = 0         NEWTON          = 1
OSR             = 0         TRAP            = 1         GEAR            = 0
BE              = 0         PROBEOP         = 0         NOLAT           = 0
NWLAT           = 0         ANALOG          = 0         BBDEBUG         = 0
NOSIZECHK       = 0         QTRUNC          = 0         UNBOUND         = 0
LCAPOP          = 0         NOAEX           = 1         AEX             = 1
AEX             = 1         STVER           = 0         MOTOROLA        = 0
AMS             = 0         ASPEC           = 0         INPUT           = 0
NOINIT          = 0         PSF             = 0         WSF             = 0
WSFASCII        = 0         NOBIN           = 0         NOCOU           = 1
WL              = 0         NODE            = 0         LIST            = 0
SPI3BIN         = 0         SPI3ASC         = 0         NOMOD           = 0
WSF             = 0         WSFASCII        = 0         NOBIN           = 0
NOCOU           = 1         WL              = 0         NODE            = 0
LIST            = 0         SPI3BIN         = 0         SPI3ASC         = 0
NOMOD           = 0         RMOS            = 0         NWRMOS          = 1
NONWRMOS        = 0         USEDEFAP        = 0         NOASCII         = 1
ASCII           = 0         MIXED           = 0         SWITCH          = 0
USERSWITCH      = 0         TIMING          = 0         MODWL           = 1
ULOGIC          = 0


***> DC CPU TIME 0s 000ms <***

DC:15 iterations FOR DC analysis

NODE          VOLTAGE       NODE          VOLTAGE       NODE
VOLTAGE
N$4            1.3625       N$5            1.5000       X
0.0000
Y              0.0000       Z              315.2784M


   VOLTAGE SOURCE CURRENT

NAME       CURRENT       VOLTAGE       POWER
V3         -2.8400P       1.5000       -4.2600P
V2          0.0000        0.0000        0.0000
V1          0.0000        0.0000        0.0000

   TOTAL POWER DISSIPATION:  4.2600P     WATTS
```

Proposed Four Quadrant Analog Multiplier Using Eldo:

```
 17          M8 GROUND V4 N$212 N$212 P L=0.8U W=10U M=1
```

```
   18          M7 N$212 N$211 N$219 N$219 P L=0.8U W=10U M=1
   19          M6 N$211 V3 GROUND GROUND N L=0.5U W=1U M=1
   20          M5 N$219 N$219 N$211 N$211 N L=0.5U W=1U M=1
   21          M4 GROUND V2 N$2 N$2 P L=0.8U W=10U M=1
   22          M3 N$2 N$207 N$219 N$219 P L=0.8U W=10U M=1
   23          M2 N$219 N$219 N$207 N$207 N L=0.5U W=1U M=1
   24          M1 N$207 V1 GROUND GROUND N L=0.5U W=1U M=1
   25          M19 N$219 N$219 N$230 N$230 N L=0.5U W=1U M=1
   26          M20 N$230 V3 GROUND GROUND N L=0.5U W=1U M=1
   27          Y1 sub
   28  +         PIN: N$215 N$3 OUT
   29          V5 N$219 GROUND DC 1.5V
   30          V4 V4 GROUND SIN ( 0 -0.4v 25k 0 0 )
   31          V3 V3 GROUND SIN ( 0 0.4v 25k 0 0 )
   32          V2 V2 GROUND SIN ( 0 -0.4v 1k 0 0 )
   33          V1 V1 GROUND SIN ( 0 0.4v 1k 0 0 )
   34          M22 GROUND V2 N$638 N$638 P L=0.8U W=10U M=1
   35          M21 N$638 N$230 N$219 N$219 P L=0.8U W=10U M=1
   36          M18 GROUND V4 N$434 N$434 P L=0.8U W=10U M=1
   37          M17 N$434 N$220 N$219 N$219 P L=0.8U W=10U M=1
   38          M16 N$220 V1 GROUND GROUND N L=0.5U W=1U M=1
   39          M15 N$219 N$219 N$220 N$220 N L=0.5U W=1U M=1
   40          M14 N$3 N$3 N$219 N$219 P L=2U W=2U M=1
   41          M13 N$3 N$638 GROUND GROUND N L=0.44U W=0.44U M=1
   42          M12 N$3 N$434 GROUND GROUND N L=0.44U W=0.44U M=1
   43          M11 N$215 N$215 N$219 N$219 P L=2U W=2U M=1
   44          M10 N$215 N$212 GROUND GROUND N L=0.44U W=0.44U M=1
   45          M9 N$215 N$2 GROUND GROUND N L=0.45U W=0.45U M=1
   46  *
   47  *end
    2
    3  .LIB $ADK/technology/accusim/ami05.mod
    4  ** INCLUDING LIBRARY
/home/software/FOUNDRY/adk3_0/technology/accusim/ami05.mod
    1  * DATE: Jan 25/99
    2  * LOT: n8bn                  WAF: 03
    3  * Temperature_parameters=Default
    4  * ***temp fix*** .lib NOM
    5  .MODEL NOTCHEDROW C
    6  .MODEL HR R
    7  .MODEL N NMOS (                                LEVEL   = 53
    8  +VERSION = 3.1            TNOM    = 27            TOX     =
1.41E-8
    9  +XJ      = 1.5E-7         NCH     = 1.7E17        VTH0    =
0.7086
   10  +K1      = 0.8354582      K2      = -0.088431     K3      =
41.4403818
   11  +K3B     = -14            W0      = 6.480766E-7   NLX     = 1E-
10
   12  +DVT0W   = 0              DVT1W   = 5.3E6         DVT2W   = -
0.032
   13  +DVT0    = 3.6139113      DVT1    = 0.3795745     DVT2    = -
0.1399976
   14  +U0      = 533.6953445    UA      = 7.558023E-10  UB      =
1.181167E-18
   15  +UC      = 2.582756E-11   VSAT    = 1.300981E5    A0      =
0.5292985
```

```
   16  +AGS      = 0.1463715      B0       = 1.283336E-6    B1       =
1.408099E-6
   17  +KETA     = -0.0173166     A1       = 0              A2       = 1
   18  +RDSW     = 2.268366E3     PRWG     = -1E-3          PRWB     =
6.320549E-5
   19  +WR       = 1              WINT     = 2.043512E-7    LINT     =
3.034496E-8
   20  +XL       = 0              XW       = 0              DWG      = -
1.446149E-8
   21  +DWB      = 2.077539E-8    VOFF     = -0.1137226     NFACTOR =
1.2880596
   22  +CIT      = 0              CDSC     = 1.506004E-4    CDSCD    = 0
   23  +CDSCB    = 0              ETA0     = 3.815372E-4    ETAB     = -
1.029178E-3
   24  +DSUB     = 2.173055E-4    PCLM     = 0.6171774      PDIBLC1 =
0.185986
   25  +PDIBLC2 = 3.473187E-3    PDIBLCB = -1E-3           DROUT    =
0.4037723
   26  +PSCBE1   = 5.998012E9     PSCBE2   = 3.788068E-8    PVAG     =
0.012927
   27  +DELTA    = 0.01           MOBMOD   = 1              PRT      = 0
   28  +UTE      = -1.5           KT1      = -0.11          KT1L     = 0
   29  +KT2      = 0.022          UA1      = 4.31E-9        UB1      = -
7.61E-18
   30  +UC1      = -5.6E-11       AT       = 3.3E4          WL       = 0
   31  +WLN      = 1              WW       = 0              WWN      = 1
   32  +WWL      = 0              LL       = 0              LLN      = 1
   33  +LW       = 0              LWN      = 1              LWL      = 0
   34  +CAPMOD   = 2              XPART    = 0.4            CGDO     =
1.99E-10
   35  +CGSO     = 1.99E-10       CGBO     = 0              CJ       =
4.233802E-4
   36  +PB       = 0.9899238      MJ       = 0.4495859      CJSW     =
3.825632E-10
   37  +PBSW     = 0.1082556      MJSW     = 0.1083618      PVTH0    =
0.0212852
   38  +PRDSW    = -16.1546703    PK2      = 0.0253069      WKETA    =
0.0188633
   39  +LKETA    = 0.0204965       )
   40  *
   41  .MODEL P PMOS (                                LEVEL    = 53
   42  +VERSION = 3.1             TNOM     = 27             TOX      =
1.41E-8
   43  +XJ       = 1.5E-7         NCH      = 1.7E17         VTH0     = -
0.9179952
   44  +K1       = 0.5575604      K2       = 0.010265       K3       =
14.0655075
   45  +K3B      = -2.3032921     W0       = 1.147829E-6    NLX      =
1.114768E-10
   46  +DVT0W    = 0              DVT1W    = 5.3E6          DVT2W    = -
0.032
   47  +DVT0     = 2.2896412      DVT1     = 0.5213085      DVT2     = -
0.1337987
   48  +U0       = 202.4540953    UA       = 2.290194E-9    UB       =
9.779742E-19
   49  +UC       = -3.69771E-11   VSAT     = 1.307891E5     A0       =
0.8356881
```

```
   50  +AGS      = 0.1568774      B0       = 2.365956E-6    B1       = 5E-
6
   51  +KETA     = -5.769328E-3   A1       = 0              A2       = 1
   52  +RDSW     = 2.746814E3     PRWG     = 2.34865E-3     PRWB     =
0.0172298
   53  +WR       = 1              WINT     = 2.586255E-7    LINT     =
7.205014E-8
   54  +XL       = 0              XW       = 0              DWG      = -
2.133054E-8
   55  +DWB      = 9.857534E-9    VOFF     = -0.0837499     NFACTOR =
1.2415529
   56  +CIT      = 0              CDSC     = 4.363744E-4    CDSCD    = 0
   57  +CDSCB    = 0              ETA0     = 0.11276        ETAB     = -
2.9484E-3
   58  +DSUB     = 0.3389402      PCLM     = 4.9847806      PDIBLC1 =
2.481735E-5
   59  +PDIBLC2 = 0.01           PDIBLCB = 0              DROUT    =
0.9975107
   60  +PSCBE1   = 3.497872E9     PSCBE2   = 4.974352E-9    PVAG     =
10.9914549
   61  +DELTA    = 0.01           MOBMOD   = 1              PRT      = 0
   62  +UTE      = -1.5           KT1      = -0.11          KT1L     = 0
   63  +KT2      = 0.022          UA1      = 4.31E-9        UB1      = -
7.61E-18
   64  +UC1      = -5.6E-11       AT       = 3.3E4          WL       = 0
   65  +WLN      = 1              WW       = 0              WWN      = 1
   66  +WWL      = 0              LL       = 0              LLN      = 1
   67  +LW       = 0              LWN      = 1              LWL      = 0
   68  +CAPMOD   = 2              XPART    = 0.4            CGDO     =
2.4E-10
   69  +CGSO     = 2.4E-10        CGBO     = 0              CJ       =
7.273568E-4
   70  +PB       = 0.9665597      MJ       = 0.4959837      CJSW     =
3.114708E-10
   71  +PBSW     = 0.99           MJSW     = 0.2653654      PVTH0    =
9.420541E-3
   72  +PRDSW    = -231.2571566   PK2      = 1.396684E-3    WKETA    =
1.862966E-3
   73  +LKETA    = 5.728589E-3     )
   74  * ***temp fix*** .ENDL
   75  *END
    4  ** END OF LIBRARY
/home/software/FOUNDRY/adk3_0/technology/accusim/ami05.mod
    4  .PLOT TRAN  V(OUT)  V(V1)  V(V2)  V(V3)  V(V4)
    5
    6
    7  .OPTION NOASCII
    8  .OPTION MODWL
    9  .OPTION ENGNOT
   10  .OPTION AEX
   11  .OPTION LIMPROBE = 10000
   12  .TRAN  0 3m 0
   13  .END

End of file
```

```
***** 0  error(s).
***** 0  warning(s).


INFORMATION ABOUT COMPILATION


Memory space allocated (bytes): 3541173
28 elements
16 nodes
5 input signals
Detail about objects and nodes found in the design...
Number of nodes                     16
Number of intrinsic nodes           0
Number of input signals             5
Number of resistors                 0
Number of floating capacitors       0
Number of grounded capacitors       0
Number of inductors                 0
Number of voltage sources           5
Number of current sources           0
Number of dependent sources         0
Number of diodes                    0
Number of BJT                       0
Number of JFET                      0
Number of MOS                       22
Number of SWITCHES                  0
Number of transmission lines        0
CFAS devices                        1
Total number of elements            28

Eldo VERSION : ELDO 2008.1 Production Mon Jun 30 08:51:48 GMT 2008


TEMPERATURE : 27.000000 degrees C

1***************23-Apr-2009 **********************  ELDO 2008.1
Production  (v6.11_1.1)
**********************14:54:44*****************

0* Component: /home/neeti/labs/ami/projec
0****                  MODELS PARAMETERS
TEMPERATURE =   27.000 DEG C

0*********************************************************************
************************************************

 DEVICE          MOS
 MODEL: N
 TYPE            N
 LEVEL 53 : Bsim3v3 version 3.1

  names    values    units     names    values    units     names
values    units
  -----    ------    -----     -----    ------    -----     -----    --
----    -----
```

```
VER     = 3.1000E+00 -       MOBMOD  = 1          -       CAPMOD  = 2
-
VFBFLAG = 0          -       NQSMOD  = 0          -       NOIMOD  = 1
-
DERIV   = 1          -       BINFLAG = 0          -       PARAMCHK= 0
-
IIMOD   = 0          -       FNLEV   = 0          -

 * Threshold voltage related model parameters *
   -------------------------------------------
VTH0    = 7.0860E-01 V       DELVTO  = 0.0        V       K1      =
8.3546E-01 V^1/2
K2      =-8.8431E-02 -       NCH     = 1.7000E+17 At/cm^3 K3      =
4.1440E+01 -
K3B     =-1.4000E+01 1/V     DVT0    = 3.6139E+00 -       DVT1    =
3.7957E-01 -
DVT2    =-1.4000E-01 1/V     DVT0W   = 0.0        -       DVT1W   =
5.3000E+06 1/m
DVT2W   =-3.2000E-02 1/V     DSUB    = 2.1731E-04 -       ETA0    =
3.8154E-04 -
ETAB    =-1.0292E-03 1/V

 * Subthreshold related parameters *
   --------------------------------
NFACTOR = 1.2881E+00 -       CDSC    = 1.5060E-04 F/m^2   CDSCB   = 0.0
F/Vm^2
CDSCD   = 0.0        F/Vm^2  VOFF    =-1.1372E-01 V       CIT     = 0.0
F/m^2

 * Mobility related model parameters *
   ----------------------------------
UA      = 7.5580E-10 m/V     UB      = 1.1812E-18 (m/V)^2 UC      =
2.5828E-11 m/V^2
U0      = 5.3370E-02 unit1

 * Saturation related parameters *
   ------------------------------
PCLM    = 6.1718E-01 -       KETA    =-1.7317E-02 1/V     DELTA   =
1.0000E-02 V
A0      = 5.2930E-01 -       A1      = 0.0        1/V     A2      =
1.0000E+00 -
B0      = 1.2833E-06 m       B1      = 1.4081E-06 m       PVAG    =
1.2927E-02 -
PDIBLC1 = 1.8599E-01 -       PDIBLC2 = 3.4732E-03 -       PDIBLCB =-
1.0000E-03 1/V
DROUT   = 4.0377E-01 -       VSAT    = 1.3010E+05 m/s     PSCBE1  =
5.9980E+09 V/m
PSCBE2  = 3.7881E-08 m/V     PRWB    = 6.3205E-05 V^-1/2  PRWG    =-
1.0000E-03 1/V
RDSW    = 2.2684E+03 Ohm.um  AGS     = 1.4637E-01 1/V

 * Geometry modulation related parameters *
   ---------------------------------------
LREF    = 0.0        m       WREF    = 0.0        m       LINT    =
3.0345E-08 m
DLC     = 3.0345E-08 m       LL      = 0.0        m       LW      = 0.0
m
```

```
LWL     = 0.0        m       LLN     = 1.0000E+00 -       LWN     =
1.0000E+00 -
WINT    = 2.0435E-07 m       DWC     = 2.0435E-07 m       WL      = 0.0
m
WW      = 0.0        m       WWL     = 0.0        m       WLN     =
1.0000E+00 -
WWN     = 1.0000E+00 -       WR      = 1.0000E+00 -       W0      =
6.4808E-07 m
DWG     =-1.4461E-08 m/V     DWB     = 2.0775E-08 m/V^1/2

 * Temperature effect parameters *
   ----------------------------
UPDATEPHI= 0          -       AT      = 3.3000E+04 m/sec   UTE     =-
1.5000E+00 -
KT1     =-1.1000E-01 V       KT2     = 2.2000E-02 -       KT1L    = 0.0
mV
UA1     = 4.3100E-09 m/V     UB1     =-7.6100E-18 (m/V)^2 UC1     =-
5.6000E-11 m/V^2
PRT     = 0.0        Ohm.um  RDSWTPOS= 1          -

 * Overlap capacitance related and dynamic model parameters *
   ---------------------------------------------------------
XPART   = 4.0000E-01 -       CLC     = 1.0000E-07 m       CLE     =
6.0000E-01 -
CGDO    = 1.9900E-10 F/m     CGDL    = 0.0        F/m     CGSO    =
1.9900E-10 F/m
CGSL    = 0.0        F/m     CGBO    = 0.0        F/m     CKAPPA  =
6.0000E-01 V
CF      = 7.4302E-11 F/m     ELM     = 5.0000E+00 -       VFBCV   =-
1.0000E+00 -

 * Substrate current related model parameters *
   -------------------------------------------
ALPHA0  = 0.0        m/V     BETA0   = 3.0000E+01 V

 * Process and parameters extraction related model parameters *
   -----------------------------------------------------------
TOX     = 1.4100E-08 m       DTOXCV  = 0.0        m       NGATE   = 0.0
At/cm^3
NLX     = 1.0000E-10 m       XL      = 0.0        m       XW      = 0.0
m
ND      = 1.0000E+20 At/cm^3

 * Noise effect related model parameters *
   -------------------------------------
THMLEV  = 0          -       FLKLEV  = 0          -       AF      =
1.0000E+00 -
KF      = 0.0        -       EF      = 1.0000E+00 -       NSTAR   =
2.0000E+14 -
FLKFLAG = 0.0        -       NOIFLAG = 0.0        -       NOIA    =
1.0000E+20 unit2
NOIB    = 5.0000E+04 1/V     NOIC    =-1.4000E-12 unit3   EM      =
4.1000E+07 V/m

 * Sidewall parasitic capacitances at gate side *
   --------------------------------------------
```

```
MJSWG   = 1.0836E-01 -       PBSWG   = 1.0826E-01 V       CJSWG   =
3.8256E-10 F/m
WPEMOD  = 0.0        -       SCREF   = 1.0000E-06 m       KVTH0WE = 0.0
V
K2WE    = 0.0        -       KU0WE   = 0.0        -       WEB     = 0.0
-
WEC     = 0.0        -

 * Binning Parameters *
   ------------------
BINUNIT = 1.0000E+00 -
* Display only non null Binning Parameters *
PK2     = 2.5307E-02 -       LKETA   = 2.0497E-02 -       WKETA   =
1.8863E-02 -
PRDSW   =-1.6155E+01 -       PVTH0   = 2.1285E-02 -
   ---------------------------------------------------------------------
----

 *** Common extrinsic model parameters ***
OPTACM  = 0          -       ALEV    = 0          -       RLEV    = 4
-
 * Access resistances related parameters *
RD      = 0.0        Ohm     RS      = 0.0        Ohm     RSH     = 0.0
Ohm/Sq.
RDC     = 0.0        Ohm     RSC     = 0.0        Ohm
 * Geometry related parameters *
LD      = 3.0345E-08 m       WD      = 2.0435E-07 m       DL      = 0.0
m
DW      = 0.0        m       LDIF    = 0.0        m       HDIF    = 0.0
m
WMLT    = 1.0000E+00 -       LMLT    = 1.0000E+00 -       DEL     = 0.0
m
XJ      = 1.5000E-07 m
 * Static bulk-diode related parameters *
DIOLEV  = 6          -       JS      = 1.0000E-04 A/m^2   JSW     = 0.0
A/m
IS      = 1.0000E-14 A       NJ      = 1.0000E+00 -       NDS     =
1.0000E+00 -
VNDS    =-1.0000E+00 V       VDLIN   = 5.0000E-01 -
 * Dynamic bulk-diode related parameters *
DCAPLEV = 4          -       CJGATE  = 0.0                CBD     = 0.0
F
CBS     = 0.0        F       CJ      = 4.2338E-04 F/m^2   CJSW    =
3.8256E-10 F/m
FC      = 0.0        -       MJ      = 4.4959E-01 -       MJSW    =
1.0836E-01 -
TT      = 0.0        s       PB      = 9.8992E-01 V       PBSW    =
1.0826E-01 V
 * Temperature related Parameters
EG      = 1.1100E+00 eV      GAP1    = 7.0200E-04 eV/degK GAP2    =
1.1080E+03 degK
TNOM    = 2.7000E+01 degC    TLEV    = 0          -       TLEVC   = 0
-
TLEVI   = 3          -       XTI     = 3.0000E+00 -
 * Temperature Access Resistance related parameters * TLEVR = 1
TRD1    = 0.0        1/degK  TRS1    = 0.0        1/degK  TRSH1   = 0.0
1/degK
```

```
TRD2    = 0.0        unit4   TRS2    = 0.0        unit4   TRSH2   = 0.0
unit4

unit1 represents m^2/V/sec
unit2 represents V^-1.m^-2
unit3 represents V^-1.m^2
unit4 represents 1/degK^2

 DEVICE          MOS
 MODEL: P
 TYPE            P
 LEVEL 53 : Bsim3v3 version 3.1

  names    values    units     names    values    units     names
values    units
  -----    ------    -----     -----    ------    -----     -----    --
----    -----
VER     = 3.1000E+00 -       MOBMOD  = 1          -       CAPMOD  = 2
-
VFBFLAG = 0          -       NQSMOD  = 0          -       NOIMOD  = 1
-
DERIV   = 1          -       BINFLAG = 0          -       PARAMCHK= 0
-
IIMOD   = 0          -       FNLEV   = 0          -

 * Threshold voltage related model parameters *
   ----------------------------------------
VTH0    =-9.1800E-01 V       DELVTO  = 0.0        V       K1      =
5.5756E-01 V^1/2
K2      = 1.0265E-02 -       NCH     = 1.7000E+17 At/cm^3 K3      =
1.4066E+01 -
K3B     =-2.3033E+00 1/V     DVT0    = 2.2896E+00 -       DVT1    =
5.2131E-01 -
DVT2    =-1.3380E-01 1/V     DVT0W   = 0.0        -       DVT1W   =
5.3000E+06 1/m
DVT2W   =-3.2000E-02 1/V     DSUB    = 3.3894E-01 -       ETA0    =
1.1276E-01 -
ETAB    =-2.9484E-03 1/V

 * Subthreshold related parameters *
   -------------------------------
NFACTOR = 1.2416E+00 -       CDSC    = 4.3637E-04 F/m^2   CDSCB   = 0.0
F/Vm^2
CDSCD   = 0.0        F/Vm^2  VOFF    =-8.3750E-02 V       CIT     = 0.0
F/m^2

 * Mobility related model parameters *
   ---------------------------------
UA      = 2.2902E-09 m/V     UB      = 9.7797E-19 (m/V)^2 UC      =-
3.6977E-11 m/V^2
U0      = 2.0245E-02 unit1

 * Saturation related parameters *
   -----------------------------
PCLM    = 4.9848E+00 -       KETA    =-5.7693E-03 1/V     DELTA   =
1.0000E-02 V
```

```
A0      = 8.3569E-01 -       A1      = 0.0        1/V     A2      =
1.0000E+00 -
B0      = 2.3660E-06 m       B1      = 5.0000E-06 m       PVAG    =
1.0991E+01 -
PDIBLC1 = 2.4817E-05 -       PDIBLC2 = 1.0000E-02 -       PDIBLCB = 0.0
1/V
DROUT   = 9.9751E-01 -       VSAT    = 1.3079E+05 m/s     PSCBE1  =
3.4979E+09 V/m
PSCBE2  = 4.9744E-09 m/V     PRWB    = 1.7230E-02 V^-1/2  PRWG    =
2.3486E-03 1/V
RDSW    = 2.7468E+03 Ohm.um  AGS     = 1.5688E-01 1/V

 * Geometry modulation related parameters *
   ---------------------------------------
LREF    = 0.0        m       WREF    = 0.0        m       LINT    =
7.2050E-08 m
DLC     = 7.2050E-08 m       LL      = 0.0        m       LW      = 0.0
m
LWL     = 0.0        m       LLN     = 1.0000E+00 -       LWN     =
1.0000E+00 -
WINT    = 2.5863E-07 m       DWC     = 2.5863E-07 m       WL      = 0.0
m
WW      = 0.0        m       WWL     = 0.0        m       WLN     =
1.0000E+00 -
WWN     = 1.0000E+00 -       WR      = 1.0000E+00 -       W0      =
1.1478E-06 m
DWG     =-2.1331E-08 m/V     DWB     = 9.8575E-09 m/V^1/2

 * Temperature effect parameters *
   ------------------------------
UPDATEPHI= 0          -       AT      = 3.3000E+04 m/sec   UTE     =-
1.5000E+00 -
KT1     =-1.1000E-01 V       KT2     = 2.2000E-02 -       KT1L    = 0.0
mV
UA1     = 4.3100E-09 m/V     UB1     =-7.6100E-18 (m/V)^2 UC1     =-
5.6000E-11 m/V^2
PRT     = 0.0        Ohm.um  RDSWTPOS= 1          -

 * Overlap capacitance related and dynamic model parameters *
   ----------------------------------------------------------
XPART   = 4.0000E-01 -       CLC     = 1.0000E-07 m       CLE     =
6.0000E-01 -
CGDO    = 2.4000E-10 F/m     CGDL    = 0.0        F/m     CGSO    =
2.4000E-10 F/m
CGSL    = 0.0        F/m     CGBO    = 0.0        F/m     CKAPPA  =
6.0000E-01 V
CF      = 7.4302E-11 F/m     ELM     = 5.0000E+00 -       VFBCV   =-
1.0000E+00 -

 * Substrate current related model parameters *
   --------------------------------------------
ALPHA0  = 0.0        m/V     BETA0   = 3.0000E+01 V

 * Process and parameters extraction related model parameters *
   ------------------------------------------------------------
TOX     = 1.4100E-08 m       DTOXCV  = 0.0        m       NGATE   = 0.0
At/cm^3
```

```
NLX     = 1.1148E-10 m       XL      = 0.0        m       XW      = 0.0
m
ND      = 1.0000E+20 At/cm^3

 * Noise effect related model parameters *
   -------------------------------------
THMLEV  = 0          -       FLKLEV  = 0          -       AF      =
1.0000E+00 -
KF      = 0.0        -       EF      = 1.0000E+00 -       NSTAR   =
2.0000E+14 -
FLKFLAG = 0.0        -       NOIFLAG = 0.0        -       NOIA    =
9.9000E+18 unit2
NOIB    = 2.4000E+03 1/V     NOIC    = 1.4000E-12 unit3   EM      =
4.1000E+07 V/m

 * Sidewall parasitic capacitances at gate side *
   ---------------------------------------------
MJSWG   = 2.6537E-01 -       PBSWG   = 9.9000E-01 V       CJSWG   =
3.1147E-10 F/m
WPEMOD  = 0.0        -       SCREF   = 1.0000E-06 m       KVTH0WE = 0.0
V
K2WE    = 0.0        -       KU0WE   = 0.0        -       WEB     = 0.0
-
WEC     = 0.0        -

 * Binning Parameters *
   -------------------
BINUNIT = 1.0000E+00 -
* Display only non null Binning Parameters *
PK2     = 1.3967E-03 -       LKETA   = 5.7286E-03 -       WKETA   =
1.8630E-03 -
PRDSW   =-2.3126E+02 -       PVTH0   = 9.4205E-03 -
   ---------------------------------------------------------------------
----

 *** Common extrinsic model parameters ***
OPTACM  = 0          -       ALEV    = 0          -       RLEV    = 4
-
 * Access resistances related parameters *
RD      = 0.0        Ohm     RS      = 0.0        Ohm     RSH     = 0.0
Ohm/Sq.
RDC     = 0.0        Ohm     RSC     = 0.0        Ohm
 * Geometry related parameters *
LD      = 7.2050E-08 m       WD      = 2.5863E-07 m       DL      = 0.0
m
DW      = 0.0        m       LDIF    = 0.0        m       HDIF    = 0.0
m
WMLT    = 1.0000E+00 -       LMLT    = 1.0000E+00 -       DEL     = 0.0
m
XJ      = 1.5000E-07 m
 * Static bulk-diode related parameters *
DIOLEV  = 6          -       JS      = 1.0000E-04 A/m^2   JSW     = 0.0
A/m
IS      = 1.0000E-14 A       NJ      = 1.0000E+00 -       NDS     =
1.0000E+00 -
VNDS    =-1.0000E+00 V       VDLIN   = 5.0000E-01 -
 * Dynamic bulk-diode related parameters *
```

```
DCAPLEV = 4          -       CJGATE  = 0.0               CBD     = 0.0
F
CBS     = 0.0        F       CJ      = 7.2736E-04 F/m^2  CJSW    =
3.1147E-10 F/m
FC      = 0.0        -       MJ      = 4.9598E-01 -      MJSW    =
2.6537E-01 -
TT      = 0.0        s       PB      = 9.6656E-01 V      PBSW    =
9.9000E-01 V
 * Temperature related Parameters
EG      = 1.1100E+00 eV      GAP1    = 7.0200E-04 eV/degK GAP2    =
1.1080E+03 degK
TNOM    = 2.7000E+01 degC    TLEV    = 0          -      TLEVC   = 0
-
TLEVI   = 3          -       XTI     = 3.0000E+00 -
 * Temperature Access Resistance related parameters * TLEVR = 1
TRD1    = 0.0        1/degK  TRS1    = 0.0        1/degK  TRSH1   = 0.0
1/degK
TRD2    = 0.0        unit4   TRS2    = 0.0        unit4   TRSH2   = 0.0
unit4

unit1 represents m^2/V/sec
unit2 represents V^-1.m^-2
unit3 represents V^-1.m^2
unit4 represents 1/degK^2


Searching Operating Point between -1.500000E+00V and
                                  3.000000E+00V



1***************23-Apr-2009 **********************  ELDO 2008.1
Production  (v6.11_1.1)
**********************14:54:44*****************

0* Component: /home/neeti/labs/ami/project  Viewpoint: eldonet
0****                  OPTION SUMMARY
TEMPERATURE =   27.000 DEG C

0*************************************************************************
***********************************************
*** DC Control Options :

GMIN           = 1.00e-12 NMAXSIZE       = 60000    ITL1           =
100
GRAMP          = 0        NETSIZE        = 100      VMIN           =
UNDEF
VMAX           = UNDEF

*** Initial Accuracy Control Options (May be adjusted during
simulation):

ITOL           = 1.00e-06 EPS            = 5.00e-03 VNTOL          =
1.00e-06
RELTOL         = 1.00e-03 RELERR         = 5.00e-02 PIVREL         =
1.00e-03
```

```
PIVTOL          = 1.00e-16 ABSTOL          = 1.00e-12 FLXTOL          =
1.00e-11
MAXORD          = 2.00e+00

*** Time-step Control Options :

ZOOMTIME        = 1.00e+00 STEP            = 0.00e+00 STARTSMP        =
0.00e+00
FREQSMP         = 0.00e+00 COURESOL        = 0.00e+00 TRTOL           =
7.00e+00
HMIN            = 1.00e-12 ITL3            = 3        ITL4            = 13
FT              = 1.25e-01 DCLOG           = 1.00e+00 LVLTIM          = 2
LVLCNV          = 2        DVDT            = -1       RELVAR          =
1.50e-01
ABSVAR          = 2.00e-01 SAMPLE          = 0.00e+00 HMAX            =
UNDEF

*** MosFet default Options :

SCALE           = 1.00e+00 SCALM           = 1.00e+00 SCALEBSIM       =
1.00e+00
DEFAD           = UNDEF    DEFAS           = UNDEF    DEFPD           =
UNDEF
DEFPS           = UNDEF    DEFW            = 1.00e-04 DEFL            =
1.00e-04
DEFNRD          = UNDEF    DEFNRS          = UNDEF    XA              =
6.00e-06
LIMRMOS         = UNDEF    SHRINK          = 1.00e+00

*** General Information Options :

SDA             = 0        CPTIME          = UNDEF    STAT            = 0
TIMEDIV         = 0        SIMUDIV         = 10       SAVETIME        = 0
MAXTRAN         = 1000     MAXNODES        = 10000    MAXV            =
1.00e+13
LIMPROBE        = 10000    FLICKER_NOISE   = 0        THERMAL_NOISE   = 0
TNOM            = 2.70e+01 TMAX            = UNDEF
SPICDC          = 0        SPIOUT          = 0        NEWTON          = 1
OSR             = 0        TRAP            = 1        GEAR            = 0
BE              = 0        PROBEOP         = 0        NOLAT           = 0
NWLAT           = 0        ANALOG          = 0        BBDEBUG         = 0
NOSIZECHK       = 0        QTRUNC          = 0        UNBOUND         = 0
LCAPOP          = 0        NOAEX           = 1        AEX             = 1
AEX             = 1        STVER           = 0        MOTOROLA        = 0
AMS             = 0        ASPEC           = 0        INPUT           = 0
NOINIT          = 0        PSF             = 0        WSF             = 0
WSFASCII        = 0        NOBIN           = 0        NOCOU           = 1
WL              = 0        NODE            = 0        LIST            = 0
SPI3BIN         = 0        SPI3ASC         = 0        NOMOD           = 0
WSF             = 0        WSFASCII        = 0        NOBIN           = 0
NOCOU           = 1        WL              = 0        NODE            = 0
LIST            = 0        SPI3BIN         = 0        SPI3ASC         = 0
NOMOD           = 0        RMOS            = 0        NWRMOS          = 1
NONWRMOS        = 0        USEDEFAP        = 0        NOASCII         = 1
ASCII           = 0        MIXED           = 0        SWITCH          = 0
USERSWITCH      = 0        TIMING          = 0        MODWL           = 1
ULOGIC          = 0
```

Achievements during Project

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3. Ami Patel and Amisha Naik,”Low Power Analog Multiplier Using 130 nm CMOS technology,”*National Conference on current Trends in Technology*, pp.585-587, Nov 2008.

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