ABSTRACT

Most digital synchronous ASIC designs requires clock source to provide proper timing for information signals, which functions among all circuits in the designed blocks. In such cases the clock source is mostly a crystal oscillator. Commonly such oscillators achieve up to 30 MHz without giving too much trouble. Recent advances and applications required very high frequency Phase locked loop with minimum jitter, phase noise, low power, and wide tuning range. Phase Frequency Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillator and Frequency/Voltage Divider are basic building blocks of PLL.

The Phase locked loops (PLLs) cover wide application area such as communication systems, wireless systems, digital circuits, power systems and disk drives. It is most useful block to generate clock signal for ASIC designers. It also gives timing flexibility to cancel out clock distribution delays, adjust setup and hold times, correct clock duty cycles and minimize clock skew and jitter. Basically output phase noise of PLL is contributed by VCO, PFD and input reference signal. The selection of loop bandwidth is very important in order to achieve a low jitter low phase noise PLL. In addition to this phase noise of the VCO degrades as frequency increases.

In this thesis novel low jitter low phase noise wide band DPLL using self aligned DLL in 180 nm CMOS technology is implemented and analyzed. Based on proposed novel concept, phase difference between injection signal and Sub Harmonically Injected VCO in PLL can be aligned to reduce jitter and phase noise.

The proposed DPLL with self aligned DLL consists of a third order PLL for 7.47 GHz clock generator and a first order DLL for self aligned injection. The third order PLL is composed of a sub harmonically injection locked VCO, a divide by N frequency divider, a phase frequency detector (PFD), and an LPF. PFD is designed with Clocked Inverter and D Flip Flop using TSPC Logic. In such flip flop design only one transistor is being clocked by short pulse train which is known as True Single Phase Clocking (TSPC) flip flop. The reset path is also modified in the design. It provided minimum dead zone with least power dissipation. Charge pump and efficient higher order loop filters are designed accurately for minimum leakage current and hence to achieve low power dissipation.

The measured phase noise of proposed DPLL with self aligned injection at 1-MHz offset is 124.40 dBc/Hz with a rms jitter of 110 fs. The total dc power consumption is 27.72 mW. With self aligned injection, proposed DPLL features the lowest jitter, phase noise, and best figure of merit among reported CMOS PLLs.

Proposed DPLL has been developed and all design consideration has been reported. The design methodology has been completely verified with existing experimental results as compared with different reported PLLs. Mentor Graphics, Tanner EDA and Cadence tools are used to characterized, simulation results and layout purpose. Further Monte Carlo analysis is also made to verify and analyzed the statically results using 180 nm CMOS technology.

Keywords: PLL, CMOS, DLL, PFD, VCO, Phase Noise, TSPC, VCDL