FPGA Implementation of Digital Beam Former for Synthetic Aperture Radar (SAR) Application

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Parul Dohare

(15MECV08)

Electronics & Communication Department
Institute of Technology
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Ahmedabad-382 481

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Certificate

This is to certify that the Major Project entitled **"FPGA Implementation of Digital Beam Former for Synthetic Aperture Radar(SAR) Application "** submitted by **Parul Dohare (15MECV08)**, towards the partial fulfillment of the requirements for the Degree of Master of Technology in VLSI Design , NIRMA University, Ahmedabad is the record of work carried out by her under our supervision and guidance.In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this major project, to the best of our knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

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Certificate

This is to certify that the Project entitled "**Digital Beam Former for Synthetic Aperture Radar(SAR) Application**" submitted by **Parul Dohare (15MECV08)**, towards the submission of the Project for requirements for the degree of Master of Technology in VLSI Design, NIRMA University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

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Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at NIRMA University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

-Parul Dohare

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- Parul Dohare

15MECV08

Abstract

This thesis presents the design of a Digital Beamformer (DBF) receiver for Synthetic Aperture Radar. Conventional SAR system design is constraint by the contradicting requirements of wider swath coverage and fine resolution to be achieved simultaneously. To overcome this, digital beamforming in SAR is introduced. The exponential growth in digital hardware and signal processing capabilities stimulates the development of radar systems. In this thesis, digital beamforming for SAR at the receiver side is described. A Parabolic reflector with feed array receives the signal separately from each feed element corresponding to a particular swath region. Further DBF is used in digital domain to combine signals to form a single range line. This technique improves the performance with high resolution and coverage, gain and SNR. Based on software codes, these digital systems are more flexible and easier to reconfigure than RF-hardware. Simulation of DBF receiver is performed on the HDL and MATLAB platform.

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Abbreviation Notation and Nomenclature

DBF ..... Digital Beam Former
TRiM ..... Transmit Receive Integrated Module
DDC ..... Digital Down Converter
FPGA ..... Field programmable Gate Array
LO ..... Local Oscillator
ADC ..... Analog to Digital converter
HDL ..... Hardware Description Language
icon ..... integrated controller core

Chapter 1
Introduction

1.1 Overview and Motivation of the work

This thesis reviews the design and performance of Digital beamforming for Synthetic Aperture Radar. The exponential growth of digital technology, has impact on the way radar system are designed. More and more functions were implement on analog hardware now being performed digitally, resulting in increased performance and flexiability and reduced size and cost. This thesis will describe how these digital technologies are being applied to radar systems and the benefits they bring to system performance.

Now a days Space borne SAR systems for remote sensing applications are gaining special interest during the last decade. As a well-proven imaging tool for Earth remote sensing, synthetic aperture radar (SAR) shows its advantage in providing radiometric mapping of an area of interest for diverse purposes, independent of weather and light conditions. Future remote sensing of the Earth will require frequent global mapping with continuous wide coverage and detailed imagery. However, the conventional SAR has a basic limitation it is not possible to achieve high resolution and wide coverage simultaneously.and future imaging SAR systems have a higher resolution, larger scene size, faster acquisition of images, delivery and a possibility of obtaining SAR images of the same area in the shortest possible time as required. To overcome contradiction between coverage and resolution motivate further development for SAR to achieve wide coverage and high resolution simultaneously.

Digital Beam-Forming (DBF) techniques are their ability to provide simultaneously a wide swath (coverage) and a high resolution. Conventional RF beamformer uses a phase shifter, variable amplifier and power distribution circuit which make a high

weight, low efficiency and difficult calibration. Recent progress in digital technology in the area of increase processing speed, reduced power consumption, and decrease volume has made Digital beamforming technique more attractive. Special Digital Signal Processor (DSP) processor and FPGA computes thousands of operation in fraction of second with high speed, low power consumption and smaller volume is also involve.Analog to digital converter also have high speed and high resolution make attractive compare to conventional RF beam former. Digital beamforming provides high efficiency, accuracy, digital hardware configurable.

This thesis Digital Beamforming is explained only at receiver side. Where the received data is first digitized by ADC, Following the down-mixer and filter are employed to convert the signal to the base band. And then multiplying the digitized base band signal by weight complex weights. Subsequently, the real-time beamforming processing algorithm is implemented on the on-board FPGA.

1.2 Recent trend

Main demands on SAR systems are higher resolution, larger scene size, faster acquisition of images, delivery and a possibility of obtaining SAR images of the same area in the shortest possible time as required .Currently ,the digital beamforming synthetic aperture radar (DBSAR) is an L band airborne radar developed at National Aeronautics and space Administration (NASA) Goddard radar techniques (GSFC) for the implementation and testing of digital beam forming technique, DBSAR combines phased array architecture, re configurable waveform generation, and Field programmable Gate Array (FPGA) based data acquisition and processing system in order to enable new remote sensing capabilities in support of Earth science and Planetary exploration application.DBSAR evolved from NASA's Internal Research and Development efforts aimed at the development of active/passive space borne system concepts that combine an L-band imagining scatter meter and a synthetic thinned-array radiometer.

To overcome classical SAR limits digital beam forming SAR (DBF-SAR) architectures based on multiple receiver channels has been proposed in the recent years as the base for future SAR systems. Several architectures based on elevation DBF have been proposed mainly to address coverage limits or based on azimuth DBF to address azimuth resolution limits. The use of multiple receivers introduces new degrees of freedom in system design parameters that allow higher performance. Furthermore, the addition of multiple transmitters in a multiple input multiple output SAR (MIMO-SAR) configurations allows even greater system operation flexibility.

The National Aeronautics and Space Administration (NASA) in the United States and the Indian Space Research Organisation (ISRO) have embarked on a study of a future Earth-orbiting science and applications mission that exploits synthetic aperture radar to map Earth's surface every 12 days. To meet demanding coverage, sampling, and accuracy requirements, the system was designed to achieve over 240 km swath at fine resolution, and using full polarimetry where needed. As the partnership concept with ISRO developed, it became clear that flying dual L- and S-band SAR capabilities, with L-band electronics supplied by NASA and S-band electronics by ISRO, would satisfy science and application requirements of the US and India. To achieve these observational characteristics, a reflector-feed system is considered, whereby the feed aperture elements are individually sampled to allow a scan-on-receive "Sweep SAR" capability at both L-band and S-band.[REF: An L- and S-band SAR Mission Concept for Earth Science and Applications].

Next-generation of space-borne SAR missions will employ DBF such as Tandem-L, Sentinel-1 follow-on, NASA-ISRO and HRWS . From the last years, several successful synthetic aperture radar (SAR) systems, such as TerraSAR-X, TanDEM-X, Radarsat-2 have demonstrate the high capabilities of radar-based imaging systems and their multiple applications.

1.3 Thesis Outline

The work is organized as follows :Starting point is the overview of the radar with digital beam-forming and recent trend in SAR.Chapter 2 describes the basic of the beam forming. How Digital beamforming overcome the limitation of the RF beamforming with respect to various parameters .Detail explanation of the each block of digital beamforming with suitable diagrams and required derivation to prove equation.

Chapter 3 represent the simulation results simulate in HDL and its output compared with ideal output of MATLAB.Here for batter understanding simulation results are explained at each and every module with timing plot, Frequency spectrum and polar plots. Hardware implementation is done on virtex-5 FPGA and output data are capture on chip scope.

Chapter 4 describes the fundamental of SAR. This chapter start with explanations of basic fundamental of radar than it describes the SAR radar. SAR is explain in detail starting with introduction and application. Digital beamforming is introduced in SAR to overcome the limitation of the conventional SAR. Then this chapter further include the SAR system Design overview with respect to Digital Beam Forming by considering the NISAR(NASA-ISRO SAR Mission).it explain the each RF and Digital components in detail. And the last Digital beamforming algorithm is explained for SAR to improve the performance.

Chapter 5 represent the simulation result of the digital beamforming algorithm for SAR simulated on the HDL.Due to unavailability of the actual coefficient, algorithm implement on the dummy coefficient and inputs. Results of simulation are added to explain the every step process of algorithm. Chapter 6 conclude the thesis work.

Chapter 2
Fundamental of Digital Beam Forming

2.1 Digital Beamforming Concept

Beamforming is a digital technique that focuses the radar transmitter and receiver in a particular direction.A beamformer for a radio transmitter applies the complex weight to the transmit signal (shifts the phase and sets the amplitude) for each element of the antenna array. A beamformer for radio reception applies the complex weight to the signal from each antenna element, then sums all of the signals into one that has the desired directional pattern. beamforming can be used to receive the signal at desire direction, increase the SNR and reduce the side lobe level.

A conventional beam former uses a single parabolic dish antenna and is capable of producing a single beam. It amplifies signals from the direction it is pointed at and attenuates those from other directions. Mechanical operation for direction selection limits the number of scan able signals to one and the change of direction is slow due to a physical re-positioning of the dish. Beamforming using a phased array, the direction of focus is controlled by weighting the outputs of the array antennas. Phased array antennas are known for their capability to steer the beam pattern electronically with high effectiveness, managing to get low side-lobe levels and narrow beam widths. Implementations of phase array antenna using micro wave circuitry like phase shifter and variable amplifier. Using a micro wave component effect on performance. phase shifter consumes a high power and decrease the gain of phase array antenna. And another problem is tolerance of phase shift value. Phase shifter also varies its performance due to temperature, time,mechanical vibrations, etc. In order to achieve a specific direction of beam increment of phase shift value of phase shifter should be

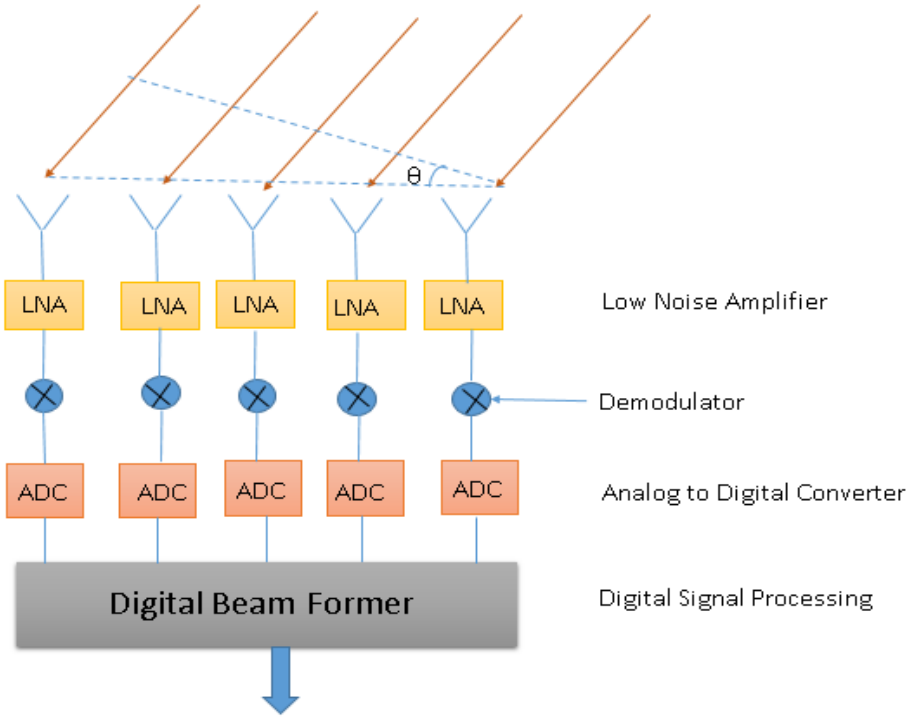

Figure 2.1: Basic Block Diagram of Basic Beamforming

equal.

Digital beam forming(DBF) technology in antenna array provides configurability and flexibility capability without using phase shifter and variable amplifier. It is desirable to eliminate the analog beamformer and produce an every-element digital beamforming system. With todays's technology, this is possible at L- and S-Band. At higher frequencies, size and power constraints often necessitate some analog beamforming. to reduce size and power while increasing bandwidth for most applications, as increased bandwidth typically requires additional current and circuit complexity. Digital beamforming relies on the coherent addition of the receiver channels.

In Digital beamforming phase shifting, amplitude scaling and addition are done digitally. By use a computational and programmable environment which processes a signal in the digital domain to control the progressive phase shift between each antenna element in the array. The advantage of digital beam former over analog beam former

is that it needed less power to steer the beam of antenna array and also advantage in reduction of variation of time, temperature and other environment changes. Operation of the digital beamformer is created and controlled by means of code written on a programmable device of the digital beamformer. And also have programmable interface adding versatility to the system. Basic block diagram of the digital beamformer as shown in figure 2.1. Signal received by the phase array antenna are not at the same time so this cause the phase difference between eachchannel. After processing the signal to LNA and demodulator signal in converted in to the digital for further processing the beamform.

Advantages of the Digital beamforming in radar system are:

• The system concept is in favour of higher efficiency and lower power consumption.

• The analog RF components of the system are reduced to a minimum.

• The requirements on the control systems and power supply units are relaxed due to the absence of the T/R modules.

• The system is reconfigurable by software and adaptable to different programmable requirements.

• Digital calibration is possible, since the phase and amplitude signal weighting is implemented in the digital domain, thus the complex calibration of the T/R modules becomes dispensable.

2.2 Digital Beam Forming (DBF) Receiver

Incidence wave are received by the phase array antenna then it proceeds by the Digital beam forming receiver.DBF Receiver has a four main component: RF translator stage, Digital down converter, complex weight multiplication and summation of complex signal.

So now first stage is RF translator. Basically it is not implemented digitally but the essential part of the receiver. It is implemented by heterodyning process (RF mixer). it is necessary to include Low Noise Amplifiers at the RF translator Stage.The LNAs help to reduce the Noise figure in a microwave circuit and increase the Signal-to-

Noise Ratio (SNR). Therefore, the RF translator Stage of each antenna channel has one LNA and one RF mixer. This stage is necessary because incoming signal is at high frequency component compare to speed of ADC.For convert the signal in to digital domain shift the signal from high frequency to low frequency.

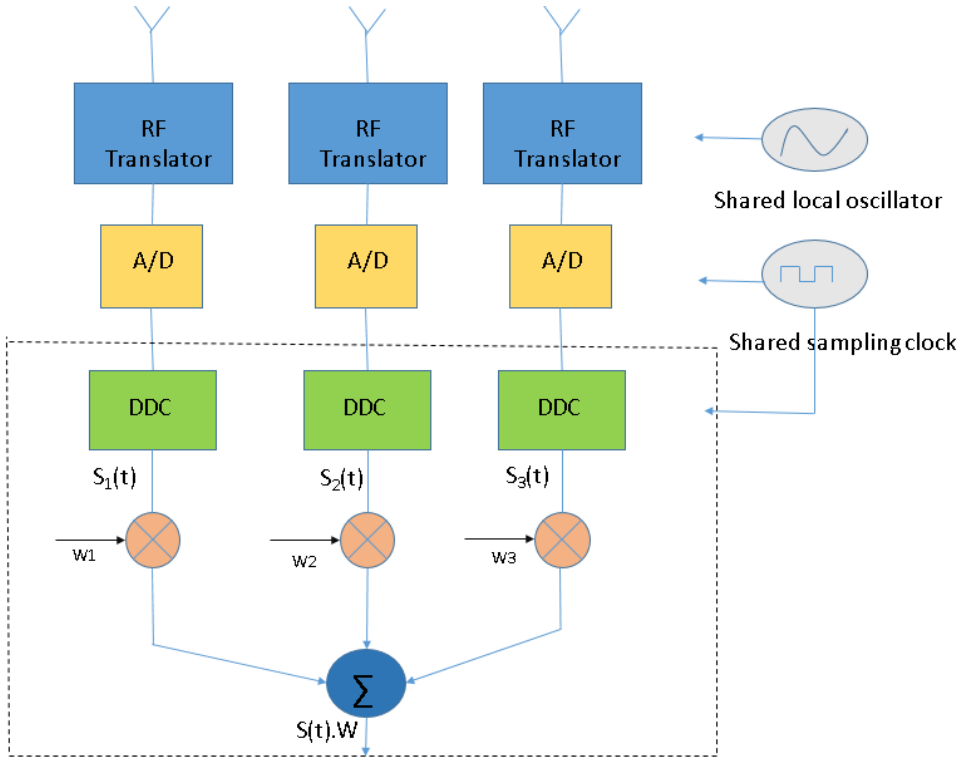

Figure 2.2: Block diagram of DBF Receiver

The RF Modulation Stage has convert RF to IF in a two stage of LO mixing and filtering.A Local Oscillator (LO) with a frequency of W_{LO} is mixed with RF signal,using trigonometric identities,it generates the signal with two frequencies, $W_{IF} = W_{RF} - W_{LO}$ and $W_{IM} = W_{RF} + W_{LO}$. By using a band pass filter with centre frequency W_{IF}. We get the output signal with frequency component W_{IF}.The phase is remain unchanged in this process.

Now the output RF translator in the range of 50 MHz is digitized using ADC. ADC implement the operations of sampling, quantize, and encoding of the analog signal. Two important ADC parameters are the bit resolution and the sampling frequency per channel. The bit resolution parameter determines the quantization error found

in the analog-to-digital transformation. This quantization error can be represented as noise power, which affects the SNR of the antenna channels signal. The sampling rate parameter determines the analog frequency band which can be represented in the digital domain.

2.2.1 Digital Down Converter

First stage of DBF receiver is the digital down converter.After the quantized the antenna signal in digital domain, signal is further processed by DDC. down conversion consists of shifting the signal of interest to a lower frequency, removing unwanted signal components and the desired information signal at a lower sampling rate.

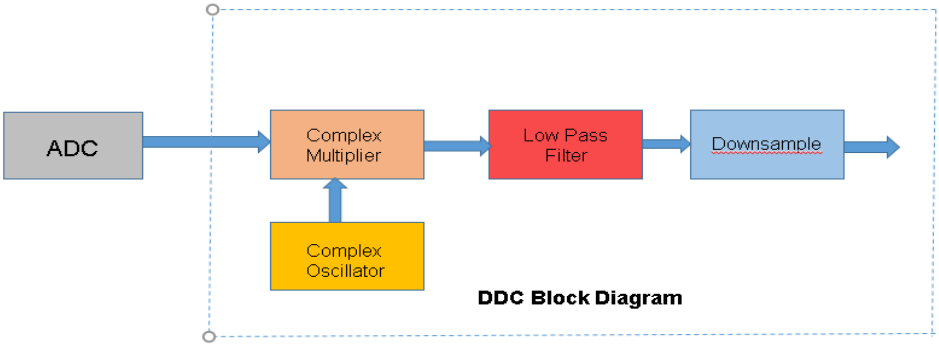

Figure 2.3: Block diagram of Digital down converter

A Digital Down Converter is basically consisting complex mixer to shifting the frequency band of interest to baseband. The first stage of the DDC is to mix, or multiply, this digitized stream of samples with a digitized cosine for the in phase channel and a digitized sine for the quadrature channel generated by local oscillator and so output is sum and dfference frequency component. Mixer Frequency is choose to move the signal to baseband. If the input frequency of DDC and local oscillator frequency is same then the output sum frequency and difference frequency.

The second step in the DDC of the DBF receiver is the filtering of the high frequency component centred at the digital frequency or image frequencies. After filtering, the

sample frequency is now much higher than required for the maximum frequency in our frequency band and so the third stage is down sample where sample frequency can be reduced or down sampled, without any loss of information.

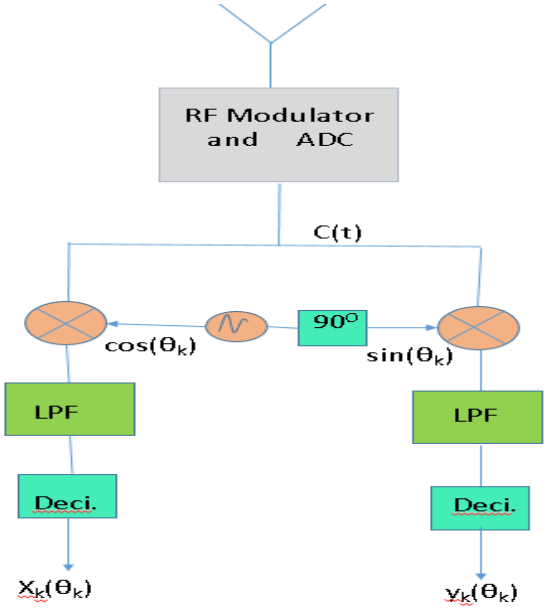

Figure 2.4: Block diagram of RF Modulator and DDC

2.2.2 Complex Weight Multiplication

The second stage of the DBF receiver is the Complex Weight Multiplication(CWM) stage.In this stage output of DDC,in phase base band signal and quadrature base band signal is multiplied by complex weight W_k.Two components are required so that both positive and negative frequencies can be represented.

where,

S_k = Complex baseband signal from the DDC for k^{th} antenna element

$x_k(\theta_k)$ = Real part of the S_k

$y_k(\theta_k)$ = Imaginary part of the S_k

For beamforming, the complex baseband signals are multiplied by the complex weights to apply the phase shift and amplitude scaling required for each antenna element.

$W_k = a_k e^{j\theta_k}$

$W_k = a_k \cos(\theta_k) + j a_k \sin(\theta_k)$

where,

W_k is complex weight for the k^{th} array antenna element

a_k is the relative amplitude of the weight

θ_k is the phase shift of the weight

complex multiplication for each antenna element:

$S_k{*}W_k{=}(x_k(\theta_k) + jy_k(\theta_k)\ ) * (\ a_k\cos(\theta_k) + ja_k\sin(\theta_k))$

$S_k{*}W_k{=}\ a_k\ [\ x_k(\theta_k)\ {*}\cos(\theta_k){-}y_k(\theta_k)\ {*}\sin(\theta_k)] + ja_k\ [x_k(\theta_k){*}\sin(\theta_k){+}y_k(\theta_k)\ {*}\cos(\theta_k)]$

$S_k{*}W_k\ {=}r(\theta_k) + js(\theta_k)$

So we are basically multiplied the phase shifted signal with complex weight associated with each phase array. If the incoming signal is coming from another direction in space, the multiplication of the complex weight and the complex coefficient will not cancel the phase.

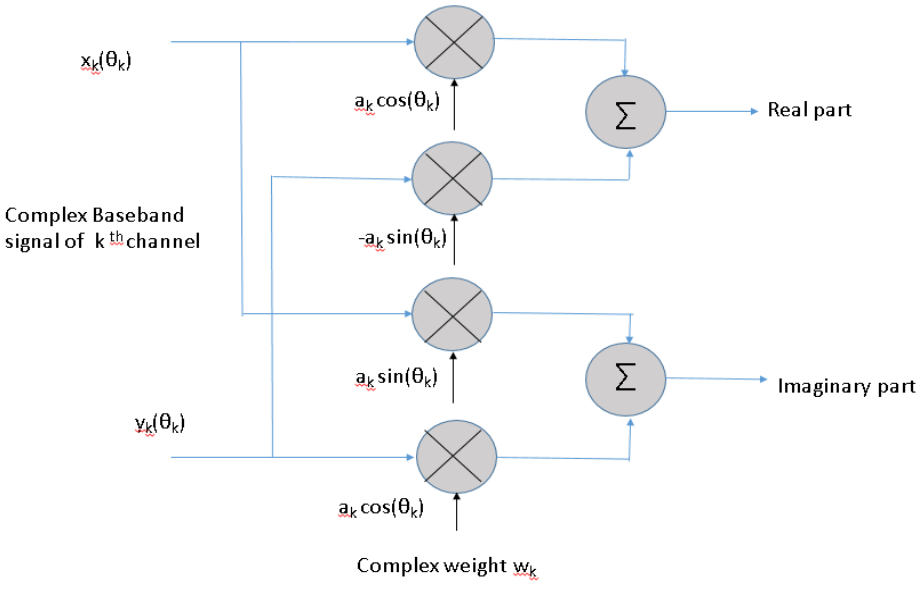

Figure 2.5: Diagram of complex multiplication

2.2.3 Complex addition

This is the last stage of DBF receivers in this stage result of all complex multiplication of all channel of array antenna are added simultaneously. Here in phase base band signal and quadrature phase base band signal of every channel are added to give in phase resultant output and quadrature resultant output. No of addition are required is depend on the no of channels. An amplitude scaling is needed to recover the original signal.

Chapter 3
Simulation and Hardware Implementation Results of Digital Beam Forming

In this chapter, Digital beam forming for four channel are presented. Simulation is done in the HDL and MATLAB platform. Ideal result of MATLAB are compared with the simulation result of FPGA and hardware implementation is done on Virtex-5 FPGA. Figure 3.1 show the basic block diagram of DBF receiver performed on HDL.

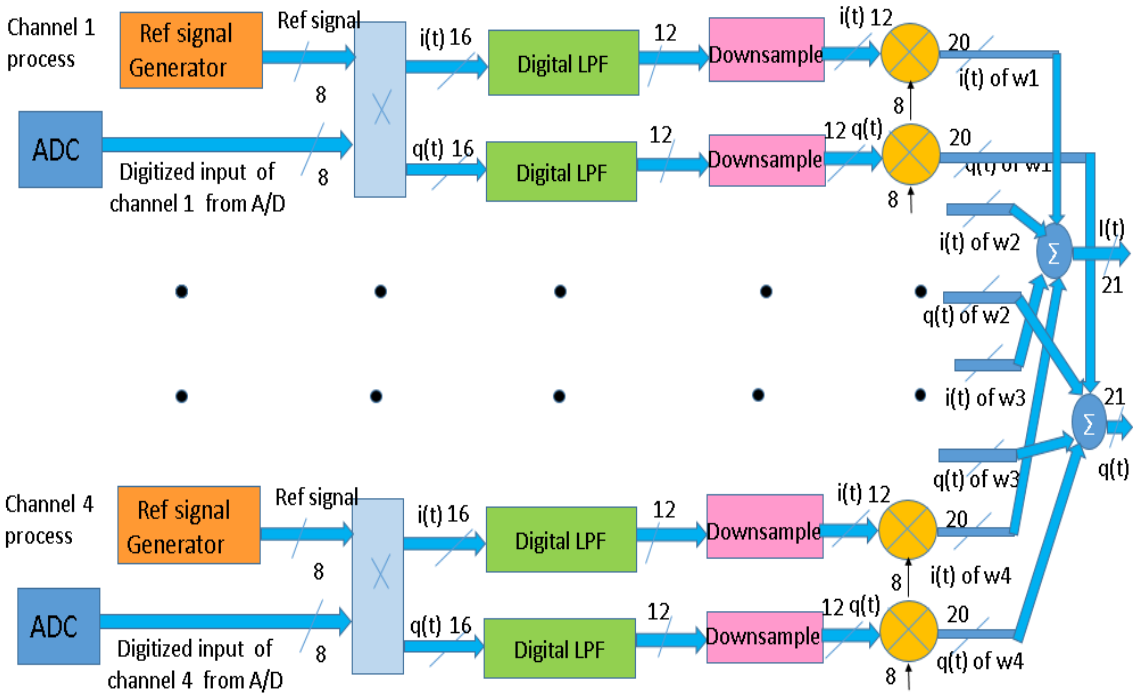

Figure 3.1: DBF flow in hdl

Figure 3.1 show the beam forming for the four channel implemented in HDL.The basic component of this process are Digital down converter, complex weight multiplier and addition of complex signal.

The signal from the RF Mixer (at 50 MHz) are digitized by Analog to digital converter (ADC) in 8-bit at 250 MHz sampling clock. This 8-bit digital input processed on FPGA for beam forming process. This digitized input processes by the DDC to shift the signal in to the base band.DDC signal is processes in to three stapes as follows: First the 8 bit input is multiplied by the 8-bit reference signal (at 50 MHz and 250 MHz clock frequency) generated by the DDS IP core of the Xilinx .It generate the in phase and quadrature phase component at difference (0 MHz) and sum (1 MHz) frequency. so eliminate the high frequency component low pass filter is used. In Xilinx, FIR compiler IP core is used for low pass filtering the high frequency component (1 MHz) in phase and quadrature phase of each channel.After filtering, last step is down sample the filter output by 3.Output of DDS is multiplied with complex weight (8 bit) associated with each channel. These complex weight coefficients are already stored in memory of FPGA for each channel. After that real and imaginary part of each channel are added to get the beam.Next section presents the output result of HDL and MATLAB at each and every step of the receiver.

3.1 HDL and MATLAB Simulation Result

Figure 3.2 show the quantize input of four channel .Currently as an example beam forming done for four channels, channel 1 is the cos signal and the channel 2 is the 20^0 degree phase shift, channel 3 is 40^0 degree phase shift and channel 4 is 60^0 degree phase shifted of cos signal generated in MATLAB .

channel_1 = cos (2*pi*f_c*t)

channel_2 = cos (2*pi*f_c*t+ phi) phi = 20^0

channel_3 = cos (2*pi*f_c*t+ phi1) phi1 = 40^0

channel_4 = cos (2*pi*f_c*t+ phi2) phi2 = 60^0

f_s = 250MHz and f_c = 50MHz

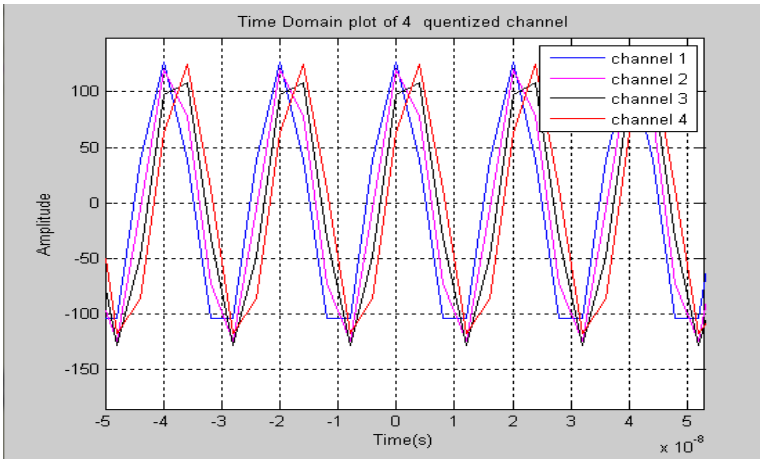

Figure 3.2: Time Domain plot of quantized 4 channels

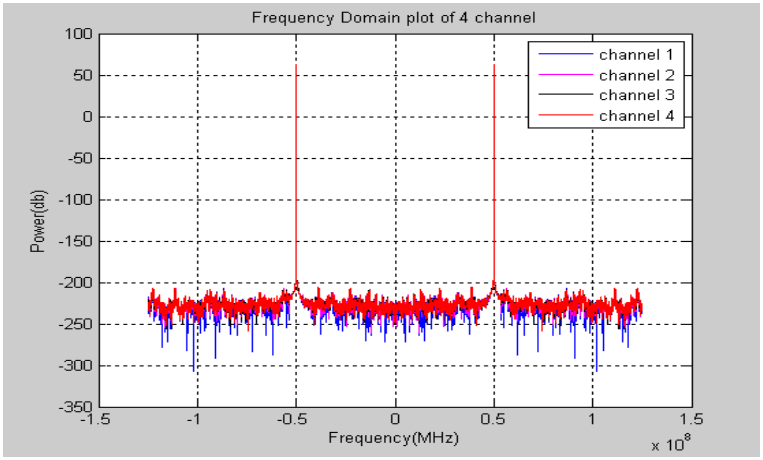

Figure 3.3: Frequency spectrum of quantized 4 channels

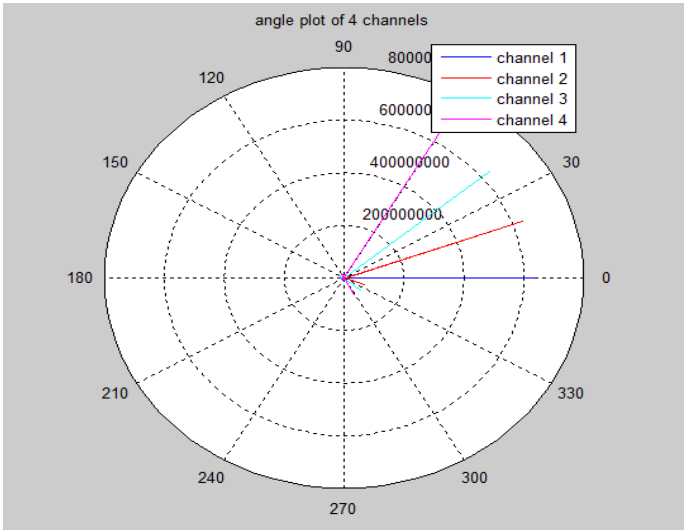

Figure 3.4: Polar plot four channels

Figure 3.2 shows time domain for 4 channels each are shifted with 20 degree phase shift and the figure 3.3 shows the frequency domain spectrum of all channels are at 50MHz.and figure 3.4 the polar plot shows the phase shift between the channel.

Generation of Reference signal

First step of the DDC is multiplication of input signal with local oscillator (Reference signal). So The Reference signal is generated in matlab (at 50MHz cutoff , 250MHz sampling frequency) and in hdl reference signal generated by using DDS IP core. A common method for digitally generating a complex or real valued sinusoid employs a lookup table scheme. DDS IP Core uses the lookup table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the lookup table to the desired output waveform. Only one DDS core is needed for the generation of the reference signal to provide synchronization.

figure 3.5 and 3.6 shows the result of reference signal in time domain generated in MATLAB and HDL.which is nearly same And Figure 3.7 and 3.8 shows the reference signal generated at 50 MHz frequency.

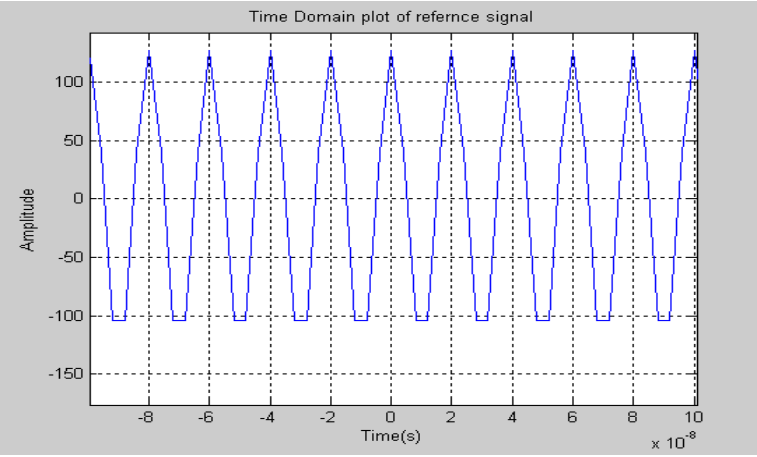

Figure 3.5: Time Domain signal Generated in Matlab

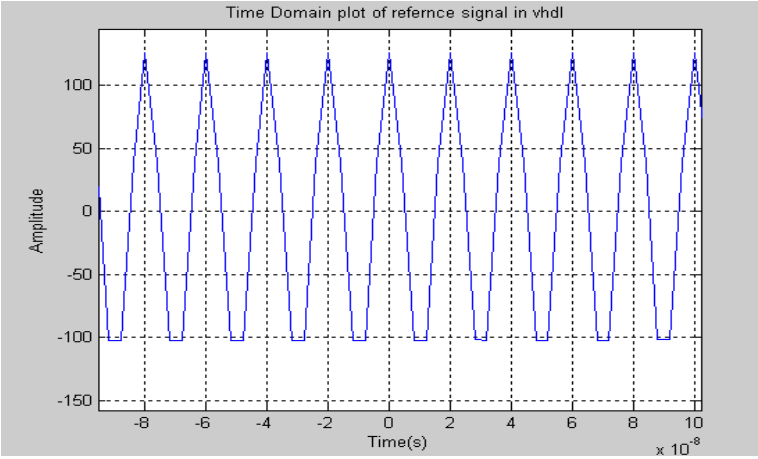

Figure 3.6: Time Domain signal Generated in hdl

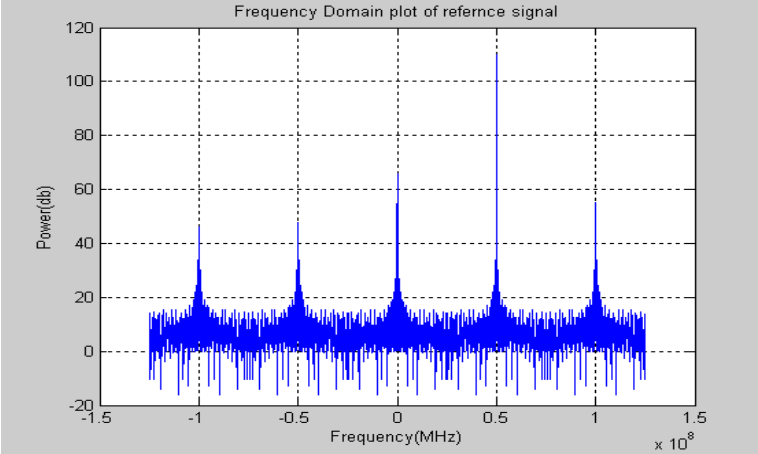

Figure 3.7: Frequency spectrum of Reference signal in matlab

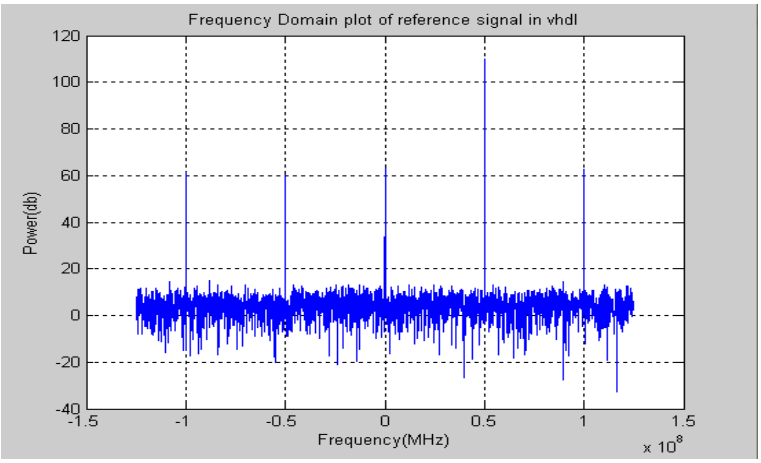

Figure 3.8: Frequency spectrum of Reference signal in hdl

Multiplication of reference signal with four channels

Figures shows the frequency spectrum of multiplied signal.Multiplied the all channels with reference signal generate the in phase signal and quadrature phase signal at two different frequency, one is difference frequency and other at sum frequency. Here it generates the frequency at 0 MHz and 1 MHz as shown in frequency spectrum. Figure 3.9 and 3.10 shows the frequency spectrum in MATLAB and HDL.

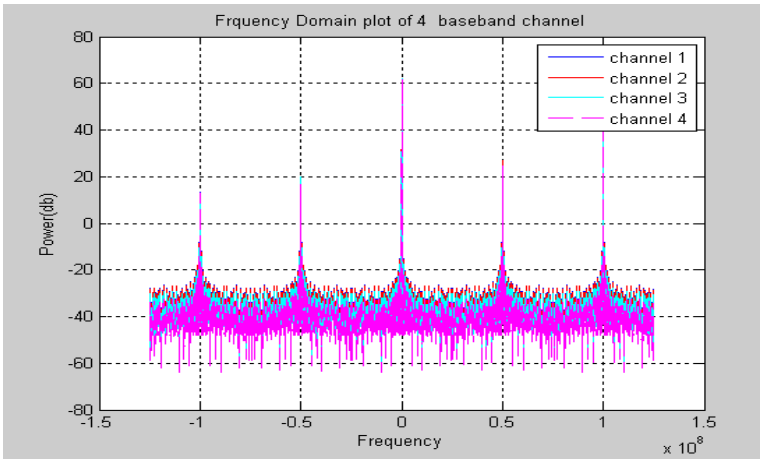

Figure 3.9: Frequency spectrum of multiplied with reference signal in matlab

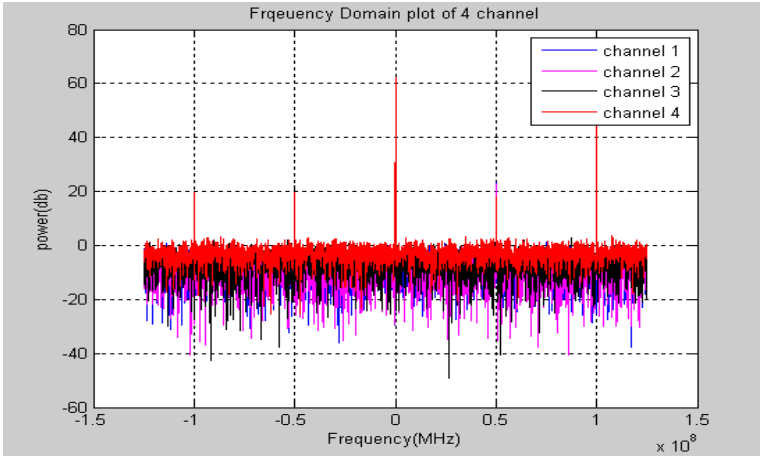

Figure 3.10: Frequency spectrum of multiplied with refernce signal in vhdl

Low pass filter output

Second step of DDC remove unwanted image frequency by using the low pass filter. Figure 3.11 shows the frequency spectrum of generated low pass filter. In matlab,

LPF is generated using fda (Filter Design and Analysis)tool and in hdl, FIR Compiler is used and coefficients are load from the matlab by .coe file .Here for the four channels required a total eight filter in hdl each for inphase and quadrature phase

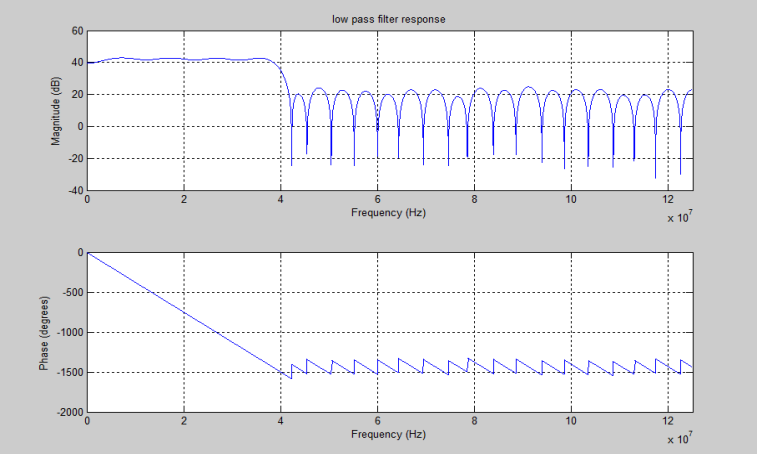

Figure 3.11: Filter Response

Figures 3.11 shows the LPF filter response generated in matlab and hdl.as shown in figure it attenuate the high frequency component by 20db.Filtered signal in MATLAB and HDL output as shown in figure 3.12 and 3.13.

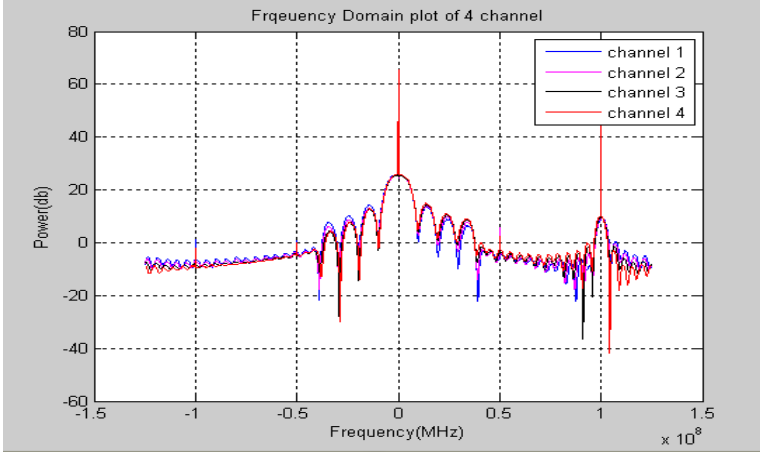

Figure 3.12: Frequency spectrum of filtered signal in matlab

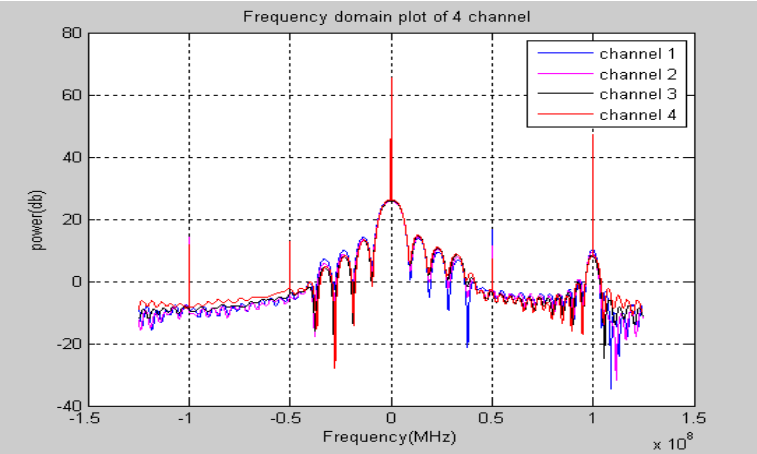

Figure 3.13: Frequency spectrum of filtered signal in hdl

Decimated output

After filtering we does not require a that much sample value so here we down sample the filter output by 3.In MATLAB,down sample are done by command and in HDL mod-3 counter is used in hdl for decimate.Frequency spectrums are shown in figure 3.14 and 3.15.

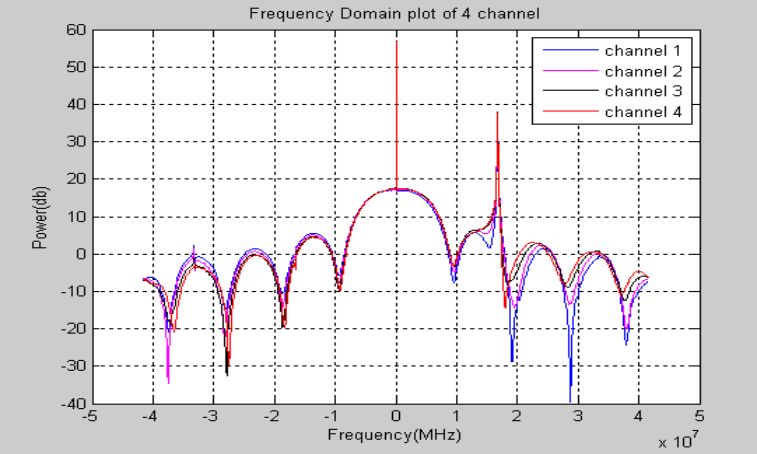

Figure 3.14: Frequency spectrum of decimated output in matlab

Multiplication with complex weight output

This is the second stage of DBF receiver. In this stage output of DDC is multiplied by suitable complex weight coefficient to correct the phase of the shifted signal.Here for the complex multiplication requires a four multiplier and two adders per channel.

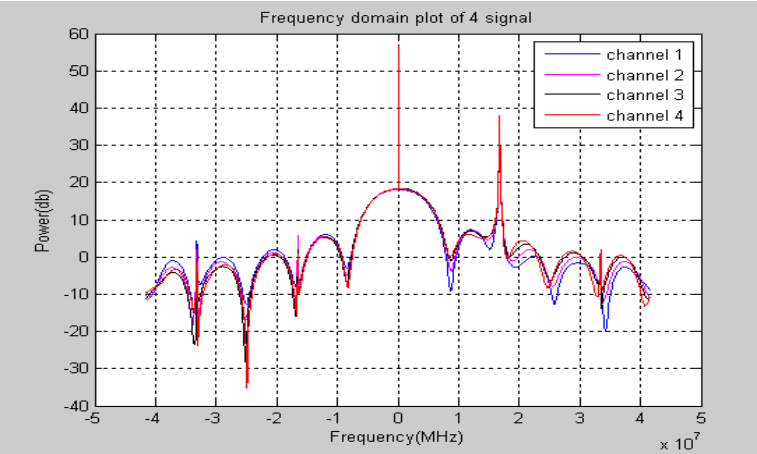

Figure 3.15: Frequency spectrum of decimated output in hdl

Following figure 3.16 and 3.17 shows the by weight multiplicand to channel doesnot change the frequency domain.It change the phase of the each channel as shown in the polar plot phase corrected in matlab and hdl.

Figure 3.18 and 3.19 shows the polar graph the corrected phase of all channels.Here phase of channel 2 is shifted from 20^0 degree to 0^0 and so on.so now all four signals are at same phase and add in constructive interference.

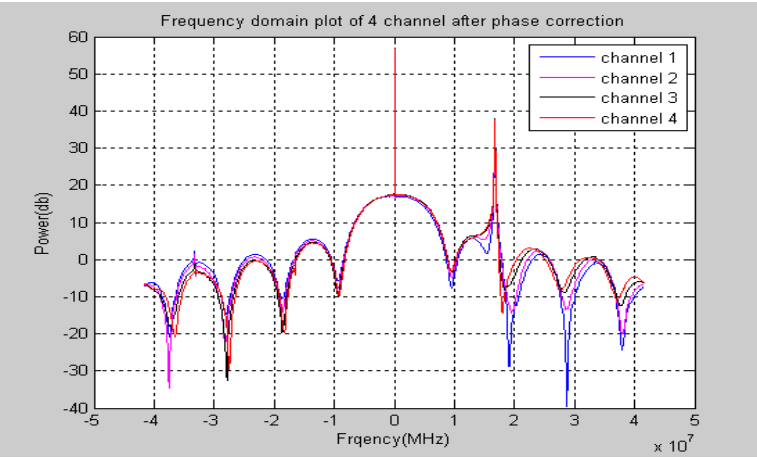

Figure 3.16: Frequency spectrum after phase correction for four channels in matlab

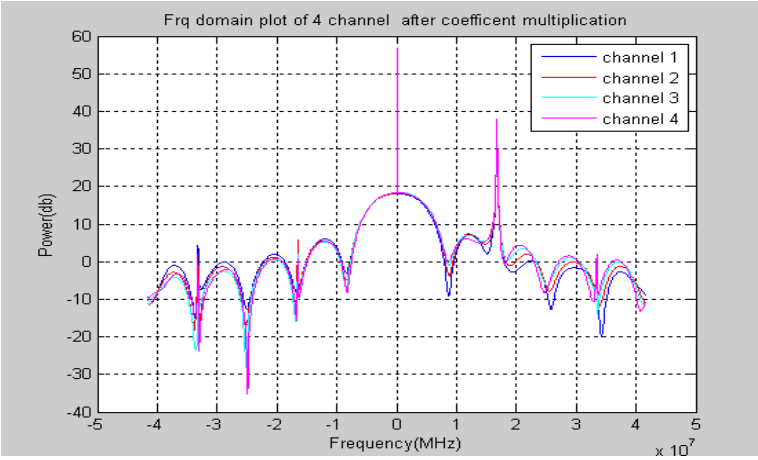

Figure 3.17: Frequency spectrum after phase correction for four channels in hdl

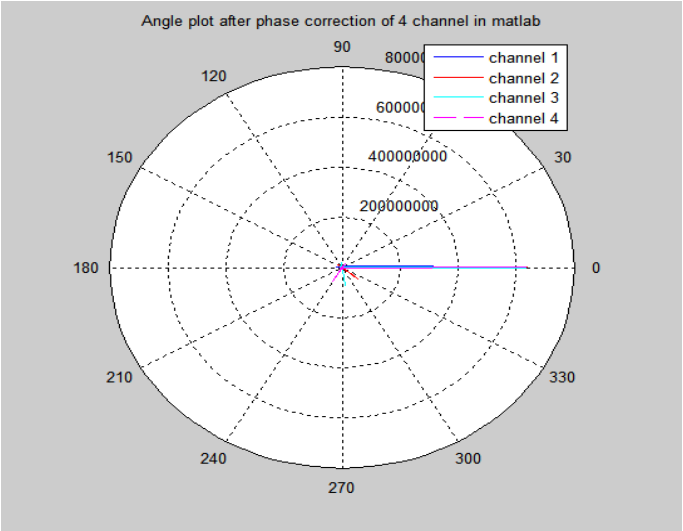

Figure 3.18: Polar plot of Phase correction in matlab

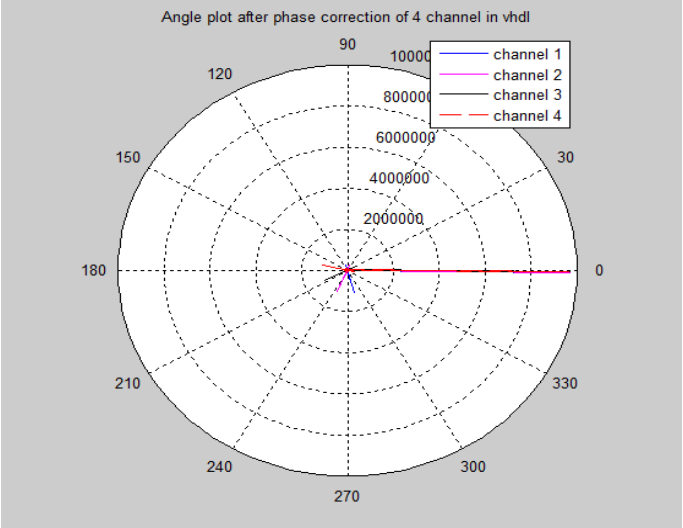

Figure 3.19: Polar plot of Phase correction in hdl

Addition of phase corrected output

This is the final step of the DBF receiver.Where we add the phase corrected output of each channel.So all the signals are at the same phase and they will add in the constructive manner and get the beam at desire direction. Here phase of all channel are same so it will constructively add in the same direction. Number of addition required depends on the no of channels. Figure 3.20 and 3.21 shows frequency domain and Figure 3.22 and 3.23 polar plot of beam formed output

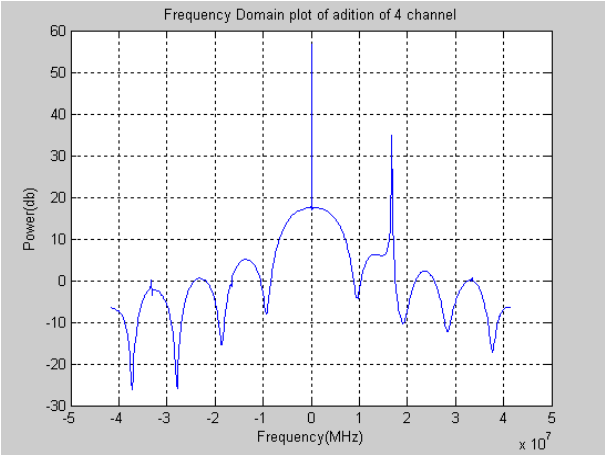

Figure 3.20: Frequency domain plot of beamform in matlab

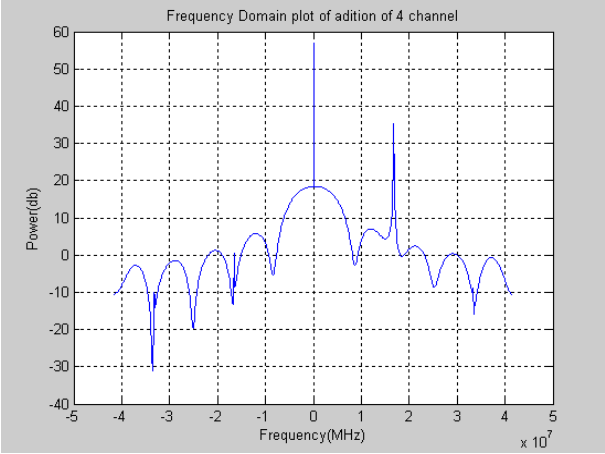

Figure 3.21: Frequency domain plot of beamform in hdl

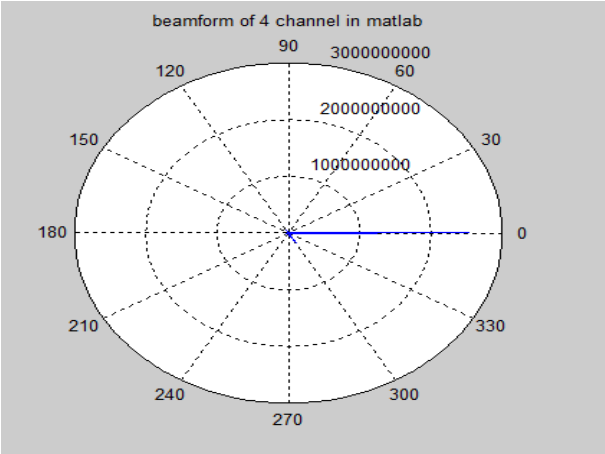

Figure 3.22: Polar plot of beamform in matlab

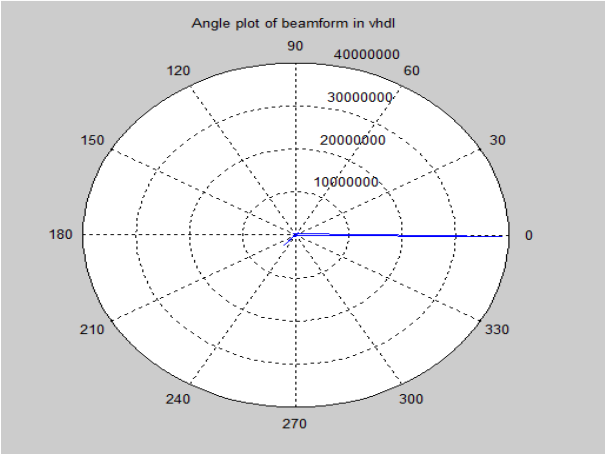

Figure 3.23: Polar plot of Beamform in hdl

3.2 Hardware Implemetaion Results

In perivious sction Digital beamforming is simulated in HDL and MATLAB platform .This section present the hardware implenation of Digtal beamforming on Digital Beam Former (DBF) board. DBF Board consist the Virtex 5 FPGA (XC5VFX130T) and four ADCs to digitize the data and it also consist high fidelity synchronous clock distribution as well as high-speed transmission of digital data. High Speed A/D Converters are required considering the high sampling rate and bandwidth requirements. This ADC is capable to digitize dual channels at a 12-bit resolution and has synchronization signals to synchronize with other ADCs, hence very much suited for DBF

board. Where very fine synchronization among channels is required for performing beam forming operation.Program is implemented on FPGA and its hardware result is capture on chip scope .Detail explanation of virtex-5 and chip scope analyser is given below.

Virtex 5 FPGA :

Figure 3.24: Virtex-5

The Virtex 5 FPGA offers dramatic increases in available resources to implement digital signal processing algorithms. Virtex-5 FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices and it also include power-optimized, high-speed serial transceiver blocks for enhanced serial connectivity. The Virtex-5QV FPGA combines unparalleled density, performance, and radiation hardening with the flexibility of reconfigurability without the high risk of ASICs. We are able to utilize the full capacity of the FPGA resources because the rad-hard by design approach of this chip eliminates the need for triple modular redundancy atthe logic level for space applications. The use of Xilinx Virtex-5 FX130 FPGA has been selected as it offers the advantages like dramatic resources, high speed, re-configurability, SEU hardened configuration memory and user registers as well as high total dose rate.Virtex-5 FX provides the High-performance embedded systems with advanced serial connectivity.

Chip scope:

ChipScope is an embedded, software based logic analyzer. ChipScope is a set of tools made by Xilinx that allows you to easily probe the internal signals of your design inside an FPGA, much as you would do with a logic analyzer.For example, while your design is running on the FPGA, We can trigger when certain events take place and view any of your design's internal signals.

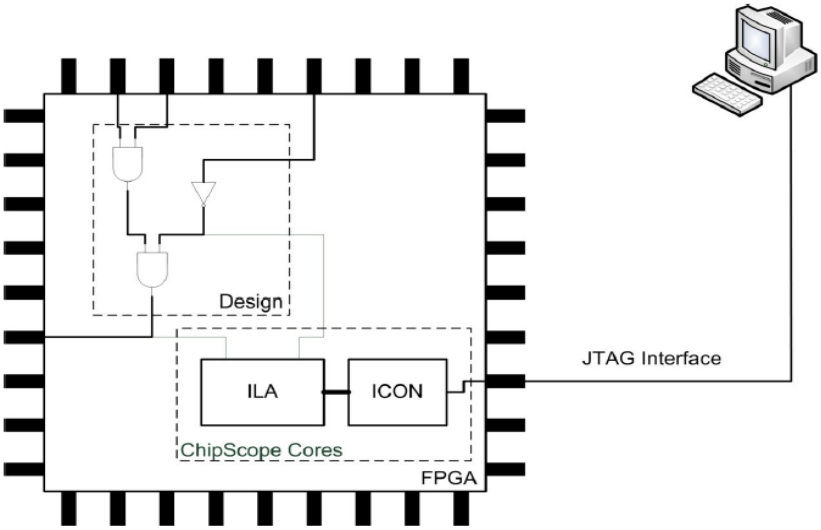

Figure 3.25: Testing and Debug using Chipscpoe pro

In order to use the ChipScope internal logic analyzer in an existing design project, you first generate the ChipScope core modules, which perform the trigger and waveform capturing functionality on the FPGA. Afterwards, you instantiate these cores in your HDL code, and you connect those modules to the signals you want to monitor. The complete design isthen recompiled. Instead of loading the resulting .bit file onto the FPGA using iMAPCT, the ChipScope Analyzer application is used to configure the FPGA.

By inserting an integrated controller core (icon) and an integrated logic analyzer (ila) into your design and connecting them properly, we can monitor any or all of

the signals in your design. ChipScope provides us with a convenient software based interface for controlling the integrated logic analyzer, including setting the triggering options and viewing the waveforms.

Hardware Result

Here four signals are generated by the waveform generator by 20^0 phase shift from each signal channel.These signals are quantized by the analog to digital converter on board.Now this quantized data is applied to Virtex -5 FPGA for beam forming where the weight coefficient for beamforming is already stored in FPGA memory .As the data received by the ADC is first converted to baseband and then multiplied each channel by the suitable coefficient, the final step we get is the addition of the all phase corrected signals. here complex signal output is captured on chipscope .figure 3.26 shows the captured signal(real and complex parts) on chip scope .This data is loaded onto matlab and the angle plot is plotted to compare with the simulation result of the output of HDL code.Figure 3.27 and 3.28 shows the beamform on hardware and hdl.

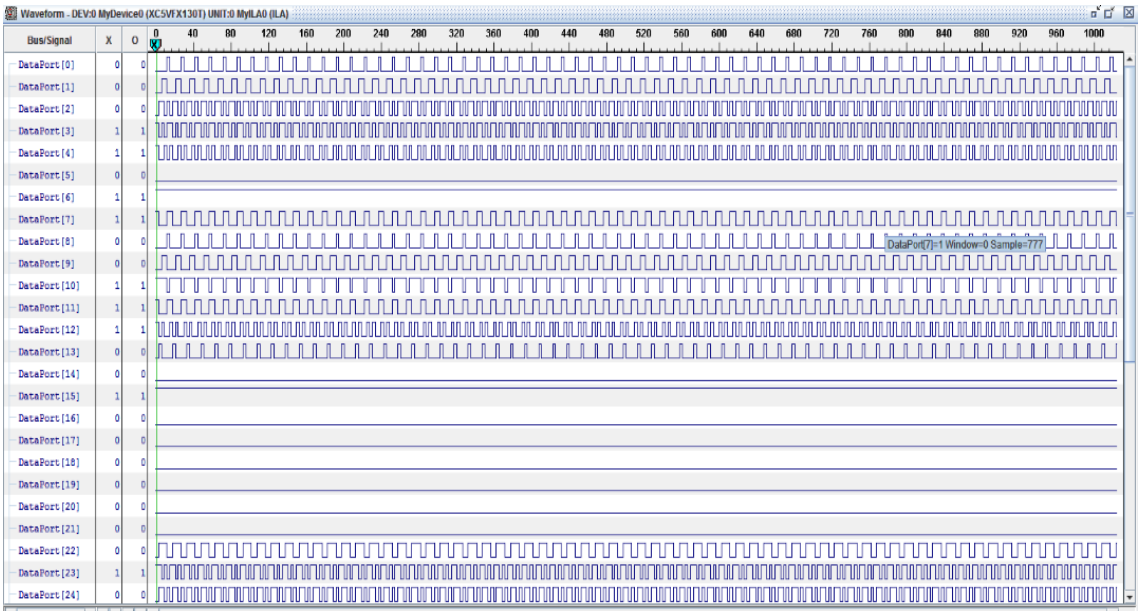

Figure 3.26: Captured output data on chip scope

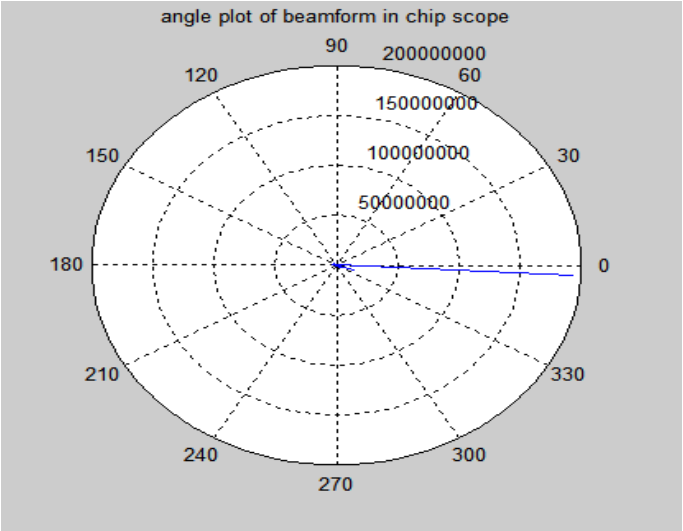

Figure 3.27: 4 channels Beamforming implemented on hardware

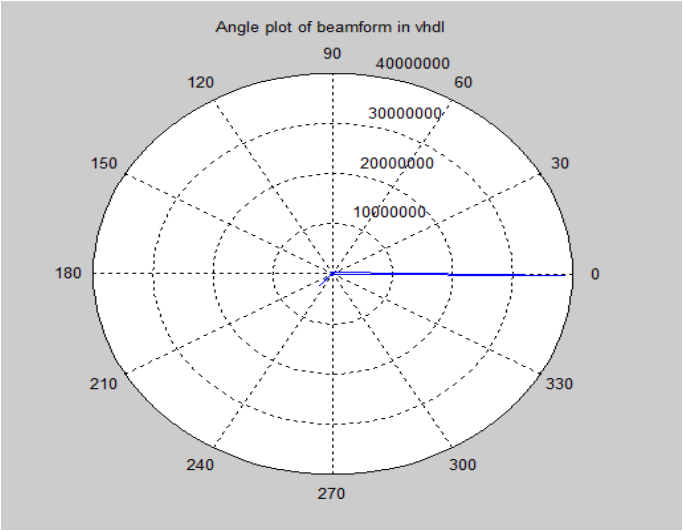

Figure 3.28: 4 channels Beamforming on hdl

Chapter 4
Fundamental of SAR

4.1 Introduction of the SAR

The original radar system developed during World War II was designed to measure range (to a target via echo time delay) and direction (of a target via antenna directivity). while, Doppler shift were used to measure the speed.Carl Wiley proposed in 1951 that Doppler shifts could be processed to obtain fine resolution in a direction perpendicular to range.The 2D images of ground surface can be made by creating the effect of a very long antenna in signal processing stage. This method was termed Synthetic Aperture Radar (SAR). Up to now, SAR images have been applied to various research topics such as mapping, geology, forestry, agriculture, oceanography.

The Synthetic Aperture Radar is a coherent Radar system, which is able to retrieve high resolution images of the Earth's surface. SAR is unique in its imaging capability: It provides high-resolution two dimensional images independent from daylight, cloud coverage and weather conditions. Radars provide their own electromagnetic signals to detect the presence of objects. so they can operate during day or night. In addition, radar signals penetrate through clouds and rain, which means that radar images can be acquired not only during day or night, but also under all weather conditions. It is predestined to monitor dynamic processes on the Earth surface in a reliable, continuous and global way.

SAR systems have a side-looking imaging geometry and are based on a pulsed radar installed on a platform with a forward movement. The radar system transmits electromagnetic pulses with high power and receives the echoes of the backscattered signal in a sequential way. Typical values for the pulse repetition frequency range from a

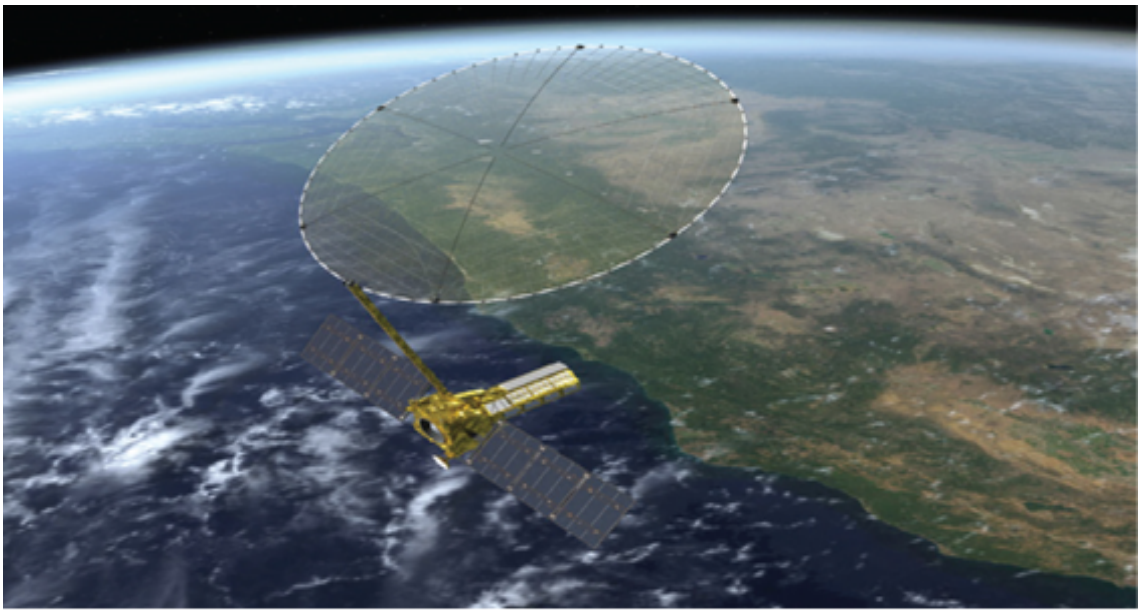

Figure 4.1: Synthetic Aperture Radar

few hundred to a few thousand Hertz for airborne and space borne systems, respectively.The transmitted pulse interacts with the Earth surface and only a portion of it is backscattered to the receiving antenna which can be the same as the transmit antenna (for a monostatic radar) or a different one (for a bi- or multi-static radar). The amplitude and phase of the backscattered signal depends on the physical (i.e., geometry, roughness) and electrical properties (i.e., permittivity) of the imaged object. Depending on the frequency band, considerable penetration can occur so that the imaged objects and media must be modelled as a volume (e.g., vegetation, ice and snow, dry soil).

Radio waves are that part of the electromagnetic spectrum that has wavelengths considerably longer than visible light, i.e. in the centimetre domain. More penetration of the electromagnetic pulses in media will occur for radar systems using longer wavelengths (shorter the frequency)the stronger the penetration into vegetation and soil which usually have an accentuated volume contribution in the backscattered signal. Following wavelengths are in generally used:
P-band = 65cm AIRSAR

L-band = 23cm JERS-1 SAR, ALOS PALSAR

S-band = 10cm Almaz-1

C-band = 5cm ERS-1/2 SAR, RADARSAT-1/2, ENVISAT ASAR, RISAT-1

X-band = 3cm TerraSAR-X-1 , COSMO-SkyMed

K-band = 1.2cm Military domain

Application of SAR:

SAR images have wide applications in remote sensing and mapping of the surfaces of both the Earth and other planets. Earth's land surface is constantly changing and interacting with its interior and atmosphere. In response to interior forces, plate tectonics deform the surface, causing earthquakes, volcanoes, mountain building, and erosion, including landslides. These events shape the Earth's surface, and can be violent and damaging. Changes in ice sheets, sea ice, and glaciers are key indicators of these climate effects and are undergoing dramatic changes. Many of these changes can be measured using repeat pass synthetic aperture radar interferometry and polarimetry methods from space.

The ability of SAR to penetrate cloud cover makes it particularly valuable in frequently cloudy areas such as the tropics. Image data serve to map and monitor the use of the land, and are of increasing importance in forestry and agriculture Some geological or geomorphological features are enhanced in radar images thanks to the oblique viewing of the sensor and to its ability to penetrate (to a certain extent) the vegetation cover. SAR data can be used to georeferenced other satellite imagery to high precision, and to update thematic maps more frequently and cost-effectively, due to its availability regardless of weather conditions. In the aftermath of a flood, the ability of SAR to penetrate clouds is extremely useful.

The major application of SAR in Science requirement:

Land deformation: This includes measurement of deformation due to co-seismic and interseismic activities, landslides, land subsidence and volcanic deformation.

Cryosphere studies:This includes measurements of dynamics of polar ice sheet-ice

shelf-glacier, sea-ice types, thickness and motion, land ice velocity and ice discharge to the ocean, Himalayan snow and glacier dynamics.

Oceanography:This includes retrieval of ocean physical parameters such as surface wind, wave spectra, coastal bathymetry, identification of up welling zones and ship detection.

Coastal processes monitoring:This includes understanding of the coastal erosion processes through the study of near-shore dynamics and coastal subsidence, Assessment of coastal vulnerability to sea-level rise and shore-line change.

Geological studies: This includes mapping of structural and lithological features, lineament sand paleo-channels, mineral explorations and geo-archaeology.

Disaster response:This includes mapping and monitoring of floods, forest fires, oil spills, earthquake damage and monitoring of extreme weather events such as cyclones.

Modes of SAR

Wide swath coverage and high azimuth resolution contradicting requirements on the design of spaceborne synthetic aperture radar (SAR) systems. This motivated the development of advanced SAR different imaging modes with different trade-offs between coverage and azimuth resolution.

Scan mode SAR:

The classical solution to wide-swath SAR imaging is ScanSAR, which increases the swath width at the cost of an azimuth resolution. The ScanSAR mode is of high importance for all spaceborne remote sensing applications that require monitoring of large areas. Examples are regular land use and vegetation mapping, marine observation, and monitoring of the Arctic sea ice. Another example is differential interferometry, which compares the phase of complex SAR images acquired during different satellite passes to detect subtle deformations on the Earth's surface for many geoscience and environmental applications.

Spotlight SAR:

the other hand, there exist many remote sensing applications that required SAR images with a high spatial resolution. Examples are marine and terrestrial surveillance,

cartographic mapping, monitoring of urban areas, as well as hazard and damage assessment. Even repeat-pass interferometry would benefit from a refined resolution. The rising demand for finely resolved SAR images led to the development of the spotlight mode, which improves the azimuth resolution at the cost of non-contiguous coverage along the satellite track.

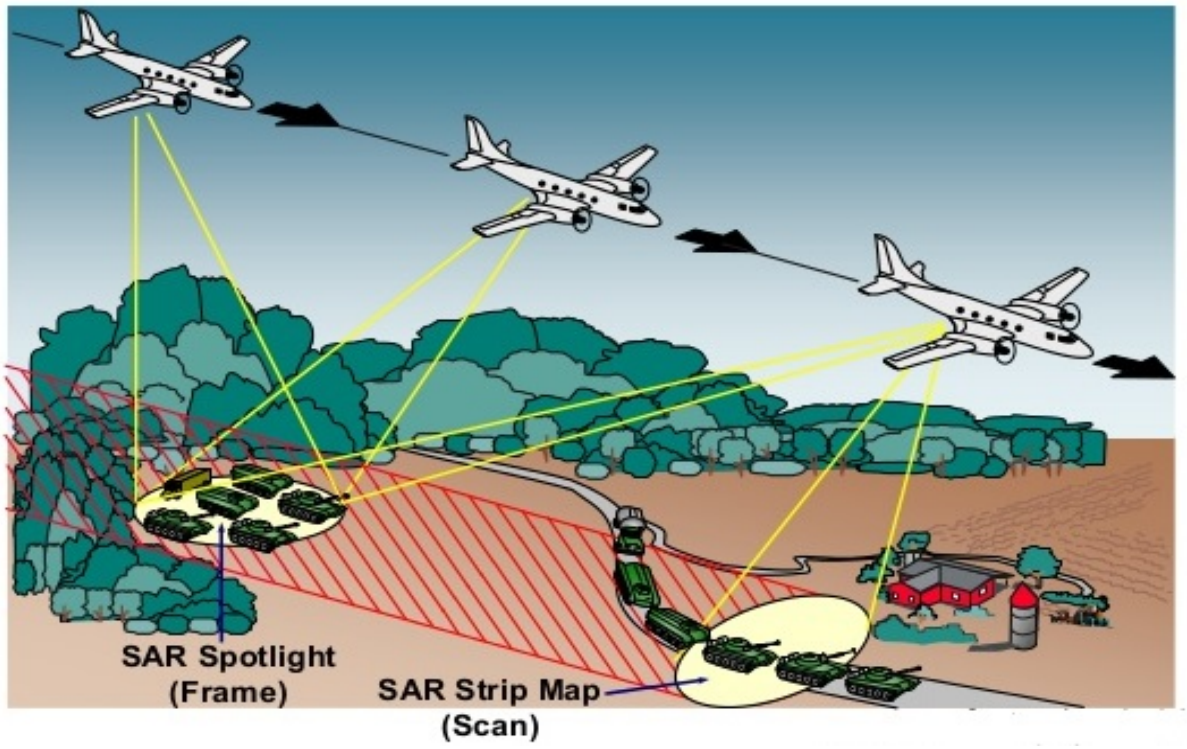

Figure 4.2: Spotlight and Stripmap SAR

Now Combine the benefit of Scan mode SAR and Spot mode SAR motivate the develop the advance SAR that allow high resolution and wide swath coverage without restrict contradiction.This concludes the basic concepts of SAR. The current project is based on implementing digital beam forming for NASA-ISRO Dual frequency Sweep SAR (NISAR).The NASA-ISRO Dual frequency Sweep SAR (NISAR) has been conceptualized to provide L and S band space-borne SAR data with high repeat cycle, high resolution, and larger swath, with capability of full-polarimetric and Interferometric modes of operation.

4.2 SAR system Design overview

This topic covers Design overview of the SAR system. The antenna system consists of parabolic reflector fed by planar aperture of feed arrays. Digital processing operations are obtained using the common reflectors illuminated by array aperture feeds. The characteristics of the radiation patterns are composite transmit pattern and multiple receive beams.The transmit secondary beam is generated by illumination of reflector by collimated primary beam of the phased array feed.The receive beams are switched beams in elevation plane by exciting the feed elements in the elevation plane sequentially. Figure 4.3 shows the antenna design with reflector with feed arrays.

The Feed Aperture is required to generate multiple receive beams and one composite transmit beam. The transmit beams are generated by combining all the receive beam ports in equal phase and amplitude. The feed array is supposed to be light in weight, compact in size and volume, structurally stiffer, thermally stable, electrically shielded and packaged intact, into absolutely stress free modules and these involve multi-materials and multi-constraint joints, precisely manufactured to the required mechanical precision and perfectly assembled to perform the intended antenna function of the feed array within the acceptable environment limits.

SAR consist the Digital Beam Forming unit subsystem. Signal Processing in DBF includes various operations like Jitter Measurement and correction on digitized multiple-channel data, Heterodyning, Digital Filtering, Digital Beam Forming, BAQ data compression, data formatting etc. SAR system consists multiple channels, which necessitates data acquisition hardware to receive and perform digitization on multiple channels and subsequently feed digitized multiple-channel data to Digital Beam Former unit. It required multiple channel with TRiM units and digitization and signal processing will then be performed in DBF subsystem.

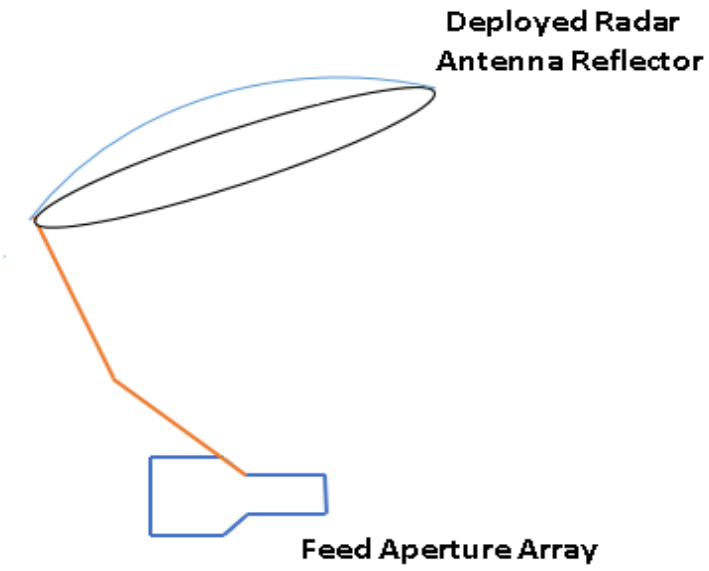

Figure 4.3: SAR Configuration

4.3 Beamforming for SAR

Here Digital beamforming explain for receiver side only. The radar system is split up into a transmit and a receive subsystem respectively. In principle the two subsystems can be mounted on a single or placed on separate platforms, however, in the SAR system in this work one common platform will be assumed for both subsystems.

SAR uses a parabolic reflector with a feed array consisting of multiple T/R elements in elevation. Each beam illuminates a section of range swath which is partially overlapped with the illumination swath of adjacent beam. For a region of swath on-ground only few receive channels are activated with highest gain.This process of selective receiver cannel activation reduces range ambiguities. In order to gain SNR advantage by digital beam forming each channel output is weighted before addition. The main advantage of this beamforming method is that it can produced wide swath over strip mapping with no reduction in azimuth resolution as in Scan SAR mode. The received multi-channel RF data transfers to DBF digital subsystem.The data passed through Analog to Digital converter and then feed to the DBF FPGA after IF sampling. DBF module translates received data to base band and initiates the beam forming

operation.

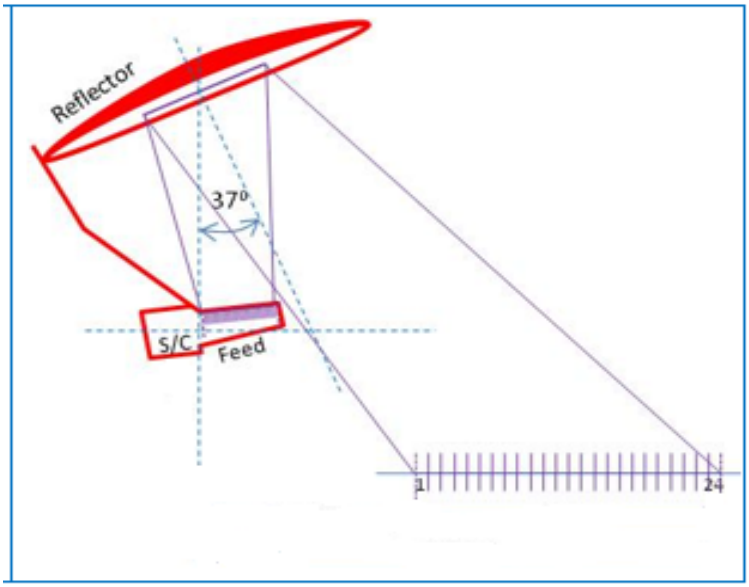

Figure 4.4: Transmitting Beam at Ground

During Transmit, all the TRiMs radiate simultaneously, thereby resulting in aperture illumination on the reflector, which is narrow in the elevation direction, but full in the azimuth. This, in turn, translates into wide footprint over the imaging region. As shown in figure all TR modules are illuminated which form a small footprint on the reflector. Small footprint on reflector works as a small aperture and reflect the signal falling on its towards The earth surface forming a large footprint on the ground.

During receive, each TRiM is activated one-at-a-time thereby, maximizing receive-aperture.This results in higher gain of the ground-return signal, but narrow footprint on the imaging region. The pointing angle of the secondary beam depends on the position of the receiving patch on the feed-structure.Receiving the narrow beam increase the power per unit scan area so it increases the signal to noise ratio. As the location of the patches is linearly distributed in the elevation direction,if there are 24 TRiMs, this 24 TRiMs will result in 24 receive-beams spanning the entire swath which is coincident with the wide-footprint of transmit-beam.

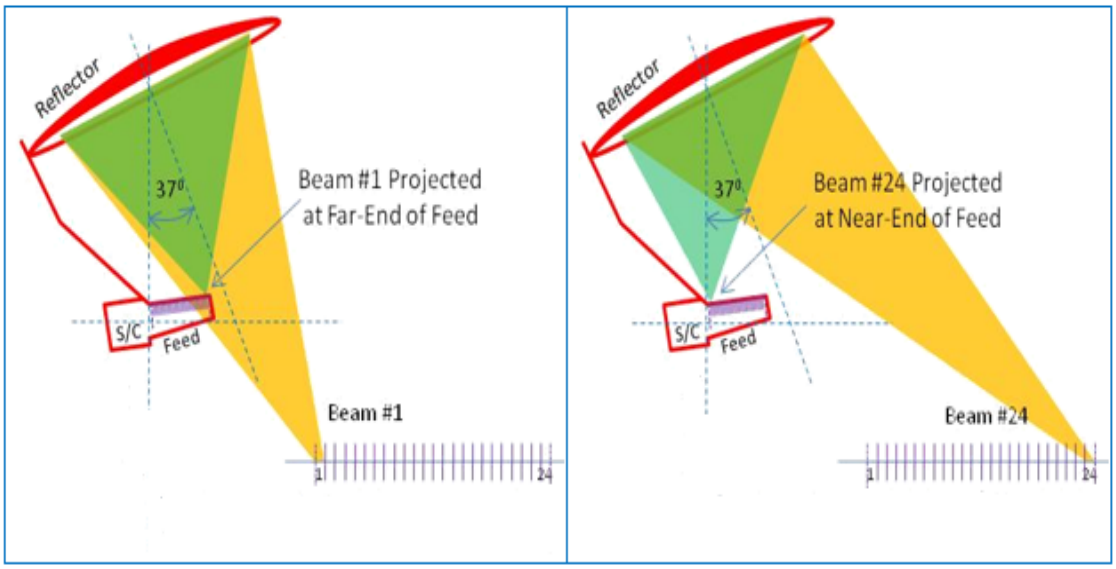

Figure 4.5: 1) Beam 1 and corresponding receive beam TRiM location on Feed 2) Beam 24 and corresponding receive beam TRiM location on Feed

As shown in figure 4.4 large footprint is treated as divided in multiple sub footprints and reflector routes the echo signal from different footprint towards the corresponding TR module based on range and angle.Thus echo from all beam are received using different parts of receive feed array.This cause different antenna gain for different beam at the time of the reception.

After receiving the signal from all T/R module.On-board DBF system combined the received channel data.The SAR DBF received data from all the 24 channels and generates a composite range line. This process reduces the overall data rate for wide swath SAR configuration. DBF coefficients will be stored in on-board E^2 PROM. The coefficients look up tables for all the channels will be generated on the basis of the transmitted and received antenna pattern and optimized signal to noise ratio (SNR) across the swath. Apart from this, the provision of coefficient upload facility will be incorporated in the payload so that any correction/adjustment or new table update can be performed to get the better results.

Signal Processing Flow for Digital Beam Forming for SAR

Figure presents Signal Processor flow diagram for digital beamforming.Band pass sampling is performed on received 24-channels signal, centred at IF of 200 MHz from RF section, by feeding them to multiple digitizers.Heterodyning operation is then performed on multiple-channel digitized data to extract I and Q data to bring data at base band. Post Heterodyning, low pass filter operation followed by decimation will be performed, the decimation factor of which depends on design constrain.Digital beam forming (DBF) operation will then be carried out on decimated data, with overlap of max five data widows at a time.

Coefficients required for DBF operation will be stored in memory. Inputs to DBF operation shall be data window (channel) number and sample number, which will be used for fetching coefficients from memory.Two operating modes are identified for Signal Processor: DBF Mode and DBF Bypass mode. In DBF mode, data post DBF will be fed to BAQ logic and will be sent to formatter for final frame formatting. In DBF Bypass mode, all 24 channels I and Q data will be fed to individual BAQ logic blocks and will be sent to formatter for final frame formatting. Since there will be skew among multiple channels, a separate Jitter estimation and correction logic is required to adjust the delay among channels before performing Beam forming operation.

As shown in figure 4.6 Signal processing flow of DBF. Before applying the Beam forming process Signal received by 24 TRiM module process throught some RF component like, a time correction and interpolation prorcess is done to correct the jitter and then signal process to DBF to where first signal translate to baseband and then signal is multiplied with Complex Coefficient DBF array and at the last step Complex addition for overlapping channel data array in time to obtain the composite line. Detail explains is given below.

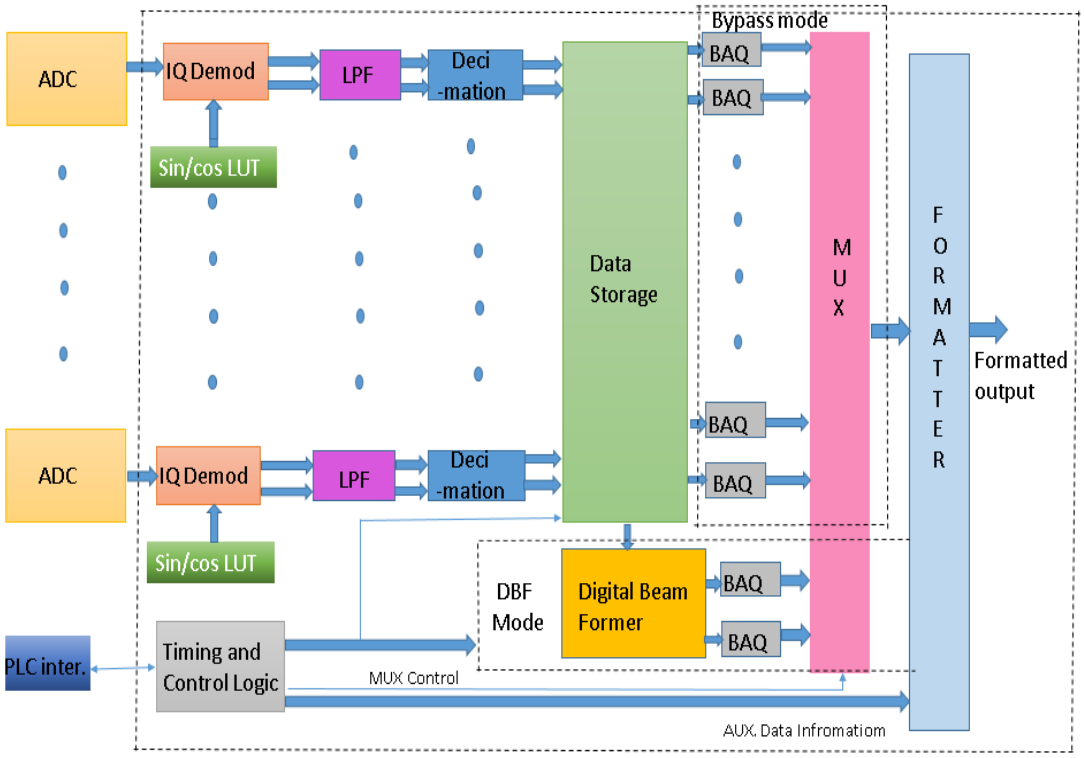

Figure 4.6: Digital Beamforming Processing flow for SAR

BDF coefficients are computed and stored in a memory before launch for each TRiM based on its antenna pattern. These arrays are stored according to look-angle or elevation time of signal arrival. Since data window start time may change for each TRiM channel, memory start pointer for each channel needs ground uploaded information or computation on-board according to start data window time. Process also needs end data pointer which can be computed from "data window duration" and sampling frequency for imaging session as per range bandwidth.

DBF system will get the overlapped sampled number information and compute the coefficient values for different beams. As shown in figure 4.7 five beam overlapped scheme is displayed in which a sample of combined beam is calculated on the basis of the sample value of each beam and their respective coefficient values.This scheme will continue till the formation of entire range line (all 24 receive channels) and digital Beam formed output will be transmitted after the Block Adaptive Quantizer (BAQ) and proper formatting. In case of bypass mode, same digital beam form operation

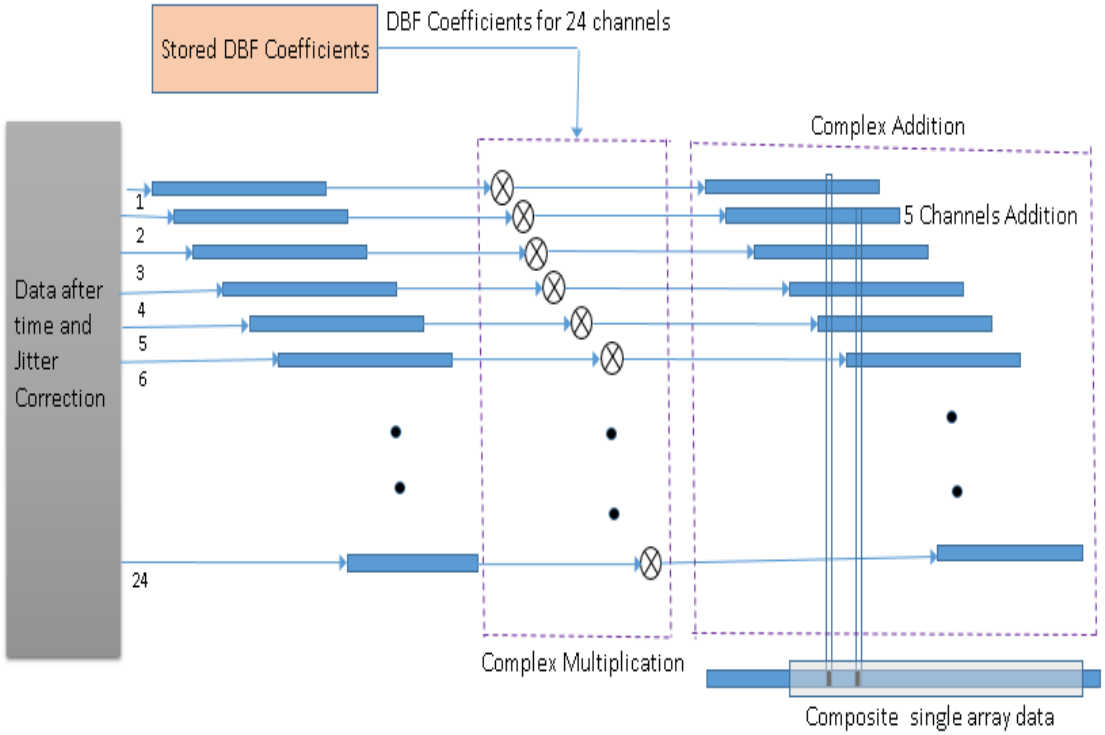

Figure 4.7: Digital Beamforming Signal processing algorithm

will be incorporated in the ground processing unit which will perform DBF operation on the BAQ decoded raw data and generate the beam formed output. As shown in figure 4.7 overlap of 4 to 5 beams will exist in the received window hence to do the beam forming, formatting and then transfer data to BDH unit in real time, the adequate storage is required.

Chapter 5
Simulation Result of Digital Beam Forming for SAR

This chapter explain the simulation result of the digital beamforming algorithm for SAR in HDL. Due to the unavailability of actual weight coefficients of SAR for beamforming, unfortunately the algorithm cannot be implemented on hardware. So the algorithm was checked in ISIM Simulator using dummy coefficients and it was found to be correct producing the desired output.The code and its output are presented below in detail.

Figure shows the beamforming algorithm results simulated in vhdl. Here Dummy inputs and coefficients are taken to explain the Beamforming algorithm. As shown in figure 5.1 and 5.2 dummy inputs are taken one and weight coefficients are ramp signal. According to algorithm as the input signal received from ADC they are multiplied by the coefficient according to the input signal from each channel. coefficients are already computed for each channel and stored in the FPGA memory. The beam from the parabolic reflector illuminates the five TRim modules on feed array so to get the data from each section of the ground beam, overlapping of the five signal are taken. as shown in figure output from multiplication signal are added by taken the overlapping of five channels sample at any instant of time.

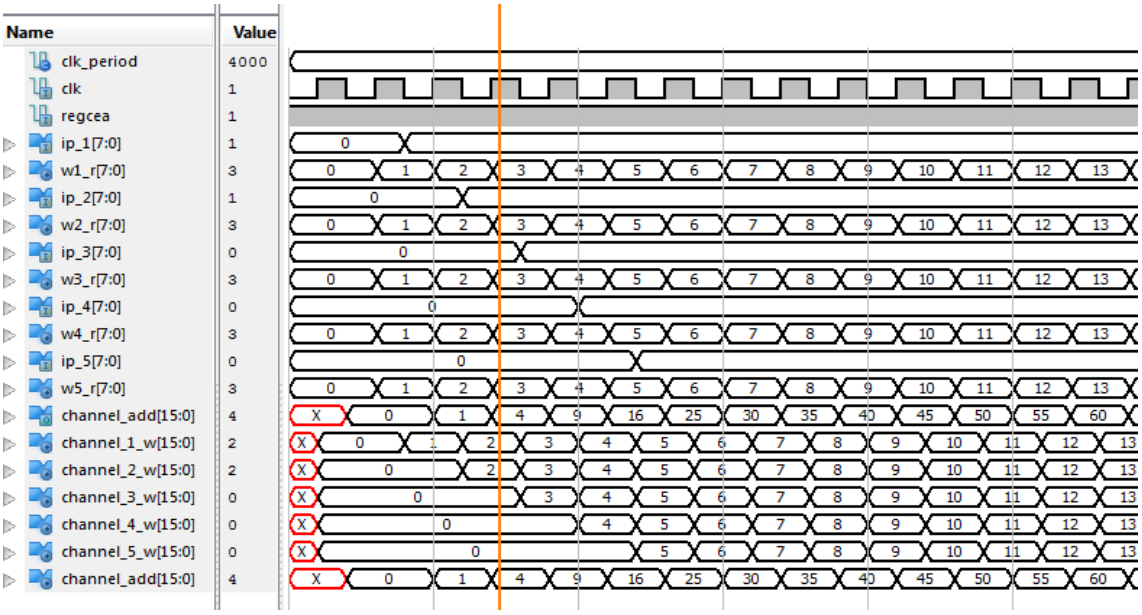

Figure 5.1: Digital Beam Forming Processing algorithm in hdl

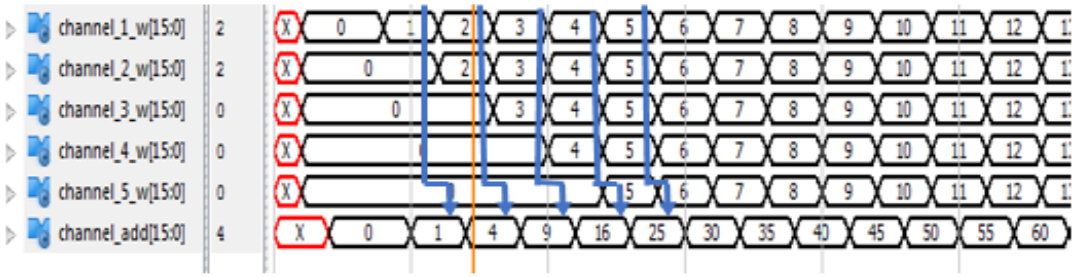

Figure 5.2: Combine single Beam Form output in hdl

Chapter 6
Conclusion

From this thesis it is conclude that the digital beamforming at receiver side has increase the improve in the SAR system. The new generation of digital radar sensors will be able to resolve the contradicting requirements for high resolution and wide coverage. This thesis mainly has two parts: first part explains the basic of the Digital beam forming with suitable simulations results and implantation on FPGA.and second part explains the Digital beamforming for the SAR system. Here new concept of the digital beam forming for SAR is introduced to achieve the High resolution and Wide swath simulatiously.this concept includes the deployable reflector antennas to alternative direct radiating arrays and a low number of receiver TRim modules. at the receiving side it is not necessary to cover the full swath at a one time .Instead to achieve good resolution and wide swath it could be receive the narrow beam from the small portion of the ground swath coverage and digitally steered through dynamic beam formation to follow the return of the echo as it moves across the angle space. so this technique allowed the take the advantages narrow received beam pattern from the reflector antenna and help the improve resolution and wide swath simulations

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