ASIC Design of 8-bit 250MSPS Two-Step Flash ADC

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Shruti Doshi

(15MECV26)

Electronics & Communication Department
Institute of Technology
NIRMA University
Ahmedabad-382 481

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Under the guidance of

External Project Guide:
Mr. Sanjay Trivedi
Head of MSDPD
SAC ISRO
Ahmedabad

Internal Project Guide:
Dr. N.M. Devashrayee
Institute of Technology,
NIRMA University,
Ahmedabad.

Electronics & Communication Engineering Department
Institute of Technology
NIRMA University
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May 2017

Certificate

This is to certify that the Major Project entitled **"ASIC Design of 8-bit 250MSPS Two-Step Flash ADC "** submitted by **Shruti Doshi (15MECV26)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in VLSI Design , NIRMA University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this major project, to the best of our knowledge,haven't been submitted to any other university or institution for award of any degree or diploma.

Dr. N. M. Devashrayee
Internal Guide

Dr. N. M. Devashrayee
PG Coordinator (VLSI Design)

Dr. Dilip Kothari
Head, EC Dept.

Dr. Alka Mahajan
Director, IT-NU

Date:

Place: Ahmedabad

Certificate

This is to certify that the Project entitled "**ASIC Deisgn of 8-bit 250MSPS Two-Step Flash ADC**" submitted by **Shruti Doshi (15MECV26)**, towards the submission of the Project for requirements for the degree of Master of Technology in VLSI Design, NIRMA University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

Mr. Sanjay Trivedi
Head of MSDG/MSDPD,
SAC ISRO,
Ahmedabad

Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at NIRMA University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Shruti Doshi

Acknowledgement

I would have never succeeded in my thesis without the cooperation, encouragement and help provided to me by various people. Firstly, my sincere thanks to my team for their help during this ongoing internship. Their wisdom, clarity of thought and support motivated me to bring this project to its present state.

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Last but not the least I wish to thank my friends for their delightful company which kept me in good humor throughout the year and thus helping me complete the degree program successfully.

- Shruti Doshi

15MECV26

Abstract

Modern wireless communication devices demand high data rate and low power consumption. The key components in the portable device which acts as an interface between analog and digital domains are Analog to Digital converters. As the demand for portable devices is increasing, more importance is given to the low power methodologies for high speed applications. Power consumption can be reduced by using small feature size processes. But as the power consumption reduces, process variations and other parameters affect the overall performance of the device. High speed, medium resolution and low power consumption are the major requirements in portable devices.

The aim of this project is to design an 8-bit 250MSPS ADC. It is a mixed signal ADC ASIC. The architecture chosen for this design is sub-ranging type 2-step flash ADC. The ADC is designed in two steps of 4-bit flash type ADC.ADC design consists of sample and hold block, comparator block, op-amp, bias circuit and TGB encoder. Sample and hold design is implemented using switched capacitor logic and it also consists of an operational amplifier (opamp). A general purpose op-amp is designed which could be used in 3 different modules of ADC, S/H amplifier, Subtractor and Residual amplifier. After in-depth analysis of different op-amp topologies with reference to given specifications, Two Stage Folded Cascade topology is selected.The comparator is of clocked type.

The ADC has been designed, implemented and analyzed in 180nm technology using Cadence Virtuoso 6.1.5 in spectre simulator.

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Introduction

1.1 Introduction

The signals in the real world are mostly analog in nature for example voltage and current. This signal has to be converted into digital form so that a computer can process, transmit or store information. This conversion is achieved using Analog to Digital Converter. Analog to Digital converter is one of the important components in signal processing and communication system. Digital to Analog converter is required whenever analog signal is needed back.

Analog to Digital converter plays an important role in the design of electronic system where analog data is to be processed using digital logic. Even though the functionality is increasing, the size of these devices are decreasing day by day. Power consumption is the most important criteria in the design of such systems since most of this appliances run on batteries.

There are various types of converters available for conversion of analog to digital form. A particular ADC is chosen depending upon its application. Cell phones, cameras are example of devices that uses ADC. The prime requirement of high speed ADC are sample and hold circuits. It is necessary to generate CMOS implementation to reduce the size and cost. As compared to discrete component, the design of mixed signal ASIC design reduces the overall power and area requirement. In space application such as video processing temperature sensor, bias generator ADC is the main analog block. In ADC design, op-amp is the key component.

ADC can be classified in terms of speed and accuracy as :

(1) Low-to-medium speed and high accuracy

i. Integrating Oversampling ADC

(2) Medium speed and medium accuracy

i. Successive Approximation ADC

(3) High speed and low-to-medium accuracy

i. Two-step Flash ADC

ii. Pipeline ADC

Two-step Flash ADC is selected for microwave radar and signal processing due to its high speed and better accuracy requirements.

It consists of sample and hold block, comparator block, op-amp, bias circuit, TGB encoder, Subtractor circuit, residual amplifier and DAC block. The primary requirement of the design is to implement the Op-amp. So the work started with the design of op-amp according to the given specifications. The comparator is also a crucial block. It is implemented in Clocked Comparator configuration. Various parameters such as speed, offset, delay are calculated to analyze the performance of comparator. Op-amp shall meet the specifications for space application such as slew rate, gain bandwidth product, CMRR and offset voltage. For this purpose, various op-amp topologies are compared and two stage folded cascode op-amp is found to be suitable for this application.

1.2 Purpose and Goals

In data convertors with increasing speed, need of resolution and accuracy also increased.

First goal is to create an Op-Amp which should be used in sample and hold, residual amplifier. The Op-Amp created should match requirements of complete 8-Bit ADC modules. Other specification for ADC is listed above in the table 1. Here design of voltage references arises because from fabrication point of view the design should be insensitive to parameter variation such as supply, temperature, resistance. To generate such type of voltage reference there are four methods, resistive ladder, capacitive ladder, band gap references current mirror. Out of which the voltage is generated

Table 1: Specifications for 4-bit ADC

Sr. no	Parameters	Specifications
1.	ASIC type	Mixed Signal ASIC
2.	Foundry	SCL, Chandigarh
3.	ADC Sampling Frequency	250MHz
4.	Analog Bandwidth	100MHz max
5.	ADC Resolution /ENOB	4-Bits / >3.5 bits
6.	ADC Input Single Ended	1 V p-p
7.	Voltage Reference	1.65 , 2.15 , 1.15
8.	INL / DNL	$\pm 1LSB$
9.	Output	4-Bit LVCMOS parallel data
10.	Power Supply	3.3 V Analog
11.	Junction Temp.	-15° C to +80° C
12.	Power Dissipation	< 200mW

by using band gap references as it less affects the gain and it generate more stable output compared to other design.

Analog bandwidth is calculated 50MHz. All 4-Bit results are obtained with 50 MHz analog bandwidth input signal. To specify performance of ADC typical parameter is calculated with high performance tool.

1.3 Salient Features of ADC

1. It is a mixed signal ASIC with 180nm CMOS process through SCL foundry
2. 8-bit resolution at the rate of 100MHz Sampling frequency
3. Compatible with 250MHz analog bandwidth signal as single ended/differential input
4. 3V supply for analog design and 1.8V supply for digital design.
5. 1 LSB of INL/DNL
6. Power dissipation less than 250mW

For the design of ADC, various architectures were studied like flash, successive approximation, sigma delta, pipeline and sub-ranging. With the given specifications of 8-bit resolution, 100 MHz sampling frequency; flash type of architecture is chosen and implemented in 2 step flash type of architecture. As shown in figure-1.1 we are going to implement two stage Flash type architecture in a subranging way. In the first stage, 4-bit flash ADC output will be converted into analog signal by 4-bit DAC which is subtracted from the input signal and residual signal is further amplified for the second stage 4-bit flash ADC input. First ADC output will act as a MSB and second ADC output acts as a LSB. Total 8-bit data will be latched and then error detection and correction logic will be implemented on this for the final 8-bit output.

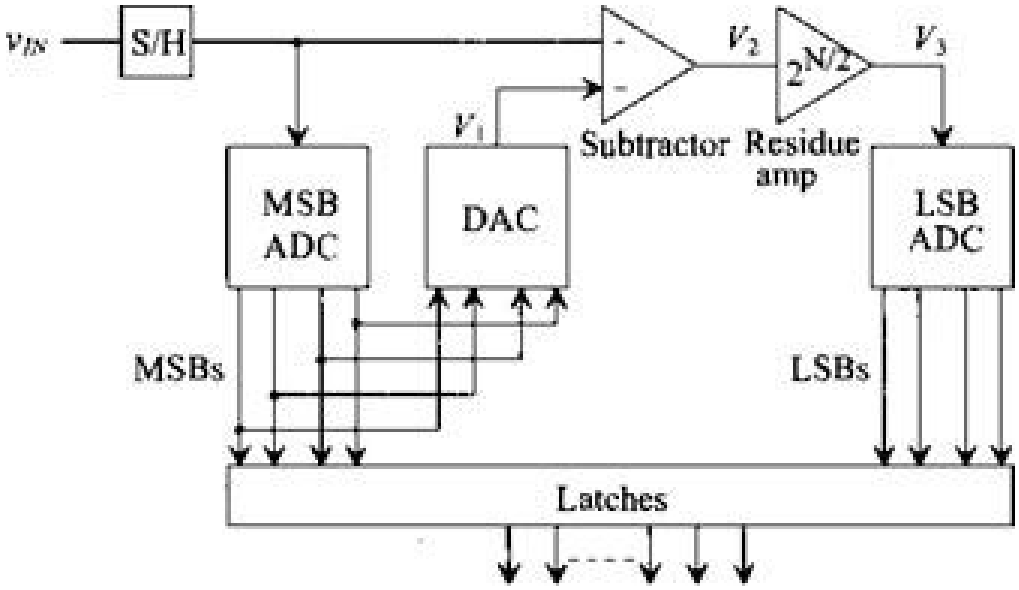

Figure 1.1: Generalised Block Diagram of 2-step Flash ADC

1.4 4-Bit Flash ADC

For realizing 4-bit ADC, 2^4-1 (15) Comparator modules and 2^4 (16) resistors are required. The output of this will be thermometer code which is to be converted into binary code. The comparator module is designed using clocked comparator type of topology.

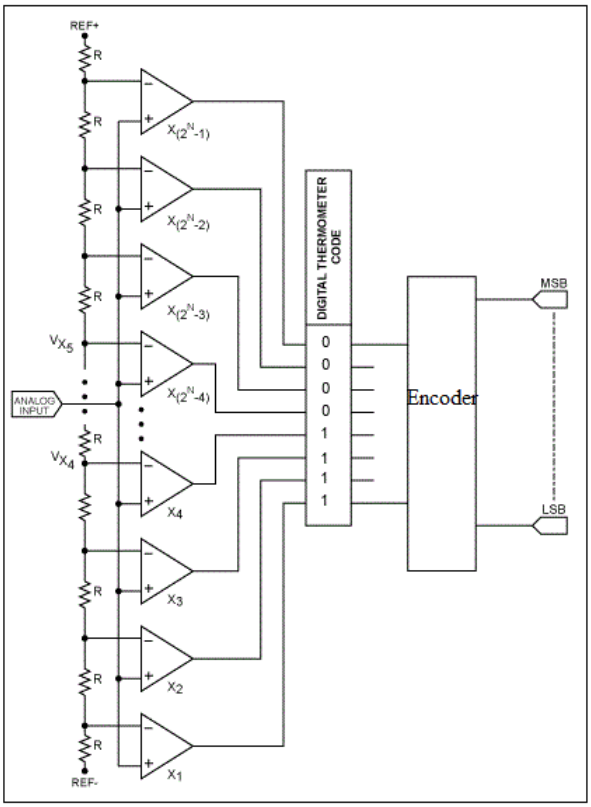

Figure 1.2: Flash ADC

Chapter 2
Thermometer to Binary Encoder

2.1 Introduction

The outputs from the comparator array in a flash ADC is in thermometer code format because of its parallel structure. Since the number of comparators in a flash ADC is 2^n-1, hence the number of bits in the thermometer code at the output of comparator array will be 2^n-1. Thermometer to encoder is used to convert this thermometer code to the binary code. The encoder is designed in two stage circuit which translates the thermometer code into the intermediate gray code and then gray to binary code to reduce the effect of bubble errors.There are numerous methods available to convert the thermometer code to the binary code. Out of these, direct conversion architecture using 2:1 multiplexers and intermediate gray code based conversion using basic gates is used very extensively. Other than, these two there are some more methods like Wallace tree encoder using full adders, a fat tree encoder are also available.

2.2 Multiplexer Based Direct Conversion Architecture

In this type of architecture, the thermometer code is directly converted to the binary code using 2:1 multiplexers based on the truth table given in table. From the truth table, it is clear that the bit B4 is equivalent to the thermometer code C8. Then the bit B3 can be obtained from C12 and C4 by taking C8 as selection line for the multiplexer. Similarly, all other bits are obtained from the input thermometer codes. Because of its low power consumption and high speed, this architecture is one of the most common architecture used in ADC design.

It requires 11 2:1 multiplexer for a 4-bit encoder

The encoder design consists of D-flip-flops also. Full implementation of TGB encoder is shown in fig 2.1

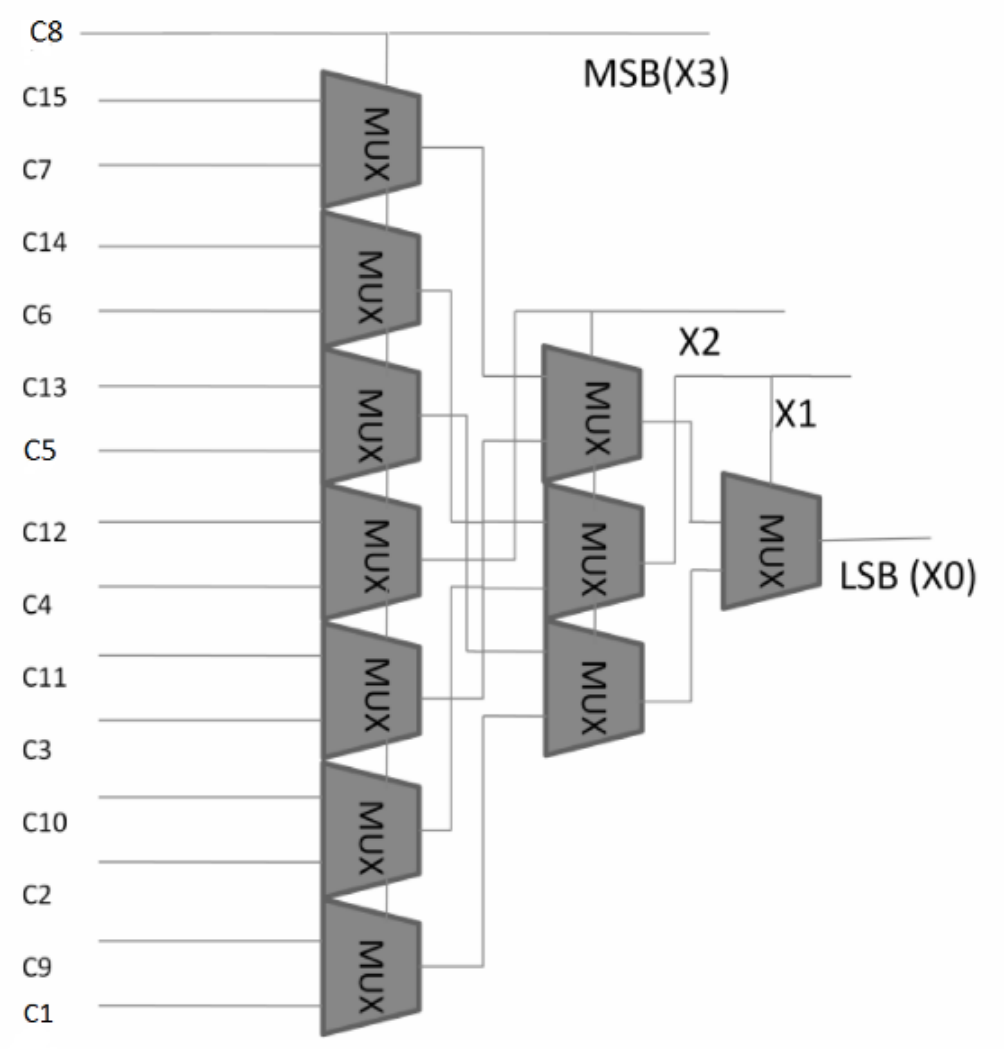

Figure 2.1: TGB Implementation

Below Table shows the conversion of thermometer code to binary code. For each combination of inputs one bit is changing, results in a one value increased at the output. Priority based approach is more preferred as compared to gate based approach.

Conversion of thermometer code to binary code

Voltage Range	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	B3	B2	B1	B0
1.15 to 1.24362	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1.24362 to 1.30614	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
1.30614 to 1.36865	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
1.36865 to 1.43116	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
1.43116 to 1.49368	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
1.49368 to 1.55619	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
1.55619 to 1.6187	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
1.6187 to 1.68122	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
1.68122 to 1.74373	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
1.74373 to 1.80624	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
1.80624 to 1.86876	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
1.86876 to 1.93127	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1.93127 to 1.99378	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
1.99378 to 2.0536	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
2.0536 to 2.11881	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
2.11881 to 2.15	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	1	1	1	1

2.3 Gate Based Encoder

Gate based Encoder can be designed by constructing K-map and solving the equation. If this approach is followed, we will see that most of the parts in the equation is repeating number of times. So this logic can be effectively implemented with mux based design. Moreover, the output generated at the output terminal of B0 and B3 have time delay. So to avoid this delay, number of logic gates are added in the path according to the requirement as shown in fig 2.2

To make this design accurate, the data should be latched at the one instance only. Therefore, in each path, D-FF latches the output. Here the data is latched with inverted clock to minimize the error. This allows the comparator sufficient time to latch data.

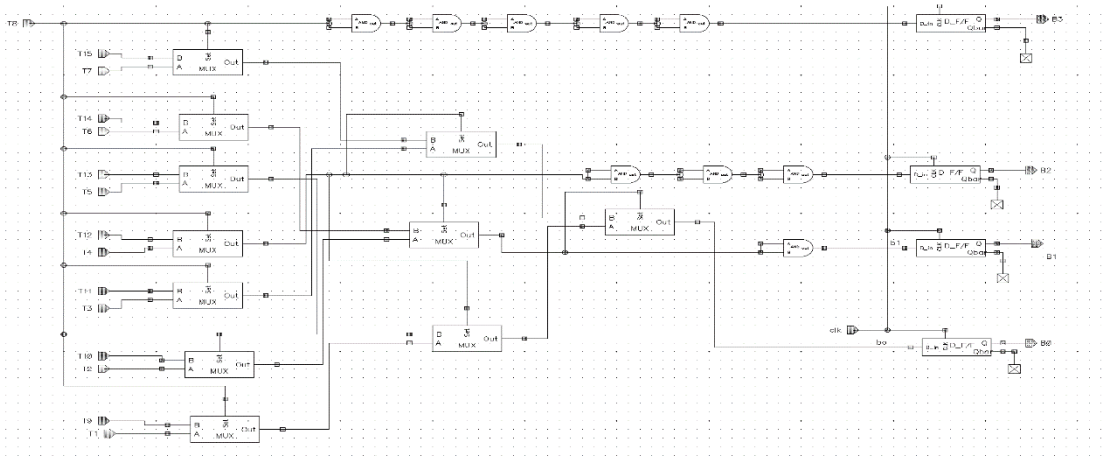

Figure 2.2: TGB Encoder Schematic

D-FF used in TGB encoder is designed using transmission gate as shown in fig 2.3. D-FF latch the data available at the input to the output only at the active edge of the clock. It will hold that value until the next clock edge.

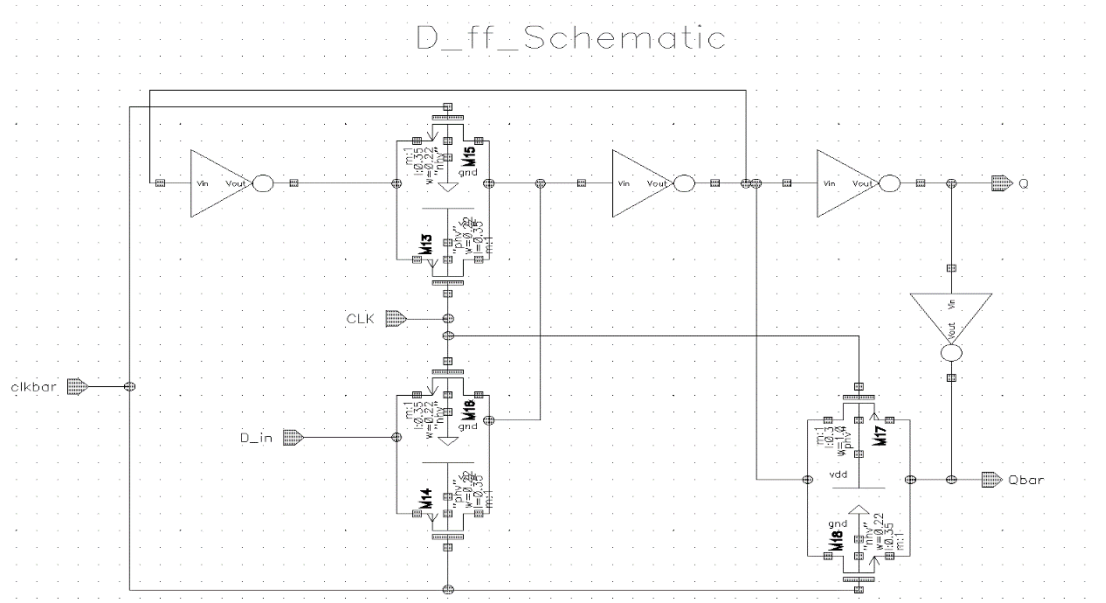

Figure 2.3: D-FF Schematic

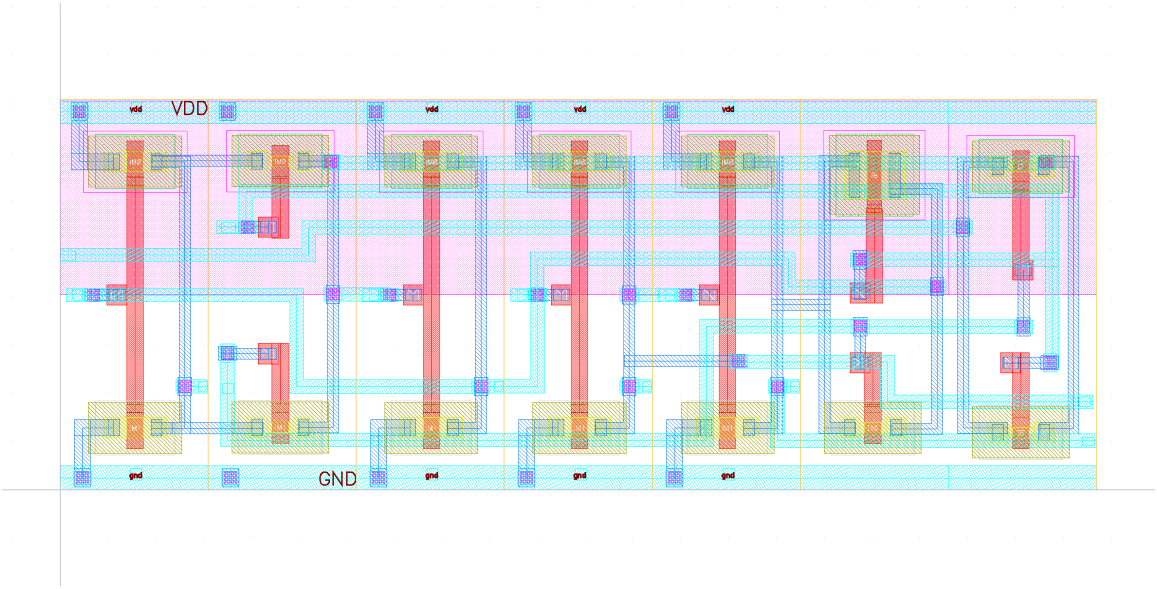

Figure 2.4: Layout of D-FF

Multiplexer is designed using CMOS topology. Fig 2.5 shows the schematic of multiplexer.

Fig 2.6 shows the layout of Multiplexer.

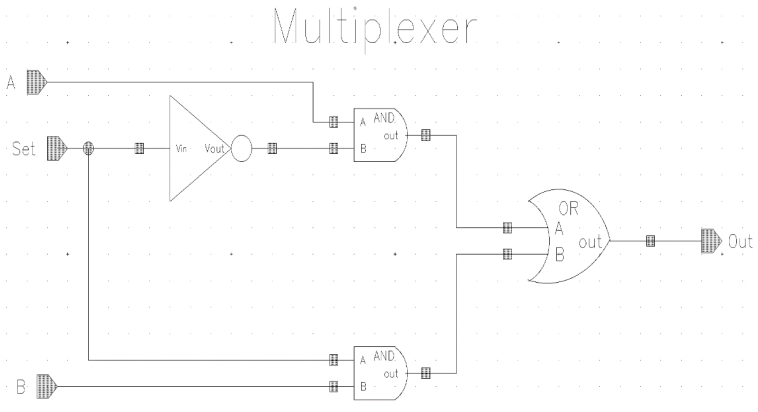

Figure 2.5: MUX Schematic

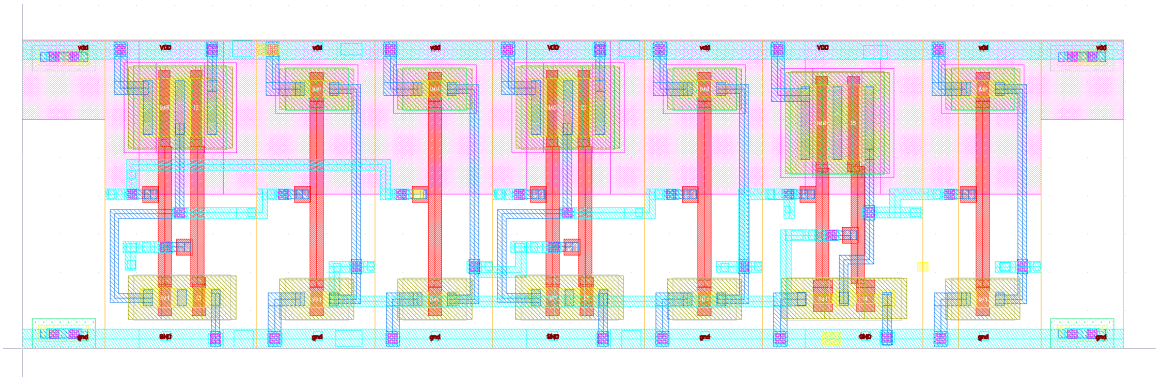

Figure 2.6: Layout of MUX

Layout of MUX,D-FF and AND is used in TGB encoder. Fig 2.7 shows the layout of TGB

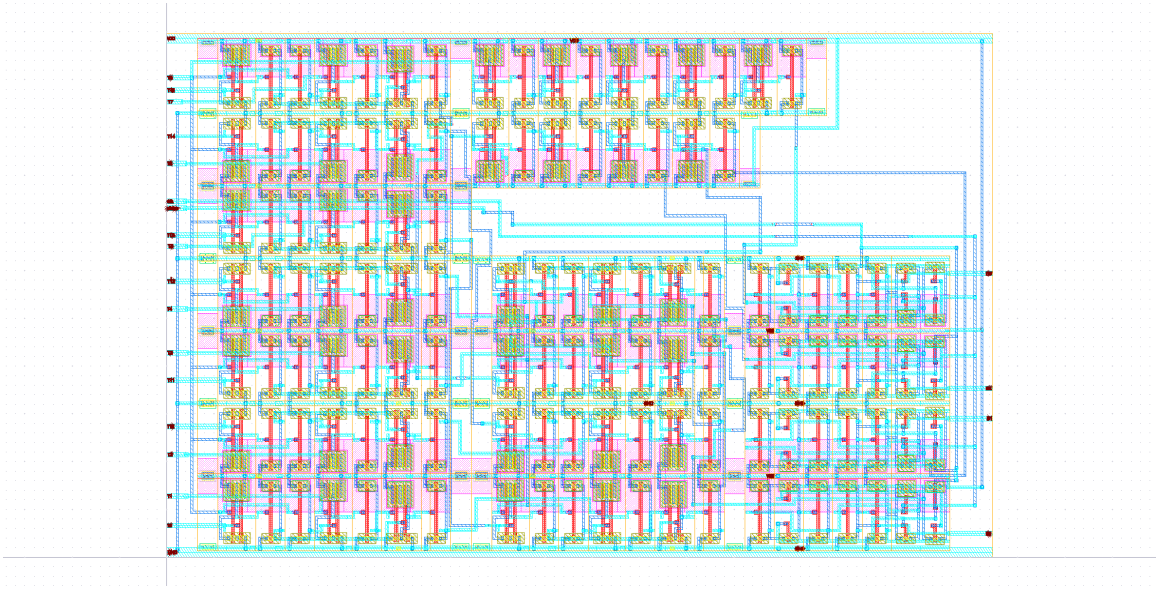

Figure 2.7: Layout of TGB

2.4 Design Rule Check

In order to ensure a lower probability of fabrication defects, the created mask layout must conform to a complex set of design rules. A rule checking tool is available with cadence which checks most of the rules. The designer must perform DRC and make sure that all the layout errors are eventually removed from the mask layout, before

the final design is saved. Here we are using Mentor Graphics tool Calibre. Following are the steps to run DRC:-

(1) Click Calibre .

(2) Click on Run nmDRC

(3) A new window will open in which various options are given → Rules, Input, Output, Run DRC etc

(4) Click on rules to load rule file.

(5) Set required input and output parameters.

(6) Then run DRC

(7) DRC report will be displayed which shows all the errors.

(8) If DRC shows errors then, click on one of the errors and it will be highlighted in the layout.Now, correct the error as per design rules. Repeat the same procedure for all remaining errors.

(9) When all the errors will be removed, DRC will be clean and now one can go for LVS.

Note:- Most of the errors found by the DRC are spacing between metals, width of metal etc. and are easy to fix.

2.5 Layout Versus Schematic

It compares the original schematic with the one extracted from the mask layout and proves that the two networks are indeed equivalent and so it is known as layout versus schematic (LVS). The LVS step provides an additional level of confidence for the integrity of the design. But a successful LVS does not mean that the extracted circuit will actually satisfy the performance requirements. It checks only topological match. Any errors that may show up during LVS should be corrected in the mask layout before proceeding to post-layout simulation.

Steps for LVS-

(1) After DRC is clean, again go to calibre.

(2) Click on Run nmLVS.

(3) A window will open which has options similar to nmDRC.

(4) Load the rule file in Rules option

(5) In input, click on netlist and uncheck the **Export from schematic viewer**

(6) Set required input and output parameters.

(7) Click on Run LVS

(8) LVS report will be displayed which shows the **correct** if both schematic and layout are similar else **incorrect**.

(9) We can highlight the error if present to correct it.It highlights the incorrect nets,ports,instances in both schematic as well as layout

Note

- This report consists of 2 columns- 1st for the source (schematic),2nd for the layout and comparison is done. The errors are mainly of incorrect nets, pins, terminals etc.
- If number of nets in layout > schematic, then some connections are left in the layout that has to be corrected.
- If number of nets in layout < schematic, then some extra connections are there in the layout that has to be corrected.

2.6 Extraction and Post-layout Simulation

Once the layout is made, there always is parasitic resistances and capacitances associated with it. This is because of the compact layouts to make the chips smaller. More you make compact layout more will it introduce these parasitic components. This interferes in the functioning and performance of the circuit in terms of timing,

speed and power consumption.

Parasitic capacitances and resistances in the layout can strongly affect the performance of a design. To evaluate the effects of parasitics and to gain a higher degree of confidence that a layout will result in a chip that meets the specifications, it is important to do post-layout simulations. The performance of a circuit predicted with parasitics accounted for will always be worse, although closer to reality, than a schematic that does not include estimated parasitics. The procedure for running post-layout simulations is very similar to simulating a Schematic. The steps to prepare a design for post-layout simulations are listed below.

1. Extracting the parasitics

To include the actual parasitics of a layout, we need to extract them. This can be achieved during the extraction phase of verification.

(1) To extract a layout with parasitic capacitors and resistors, click on Calibre → nmPEX in the layout window (after correcting all DRC and LVS violations). An extraction runs DRC and LVS again, then models the parasitic components.

(2) In the window that comes up, load the rule file.

(3) Choose your 'calibre_pex' directory as your PEX run directory.

(4) Go to Inputs → Netlist and check the Export from schematic viewer bullet.

(5) In outputs, change the format to CALIBREVIEW. Change use names from to SCHEMATIC. Set the extraction type to transistor level and "R + C + CC" to extract both parasitic capacitors and resistors. Go to setup → PEX Options. Check ground node name and name it as gnd!

(6) Run PEX

After running, on the "Calibre View Setup" form that pops up,

- Change "Calibre View Type" to "schematic"

- Change "Create terminals" to "Create all terminals"
- Change "Device Placement" to "Arrayed"
- Change "Open Calibre Cellview" to "read-mode" and then click Ok

Warnings are fine, but if errors are there, then Check that the pin names and net names match with the schematic and layout. Go through the steps above from scratch to make sure you have all of them correctly; one missing step could easily result in wrong results.

If no error is present, then following screen comes up with a parasitic diode, lots of parasitic resistors and small parasitic capacitances (to the order of atto Farads = 10^{-15}).

By zooming into one of the capacitors, we can see that between which nets the capacitance is being produced. A "calibre" view will be created in cadence that is a schematic in Virtuoso, from which you can simulate.

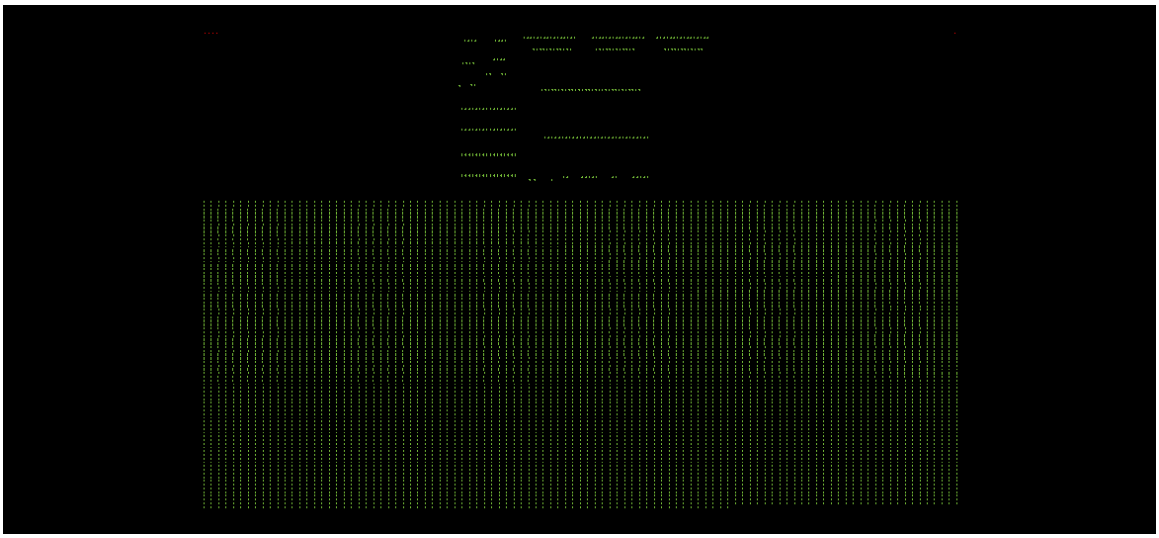

Figure 2.8: Calibre View

2. Creating a new Configuration

A config view is used to select different views (like schematic,calibre, verilog-a, verilog, extracted etc) of a cell in a schematic and enables you to run simulations for

that particular configuration.
Here is how we can create a config view.

- In the library Manager window, create a new cell view
- Go to File → New → Cell View. In the Create New File window that appears, in the "View Name" field type config and the "Tool" field should automatically change to Hierarchy-Editor. Select OK
- Two windows will appear. In the New Configuration window, select Use Template.
- In the Use Template window that appears, select "spectre " in the "Name" field drop-down list, Select Ok.
- Back in the New Configuration window, change the "View" field from my view to schematic.
- Now the Cadence hierarchy editor will appear as its default table format.
- Select Table view.
- Right click on the cell and set cell view to calibre view.
- Next, save these settings by selecting View → Update and File → Save. Close the window.

3. Post-layout Simulation

Open the config. view and simulate it in the same way as schematic (Launch ADE L and select simulator as spectre). The waveform we get is the post-layout simulation. We can also plot the pre-layout and post- layout simulation on the same window to compare.

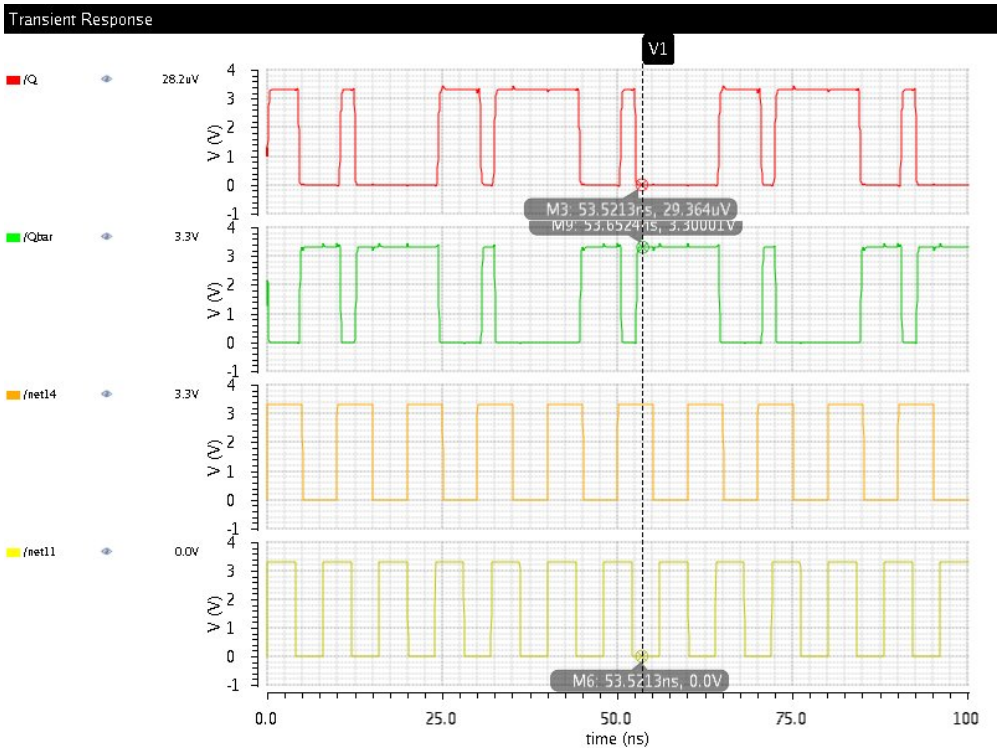

Figure 2.9: Post-layout Simulation of D-FF

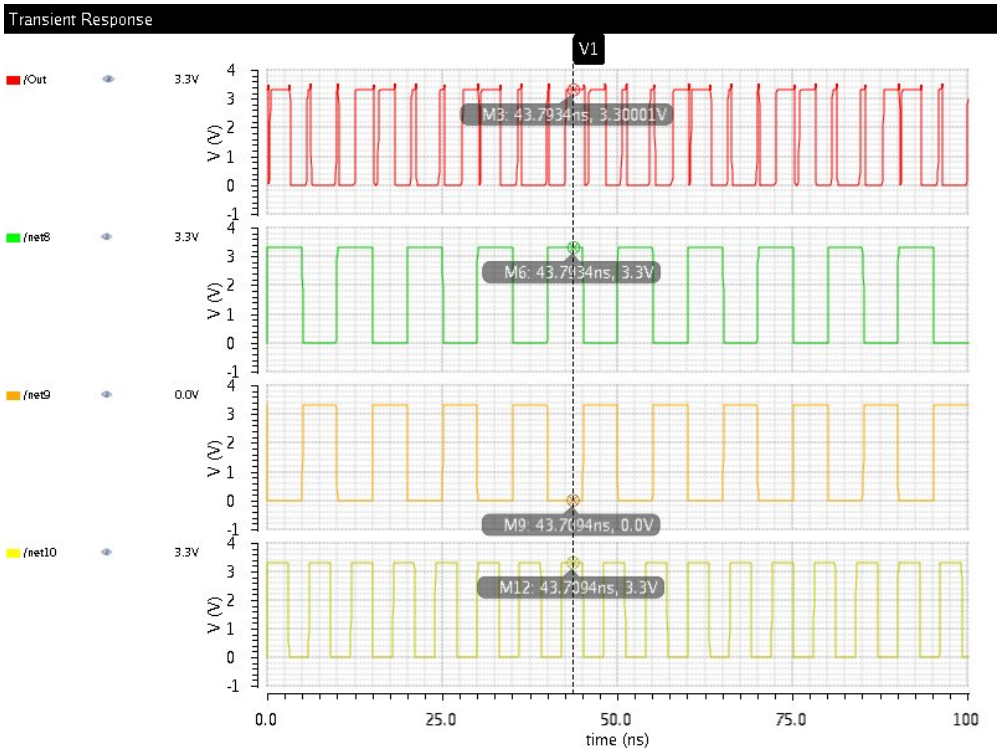

Figure 2.10: Post-layout Simulation of MUX

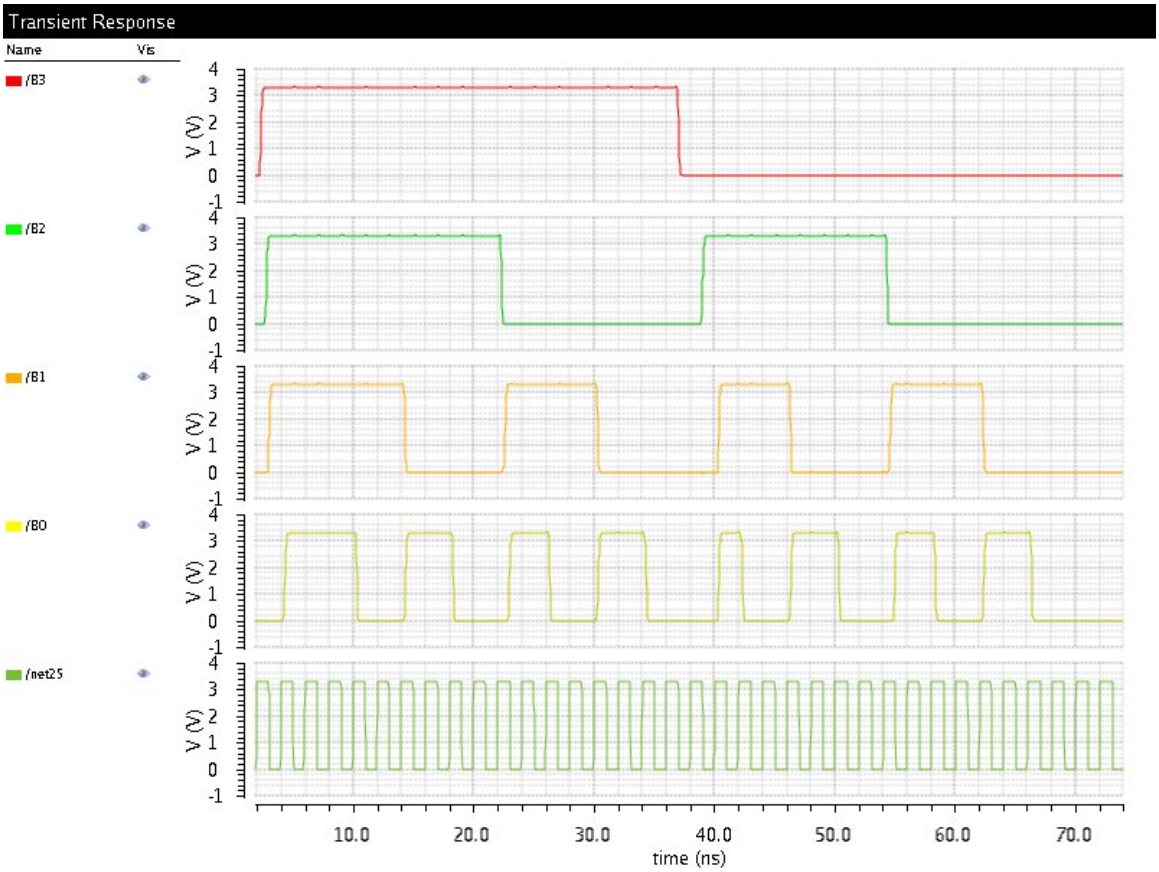

Figure 2.11: Post-layout Simulation of TGB

Chapter 3
Opamp Design

3.1 Introduction

The selection of any Opamp must be based on the understanding of what particular parameters are most important to the application

3.2 Parameters of Opamp

1. Offset Voltage

Input offset voltage is a small voltage between the inverting and non-inverting inputs of op-amp which is required to balance mismatches due to unavoidable process variations.

It is abbreviated as Vos. Vos is modelled as a voltage source driving the non-inverting input.

2. Common-mode gain

Common-mode gain measures how much the output changes with respect to a change in the common-mode input level. The common-mode gain of an op-amp is ideally zero. The amplifier should amplify only the differential-mode signal and ignore the common-mode level.

3. CMRR

Common-mode rejection ratio or CMRR is an important figure of merit in op amp design. It is defined as the differential-mode gain divided by the common-mode gain Ideally, CMRR of an amplifier should be infinite. Practically, designers try to have CMRR $>$ 60 dB , though some applications may required much higher values.

The bias point of the input differential pair is affected by the common-mode input. Because of the inherent mismatches in the input circuitry, the offset voltage changes by changing the bias point, which, in turn, changes the output voltage.

4. PSRR (Power Supply Rejection Ratio)

The output should not change if the supply of an op amp changes, but it typically does. If the supply changed by X volts produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. The definition of PSRR assumes that both the supplies are altered equally in opposite directions, otherwise common-mode change as well as a supply change will be introduced and the analysis will become more complex. This effect causes apparent differences in PSRR between the positive and negative supplies.

5. Slew Rate

The rate of change in the output voltage caused by a step input is known as Slew rate SR. Its units are $V/\mu s$.

AC analysis is used to determine the small-signal bandwidth of the op amp. The large signal effects such as slew rate, the maximum speed at which an op amp can charge and discharge its load limits the speed of amplifiers. Configure the op amp as a unity-gain buffer as shown below to measure slew rate

6. Unity Gain Bandwidth

Unity-gain bandwidth (B1) and gain bandwidth product (GBW) are very similar.

GBW specifies the gain-bandwidth product of the Op-Amp in an open loop configuration and the output loaded:

$GBW = A_{vd}f$

B1 specifies the frequency at which A_{vd} of the Op-Amp is 1.

7. -3db Small Signal Bandwidth

The -3 dB bandwidth of an op amp will almost always be greater than the full power bandwidth because the signal doesnot have to swing as far. Since Vp is reduced, the bandwidth is increased.

8. Rise Time and Fall Time

We might also have a spec for rise and fall times for high speed op amps. Ideally they should be same but typically there is some difference in practical op amps. Rise and fall times are calculated by applying a square wave to the op amp and then measuring

on the output waveform. This is closely related to slew rate. Also as is done with slew rate, we generally measure between the 10 and 90 points, so that the overshoot and ringing do not enter into the picture. Generally the input wave will be full scale, but occasionally it is specified for a smaller input signal.

9. Phase Margin

Phase margin at unity gain (fm) is the difference between the amount of phase shift a signal experiences through the Op-Amp at unity gain and 180°:

$fm = 180° - f@B1$

It is recommended that the phase margin of any amplifier be at least 45 ° (60° is recommended) for stability reasons. A phase margin below 45° will result in long settling time and increased propagation delay. The Op-Amp system can also be thought of as a simple second order linear control system with the phase margin directly affecting the transient response of the system.

The phase margin can be measured by applying the following steps in Cadence design tool:

- Obtain the AC response simulation
- Delete all the outputs in the ADE window
- Select the AC response curve (it will turn to yellow).
- From the Analog Design Environment (ADE) window: *Result* → *directplot* → *AC* magnitude and phase
- Follow the prompt at the bottom of the schematic window and select the output node
- From the ADE window : *output* → *to* be plotted
- You will get the magnitude and the phase frequency response. Split the graphs

10. Gain Margin

Gain Margin is the difference between unity gain and the gain at 180° phase shift:
$GainMargin = 1 - Gain@180°$ phase shift

11. Settling Time

A finite time is taken by the signal to propogate through the internal circuitry of an op- amp. Therefore, it takes a period of time for the output to react to a step change in the input signal.The output normally overshoots the target value, experiences damped oscillation, and settles to a final value.
Settling time, ts, is defined as the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Settling time is a design issue in data acquisition circuits when signals are changing very rapidly

For high speed, ADC must give high gain Op-Amp. Op-Amp having high end specification is only suitable for space requirement. Some of specification is listed below table.

Table 1: Opamp Specification

Sr. no	**Parameters**	**Required Value**
1.	Gain	$\geq 55dB$
2.	UGB	$\geq 400MHZ$
3.	Phase margin	$\geq 50°$
4.	Slew rate	$\geq 250volt/.sec$
5.	CMRR	$\geq 50db$
6.	PSRR	$\geq 45db$

In order to verify the Op-Amp stability with different variation such as temperature, supply; various parameter such as phase margin, Gain margin are defined. Various other parameters such as CMRR and PSRR are calculated. Listed specification value is decided based on the literature survey. Here various Op-Amp topologies are implemented to achieve this specification.

3.3 Telescopic Cascode Amplifier

Telescopic Op-Amp offer low power compare to other topology.Telescopic Op-Amp limits the swing at the output due to less offset.

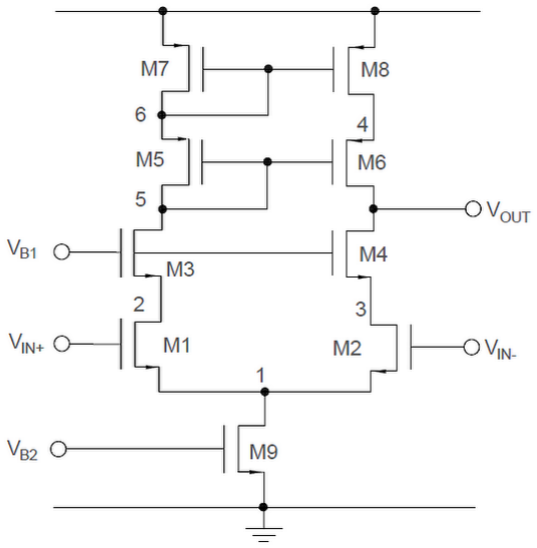

Figure 3.1: Telescopic Opamp

The voltage swing at the output of telescopic Op-Amp is limited by M9 transistor. Fig 3.1 shows the schematic of telescopic Op-Amp. It consists of differential input pair and current mirror load to generate the stable current at the load. This configuration allows high gain. It is not advantageous to increase number of load as it further degrade output voltage swing.

3.3.1 Waveform

Fig 3.2 shows the ac simulation result of telescopic Op-Amp. By this configuration, Gain achieved is high but the UGB is very less. Gain, 3 dB frequency and UGB is marked on the graph. The design is simulated using hspiceD simulator. Red plot shows the gain plot and the magnitude plot is shown with blue color.

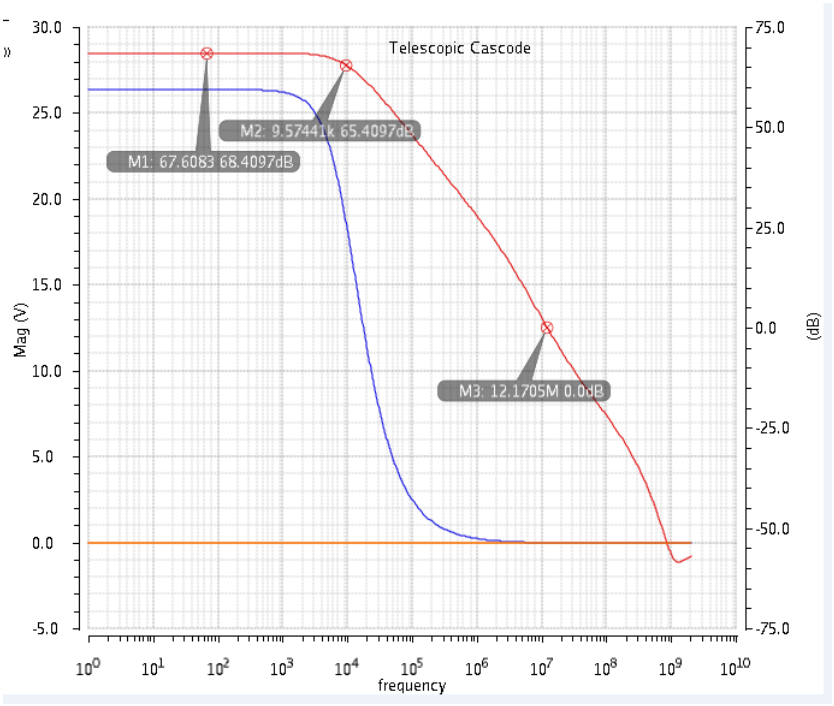

Figure 3.2: Simulation

3.3.2 Result

Gain plot is obtained by using 1pF load capacitance connected at the output terminal of an Op-amp. PSRR is calculated by connecting the output of an op-amp as feedback to the negative terminal and applying variation in the supply. CMRR is calculated by applying small signal at both the input of an Op-amp. In further section, detailed overview on other parameter calculation is shown. Table 2 shows the detailed parameter of telescopic Op-Amp.

Table 2: Specifications of Telescopic Opamp

Sr. no	Parameters	Value
1.	Gain	68.4 dB
2.	3 dB bandwidth	9.57 KHz
3.	UGB	12.17 MHZ
4.	Phase margin	51.8°
5.	Output Swing	1.72 V
6.	Slew rate	58.7 volt/Âţ.sec
7.	CMRR	53.3 db
8.	PSRR	45.7 db
9.	Offset Voltage	2mV

3.4 Two Stage Opamp

Op-amp can be two stage amplifier in which first stage is used to increase the gain while the second stage is used to increase the output voltage swing. While doing transfer function, two poles are nearer to each other which introduces instability in the design.

To eliminate this, miller compensation is used. Miller compensaton have the lowest offset as compared to other configuration for compensation and it never degrades the performance with respect to gain.

Fig 3.3 shows the schematic of two stage Op-Amp.

Here first stage can be differential stage but the second stage must be CS stage as it provides much higher swing. So each stage is a gain stage which typically gives single pole reponse. Sometimes the design may consist of a third stage which is buffer stage. This stage is not usually used for capacitive load. When Op-amp is used with negative feedback, compensation of Op-amp maintains stability. Biasing of 1.65V,2.4V is required. As the design is initiated with goal of fabrication of design, the design must be insensitive to parameter variation. So there is a need of stable source. Internal supply voltage should generate the bias.

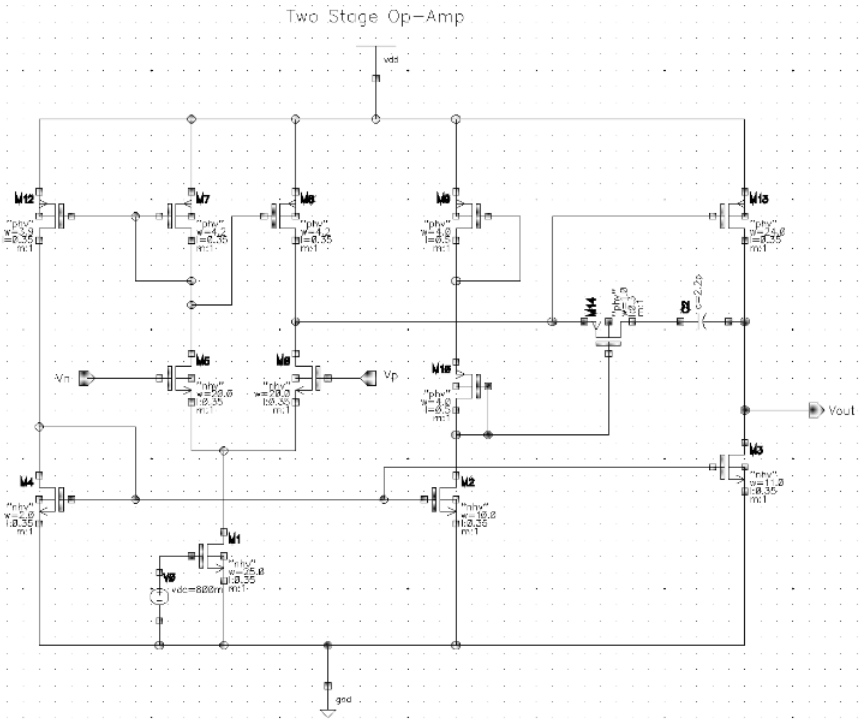

Figure 3.3: Implementation of Two Stage Opamp

3.4.1 Waveform

Fig 3.4 shows the AC simulation of gain boosted Op-Amp. The design is simulated using cadence virtuoso 6.1.5 and hspiceD simulator. The design is tested with 1 pF load at the output.

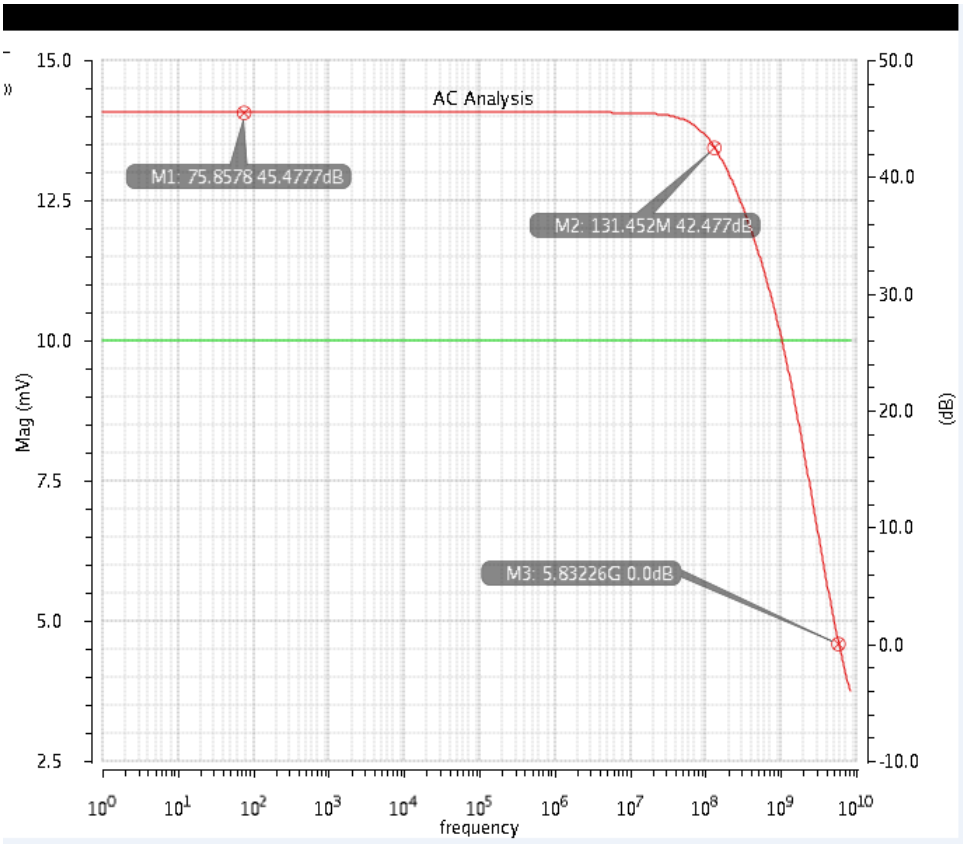

Figure 3.4: Simulation

3.4.2 Result

Two stage Op-Amp introduce high gain is 45.47 dB but that gain is not sufficient to support high speed ADC. Further the offset achieved is 3.4 mV which also limit the use of two stage Op-Amp. If Op-Amp is not perfectly compensated it affect the performance of the circuit. The CMRR achieved using this configuration is 64.26 dB and PSRR is 54.25 dB. Two stage Op-Amp have advantage with respect to UGB and phase margin. Table 3 shows the other achieved specification of two stage Op-Amp.

Table 3: Specifications of Two Stage Opamp

Sr. no	Parameters	Value
1.	Gain	34.17 dB
2.	3 dB bandwidth	138.5 MHz
3.	UGB	3.17 MHZ
4.	Phase margin	62.4°
5.	Output Swing	2.62 V
6.	Slew rate	335.8 $volt/musec$
7.	CMRR	61.26 db
8.	PSRR	54.25 db
9.	Offset Voltage	3.4 mV

3.4.3 Limitations of the Two-Stage Opamp

1. Insufficient gain
2. Poor power supply rejection ratio.

3.5 Folded Cascode Amplifier

Folded cascode Op-amp is a combination of two-stage Op-amp and gain boosting amplifier. It combines the advantages of this two. Folded cascade op amp have differential input pair that can drive through special current mirror sink. Fig 3.5 shows the schematic of Op-amp.

Folded cascode op-amp needs high end balance at the input of the differential amplifier. Here drain of the transistors are connected to each other to achieve common mode voltage input of differential amplifier. Here bias current I3,I4 and I5 are designed in such a way so that it never let the current in the mirror to go down to zero. When current in the sink is zero, it introduces delay additionally.It takes some time to turn on because of the parasitic capacitance.

The requirement of unity gain bandwidth for an Op-amp must be $>$ 500MHz for 8-bit ADC with 250 MSPS speed. Other parameter calculations are shown in section 3.6

Smaller saturation voltage, self biasing and lower power dissipation are the advantages of current mirror sink. Figure 3.5 shows the schematic diagram of Folded Cascode

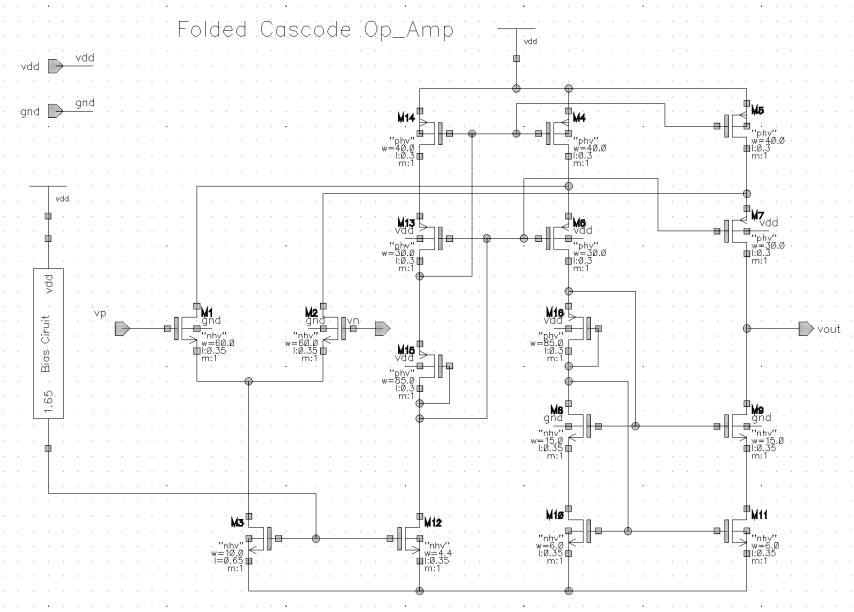

Figure 3.5: Schematic of Folded cascode opamp

Op-Amp drawn in Cadence Virtuoso 6.1.5. Here resistor is replaced by transistor during fabrication process. Figure 3.6 shows the schematic diagram of bias circuit.

3.5.1 Waveform

Fig 3.8 and 3.10 shows the ac simulation result of folded cascade Op-amp. Here resistor is replaced by the diode connected load. Gain can be increased by increasing the value of M1, M2 and M3. Larger value of R1 and R2 also increases the gain but limits the phase margin. In fig shown , various pointer marker on the graph indicates the gain, UGB.

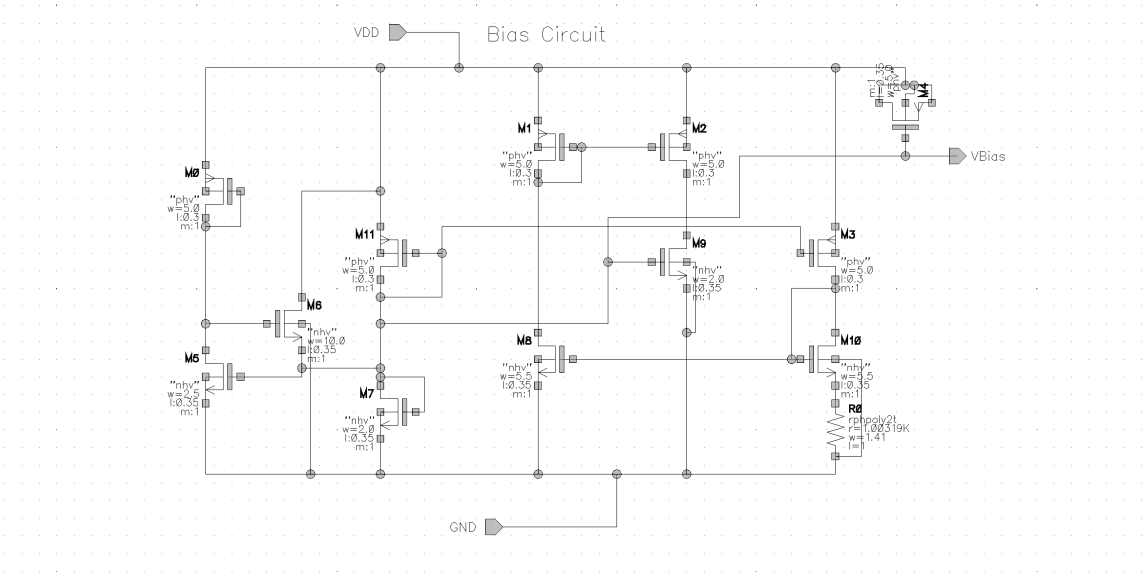

Figure 3.6: Schematic of Bias Circuit

3.5.2 Result

It should be noted that the gain of 57.87 dB is achieved using folded cascode with UGB of 633.04 MHz.Folded cascode gives the phase margin of 60° . All other parameter such as CMRR, PSRR, Slew rate are calculated by considering 1 pF load. Table shows the parameter calculated using cadence 180 nm CMOS technology.

Table 4: Specifications of Folded Cascode Opamp

Sr. no	**Parameters**	**Achieved Value**
1.	Gain	57.877 dB
2.	UGB	633 MHZ
4.	Phase margin	60°
6.	Slew rate	299.3 volt/μsec
7.	CMRR	76 db
8.	PSRR	54.27 db

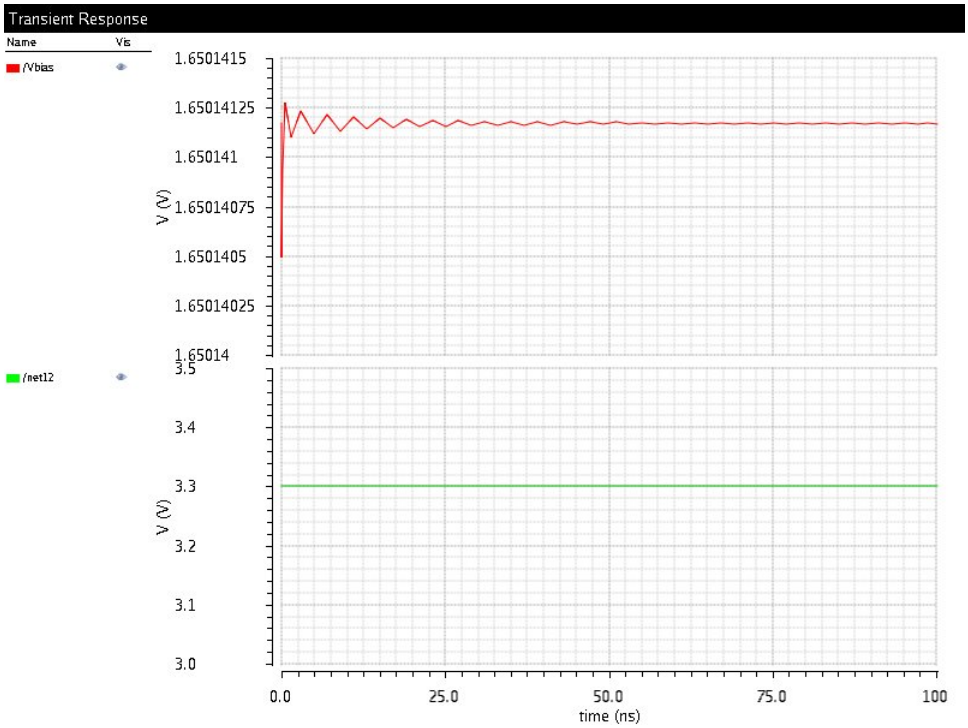

Figure 3.7: Pre-layout Simulation of Bias Circuit

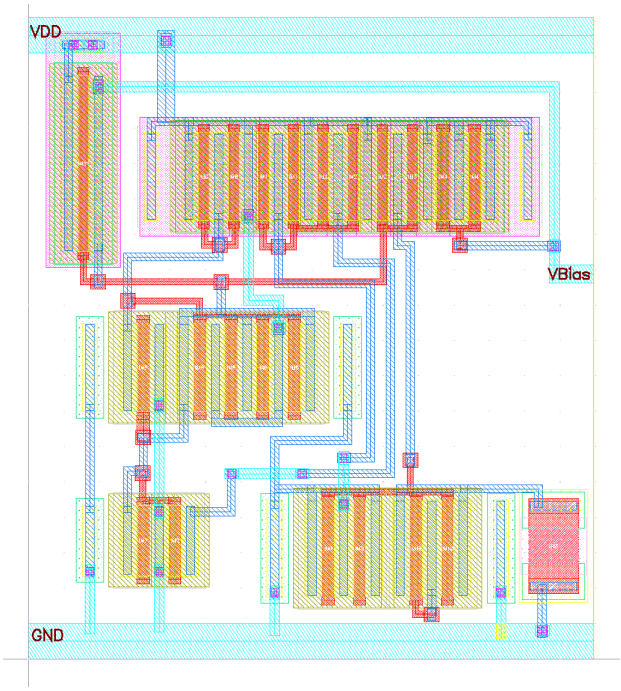

Figure 3.8: Layout of Bias Circuit

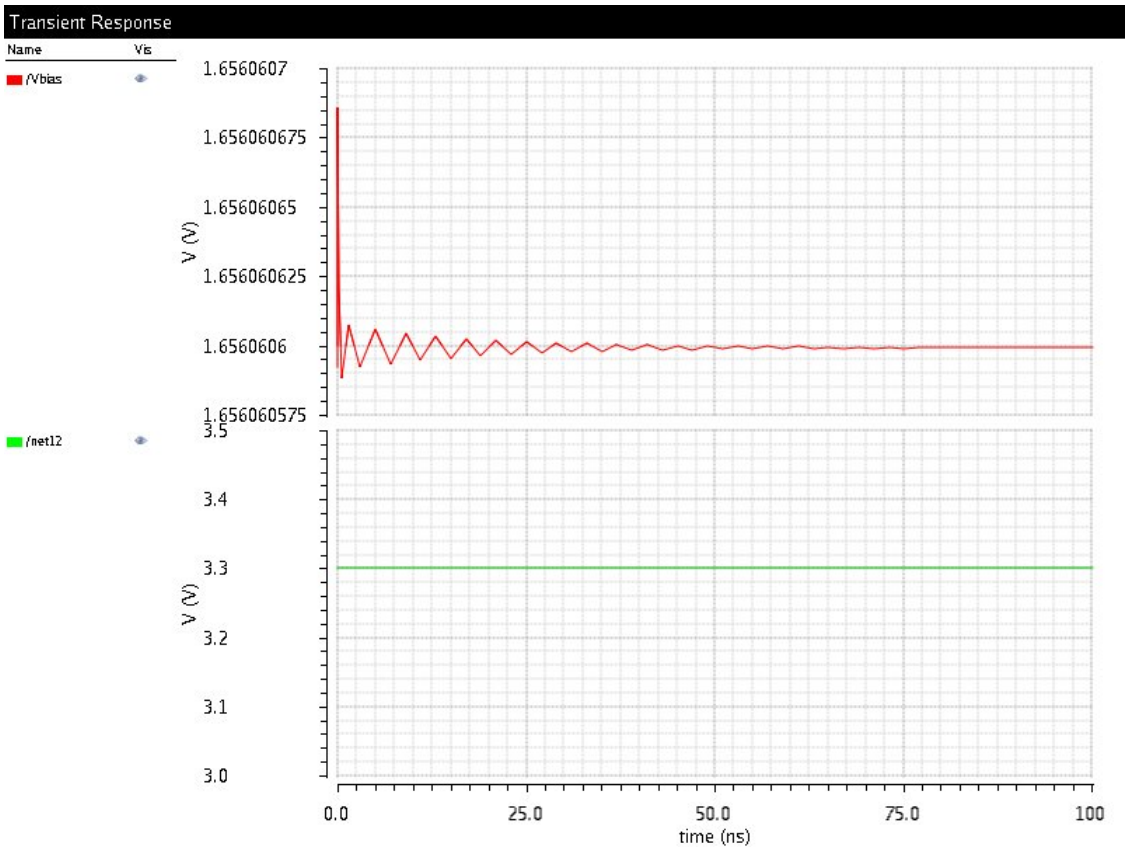

Figure 3.9: Post-layout Simulation of Bias Circuit

Figure 3.10: Pre-layout Simulation of opamp

3.6 Parameter Calculation of Opamp

The calculation step for some parameters are discussed. Here simulation result of folded cascade Op-amp is presented to give general idea of the response of various circuit analysis.

3.6.1 CMRR

Step 1: Open the schematic in schematic L window.

Step 2: Generate the symbol from the schematic.

Step 3: Now take a new schematic and once again extract symbol of Op-Amp. Give the input to the Op-amp as shown in the fig 3.11

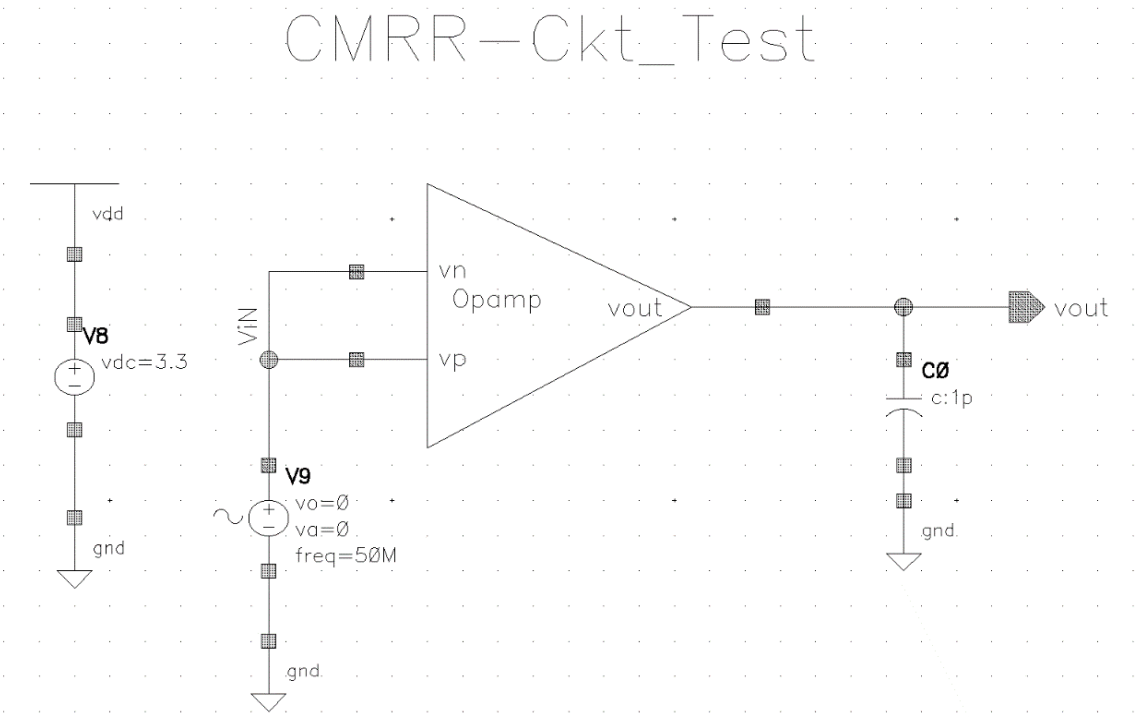

Figure 3.11: CMRR calculation test circuit

Step 4: Open ac simulation of an Op-Amp, give appropriate frequency range and run simulation

Step 5: Click on results then go to direct plot and select ac gain phase. Now first select common mode input voltage and after that select output voltage.

CMRR = db20 (vin/vout)

Step 6 : Now measure gain at particular frequency for CMRR

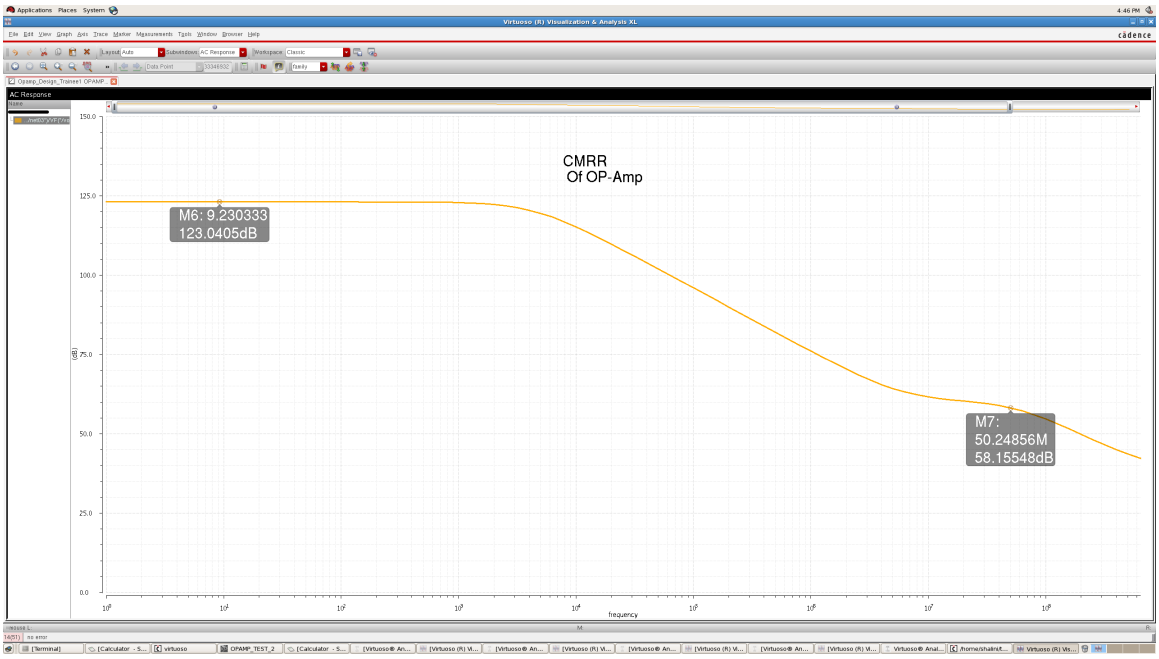

Figure 3.12: CMRR Plot

3.6.2 PSRR

Step 1: Open the schematic in schematic L window.

Step 2: Generate the symbol from the schematic

Step 3: Now take a new schematic and once again extract the symbol of Op-amp. Give the small variation in the supply voltage to the Op-Amp as shown in the fig 3.13.

Step 4 : Open ac simulation of an Op-Amp and give appropriate frequency range and run simulation.

Step 5 : Click on results then go to direct plot and select ac gain phase. Now first select the excess in power supply that is Vp and then select the output.

From results go to direct plot and select ac gain phase. Now first select the excess in power supply that is Vp and then select the output

PSRR = db20 (vp/vout)

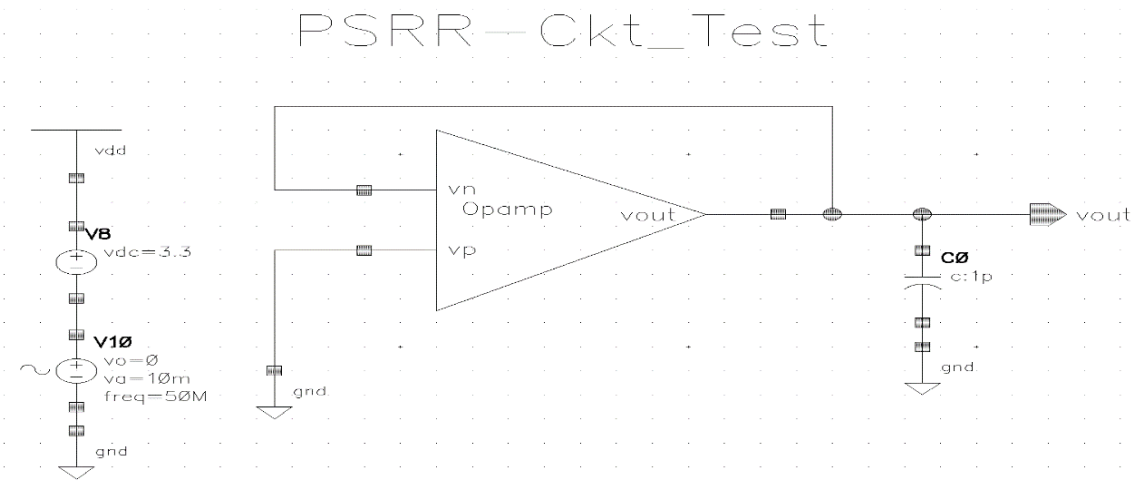

Figure 3.13: PSRR calculation test circuit

Step 6 : Now measure the gain at particular frequency for PSRR.

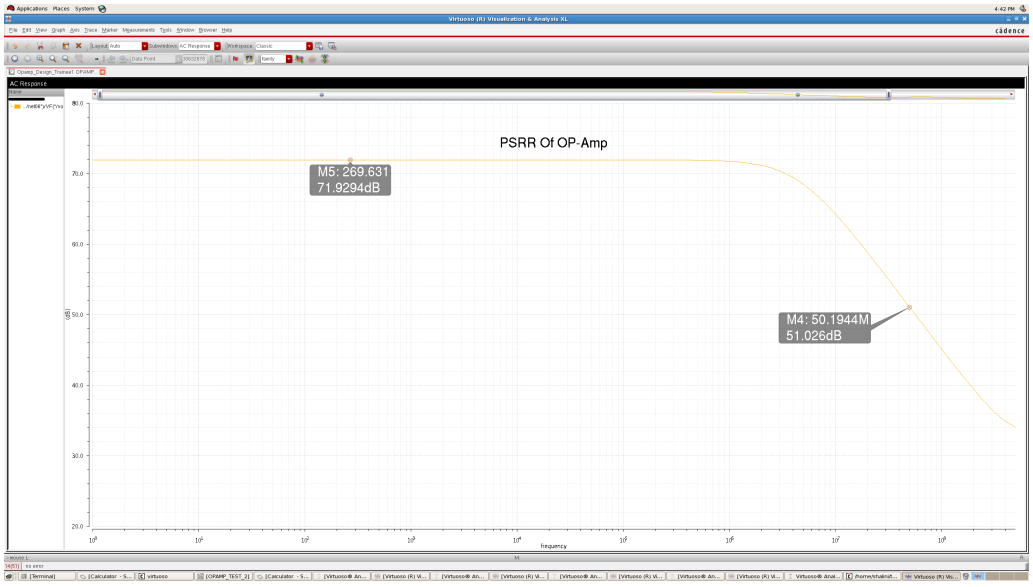

Figure 3.14: PSRR Plot

Fig 3.14 shows the AC response of folded cascode to measure PSRR

3.6.3 Slew Rate

Step 1 : Open the schematic in schematic L window.

Step 2 : Generate the symbol from the schematic.

Step 3 : Now take a new schematic and once again extract the symbol of Op-Amp.

Apply clock pulse to the Op-Amp and connect the Op-Amp unity gain configuration. Fig 3.15 shows the configuration Op-Amp for slew rate calculation.

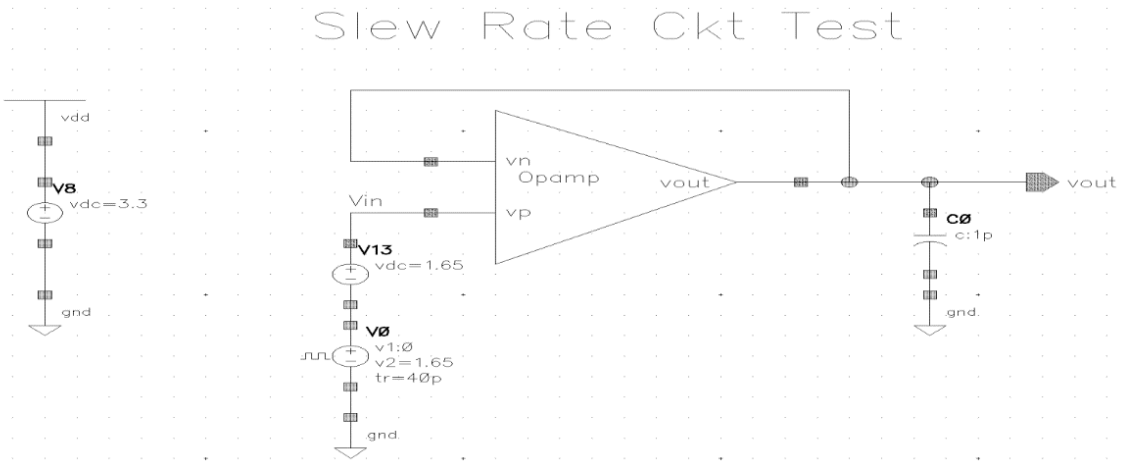

Figure 3.15: Slew Rate calculation test circuit

Step 4 : Open transient simulation of an Op-Amp give appropriate start and stop time and run simulation.

Step 5 : From calculator select special function. To calculate slew rate give below configuration. Here first three points are based on transition specification.

i. Select initial type value 0 n

ii. Give initial value and final value.

iii. Select the percentage from 10 to 90

iv. To conform calculation click on apply and ok.

v. And plot the result

Folded cascode Op-Amp having advantage compare to other configuration of Op-Amp in terms of gain, phase and unity gain bandwidth. Other parameter calculated such as PSRR, CMRR, slew rate are also meet targeted specification. Table 5 shows the comparison of achieved specification of other configuration with folded cascode Op-Amp.

For layout of folded cascode op-amp, some new techniques are learnt.

Table 5: Opamp Achieved Specifications

Parameter	Telescopic Opamp	Two Stage Opamp	Folded Cascode Opamp
Gain (dB)	68.4	34.17	57.877
UGB	12.17 MHz	3.17 GHz	633 MHz
Phase margin	51.8°	62.4°	60°
Slew rate (v/mus)	58.7	335.8	355.9
Settling time	3.4 ns	768 ps	750 ps
CMRR (dB)	53.3	61.26	76
PSRR (dB)	45.7	54.25	54.27

3.7 Layout for large transistors

Usually, the transistor size in analog circuits is much larger than in digital circuits. Long transistors should be split into smaller ones for various reasons. One reason is to fit them better into the overall layout of a block or simply to have a better aspect ratio. Another reason is to reduce the gate resistance of the device. In this the switching speed is reduced and in addition the drain area is reduced because two fingers share a common drain and therefore parasitics reduces as well.
Splitting of transistor is done such that length remains constant and the width of finger is W/k, where k is the total number of fingers. The effective length and width remains same, but the gates are now in parallel and therefore the resistance is reduced. In addition, gates are often connected at both ends to reduce the effective resistance. Splitting transistors can either be done by using multiple transistors with a single gate or with transistors that have multiple gate fingers

1) Fingers - Multiple finger technique also known as fingering has many advantages as compared to single finger transistor. It can enhance the transconductance for a single transistor because of the lower gate resistance. Transistor with multiple fingers have the disadvantage that the direction of current is different for two neighbouring fingers. For eg if for the first finger, the source is to the left then the source for the next finger will be to the right. Depending on the current direction, the properties

of transistor can change .Therefore to achieve good matching, extra care has to be taken.

2) Multiplicity - Multiple transistors with a single gate is multiplicity. It gives us as much transistor as the multiplicity indicates

Fingering reduces parasitic resistance and capacitance by reducing the overall drain/source area and perimeter. Quantitatively, when we finger a MOS device by more than 4-5, drain/source capacitance reduces by about half. It also reduces the threshold voltage by small amount in deep sub-micron technologies.

3.7.1 Matching

Accuracy and desired performance of analog circuits may be limited by process variations during fabrication. Process variations not only affect W/L ratio (aspect ratio) but also other variation like threshold voltage (Vt)etc. Matching between components in layout of analog circuits is an important issue in many designs for example current mirror, differential pairs. Mismatch in a simple differential amplifier will lead to undesirable effects like offset, poor CMRR etc. The most basic techniques to match components in layouts are interdigitization and common centroid technique.

Suppose we have two components A and B to be matched where A and B can be anything like capacitor, resistor or transistor. Now lets split A and B into 4 small components i.e A1-A4 and B1-B4. We can do matching using 2 ways -

a. Inter-digitization Technique - Components are placed alternately.
   A1 B1 A2 B2 A3 B3 A4 B4

b. Common Centroid Layout Technique - Components are placed such that they have same centroid.
   A1 B1 B2 A2 A3 B3 B4 A4
   Both A and B have common center

Even fingers are easy to match, easy to form good common centroid and interdigitization patterns than odd fingers. Multiplicity is useful when we want to split the

transistor to make some interdigitization or cross coupling matching technique. This structure provides a very symmetric and compact layout.

We can also make the common centroid layout automatically using MODGEN.

MODGEN stands for module generator.

Steps-

Steps for MODGEN are -

(1) Open the schematic in Schematic XL.

(2) Go to Windows → Assistant → Constraint Manager

(3) New window will appear on the right side (constraint manager) in which we can see various options like placement, routing, common centroid, IR drop etc

(4) Select the transistors (suppose M7, M8, M9 of 4 multipliers each) in which the common centroid or interdigitization is to be applied.

(5) Within the constraint manager window, from the 2nd drop down menu select Placement → Modgen

(6) The devices will light up and new modgen will appear on the constraint manager window (CMW)

(7) Now turn on the module generator.

(8) Edit the no of rows and no of columns (let it be 2 rows and 6 columns)

(9) From the 3rd drop down menu in the CMW, select module generator. This will bring up the layout in a new "module generator" window (MGW).

(10) Pattern setting

From within the MGW, click the pattern icon at the top

i. For routing using common centroid, click custom

ii. Notice the name mapping

A : M7 (4)

B : M8 (4)

C : M9 (4)

iii. Now set the pattern based on the mapped name :

A B C C B A

A B C C B A

If dummy is to be added, then we can set the above pattern as

* A B C C B A *

* A B C C B A *

Or

- A B C C B A -

- A B C C B A -

* and - is used to add dummy

iv. Click OK, we will see that the devices are now placed in 2 rows.

(11) Set the transistor spacing

i. Click the member alignment/spacing.

ii. Click on horizontal vertical and set both drop-downs to custom

iii. Now manually enter the spacing required. We can also use -ve numbers here to overlap devices

(12) It can be automatically routed using the route icon at the top. Here by clicking on structured routing we can edit the various options like the type of metal used for horizontal vertical routing, no of vias to be used etc.

(13) Exit the Modgen window by clicking the exit icon at the top left.

(14) Click the save button on the constraint manager window.

(15) Now Launch → Layout XL or GXL

Fig 3.16 shows the layout of opamp using common centroid method. Fig 3.17 shows the post-layout simulation of opamp.

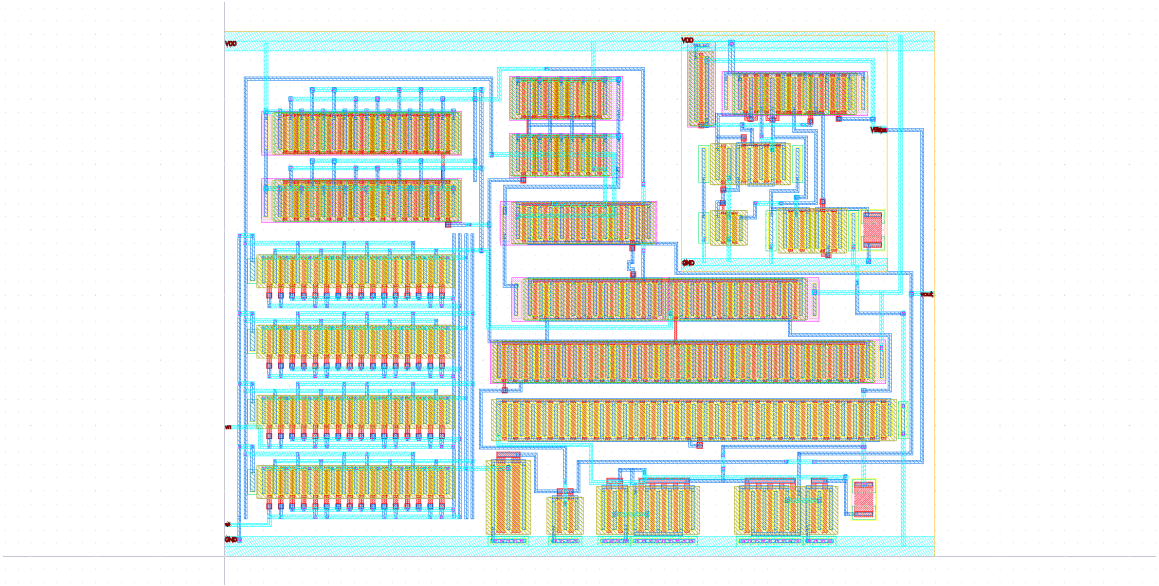

Figure 3.16: Layout of opamp

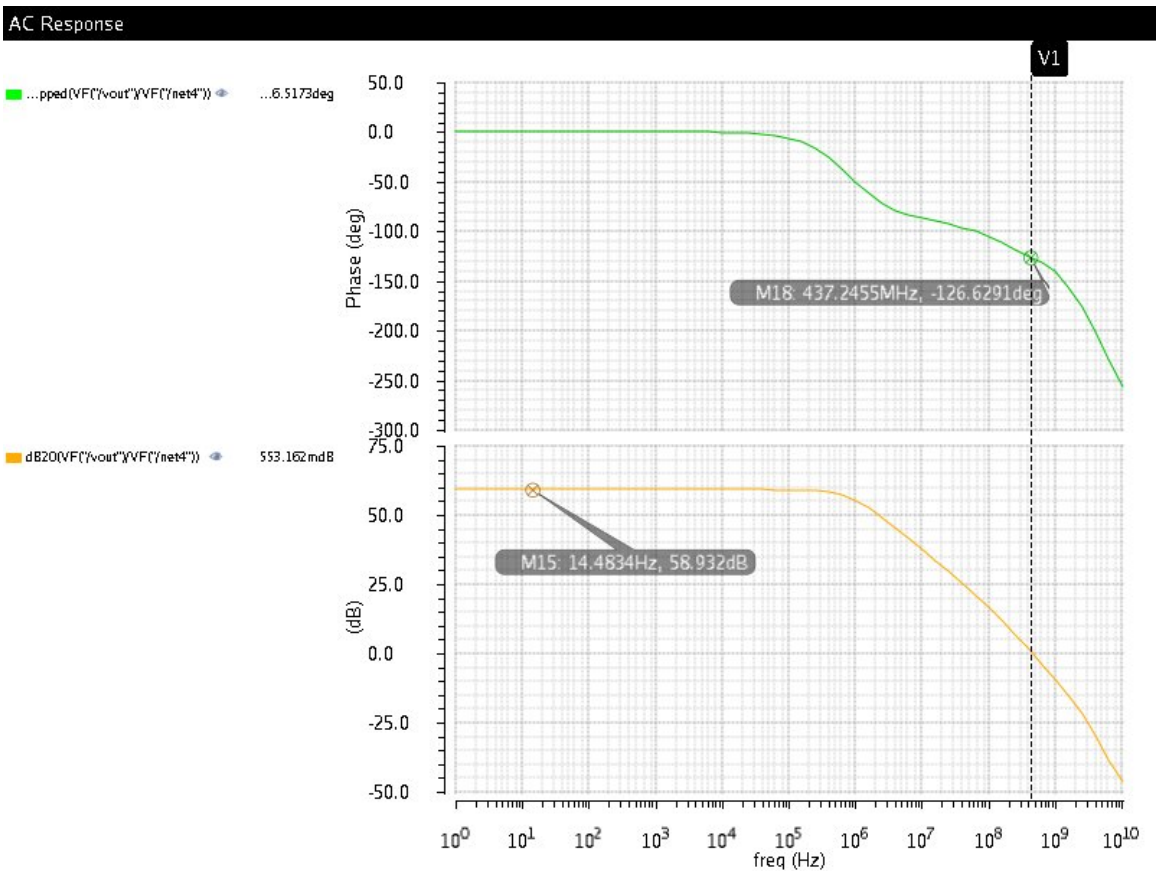

Figure 3.17: Post-layout Simulation of opamp

Chapter 4
Comparators

4.1 Introduction

The key analog building block of any flash ADC are comparators that strongly influence the performance. A high degree of comparator accuracy is essential for good ADC performance.

Comparators are the device that compares two analog voltages or currents and switches its output to indicate which one is greater. If Vp is at a greater potential than Vn, then the output Vo of the comparator is logic 1 and when Vp is at a potential less than Vn, output is at logic 0. If a pulse voltage is applied at Vp and a DC reference voltage at Vn, the output is logic 1 when the pulse amplitude is greater than the reference voltage.

Comparator is designed especially for open loop configuration without any feedback. It is the second most widely used device after op-amp in electronic circuits. Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, the input signal is first sampled then this sampled signal is applied to a number of comparators which determines the digital equivalent of the analog value. Comparators are also used in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators

The most important blocks in flash ADC is the comparator since it determines many of the performance metrics of the converter. Flash ADC architecture is parallel in structure. Therefore it requires 2N-1 comparators for an N bit ADC. The major source of power consumption in Flash ADC is the comparator array.

Nowadays demand for portable battery operated devices is increasing and a major importance is given towards low power methodologies for high speed applications. Also, the power consumption has to be minimized by using smaller feature size processes.

However when minimization of power consumption is taken into consideration, the process variations and other parameters will greatly affect the overall performance of the device. Now comparators are used in ADCs and ADCs require less power dissipation, high speed, less delay, less offset voltage, low noise, better slew rate, less hysteresis etc. Comparator must be tightly constrained to achieve these specifications.

But the comparator needs to be replaced with clocked comparator since the output must be synchronized with respect to the clock signal. The clocked comparator is implemented as shown in fig 4.1

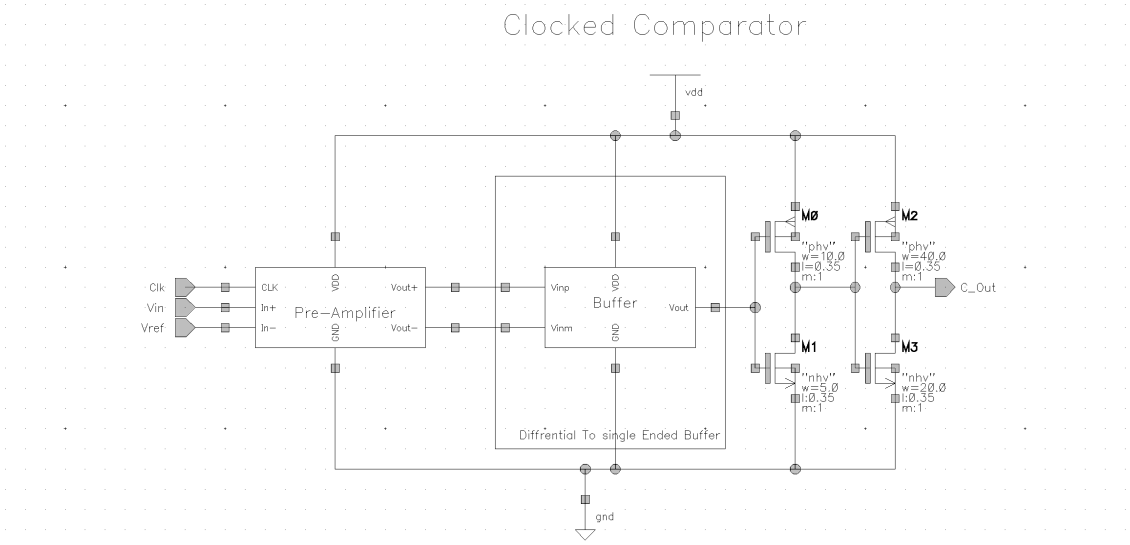

Figure 4.1: Clocked Comparator

Table 1 shows the specification of comparator for high speed requirement

Table 1: Comparator Specification Table

Sr. no	**Parameters**	**Value**	Achieved Value
1.	Input offset voltage	<5mv	2.45mV
2.	Propagation delay	<1.0 ns	539 ps
3.	Speed	>1 GHz	2 GHz
4.	Resolution	62.5mv	62.5mV
5.	Logic 1 voltage	>70 % of VDD	>70 % of VDD
6.	Logic 0 voltage	< 30 % of VDD	< 30 % of VDD
7.	Hysteresis	5 mV	4.88mV

The comparator consists of three stages -

1) Pre-amplifier

2) Dynamic latch

3) Buffer

It consists of a preamplifier with decision latch, D latch.The preamplifier stage consists of differential amplifier with active loads. The input signal is amplified by the preamplifier stage to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision. It isolates the input of the comparator from switching noise coming from the positive feedback stage. It can also reduce the input referred latch offset voltage. The sizes of mosfets are set by taking into consideration the differential amplifier transconductance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of mosfets.

Here gm1= gm2.

During active application of clock, D latch latches the data and raises the signal to sufficient level.

The positive feedback latch stage determines which of the input signals is larger and also amplifies their difference.

It also consists of an output buffer which improves the response of the comparator. The output buffer stage is consisting of a self-biased differential amplifier followed by an inverter. It gives the digital output and converts the output of the latch stage to

a full scale digital level output (logic 1 or logic 0). The output buffer stage should accept a differential input signal. It should not have slew-rate limitations

Two reference signals are used to compare the input signal. The bottom most transistor of buffer decides the current flow through the buffer.

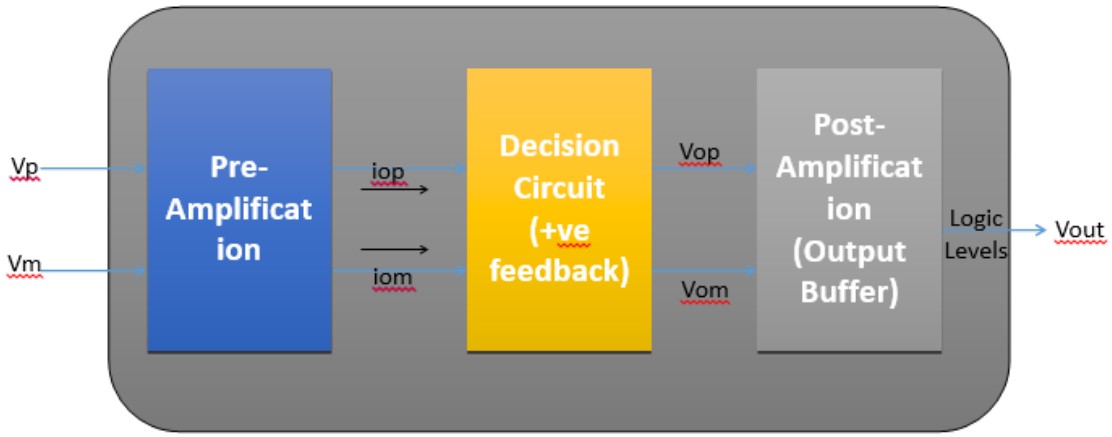

Figure 4.2: Design of Comparator module

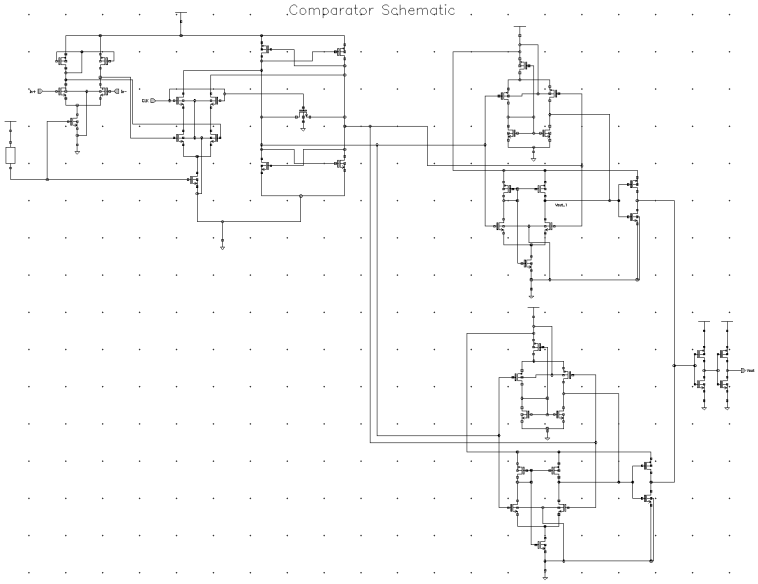

Figure 4.3: Schematic of Comparator

4.1.1 Preamplifier

A transistor level schematic diagram of the preamplifier is shown in Fig. The DC gain of the preamplifier depends mainly on the transistors M1,M2, M3 and M4. Transistors M1 and M2 act as current drivers and the gain increases with increase in gm of these two transistors. M3 and M4 act as loads and the gain increases with increase in on resistance of these transistors. M5 act as a current source and a bias voltage is given at the base of M5 to keep all the transistors in saturation region. The positive feedback given to M8 and M9 make those transistors act as regenerative latch to enhance the decision. Transistors M10 and M11 are used to reset the previous decision.

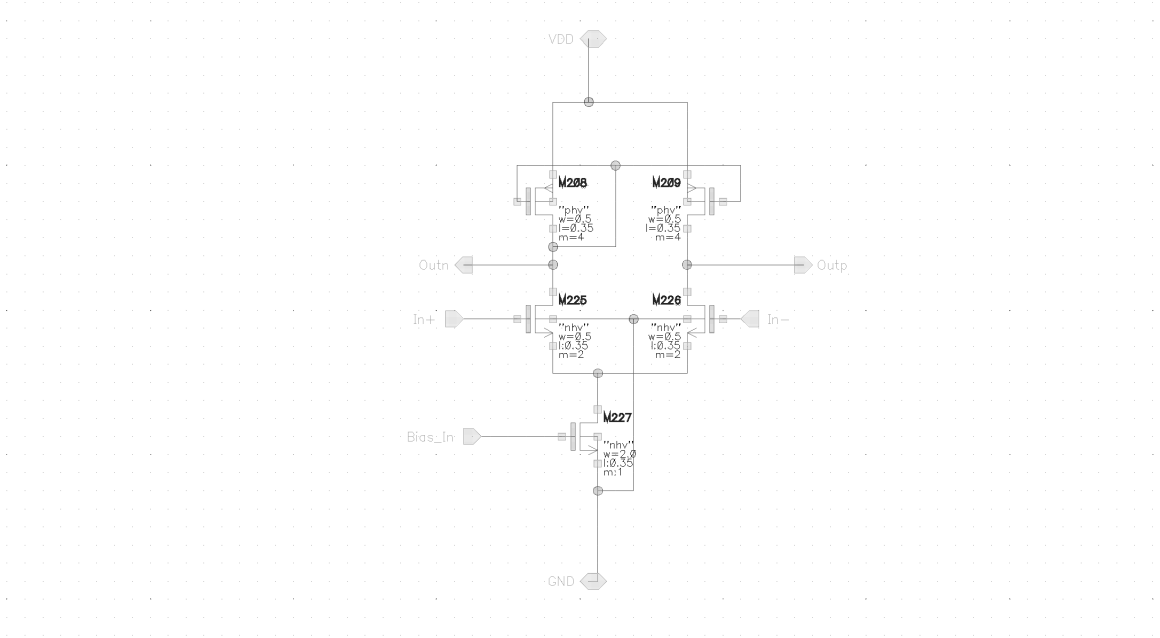

Figure 4.4: Amplifier Stage of Comparator

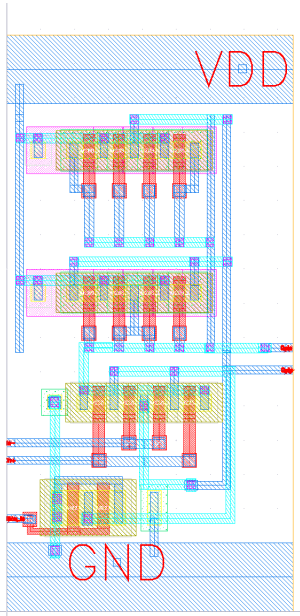

Figure 4.5: Layout of Pre-amplifier

4.1.2 D-Latch

For one complete clock cycle, D-Latch is used to maintain the output value. It will hold the present value of the latch output to that particular value till the next clock appears, so as to get perfect binary values at the output of the comparator.

4.1.3 Buffer Stage

The output bits are enhanced using output buffer by processing the output signals. Fig shows the schematic diagram of the buffer output used.

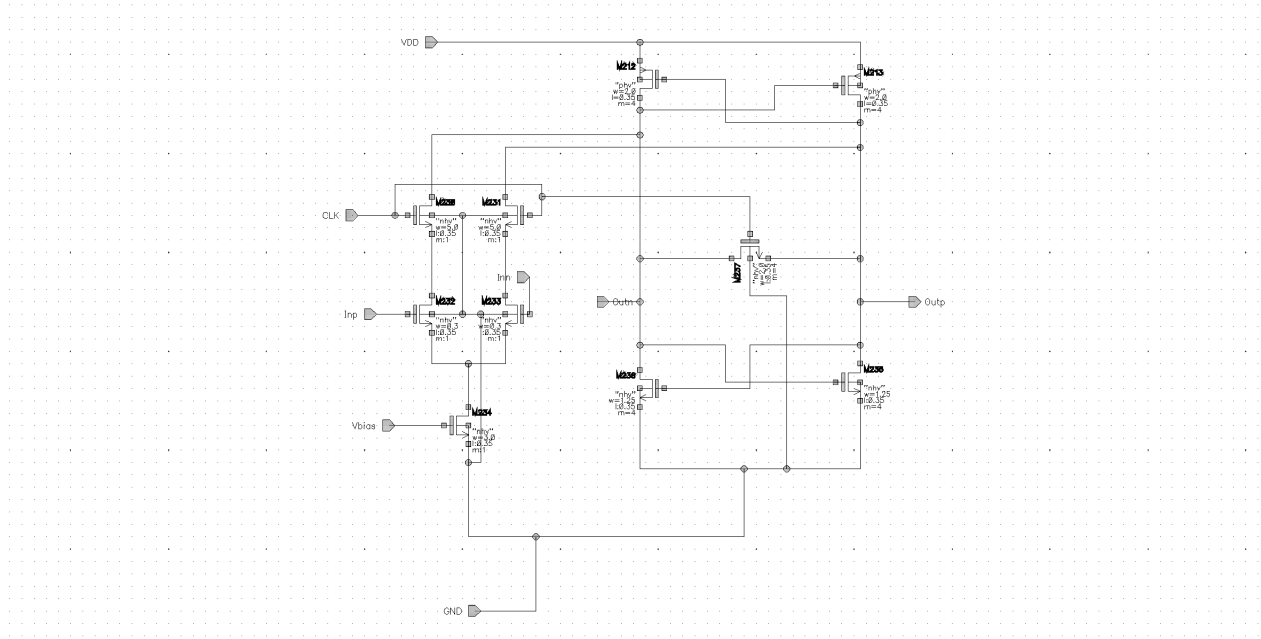

Figure 4.6: Clock Circuit

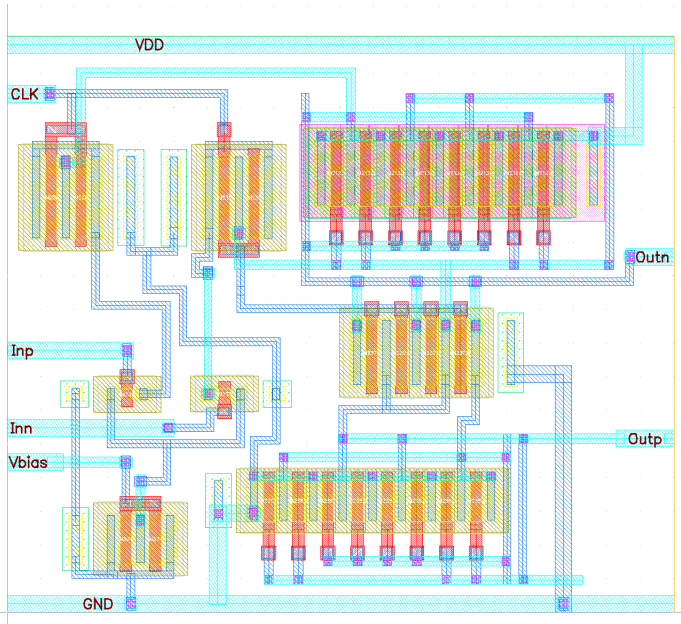

Figure 4.7: Layout of Clock Circuit

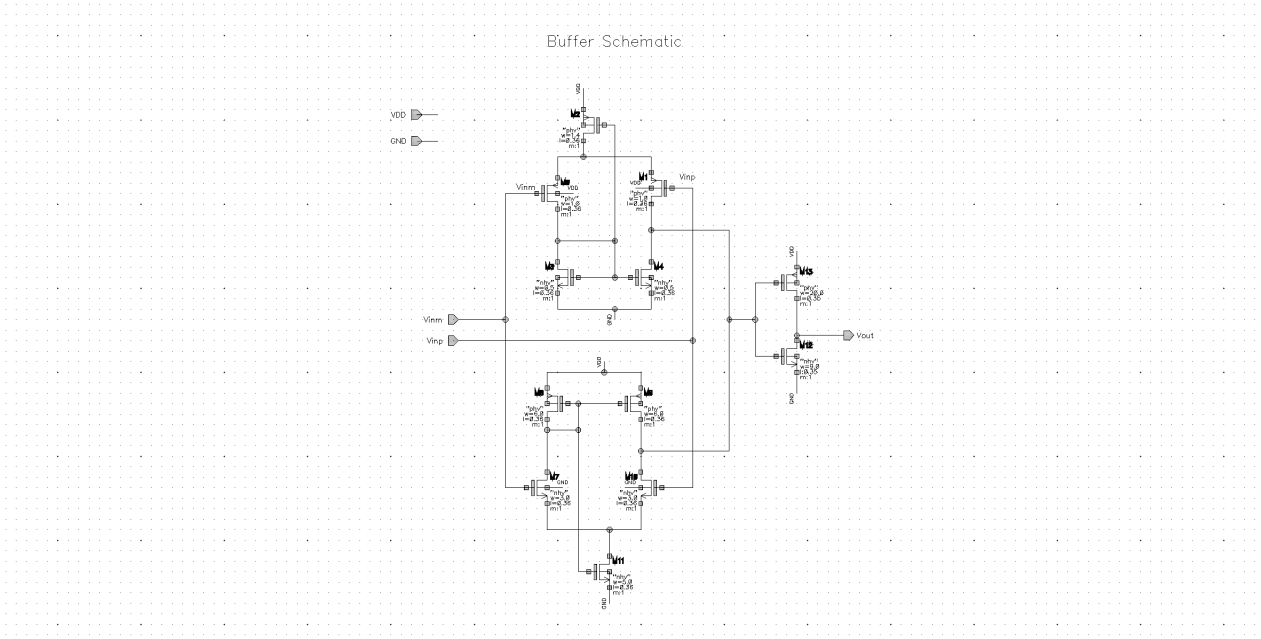

Figure 4.8: Buffer Stage of Comparator

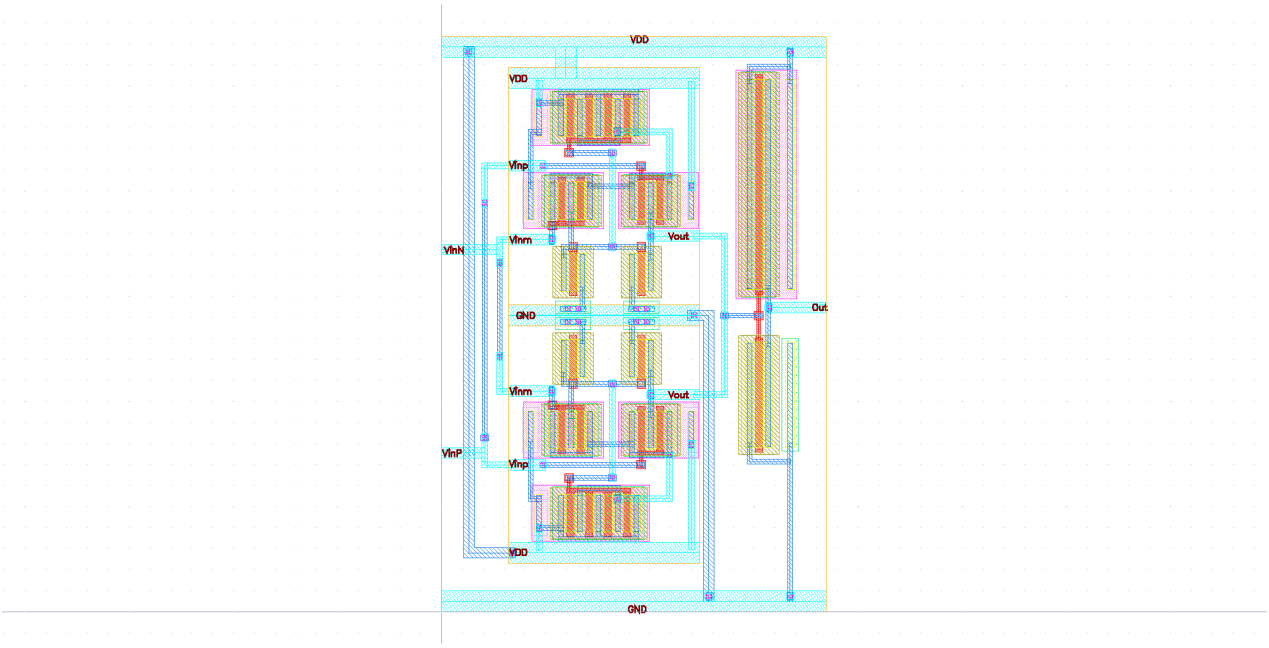

Figure 4.9: Layout of Buffer

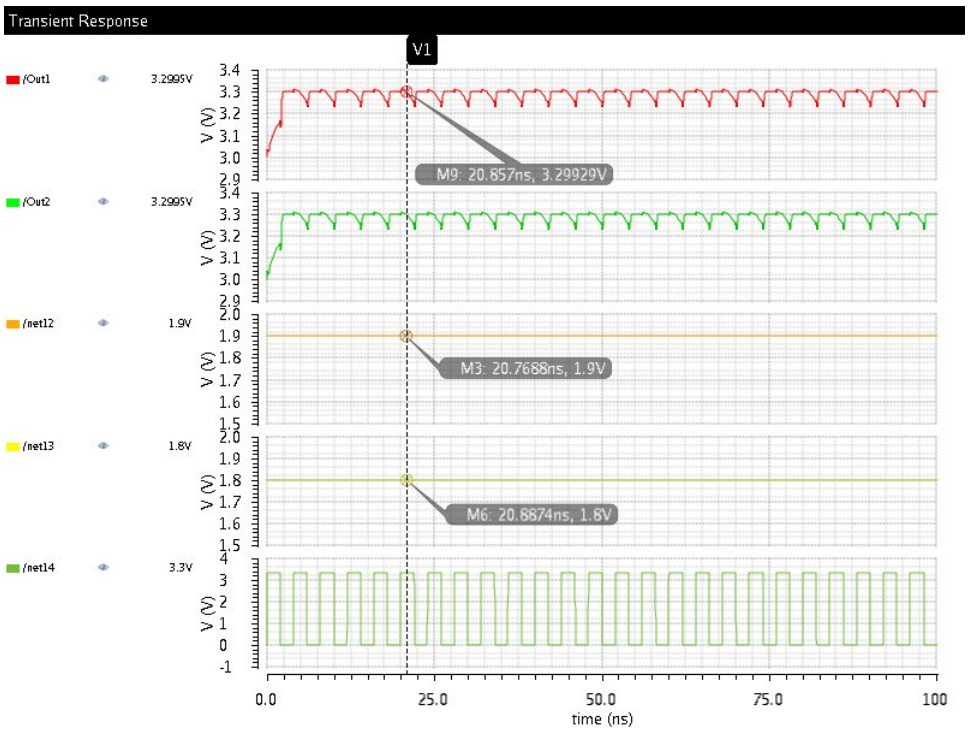

Figure 4.10: Pre-layout Simulation of Comparator

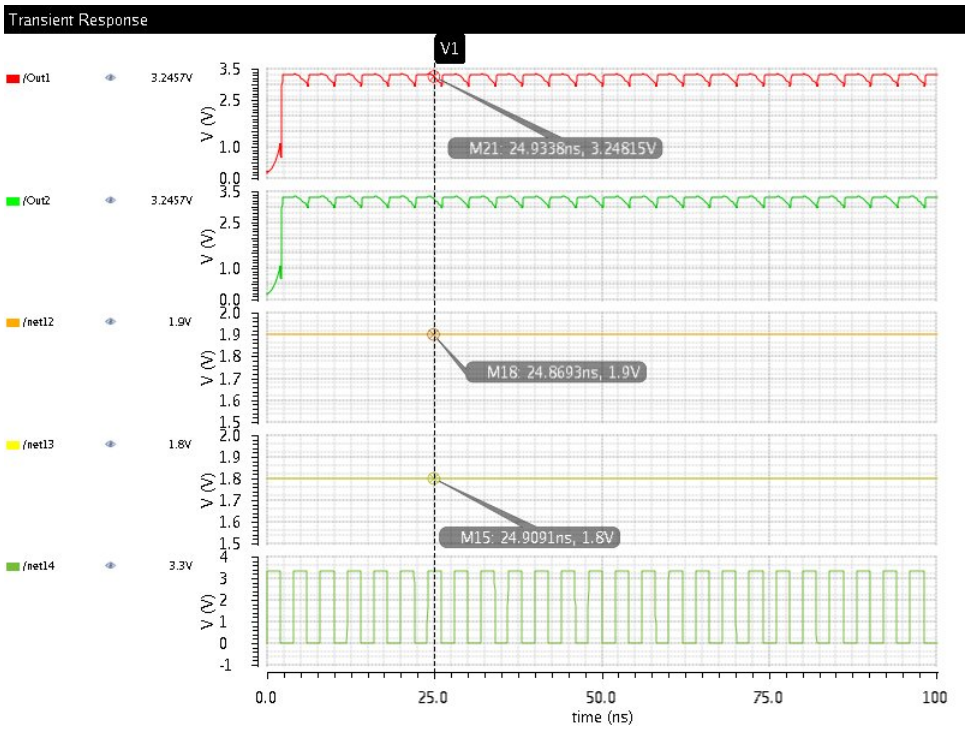

Figure 4.11: Post-layout Simulation of Comparator

Chapter 5
Sample and Hold Circuit

5.1 Introduction

Analog to digital conversion needs high speed sampling switch with less offset voltage. Sampling switch is used to connect and disconnect the part of the circuit during opposite instant of clock.

Fig shows the implementation of sample and hold switch. Transmission gate is used

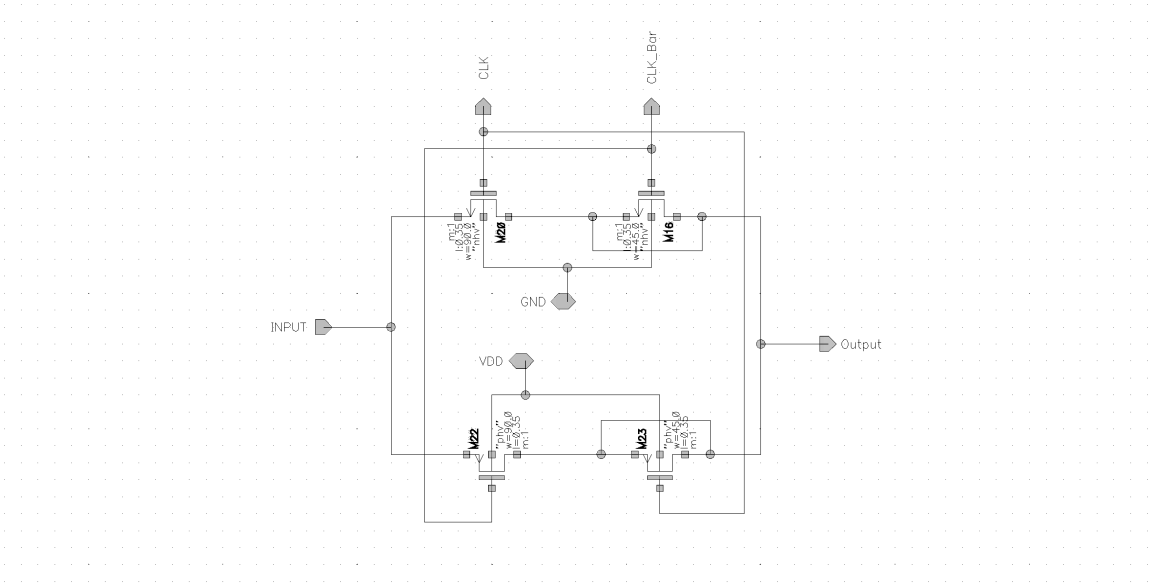

Figure 5.1: Schematic of Switch

to design the switch. Clock feed through and charge injection affects the accuracy of sample and hold circuit. Charge injection problem is caused by the leakage in the transistor during sampling instant. The measured value during hold instant is suffered from large settling time. This leads to a large delay in the comparator. Sometimes clock gets directly connected to the output due to the direct path between clock and output if switch is on. Therefore dummy transistor is introduced at each switch with opposite clock to eliminate these effects. Size of dummy transistor is half of sampling

switch with complementary clock.

Here upper switch S3 turns off first compared to S1. This will store value across capacitor which is equal to input level. This type of arrangement can eliminate the feed through and charge sharing problems. When sampling switch is turned off, charge stored inside it does not become zero within zero time. The hold phase is controlled by switch S2 and a capacitor. Op-amp is driven by switch S2 through capacitor.

The ratio of charges leaving from each side is not exactly half, but a complex function of several parameters such as the switching time or the impedance seen at each terminal of the transistor to ground. Some charges will be injected onto the sampling capacitance resulting in a voltage error. Thus, charge injection is an issue for accurately sampling the input value: a signal dependent voltage error is introduced when doing the sampling, limiting therefore total accuracy of the ADC. Dummy transistors can be added at the output of the circuit to cancel or reduce the effect of charge injection.

As the input switch and the upper feedback switch is on, the data is latched from the input during the instant of clock and the data is directly latched from input to the output. Folded cascade is used as Op-amp. Bias voltage is provided to the negative terminal of Op-amp through the switch. This instant is called as sampling instant. At the same instant, the capacitor is charged with last input voltage. The input value is taken from the charged capacitor after the application of clock. During this, the input gets disconnected from the circuit. Op-amp works in feedback fashion in this hold instant.

Table shows the achieved specification against required specification.

Table 1: Specifications of Sample and Hold Circuit

Sr. no	**Parameters**	**Spec**	Value
1.	Hold step (sample to hold offset)	31.25 mV	20.6 mV
2.	Droop rate	7.82mV/ns	3.2 mV/ns
3.	Acquisition time	2.0 ns	505 ps
4.	Slew rate	250V/Âţs	250V/Âţs
5.	Offset voltage	31.25mV	20.6 mV

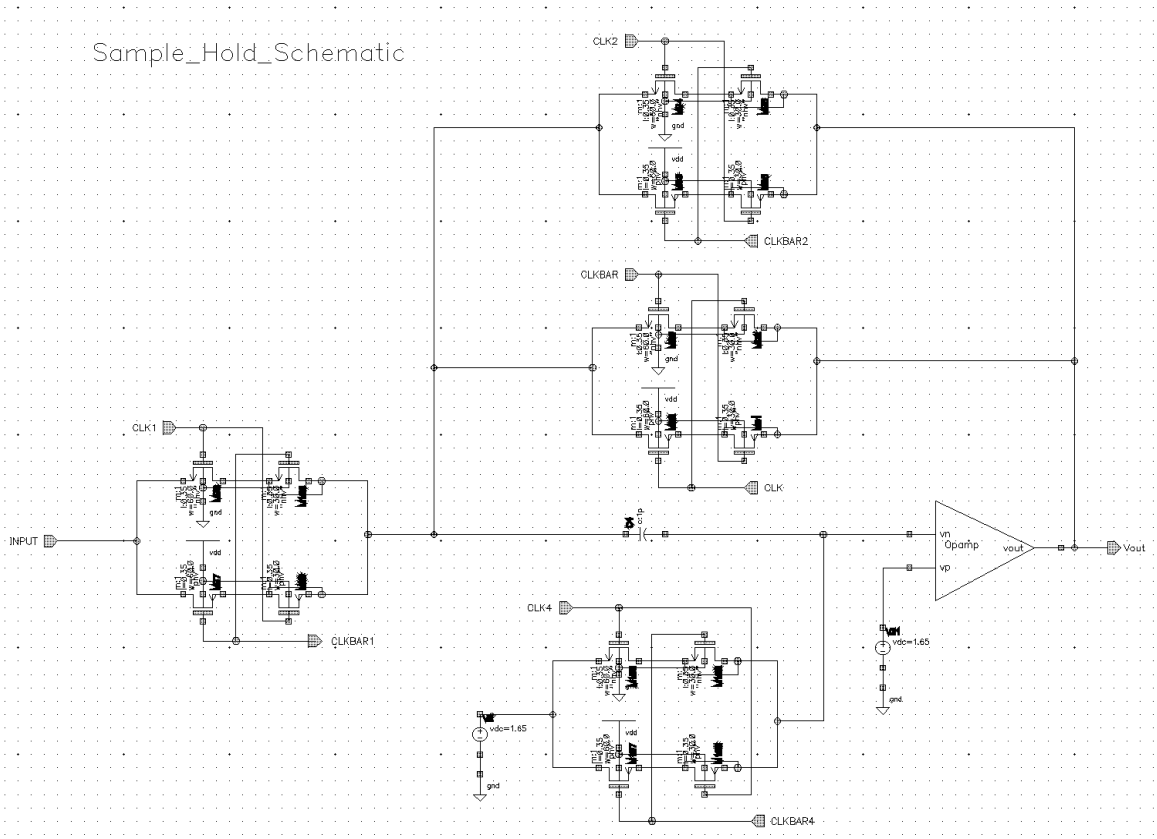

Figure 5.2: Schematic of Sample and Hold Circuit

5.2 Pre-layout Simulation

Fig shows the simulation of switch used.

The sample and hold simulation is carried out using various set of frequency. Fig shows the sample and hold response at 10Mhz and 50Mhz respectively. The simulation is done using spectre.

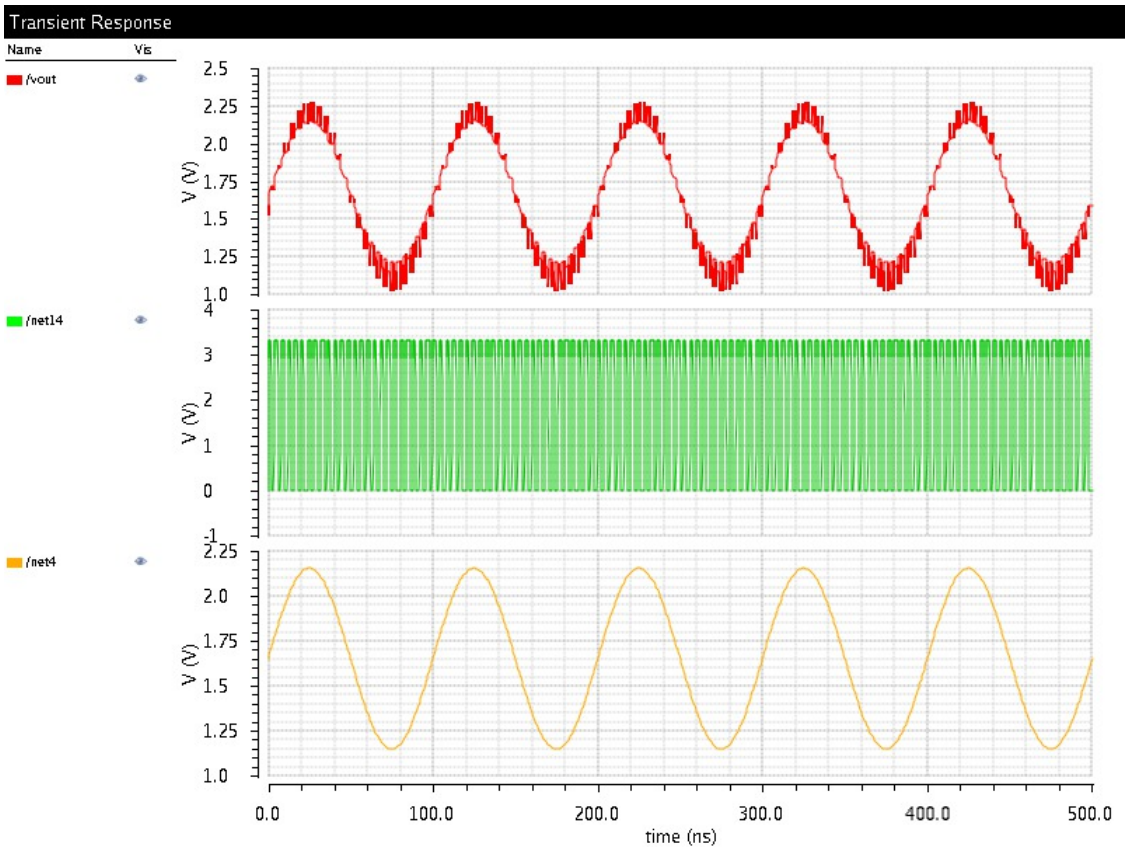

Figure 5.3: Simulation of Switch

Figure 5.4: Sample and hold output at 20 MHz Input frequency

5.3 Layout

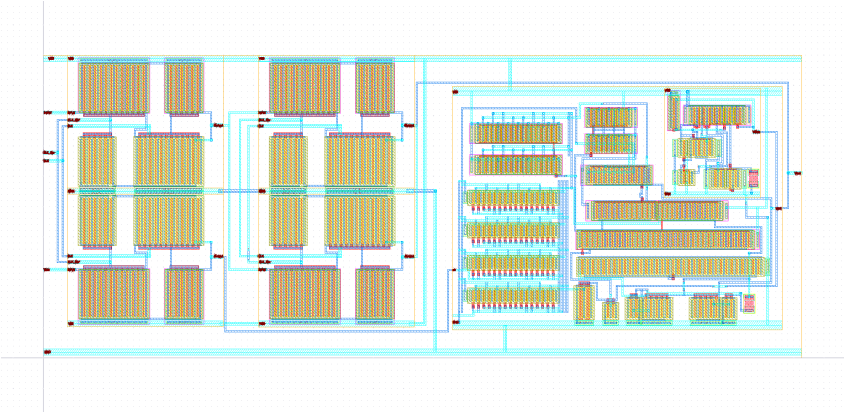

Figure 5.5: Layout of Sample and hold circuit

5.4 Post-layout Simulation

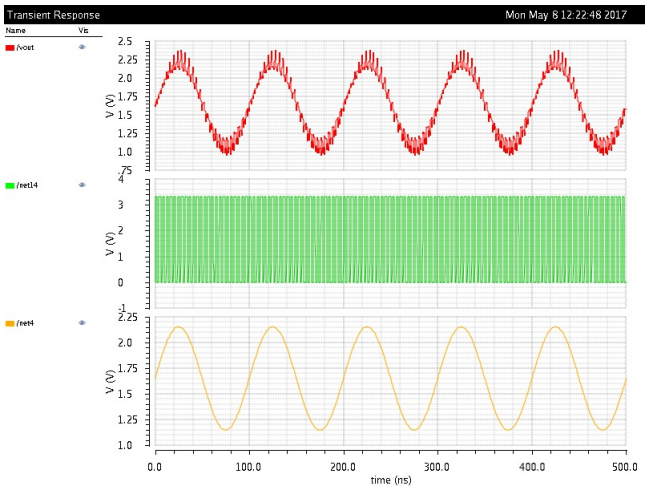

Figure 5.6: Post-layout Simulation of Switch

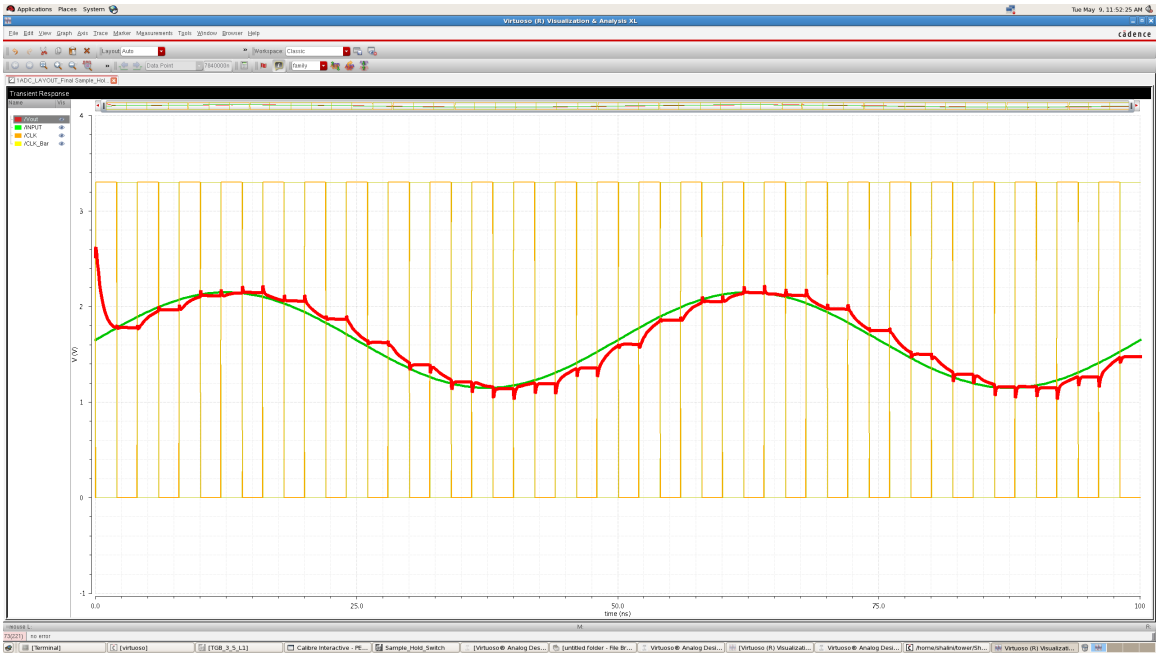

Figure 5.7: Sample and hold output at 20 MHz Input frequency

Chapter 6
4-bit ADC

4-bit ADC mainly comprises of Sample and hold circuit,Flash ADC and Encoder.The output of ADC is obtained by integrating all the modules.Fig 6.1 shows the schematic of 4-bit ADC.

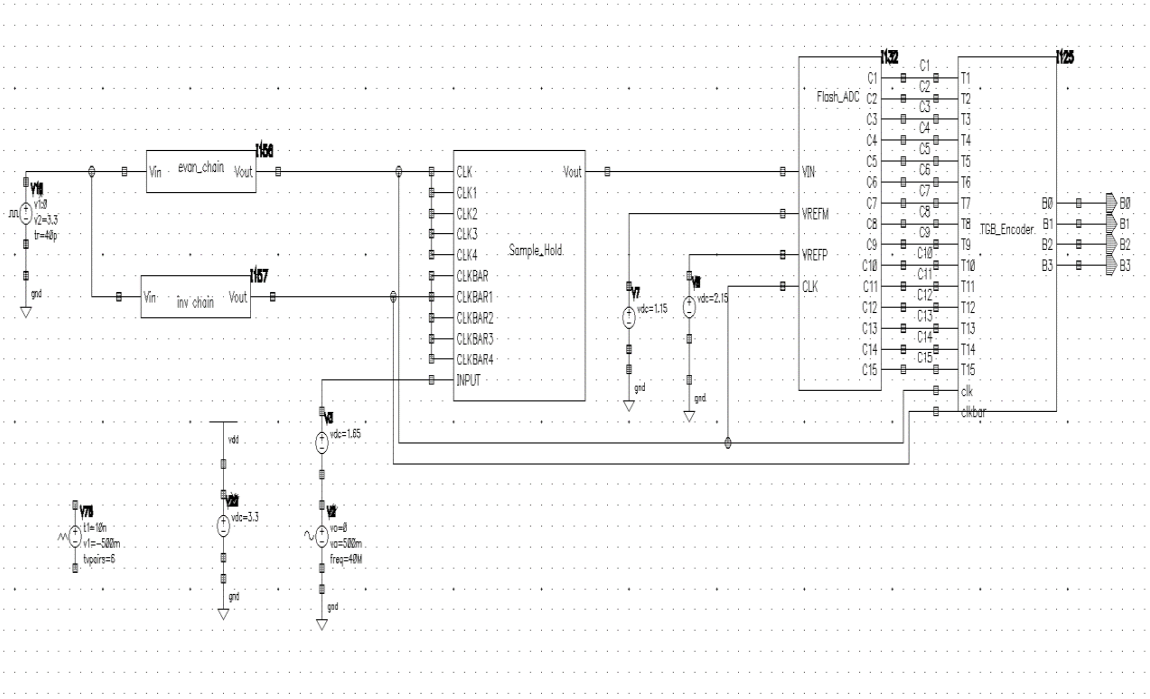

Figure 6.1: Schematic of 4-bit ADC

6.1 Flash ADC Design

Among all the ADC architectures available, Flash ADC is known for its fastest speed of operation and hence it is used in many practical applications. The very high Sample Rate, large bandwidth and the High speed of the ADC enables very high frequency applications range such as optical communication links, high density disk drives, radar processing, digital oscilloscopes and so on. Because of its parallel architecture, Flash

ADC is also called as parallel ADC.

Flash ADC requires one resistor and one capacitor per bit. In flash ADC, the voltage step is generated by the resistor and the resistor divides the whole range in 64 mV resolution for 4-bit ADC. Here 2.15V and 1.15V is the reference voltage applied to the flash ADC. The main reason for using this reference voltage is that the input is having 1.65 bias voltage and 500 mV input range added to it. We are able to verify full scale output by using this type of arrangement. Fig 6.2 shows the schematic of Flash ADC

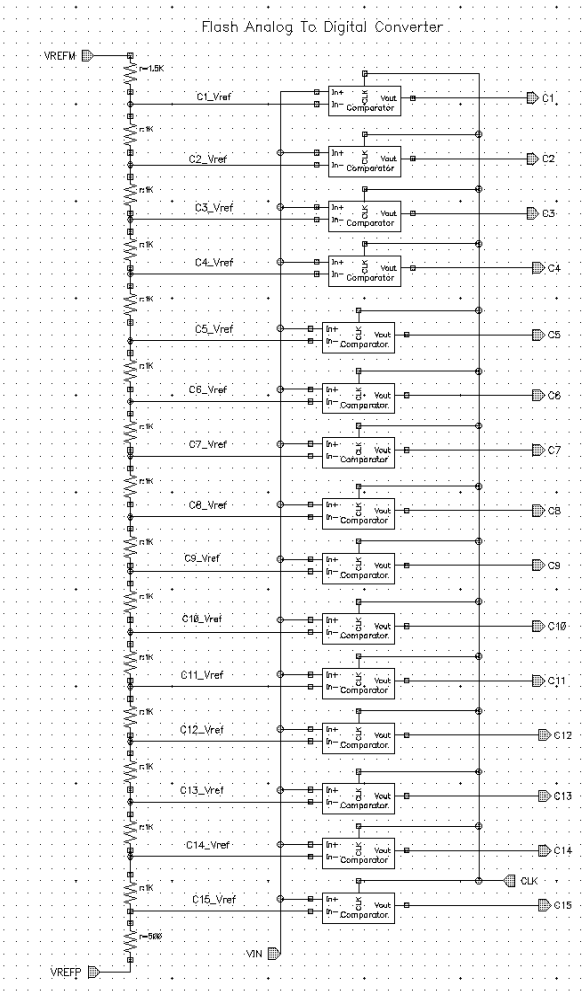

Figure 6.2: Flash ADC schematic

6.2 4-bit ADC Design

In Flash ADC, 2^n-1 comparators are used. Input voltage from the sample and hold circuit is used as a positive reference voltage. Here the comparator designed is synchronizing with clock and data is latched during active instant of clock. Sample and hold output is in hold mode during this time.

Resolution of ADC is decided based on the number of bits and the input range applied to ADC. 4-bit ADC consists of 15 comparators so the whole range is divided into 16 parts. So the resolution of ADC is,

$$Resolution = \frac{1}{16} = 64mV \tag{6.1}$$

Input offset voltage of Comparator is decided by applying reference input to one terminal of the comparator and by varying the input voltage at another terminal. Then check the difference between the two terminals. The input offset voltage is given by the change in output from high to low. Input offset voltage should be as minimum as possible.

As the number of bits increases, area required by flash ADC is increased numerously. Here the design is implemented with goal of 8-bit ADC so the area is not a prime concern. As compared to other type of ADC, Flash ADC is having high speed and better resolution. The simulation result of 4-bit ADC using spectre simulator is shown in fig 6.3 and 6.4

The output generated is not in the form of binary. The need of TGB encoder arises to convert thermometer code to binary code. Here the input clock is having time period of 4ns. So flash ADC will generate output after every 4ns and the total time taken by it to generate full scale output is 64ns. In comparator, latch stage decides that the signal is in the range or not. If signal is in the range, comparator generates logic high output. During hold phase, the value of comparator output has not changed as the comparator is synchronized with the clock. Fig 6.4 shows the simulation result with sinusoidal input signal.

Figure 6.3: ADC simulation result with ramp input

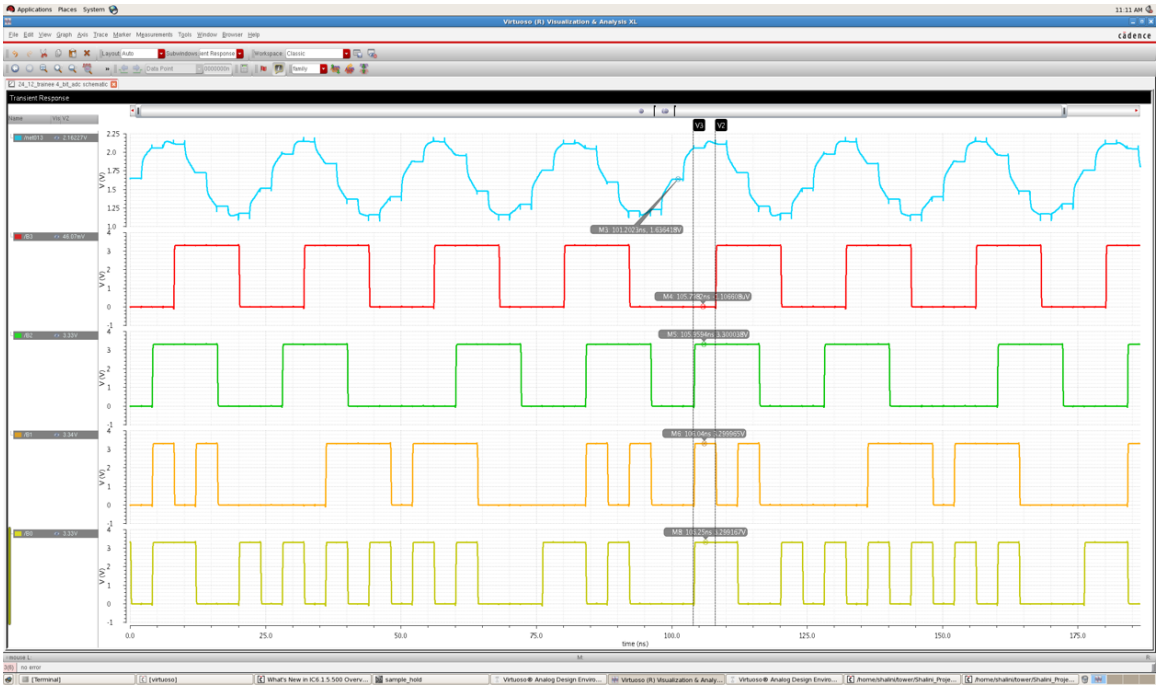

Figure 6.4: ADC simulation result with sinusoidal input

Chapter 7
Conclusion and Future Scope

7.1 Conclusion

The front-end and back-end design of 4-bit ADC has been completed.We have achieved the desired specifications.

7.2 Future Scope

This 4-bit ADC will be used in the design of complete 250MSPS 8-bit ADC. The 8-bit ADC will be used in various future microwave as well as optical payloads. This design will be completed at the SCL foundry which will be in accordance with the PM's "Make in India" initiative.

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