Design and Modelling of an on Chip Inductor

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology
in
Electronics & Communication Engineering

(Communication Engineering)

By

Anal Patel

16MECC07

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Declaration

This is to certify that

1. The thesis comprises my original work towards the degree of Master of Technology in Communication Engineering at Nirma University and Intel Technology India Pvt.Ltd and has not been submitted elsewhere for a degree.

2. Due acknowledgment has been made in the text to all other material used.

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Internal Certificate

This is to certify that the Major Project entitled **"Design and Modelling of an On chip Inductor"** submitted by **Anal Patel (16MECC07)** , towards the partial fulfillment of the requirements for the degree of Masters of Technology in Communication Engineering, Nirma University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Abstract

Passive components play very important role in the microchips for radio frequency applications. Particularly Inductors which are used in the most common circuits in RF ICs like low-noise amplifiers and oscillators. For lower frequency, we can connect an inductor externally. But at higher frequency even a single wire will have some value of inductance, resistance and capacitance so external inductor won't have the same value of inductance practically. Because as frequency increases the parasitic capacitance, parasitic resistance and all other high frequency effects will come into picture. Hence the idea of integrated inductors took place.

To design an integrated inductor for RF application is a very critical task because there will always be a trade-off among inductance, quality factor or resonant frequency. The optimization of geometric parameters can improve its performance. In this work a lumped physical model is explained which represents the characteristics of an on-chip inductor at higher frequencies. The figure of merits of integrated inductors such as quality factor, self resonant frequency, etc. depend on the layout parameters. There will always be a tradeoff between the performance of a spiral inductor and its layout parameters. In this study the layout parameters are chanegd and the effect of those changes over figure of merits are observed and discussed.

May 18, 2018

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Chapter 1

Introduction

1.1 Objective

The objective of this report is to study the various types of on chip inductors and to design and model one of the inductor for a specific RF application.

1.2 Motivation

1.2.1 Need of on chip Inductors

On-chip passive components hold the most importance in RF (radio frequency) electronics. These passive components like inductors, capacitors, varactors, and resistors, can be realized using MOS (Metal Oxide Semiconductor) technology. The performance of the circuit mainly depends on the performance of these passive components. Hence it requires high quality factor at higher frequency which needs special consideration.

The most common circuits in any chip are oscillator and other tuned circuits in which inductor in particular plays an important role. At low frequencies, these components can be connected externally. But at higher frequency each of these components will be a combination of parasitic L, R and C due to high frequency effects like skin effect, eddy current loss, and parasitic effects, etc.

For an example, tank inductance on the order of several μH is required for a VCO (Voltage Controlled Oscilator) having oscillation frequency of 10 MHz. But at higher frequency like at 10 GHz the tank inductance required is around 1 nH. To have this value externally is impossible because due to high frequency effects, the inductance associated with the package pin and bond wire can exceed 1 nH. As a result, on-chip passive components are commonly used in RF applications.

1.3 Basic structure of on chip Inductors

There are basically two types of structures: planar and multilayer inductors. But in order to construct on chip inductors, Multilevel Metallization needs to be done.

1.3.1 Multilevel Metallization

The process of interconnecting the components of the ICs by conductor layer is known as multilevel metallization. And that conductor layer will be the thin film metal layer which is produced by the multilevel metallization.

In simple words it can be described as a sandwich structure having an oxide layer between two metal layers and these metal layers will be connected with metal vias (interconnects)throgh an isolating level of dielectric material (oxide layer).This type of metallization is shown in the Figure 1.1 below.

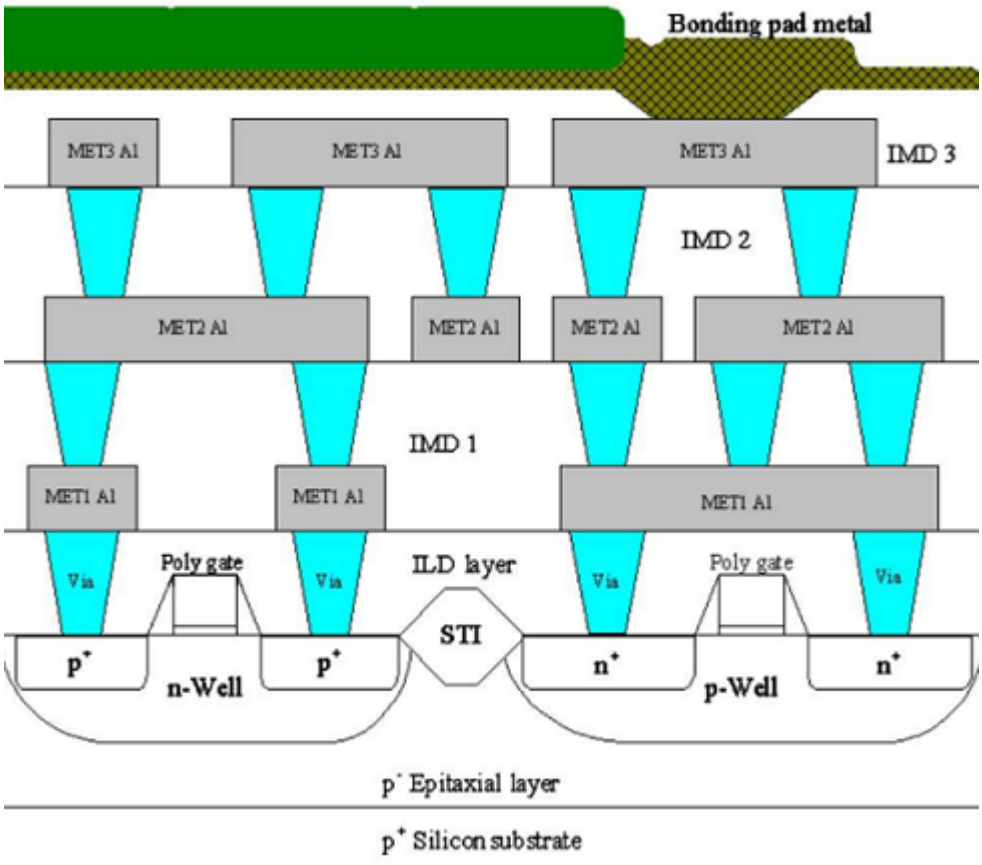


Figure 1.1: Multilevel Metallization

1.3.2 Planar Structure

The simplest structure of an integrated inductor is the planar inductor which consists of only two metal layers. One metal layer consists of spiral turns and another metal layer consists of vias or underpass.

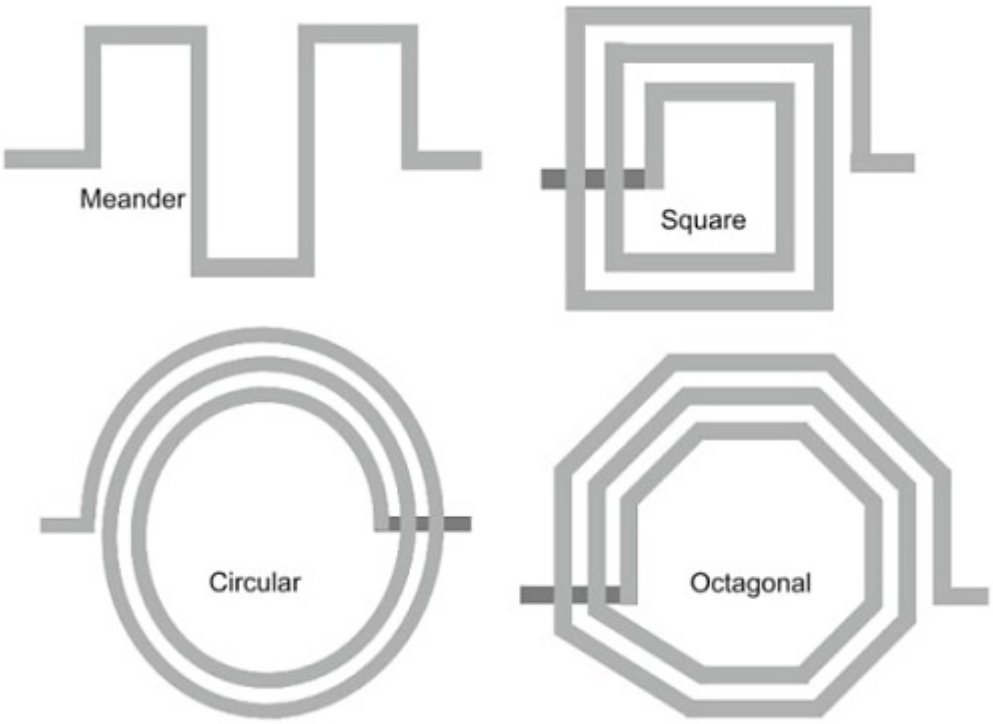


Figure 1.2: Various topologies of Planar Structure[1]

The various topologies are shown in the Figure 1.2 above. They all have their own merits and demerits and can be used according to the application requirements.

1.3.3 Multilevel Structure

More than two metal levels are required to build multilevel inductors.It will have inductor turns in multiple metal levels as shown in Figure 1.3.

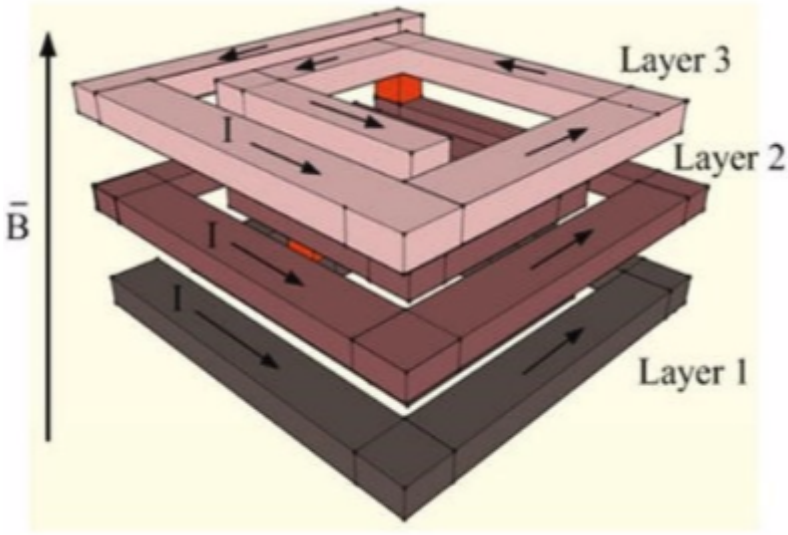


Figure 1.3: Multilevel Structure

The inductance computation for this kind of spiral is discussed in one of the next chapters.

1.4 Organization of Thesis

This dissertation is constructed with nine different chapters.

The First chapter introduces the need of on chip inductors in RF application and basic structures of on chip inductors and describes the aim of this dissertation.

The Second chapter introduces the figure of merits of an inductor and ideal characteristics of an inductor.

The Third chapter reviews High frequency effects like eddy current loss, skin effect and proximity effect that affects the overall performance of the inductor.

The Fourth chapter introduces the lumped physical model of an inductor which gives clear idea about total inductance, resistance and capacitance considering substrate losses and high frequency effect.

The Fifth Chapterrepresents the generic relation between inductance and layout parameters just to have an idea how the changes in layout parameters affect the inductance value.

The Sixth chapter reviews the Q factor variation with layout parameters as it is the most important parameter. It describes how the Q factor varies with the metal width, spacing between metal tracks, number of turns,and with area.

The Seventh chapter reviews significant amount of most updated literatures related to the topic, and offers a clear clue about on-chip inductor physics and modelling.

The Eighth chapter represents the layouts of inductor varying number of turns, spacing between tracks and width of the tracks and its simulation results done in ADS (Advanced Design System).

The Ninth chapter concludes the thesis work and leads to the future scope.

Chapter 2

Figure of Merits

2.1 Ideal Characteristics of an Inductor

An ideal characteristics of an inductor with frequency are shown in Figure 2.1 and 2.2, respectively.

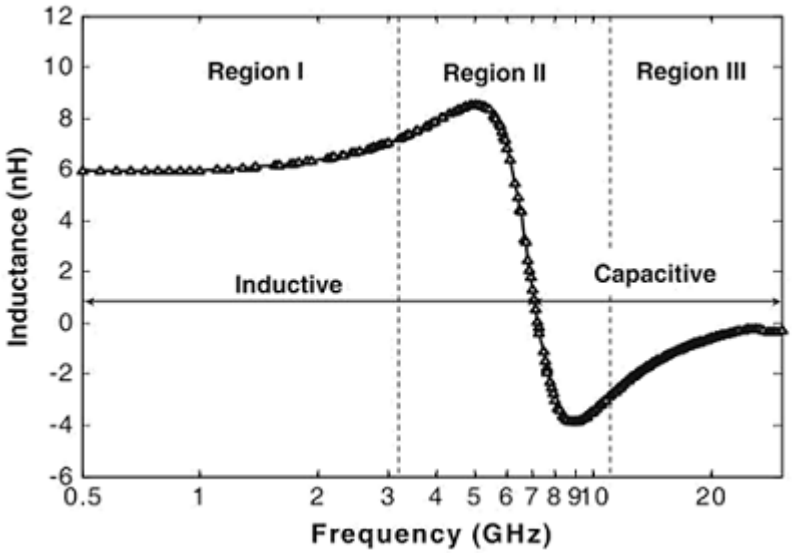


Figure 2.1: Inductance as a function of Frequency[1]

As we can see here, the effect of frequency on the inductance value can be represented in three different regions. In region I,for lower frequency the inductance value remains relatively constant.This is useful region of operation.In Region II, the drastic change in inductance value is noticed and at some frequency it becomes negative. This region is defined as transition region as inductance value crosses zero.The self resonant frequency is the one at which the inductance value crosses zero. In Region III, the inductor behaves as a capacitor and no longer works as an inductor. This region is not preferred for the operation of an inductor.

2.2 Figure of Merits

The ideal response of inductor for its quality factor to the frequency is shown in the Figure 2.2 below.

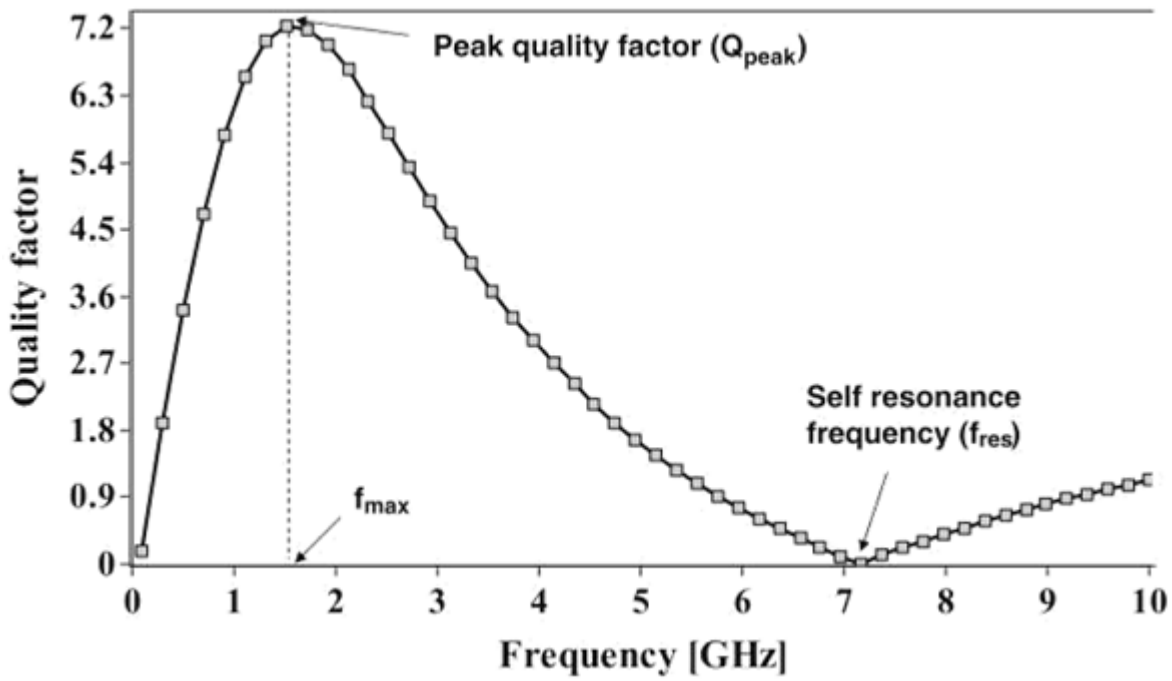
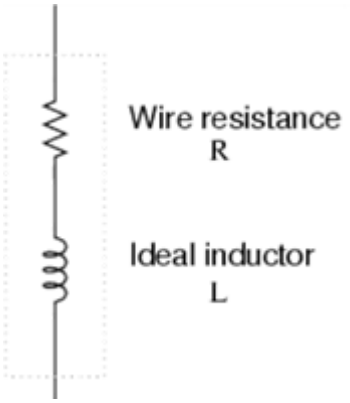


Figure 2.2: Q Factor as a function of Frequency[1]

1.Q Factor

At higher frequency every passive component will have a finite amount of resistance which converts electric current into heat. Due to this effect the inductive quality of an inductor reduces.



So quality factor is defined as ratio of inductive reactance to its series resistance.It is the measure of its efficiency.

$$Q = \frac{X_L}{R_s} \quad \text{where} \quad X_L = 2\pi f L$$

For an inductor, the energy is stored in the magnetic field. Hence the quality factor in terms of magnetic field can be defined as,

$$Q = 2\pi \left\{ \frac{Peak\ magnetic\ energy\ - Peak\ Electric\ energy}{Energy\ loss\ in\ one\ oscillation\ cycle} \right\}$$

Basically, it describes how good an inductor can work as an energy-storage element. In the ideal case,at lower frequency the Q factor will be infinity as inductor will be pure an inductor and not the combination of R, L and C. But at higher frequency parasitic resistance and capacitance reduce Q. This is because the parasitic resistance consumes stored energy, and the parasitic capacitance reduces inductivity. More will be discussed later about Q factor.

2. Optimum frequency: Fmax

The frequency at which the quality factor reaches its maximum value is called optimum frequency.

3. Self resonant frequency: Fres

At low frequencies, the inductance of an integrated inductor will be relatively constant, and that is known as the flat-bandwidth region.

When the operating frequency increases, the effect of parasitic capacitances increases and the inductance value is no longer constant. And at one frequency point, inductor will stop behaving like an inductor and will act as a purely resistive load to the circuit. This frequency is called the self resonance frequency (SRF) at which inducatnce value and quality factor will be zero.

Hence we can conclude that at higher frequency integrated inductors will have limited bandwidth over which they can be used. As the size of an inductor increases parasitic capacitances increases and as a result self resonant frequency decreases.

4. Inductance to area: L/A

The main concern in designing of an inductor is having small size as much as possible but with required inductance and quality factor. This ratio should be as high as possible.

Chapter 3

High Frequency Effects

Inductance is measured by the distribution of magnetic field inside the conductor or near the current carrying conductor. Inductance can be seen as the ability of a conductor to store magnetic energy or to link the magnetic flux. Inductors are available in various shapes and sizes like toroidal, solenoid and many more. The planar spiral integrated inductor is the simplest type of integrated inductor and is an important part of any radio frequency or microwave circuits. The high frequency effects that affect the overall performance of an integrated inductor are listed below:

1. Electric field penetration into the substrate
2. Skin effect—current redistribution within the metal conductor cross section
3. Proximity effect—current redistribution due to neighbouring current carrying conductors
4. Magnetic field penetration into the substrate.

3.1 Eddy Current Loss

Due to magnetically induced current at high frequencies, there will be nonuniformity in the current of the coil. The section of a circular inductor is shown in Figure 3.1. I_{coil} is the curent in the coil while B_{coil} is the associated magnetic flux. The magnetic flux lines entering the page near the turn n will come out of the page in the center of the inductor. If we keep the inner diameter too small, the magnetic fields from outer turns will pass through some of the innermost turns.

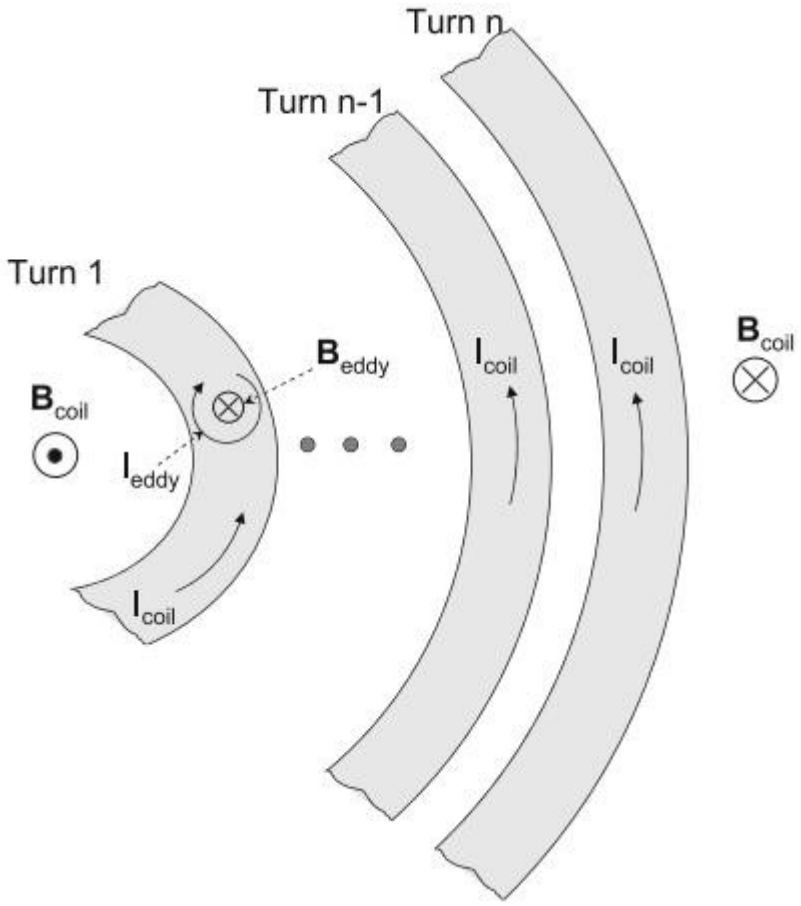


Figure 3.1: Eddy current formation in circular planar inductor[1]

According to the famous laws of Faraday and Lenz, there will be eddy currents in the inner most turns of an integrated inductor which is shown in Figure 3.1. An opposing magnetic field B_{eddy} will also be developed due to the eddy current. From the figure we can see that the current density will higher on the inner side than on the outer side and result in a nonuniform current in the metal turns of the spiral inductor.

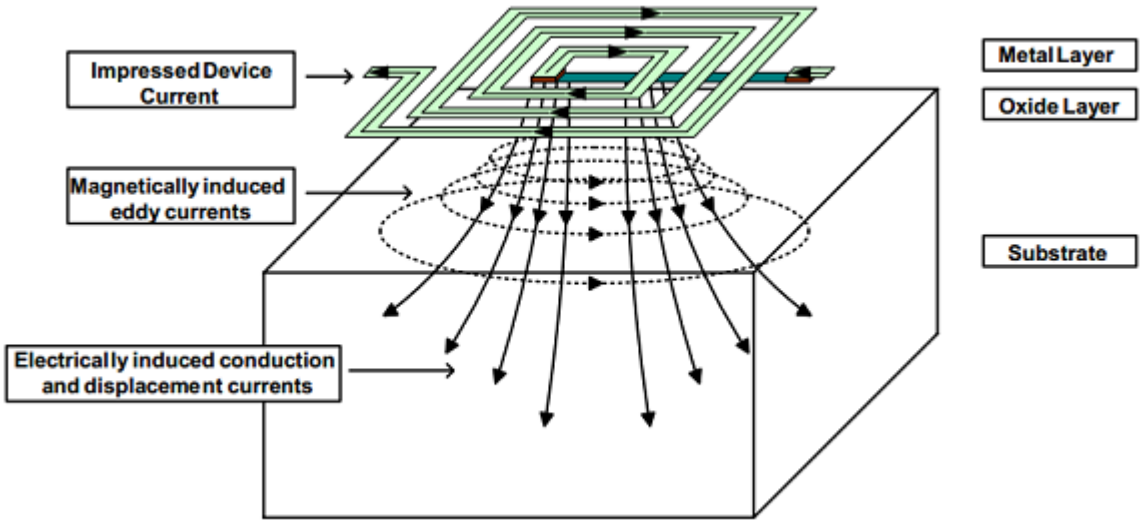


Figure 3.2: Substrate currents distribution[4]

3.2 Skin Effect

In perfect conductor, magnetic field will penetrate the whole material but in an imperfect conductor, an increasing magnetic field will penetrate the material to some extent which induces voltage. And due to this the current flows in such a manner that it prevents the magnetic field from passing through the conductor. In simple words. it forces the current to flow through the outer surface only. That means it increases the resistance to the center. This effect is known as "Skin Effect".

The losses in the conductor is proportional to the resistance of the metal. At low frequencies the series resistance will be given by

$$R = \frac{\rho l}{W.t}$$

Here the length of inductor, width of turns, thickness of metal layer, and the resistivity of metal layer id represented by l, W, t and ρ. Due to skin effect, at higher frequencies the series resistance increases.

Skin effect decreases the effective thickness of metal layer which is given by:

$$t_e = \delta\left(1 - e^{\frac{-t}{\delta}}\right)$$

where δ represents the skin depth of the metal. Therefore the equation of series resistance reduces to,

$$R = \frac{l\rho}{W\delta\left(1 - e^{\frac{-t}{\delta}}\right)}$$

As frequency rises, the resistance of a metal segment will increase due to the skin effect. The skin depth of metal is given by,

$$\delta = \sqrt{\left(\frac{\rho}{\mu f}\right)}$$

where resistivity of the metal, the permeability and the frequency of operation is represented by 'ρ', 'μ', and 'f' respectively.

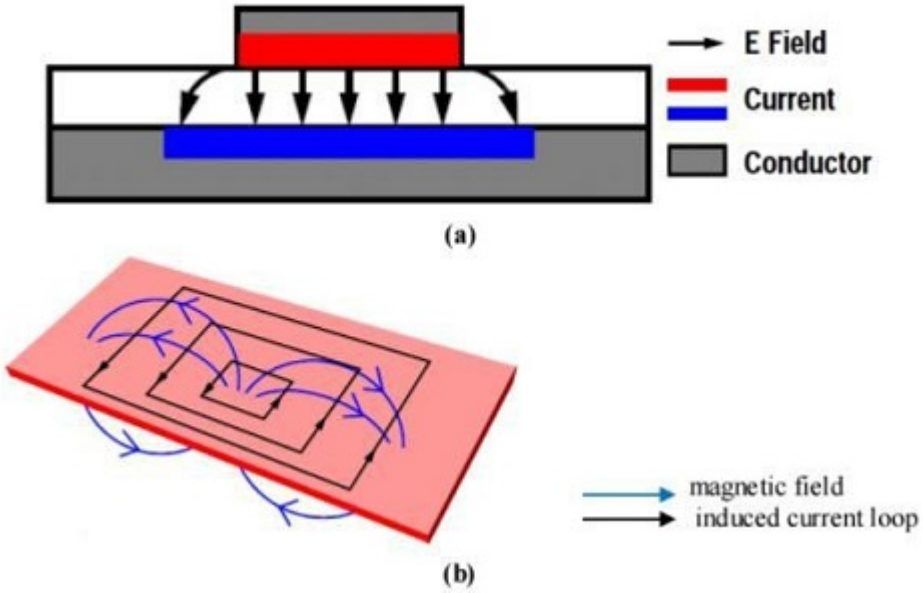


Figure 3.3: (a) cross sectional view under skin effect (b) current distribution in conductor[3]

3.3 Proximity Effect

When we put a current carrying conductor nearby an inductor then it affects the magnetic field distribution of an inductor. And as a result it will change the current distribution inside an inductor. And as like eddy current effect, smaller current loops will be generated at higher frequencies.

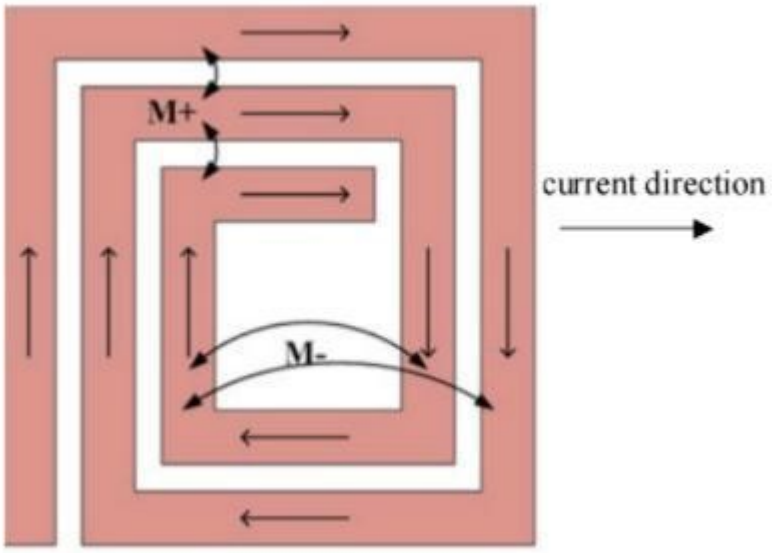


Figure 3.4: Positive and negative mutual inductance[3]

In the spiral inductor shown in Figure 3.4, there are some turns in which current flow is in same direction and there are others in which the current floe is in opposite direction. Hence this spiral will be affected by the proximity effect. Almost all spirals will be affected by this effect. The mutual inductance between turns in which the current flow is in same direction is represented by M+. And opposite to that M- defines mutual inductance between conductors in which the current flow is in opposite direction.

Chapter 4

Physical Modeling Concept

There is a well-defined and well-accepted physical model of an inductor to understand its characteristics aqt higher frequencies as shown in Figure 4.1. This lumped element model consists of the inductor, parasitics resistances and parasitis capacitances. The model may be valid upto the self-resonance frequency of the inductor.

In the following subsections, we will consider the square shaped spiral inductor and use the model in Figure 4.1 as a benchmark to discuss the issues related to an integrated inductor, including the series inductance, series resistances and series capacitances.

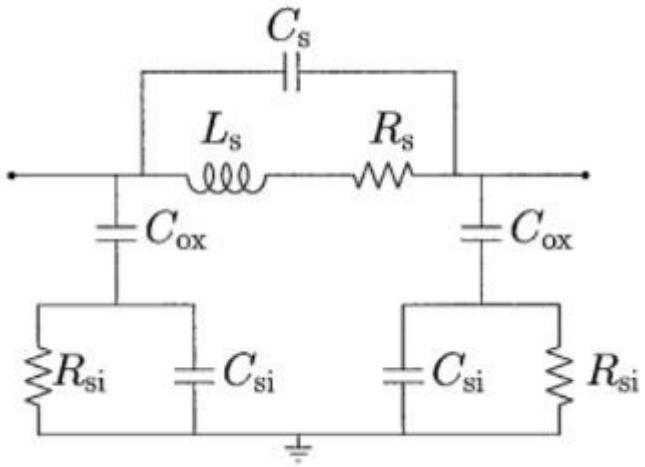


Figure 4.1: Lumped physical model of planar inductor[5]

Series inductance L_s and Series resistance R_s represents the inductance and resistance of the spiral and underpass. Series capacitance C_s represents the direct capacitive coupling between two terminals of the inductor due to the overlap between the spiral and underpass. The capacitance between the oxide layer and silicon is represented by C_{ox}. The capacitance and resistance of the substrate is represented by C_{si} and R_{si} respectively. The each of these elements is explained in detail in the following sections.

Series Inductance

the total series inductance is the combination of self inductance of a wire and the mutual inductance between a pair of wires. The self inductance of a wire having rectangular cross-section area is defined as:

$$L = 0.002\ l\left[\ln\left(\frac{2\ l}{w\ +t}\right)\ +0.50049\ +\frac{w\ +t}{3\ l}\right]$$

length of the segment, width of conductor and thickness of conductor is represented by l, w and t respectively. The mutual inductance between two parallel conductors is given by:

$$M = 2\ l\ H$$

This equation is valid for the conductors having equal length. The mutual inductance is represented as H which can be calculated as:

$$H = \ln\left\{\frac{l}{GMD} + \sqrt{\left(1 + \frac{l^2}{GMD^2}\right)}\right\} - \sqrt{\left(1 + \frac{GMD^2}{l^2}\right)} + \frac{GMD}{l}$$

Here GMD reprents the geometric mean distance between two conductors which is approximately equal to the distance d between the center of the conductors. It can be calculated as:

$$\ln GMD = \ln d - \left\{\frac{w^2}{12d^2} + \frac{w^4}{60d^4} + \frac{w^6}{168d^6} + \frac{w^8}{360d^8} + ...\right\}$$

Series Resistance

At lower frequency or at dc, the current density in the conductor will be uniform. But at higher frequencies due to eddy current formations, the current density becomes onuniform. According to Faraday's law when a conductor is subjected to a time varying magnetic field, the eddy current effect occurs. Also according to Lenz's law, the original magnetic field is opposed by the magnetic field produced by the eddy currents.

When a conductor is under the influence of a time varying field produced by a nearby conductor carrying a time varying current, eddy currents are induced. The total eddy current distribution includes the skin effect eddy current and proximity eddy currents. Due to these eddy current formations, the net current through conductor reduces. And hence the ac resistance of the conductor increases. The geometry of conductor and its orientation with respect to time varying magnetic field also affects the eddy current distribution.

Series Capacitance

The series capacitance C_s is the coupling capacitance between input port and output port of the inductor. Due to this capacitance, signal flows directly from the input port to output port without going through the spiral coils. The overlap between te spiral coils and underpass is the main reason for this coupling capacitance.

Another reason can be the crosstalk capacitance between adjacent turns. But as the potential of adjacent turns are equal, the effect of crosstalk capacitance is negligible. Generally for smaller spacing between turns, this crosstalk capacitance will be higher. Hence by increasing the spacing between turns, crosstalk capacitance can be reduced. Due to large potential difference between spiral coils and underpass, the overlap capacitance value will be larger compared to crosstalk capacitance. So the overlap capacitance is the main concern and is defined as:

$$C_s = n\ W^2\ \frac{\epsilon_{ox}}{t'_{ox}}$$

where the number of overlap, the width of spiral tracks, and the oxide thickness between the spiral and the underpass is represented by n, W, and t'_{ox} respectively.

Substrate Parasitics

The characteristics of semiconductor substrate like silicon also affects the performance of an inductor. The physical model of any substrate consists of substrate resistance R_{si}, substrate capacitance C_{si} and oxide capacitance C_{ox} between oxide layer and substrate.

The majority carrier concentration determines the conductivity of silicon substrate. The high frequency capacitive effect is modeled by the substrate capacitance C_{si}. Each of them can be defined as:,

$$C_{ox} = \frac{1}{2}\ l\ W\ \frac{\epsilon_{ox}}{t_{ox}}$$

$$R_{si} = \frac{2}{l\ W\ G_{sub}}$$

$$C_{si} = \frac{1}{2}\ l\ W\ C_{sub}$$

where G_{sub} and C_{sub} are the conductance and capacitance per unit area of the silicon substrate and tox is thickness of the oxide layer separating the spiral and the substrate.

Chapter 5

Inductance Computation

The inductor geometry is defined by the number of turns , the width of tracks , the spacing between tracks, the outer diameter , the inner diameter , the average diameter , and the fill ratio. The thickness of the metal layers has a very small effect on inductance and hence it is ignored in this computation.

Input parameters:
n = number of turns
w = turn width in μm
s = spacing between turns in μm ($\leq$ w)
d_{in} = input diameter in μm
d_{out} = outer diameter in μm
$d_{out} = d_{in}$ + 2wn + 2s(n-1)

5.1 Modified Wheeler Formula[10]

Many equations are proposed to calculate the inductor parameters but the most used and suggested equations by researchers are described here. These equations are just for modelling purpose, it won't give the inductance value at specific frequency but will let us know how the inductance value can be affected by layout parameters.

$$L_{mw} = K_1 \ \mu_0 \ \frac{n^2 \ d_{avg}}{1 \ + K_2 \ \rho}$$

Where,
n = number of turns
K_1 , K_2 = layout dependent parameters which are shown in the table 5.1 below

layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.35

Table 5.1: Layout parameters value used in Modified wheeler formula

$$\begin{aligned}\rho &= fillfactor \\ &= \frac{d_{out} - d_{in}}{d_{out} + d_{in}}\end{aligned}$$

The ratio represents how hollow the inductor is: for small ρ we have a hollow inductor ($d_{out} = d_{in}$) and for a large ρ we have a full inductor ($d_{out} \geq d_{in}$).

5.2 Expression based on current sheet approximation[10]

Another simple expression for the planar integrated inductors are as below. It is valid for all the standard topologies.

$$L_{gmd} = \frac{\mu\ n^2\ d_{avg}\ c_1}{2} \left[\ln\left(\frac{c_2}{\rho}\right) + c_3\ \rho + c_4\ \rho^2 \right]$$

where, c_1, c_2, c_3, c_4=layout dependent parameters which are showed in the table 5.2 below

layout	C_1	C_2	C_3	C_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circular	1.00	2.46	0.00	0.20

Table 5.2: Layout parameters value used in Expression based on current sheet approximation

Although the accuracy of this expression worsens as the ratio $^{s}/_{w}$ becomes large, it exhibits a maximum error of 8 % for s $\leq$ 3w . Note that typical practical integrated spiral inductors are built with s $\leq$ w.

5.3 Data fitted monomial Expression[10]

$$L_{mon} = \beta\ d_{out}^{\alpha_1}\ w^{\alpha_2}\ d_{avg}^{\alpha_3}\ n^{\alpha_4}\ s^{\alpha_5}$$

Where,
d_{out} = outer diameter
n = number of turn
s = spacing between metal tracks
β, α_1, α_2, α_3, α_4, α_5 = layout dependent parameters presented in the table 5.3

layout	β	α_1	α_2	α_3	α_4	α_5
Square	1.62	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	1.28	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	1.33	-1.21	-0.163	2.43	1.75	-0.049

Table 5.3: Layout parameters value used in Data fitted monomial Expression

With the help of above equations, we have calculated inductance by varying layout parameters to see how it is affected by these changes of parameters. Those results are shown in the Figure 5.1 in a tabular form. The parameter which is changing is highlighted by the black box.

						SQUARE	
N	W	S	Dout	Din	Lmw	Lgmd	Lmon
5	2	2	440	404	27.766	32.749	31.811
5	6	2	440	364	23.455	24.897	24.089
5	12	2	440	304	18.199	18.287	18.061
5	20	2	440	224	12.882	12.735	12.751
5	30	2	440	124	8.159	8.149	8.12
5	40	2	440	24	4.921	5.103	4.572
5	42.3	2	440	1	4.337	4.575	4.277
5	16	16	440	152	9.308	9.25	9.399
5	16	10	440	200	11.581	11.453	11.494
5	16	6	440	232	13.343	13.194	13.121
5	16	1	440	272	15.872	15.776	15.907
5	16	0.5	440	276	16.147	16.065	16.461
2	14	2	440	380	4.015	4.392	4.365
5	14	2	440	284	16.71	16.662	16.538
8	14	2	440	188	28.093	27.803	27.137
10	14	2	440	124	32.637	32.595	31.191
13.85	14	2	440	0.8	33.24	35.072	30.826
5	14	2	440	284	16.71	16.662	16.538
5	14	2	400	244	14.207	14.11	14.013
5	14	2	350	194	11.179	11.064	10.985
5	14	2	320	164	9.431	9.324	9.249
5	14	2	270	114	6.667	6.599	6.518
5	14	2	200	44	3.252	3.269	3.156

Figure 5.1: Effect of changing layout parameters on inductance

Observation

The most fundamental way to increase the inductance is to increase the number of turns keeping the width, spacing and area constant.But due to decremented inner diameter, magnetic field of outermost turns will pass through some of the innermost turns inducing eddy current loops which results in increased resistance. Hence it will have lower Q factor comparatively.

If the area is limited or fixed we can increase the inductance by either reducing width or spacing keeping the number of turns constant. To do this the inner diameter has to be increased and hence the eddy current effect will be less. So theoretically it should provide higher Q factor and resonant frequency.

If we have no restriction on area then to increase inductance, inner diameter and outer diameter needs to be increased keeping all other layout parameters constant.

Apart from these way there may be several ways to have higher inductance or quality factor by having some advanced topology as discussed in the following chapter.

Chapter 6

Q Factor dependence on Layout Parameters

The performance of integrated inductor depends on their geometry or structure which includes few layout parameters as listed below:

1. Number of turns N
2. Metal track/turn width W
3. Spacing between metal tracks/turns S
4. Outer diameter D_{out}
5. Inner diameter D_{in}

The aim of an integrated inductor is to have a high quality factor for desired inductance value. As discussed earlier, Quality factor can be defined as the difference between the peak magnetic energy and electric energy. With the increase in frequency quality factor increases and reaches its maximum value. After that due to high frequency losses and substrate losses quality factor decreases. The following sections describes the effect of varying these layout parameters on quality factor.

6.1 Q Factor variation with number of turns[1]

As we go for higher frequencies, Quality factor increases for a given number of turns. But then due to parasitics caused by high frequency effects quality factor decreases. By keeping the inductance constant, if we increase the number of turns the inner and outer diameter needs to be reduced. This is based on the inductance formula explained in the last chapter. The effect of increasing number of turns on the outer diameter is shown in the table 6.1.This change will lead us to the smaller area and longer length of the spiral. Smaller diameter also increases the eddy current effect.

Fixed L, W, and S			
Number of Turns	3	5	7
Outer Diameter	226 μm	163.3 μm	158 μm

Table 6.1: Effect of increasing number of turns to achieve the same inductance

The another reason for lower quality factor is spiral's longer length due to higher number of turns. Because series resistance increases as lenth of spiral increases. To have higher quality factor we must increase the inner diameter to reduce the eddy current effect.

6.2 Q Factor variation with turn width[1]

The turn width is an important parameter. For a fixed number of turns,if we want to achieve the same inductance by increasing width, the area will increase. At lower frequencies (below 2 GHz), as the width increases quality factor increases. This is because quality factor is inversely proportional to the series resistance of spiral which will decrease for larger width.

But at high frequencies (above 1.8 GHz) quality factor decreases with increase in width. Because the resistance increases due to high frequency effects like skin effect and current crowding problem. The effect of variation in width on area of an inductor is shown in the table 6.2.

Fixed L, N, and S			
Width of Tracks	5.5 μm	8 μm	10.5 μm
Outer Diameter	226 μm	244.8 μm	262.8 μm

Table 6.2: Effect of increasing width to achieve the same inductance

Another reason of lower quality factor is higher substrate coupling capacitance due to increased surface area. Hence for larger width, quality factor and resonant frequency decreases faster. But quality factor will have higher value for small width. Also optimum frquency F_{max} and self resonant frequency F_{res} increases for smaller width.

6.3 Q Factor variation with spacing between tracks[1]

To observe the effect of spacing, number of turns and width of metal track is kept constant. If we increase the spacing between metal tracks, the magnetic coupling will decrease. And to achieve the same inductance, we have to increases the inner diameter keeping the number of turns constant. This is shown in the table 6.3. But this will result in increased length of spiral increasing the series resistance. And due to higher resistance quality factor decreases. Hence to achieve higher quality factor spacing between tracks should be minimum. The same effet is on the optimum frequency F_{max} and self resonant frequency F_{res}.

Fixed L, N, and S			
Width of Tracks	5.5 μm	8 μm	10.5 μm
Outer Diameter	226 μm	244.8 μm	262.8 μm

Table 6.3: Effect of increasing spacing to achieve the same inductance

6.4 Area of an Inductor[1]

Generally most of the area on die is occupied by inductor structures. While designing an inductor, the aim is always to have the size as small as possible because if area increases cost increases. We can have smaller area by reducing inner diameter and outer diameter. But on the other hand, we must be able to achieve desired results as in inductance and quality factor. Hence the area of an inductor is an important parameter.

The area of the spiral is defined as $D_{out} \times D_{out}$. To reduce the area, if we decrease the inner diameter keeping the width and spacing constant, to have same inductance we have to increase the number of turns. Also the area of the inductor will increase as we go for higher width. Also in case of spacing, keeping the width and number of turns constant, to achieve the same inductance we have to increase the inner diameter. Hence area will be smaller for smaller spacing.Thus, the spacing has to be kept as minimum as possible.

Hence if we want to design an inductor with minimum area, we should choose smallest track width, higher number of turns and minimum spacing.

6.5 Q factor variation with oxide layer thickness underneath spiral

As discussed before, Integrated inductor is just like a sandwich structure. There will be an oxide layer between spiral coils and substrate. The thickness of this oxide layer also affects the quality factor performance of an inductor.

The coupling capacitance between spiral and substrate increases as we go for smaller thickness of this oxide layer. Due to this quality factor decreases. The same effect is observed on self resonant frequency. Hence oxide layer thickness should be such that coupling capacitance is as minimum as possible.

6.6 Increasing Q factor without varying any layout parameters

There exists several ways to have better performance in terms of quality factor. One can go with advanced structures. But the following are some methods which do not require any changes in layout parameters.

1. Micromachining: This process is used to reduce substrate losses. It etches out the silicon portion that is only below the spiral coil. That way substrate losses can be minimized and can have higher quality factor and self resonant frequency.

2. PGS (Patterned Ground Shield) : Silicon parasitic of on chip inductor could also be eliminated with Patterned grounded shield. Because it acts as a short and prevents the flow of electric field through in the substrate.This type of inductor is discussed in one of the next chapters.

3. The use of silicon substrate having high resistivity might help us improving quality factor as field coupling through substrate will be less.

Chapter 7

Advanced Integrated Inductor structures

At higher frequency the design of an inductor is not an easy task as its performance will be frequency dependent. we can design an inductor having fixed area with many more combination of metal width, spacing between metal turns and number of turns to achieve the same inductance. Optimization can be done in two ways. One can change layout parameters to achieve the desired results or can come up with totally new design in terms of metal layers configurations. Some of these advanced structures are explained in the following sections.

7.1 Horizontal Structures

In horizontal inductors the spiral winding is parallel to the substrate. Mostly horizontal inductors are used nowadays as they are simple to fabricate and designer will have freedom in choosing layout parameters.

7.1.1 Structures to reduce substrate loss

Inductor with Patterned Ground Shield (PGS)

We can reduce the substrate loss in two ways either by reducing substrate resistance or by decreasing the substrate capacitance. To reduce substrate resistance, we can insert e metal or a poly silicon layer between spiral turns and the substrate and connect this layer to the ground as shown in Figure 7.1. This idea is known as the ground shielding. By doing this we just simply reduces the effective distance between the spiral metal and ground which reduces the substrate coupling resistance. And hence improves the quality factor.

The only disadvantage of this structure is the additional capacitance as the distance between spiral turns and ground reduces which decrease the self-resonance frequency.

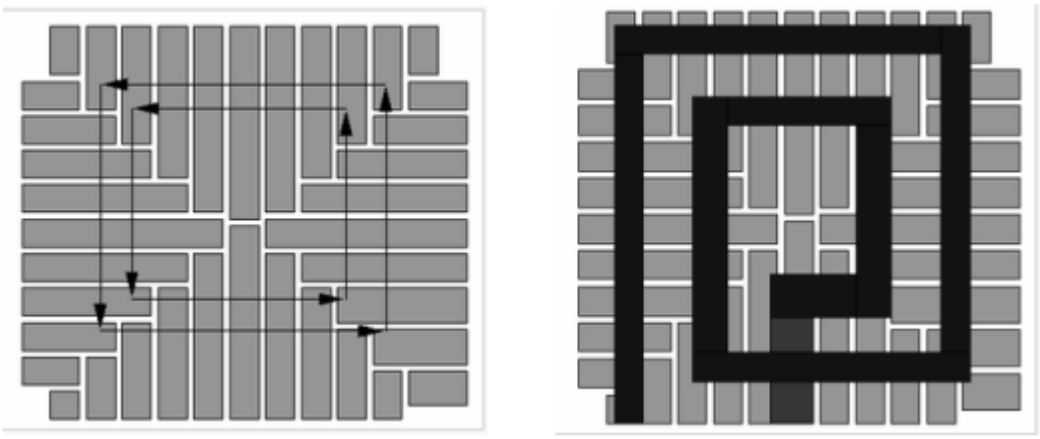


Figure 7.1: Inductor with Patterned Ground Shield

Removal of substrate

Another way to increase quality factor theoretically is to increase the substrate resistance as much as possible. Some of the ways to do this are described below:

1. One way is to use an insulator such as quartz or glass as substrate which gives better quality factor and self resonant frequency.

2. by oroton implantation Technology, for CMOS-based on-chip inductors, it is possible to make a region with high resistivity for placing only the inductor. This can be done .

3. Using an advanced micromachinary process, an inductor can be built above the silicon.

4. The silicon underneath only the inductor can be removed using the deep-trench technology.

7.1.2 Structures to increase Inductance

As per standard rule, quality factor is directly proportional to the series inductance. So to have better performance in terms of quality factor we can increase the series inductance.

Stacked Structure

Number of planar inductors in different metal layers connected in series make the stacked structure as shown in Figure 7.2. The main advantage of this multilevel or stacked structure is higher inductance to area ratio.

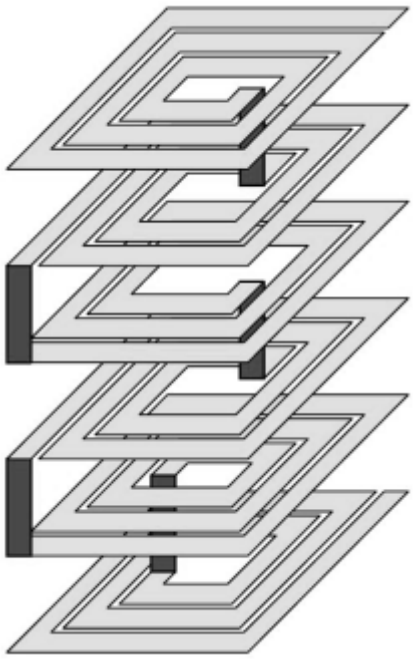


Figure 7.2: Stacked Inductor with six metal layers

But due to the stacked structure, substrate capacitances and metal to metal capacitances increase. Hence it provides the lower quality factor and self resonant frequency.

Miniature 3D inductor

This 3D structure is same as stacked structure in terms of series connection. The only difference is that every stacked inductor has only one turn in every metal layers as shown in Figure 7.3.

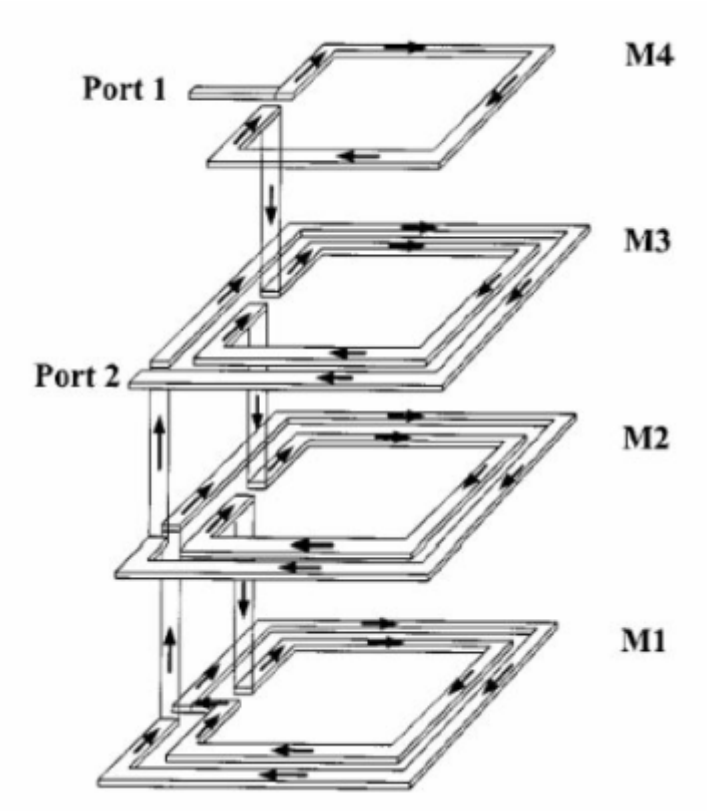


Figure 7.3: Strucute of Miniature 3D inductor

7.1.3 Structures to reduce series resistance

Vertically shunted metal layers

As the name suggests each metal layers are shunted through via arrays as shown in Figure 7.4. to increase the effective thickness of the spiral.

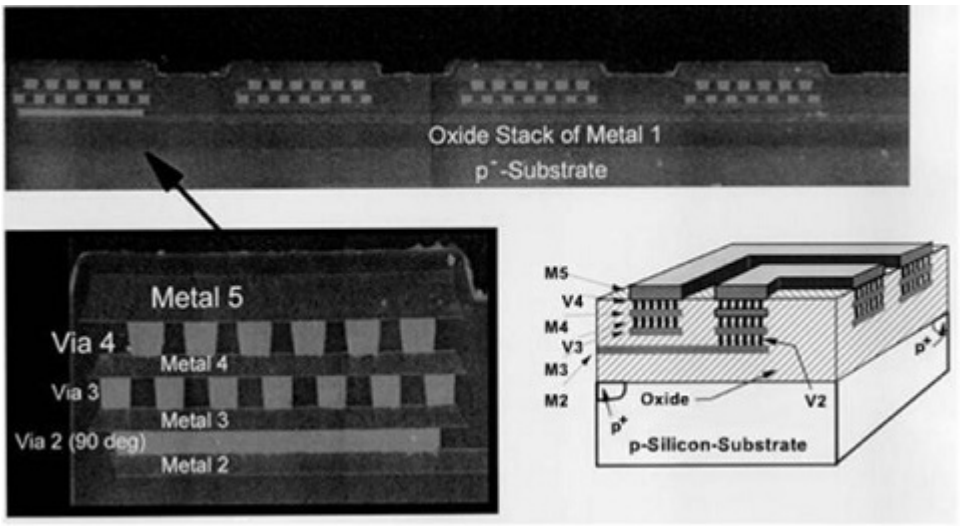


Figure 7.4: Inductor with shunted metal layers

Some of the disadvantages of using lower metal layers are listed below.

• As we increase the shunting of metal layers, the distance between metals and substrate will reduce. That will increase the metal to substrate capacitance. Also the capacitance between metal lines also increases. Due to increment in these capacitance, resonance frequency will decrease.

• The capacitance among the metal lines would also increase.

Inductor with horizontally shunted metal layers

The main purpose of this kind of structure is to suppress the current crowding effect as it one of the reasons of nonuniform current distribution and increased resistance. Current crowding effect is maximum in square structure. So to reduce this effect one can go with circular layout or further divide the spiral inductor in several parallel current paths, each with an identical resistance and inductance as shown in Figure 7.5 below. For the same line width, the Q factor increases with increasing number of splits.

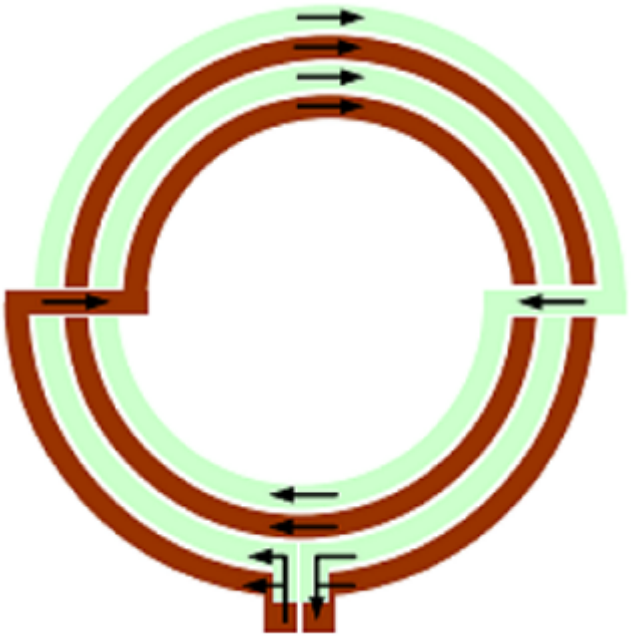


Figure 7.5: Inductor with horizontally shunted metal layers[2]

Tappered Inductor

The origin of these magnetic losses stems from the fact that the magnetic flux increases as we move towards the center of the spiral, due to the additive nature of the flux from each successive loop of the spiral.

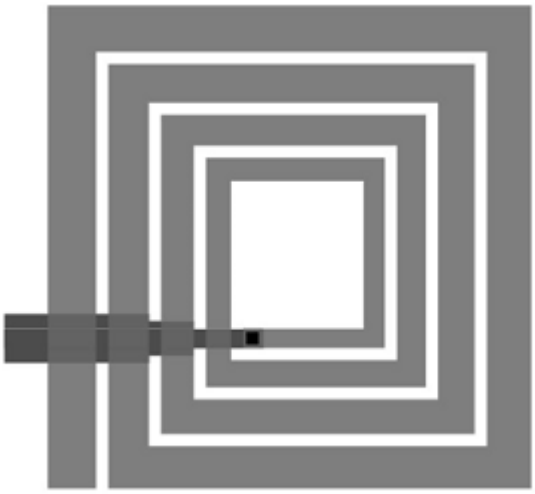


Figure 7.6: Tappered inductor

If the width of the structure is tapered as shown in Figure 7.6, the performance can be improved.

Since the wide inner turns do not lower the resistance (due to current constriction), it is better to transfer the width to the outer turns, while keeping the total area of the spiral constant.

7.1.4 Toroidal Inductor

It consists of pair of strips in two metal layers which are connected by vias as shown in Figure 7.7 below.

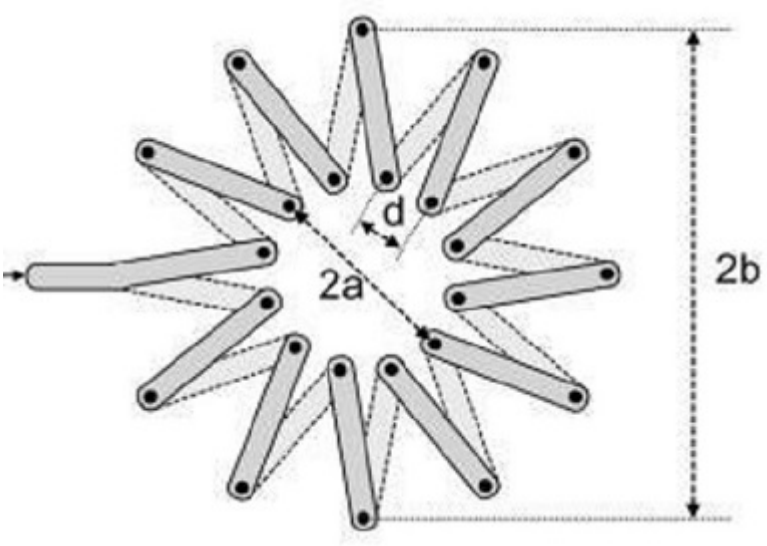


Figure 7.7: Toroidal Inductor

To design this kind of inductor on chip is very defficult and there are very few tools available that can model toroidal inductors.It is used when some higher value of inductance can only be achieved by increasing number of turns.

7.1.5 Novel Inductor

Novel inductor is designed in such a way that each turn covers both the layers as shown in Figure 7.8 below. Depending on the application requirement one can change the configuration of turns.

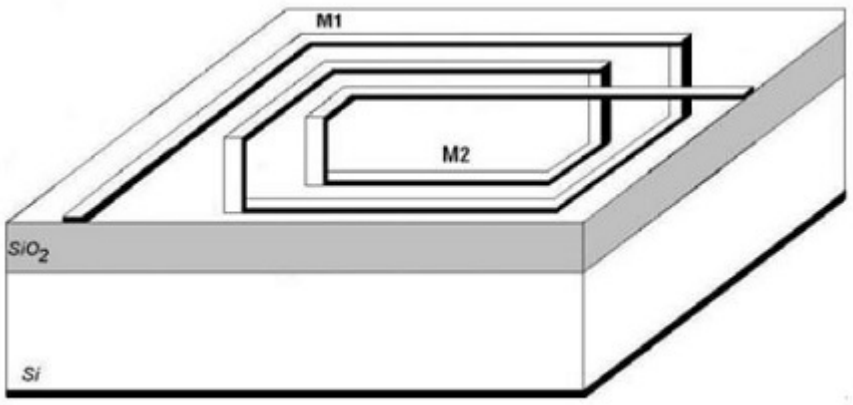


Figure 7.8: Novel Inductor[8]

Merits:

1. Fewer turns are required to meet specified inductance compared to planar square inductor.

2. Increased Q factor for fixed inductance compared to planar square inductor.

3. Reduction in the number of parallel conductors on the same level leads to a total reduction of proximity effects and capacitive coupling.

7.2 Vertical Inductors

In horizontal inductors, spiral winding is parallel to the substrate so they consume larger area and hence increases the total cost. But in vertical inductors, spiral winding is perpendicular to the substrate as shown in Figure 7.9.

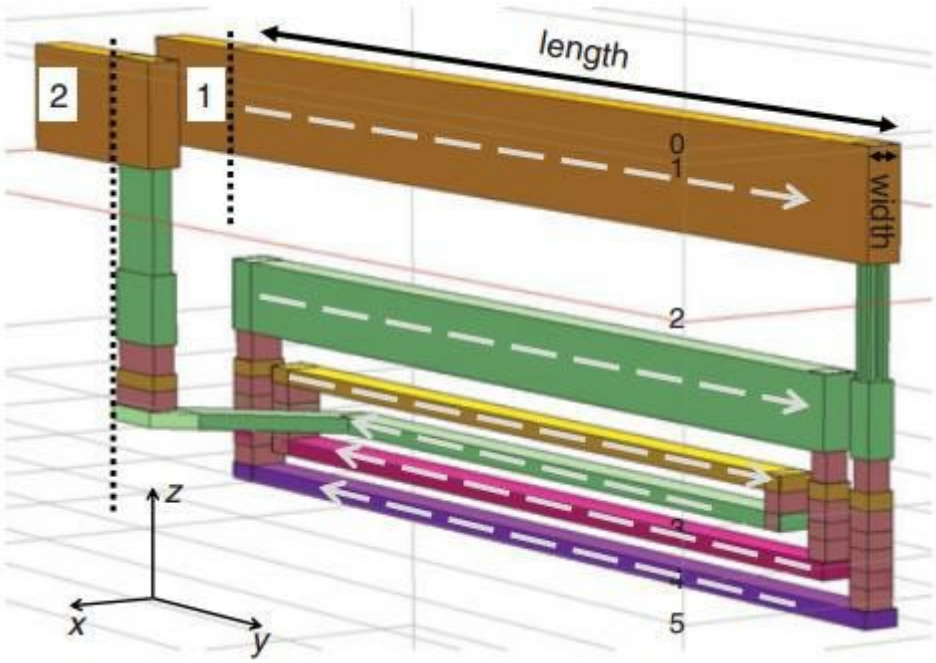


Figure 7.9: Vertical Inductors[11]

Merits:

1. As it consumes smaller area than horizontal inductors, it exhibits larger inductance to area ratio.

Demerits:

1. Lower Q factor :Vertical inductor uses lower metal layers which increases the coupling capacitance to the substarte. Hence it has lower quality factor compared to horizontal inductors.

2. To achieve the same inductance we need to use higher number of turns or longer length compared to horizontal structures.

Chapter 8

Physical Layout Designing and Simulation

Layout Design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit.

Traditionally, spiral inductors are made in square shape due to its ease of design and support from drawing tools. From the performance point of view, however, the most optimum pattern is a circular spiral because it suffers less resistive and capacitive losses. But the circular inductor is not widely used because only a few commercial layout tools support such a pattern. Hexagonal and octagonal structures are good alternatives, as they resemble closely to the circular structure and are easier to construct and supported by most computer-aided design tools.

Generally there are two cases of designing an indutor, one within the fixed area and the one with no restriction on area. The most likely case is of fixed area as our chips are becoming smalller and smaller. So here I have made some layout varying layout parameters within the same area.

The layouts and simulation both are done in different softwares. The simulations are done in ADS (Advanced Design System). The layouts and simulation results are presented in the sections below.The results also depend on the metal types and their properties from which the inductor is made.

8.1 Schematic Simulation set up

There will be two simulation, layout and schematic simulation. First of all Layout simulation needs to be done to get S parameter results which will be used in schematic simulation to get the results. In all layouts, the input and output ports are in the top metal layer which is indicated in the figures by blue colour.The coils are below the top metal layer.That coil metal layer is indicated by brown color in the given layouts.The ends of the coil are connected to top metal layers through vias to make input and output ports available to other circuits.

Schematic simulation set up is shown below in Figure 8.1. In which the square data block represents the inductor itself. The name of file .s2p represents the inductor's S parameter file having 2 ports. This schematic calculates S, Z, and Y parameters. To get the results we have to add the equations manually.
These equations are shown below:

$$Zdiff = Z(1,1) + Z(2,2) - Z(1,2) - Z(2,1)$$

$$Rs_p = real(Zdiff)$$

$$Q_p = imag(Zdiff)/Rs_p$$

$$L = imag(Zdiff)/(2 * 3.14 * freq)$$

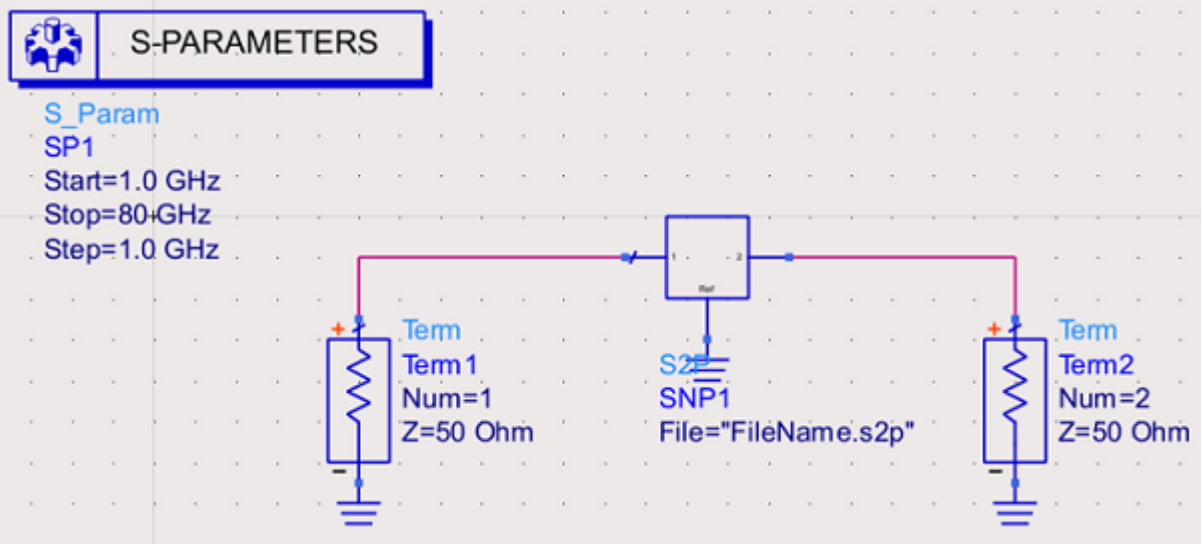


Figure 8.1: Simulation Set up for individual

The simulation setup shown in the Figure 8.2 is used when we want to compare the results for the same purpose. The first part is of DataFileList, which indicates the file name and work path of your schematic. The second part is of batch simulation. In which the variable will be our file list1. The start and stop tells the simulator for which file from the list it has to simulate.

Here in our case we want the simulation results of all three schematics, So we have mentioned stop as 3 and start as 1. SP1 analysis refers to the s parameter simulation. The s parameter set up is same as individual schematic set up. The simulation results shown in following sections are of batch simulations.

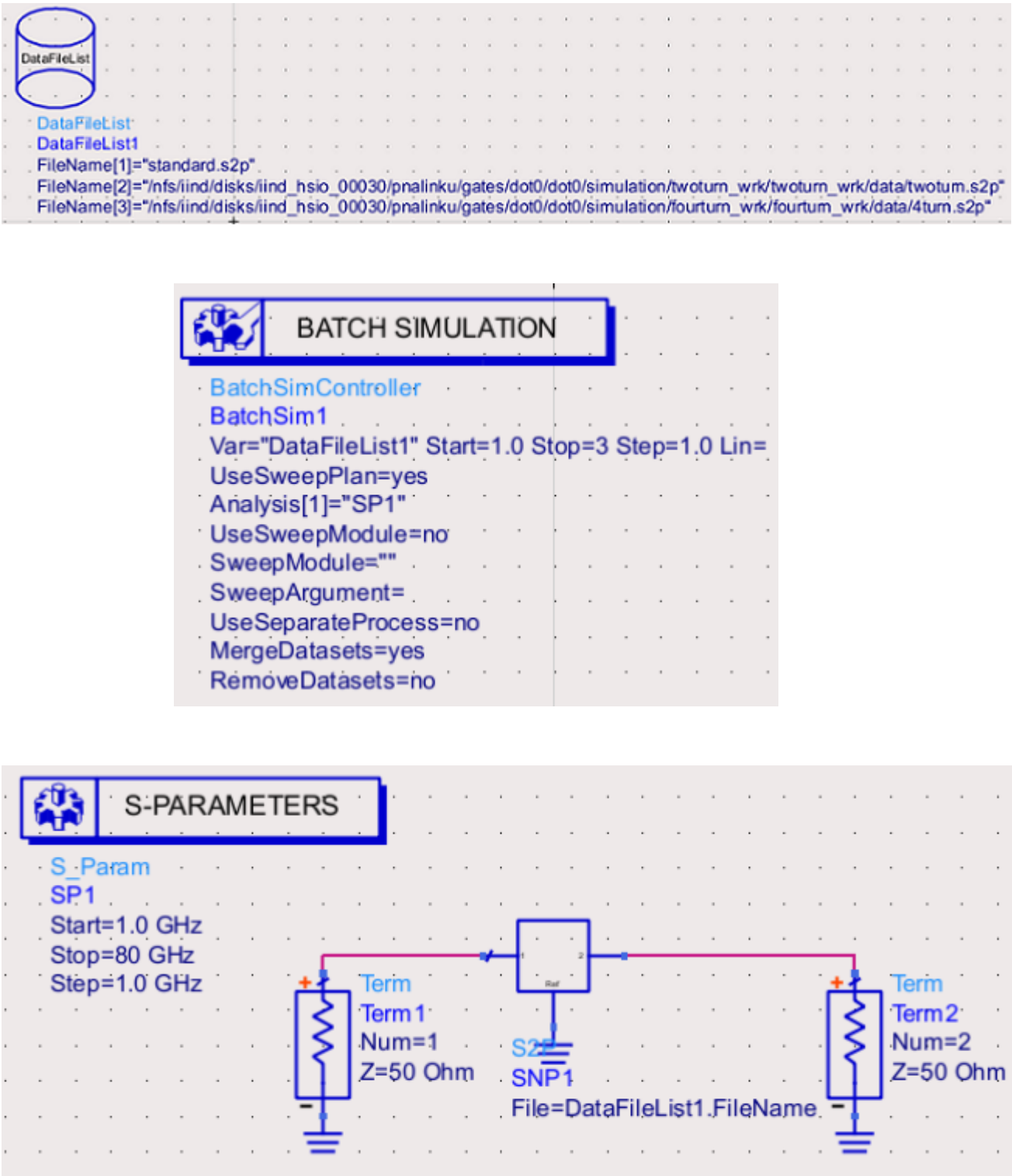
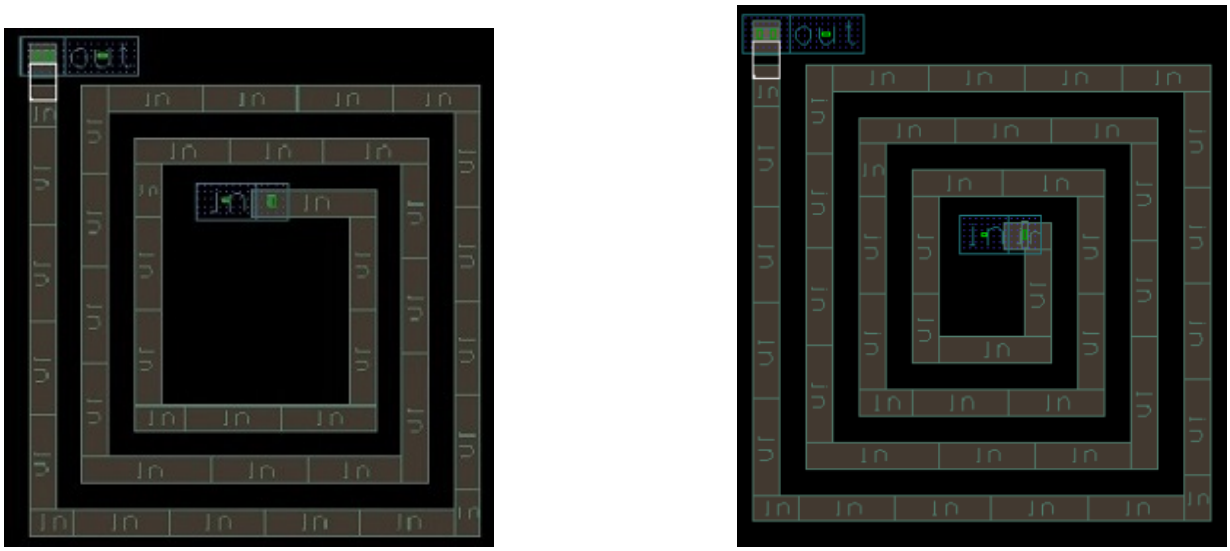


Figure 8.2: Simulation Set up for comparison

8.2 Effect of varying number of turns keeping the Area constant



(a) (b)

Figure 8.3: Layout having(a) N=3,(b) N=4, fixed s and W, d_{out}=95μm

Simulation results :

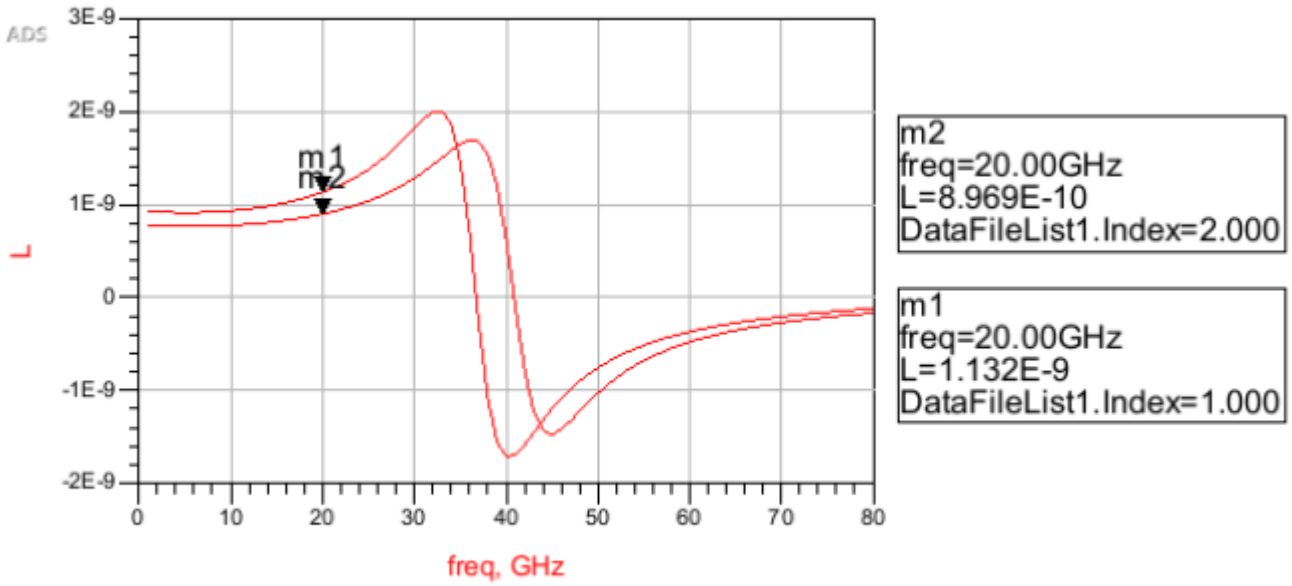


Figure 8.4: Inductance variation with number of turns

Here in Figure 8.4 index 1 and 2 reprents the inductor with N=4 and N=3 respectively. We can see that inductance value is increasing with higher number of turns as inductance is directly proportional to the number of turns.

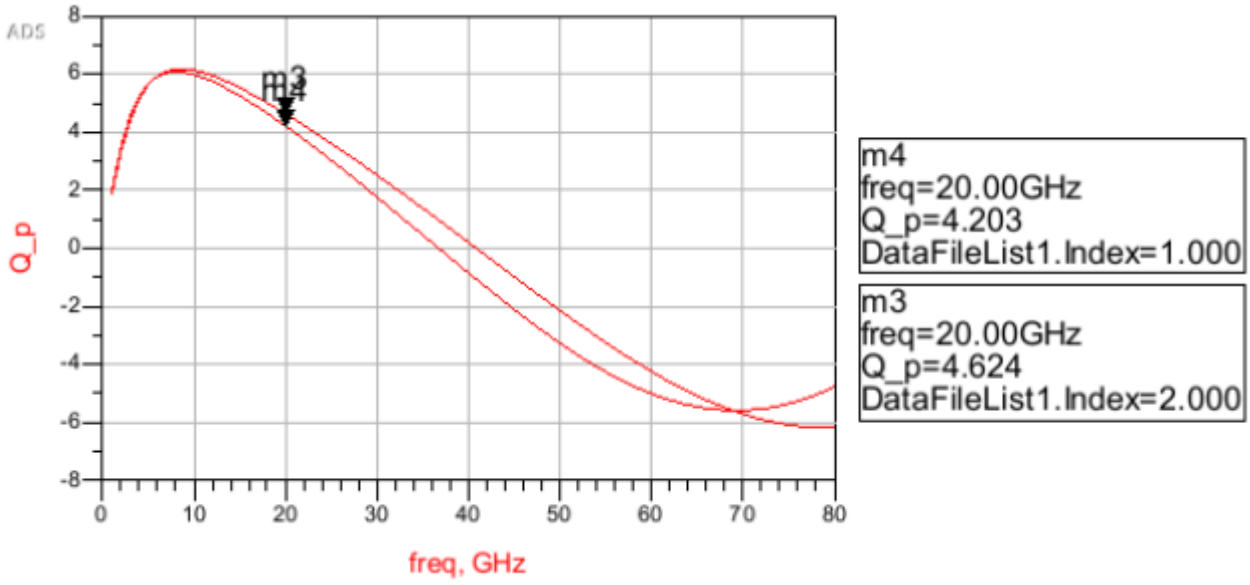
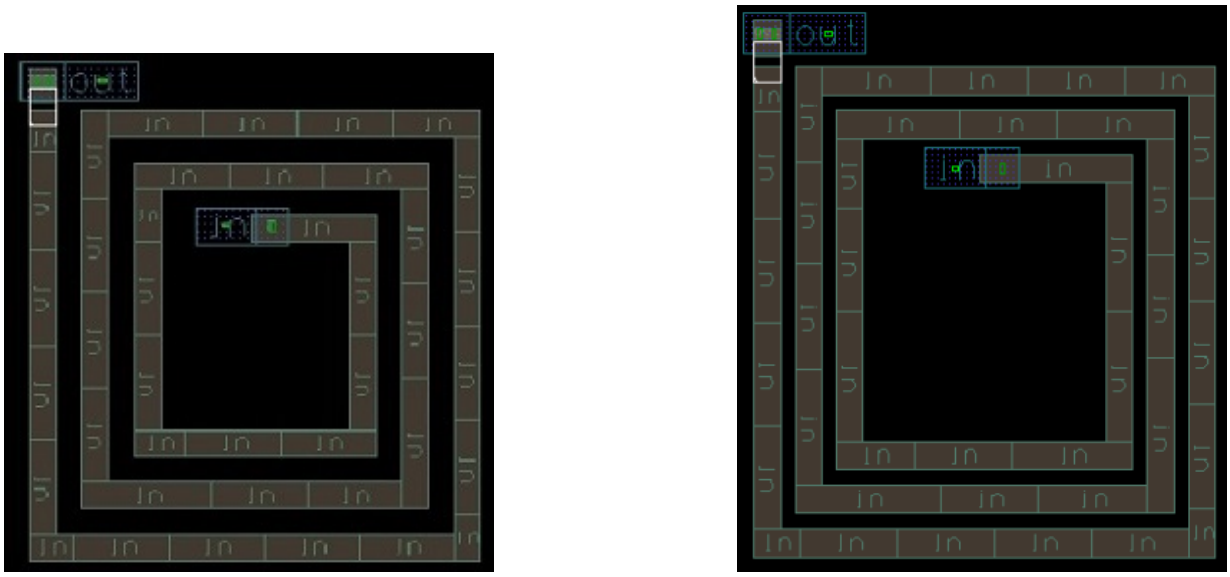


Figure 8.5: Quality factor variation with number of turns

As shown in Figure 8.5, the quality factor decreases as the number of tunrs increases. Because of the smaller inner diameter, eddy current effect will be more. As a result, quality factor decreases with increase in the number of turns. This is because the length and series resistance will increase as we go for higher turns and as a result due to higher resistance quality factor decreases.

In other words, for smaller number of turns since the inner diameter is large, the eddy current effect decreases and the quality factor increases.

8.3 Effect of varying space between tracks keeping the Area constant



(a) (b)

Figure 8.6: Layout having(a) S=5.5μm,(b) S=3μm, fixed N and W, d_{out}=95μm

Simulation results :

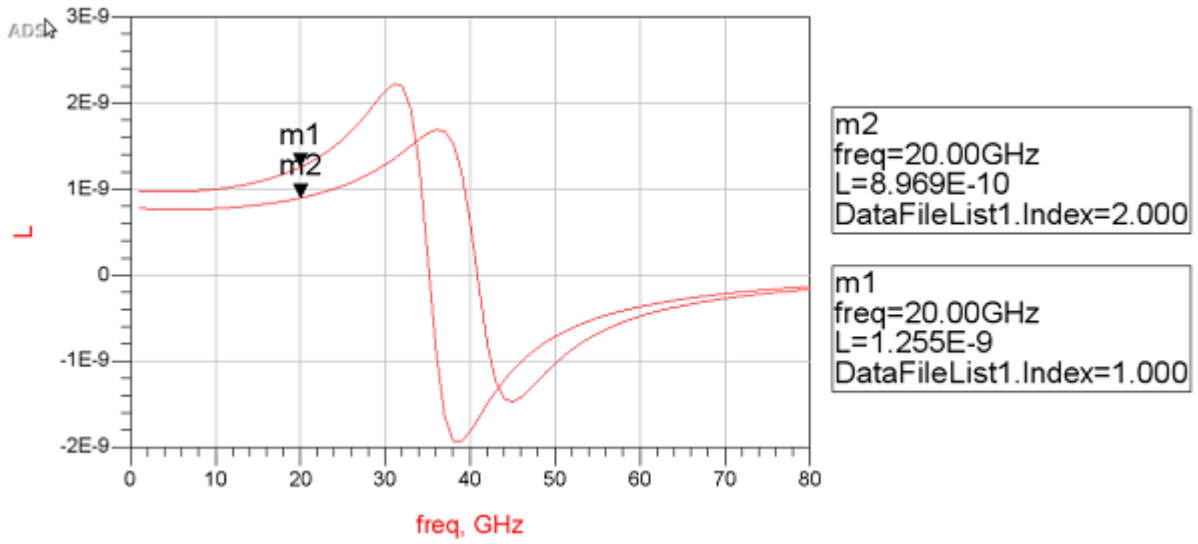


Figure 8.7: Inductance variation with spacing

Here in Figure 8.7 index 1 and 2 reprents the inductor with S=3μm and S=5.5μm respectively. We can see that inductance value is increasing with decreased spacing between turns since mutual inductance increases between turns.

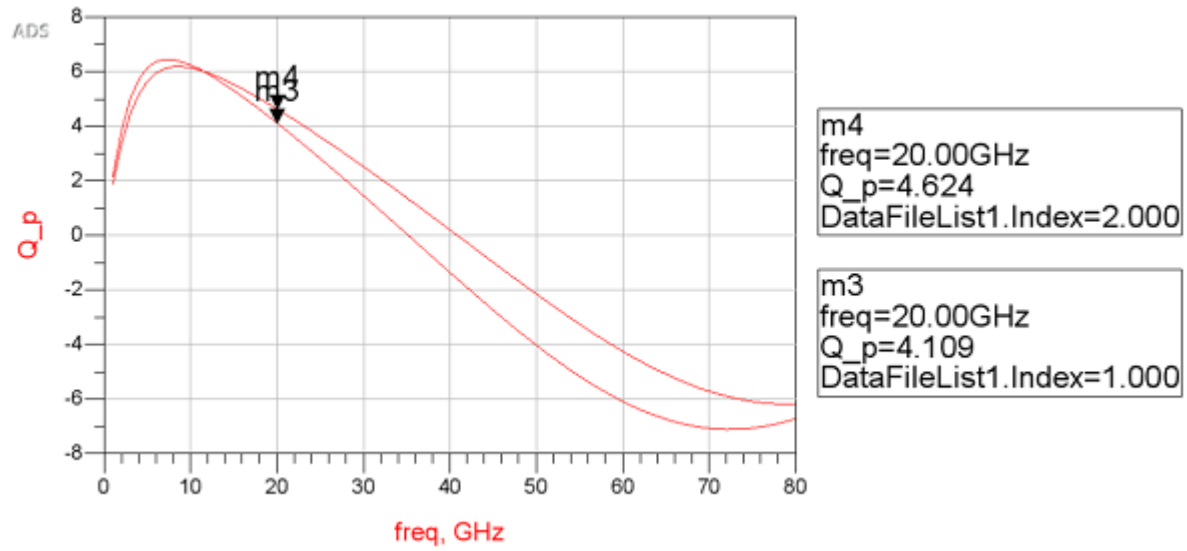
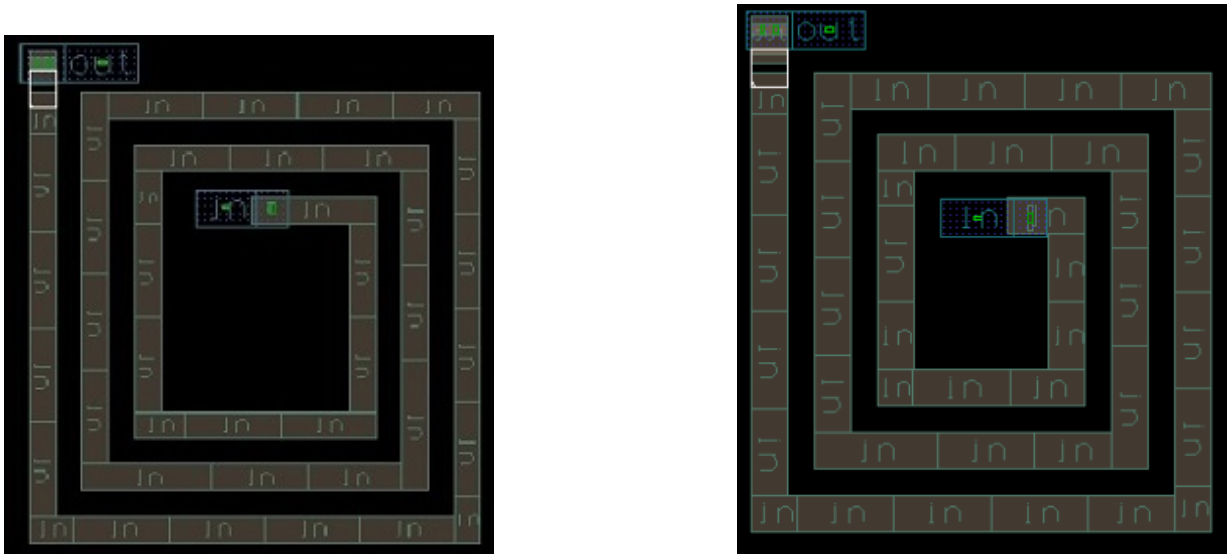


Figure 8.8: Quality factor variation with spacing

As shown in Figure 8.8, the quality factor decreases as the spacing between tracks decreases. This is because the length and series resistance will increase as we go for lower spacing and as a result due to higher resistance quality factor decreases.The same effect is on resonant frequency.

8.4 Effect of varying width of tracks keeping the Area constant



(a) (b)

Figure 8.9: Layout having(a) W=5.5μm,(b) W=7.5μm, fixed N and S, d_{out}=95μm

Simulation results :

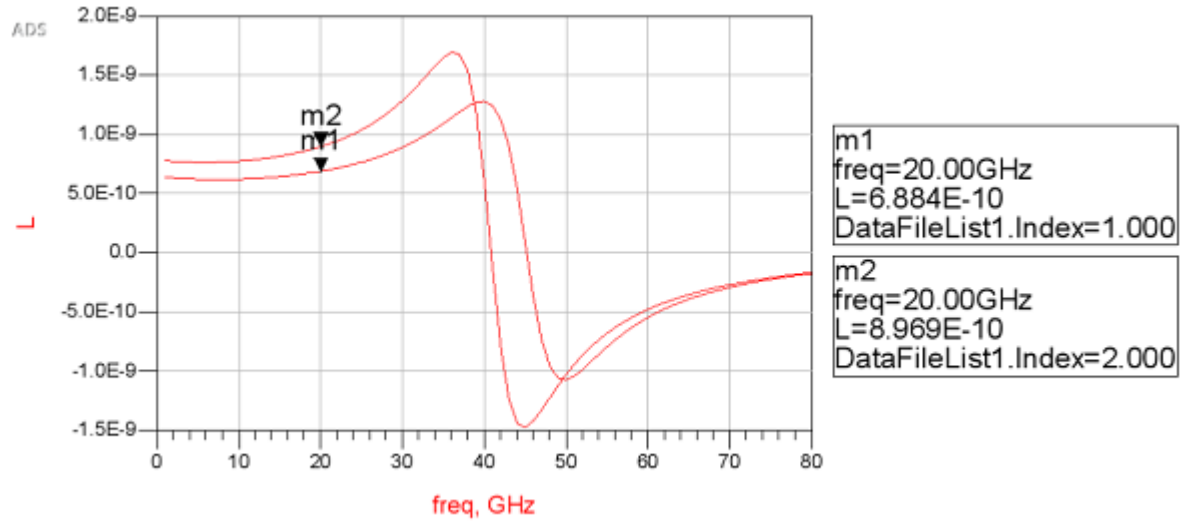


Figure 8.10: Inductance variation with track width

Here in Figure 8.10, index 1 and 2 reprents the inductor with W=7.5μm and W=5.5μm respectively. We can see that inductance value is decreasing with larger width. Because for the same area if we try to increase the width keeping the N and S constant, inner diameter has to be decreased, Which results in higher eddy current effect.Thus inductance will be less for larger width.

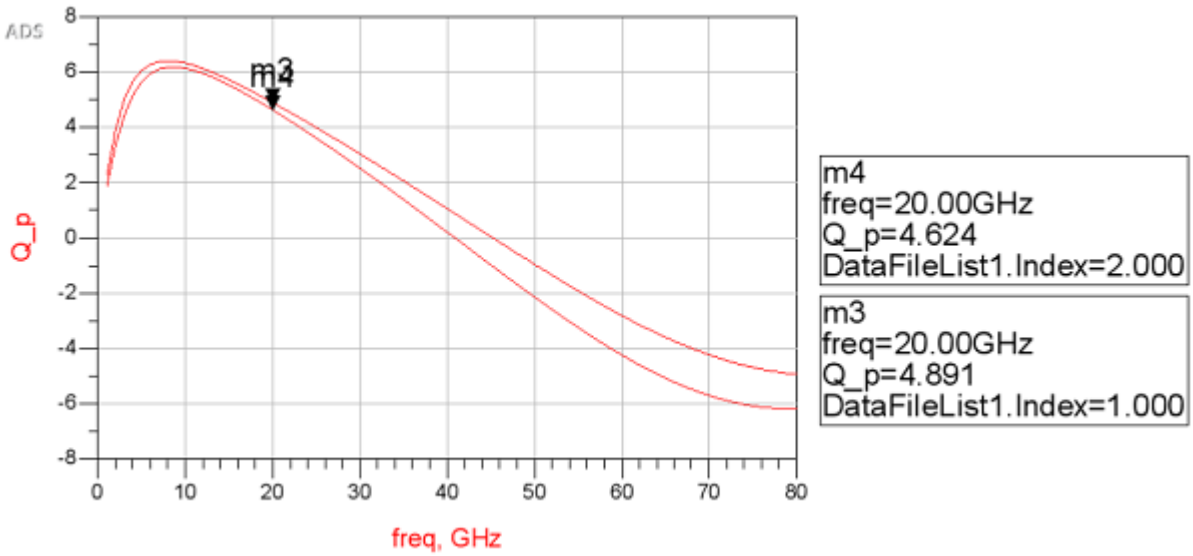


Figure 8.11: Quality factor variation with track width

As shown in Figure 8.11, the quality factor increases as the width increases. This is because for larger width the series resistnace is low. And hence the quaity factor and resonant frequency will be higher for larger width having the same area.

8.5 Result summary for constant area

- **W=5.5 µm , S=5.5 µm**

No. of Turns	Din [µm]	L [nH]	Q	Fres [GHz]
3	40	0.89	4.624	40-41
4	18	1.1	4.203	36.5-37

- **N=3, W=5.5 µm**

Spacing between Tracks [µm]	Din [µm]	L [nH]	Q	Fres [GHz]
5.5	40	0.89	4.624	40-41
3	50	1.25	4.109	35.5-36

- **N=3 , S=5.5 µm**

Width of Tracks [µm]	Din [µm]	L [nH]	Q	Fres [GHz]
5.5	40	0.89	4.624	40-41
7.5	28	0.68	4.891	45-45.5

Figure 8.12: Simulation result summary for constant area

From the above observation we can say that there will always be a trade off between inductance and quality factor or resonant frequecy.

There may be a case when there is no restriction on area usage. To understand the parameter variation in this situation I have done simulations and its summary is given below.The innner diameter is kept constant of 40μm.

Simulation frequency = 1GHz to 80GHz

Simulation Type = S parameter simulation

Inductor topology = Planar Square Integrated inductor(Single layered)

Comparison Frequency = 20GHz

No. of Turns	L [nH]	Q	Fres [GHz]
2	0.32	6.904	76-77
3	0.89	4.624	40-41
4	2.8	1.742	25-25.5

Spacing between tracks [µm]	L [nH]	Q	Fres [GHz]
2.5	0.91	5.195	42-42.5
5.5	0.89	4.624	41-41.5
8.5	1.02	3.982	38-39

Width of Tracks [µm]	L [nH]	Q	Fres [GHz]
3	0.86	5.175	45-45.5
5.5	0.89	4.624	40-41
7	0.94	4.023	37.5-38

Inner Diameter [µm]	L [nH]	Q	Fres [GHz]
12	0.34	6.956	77-78
24.5	0.57	6.036	55-56
40	0.89	4.624	40-41

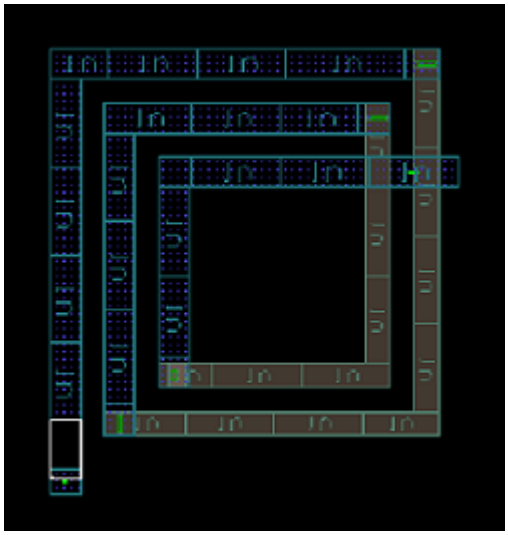
Figure 8.13: Simulation result summary for inconstant area

8.6 Some advanced layouts

Apart from the starndard spiral inductors, one can design alternative patterns by varying layout parameters or by changing metal layer (by changing spiral pattern) configuration in order to achieve the desired figure of merits like quality factor and resonant frquency.Some of the advanced designs and theiir simulation results are shown below.

8.6.1 Novel inductor

In this topology each turn of inductor covers two metal layers as shown in Figure 8.14. when the space available on the top is less one can go with this type of design.



- Number of turns N = 3
- Number of metal layers used = 2
- Inner diameter $d_{in} = 40\mu$m
- Specific Spacing between tracks and width

Figure 8.14: Novel Layout

On a typical spiral inductors, the number of turns having same and opposite current flow are mostly same as showed in Figure 8.15 and therefore the contribution from mutual inductance towards the total inductance value is either negligible or even negative.

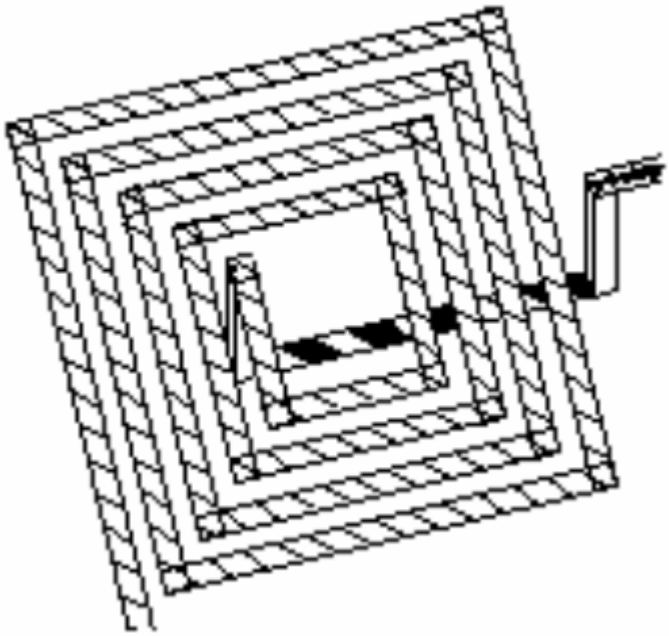


Figure 8.15: current flow in typical spiral inductor[8]

In the case of the proposed structure however, the contribution from mutual inductance towards the total inductance value is significant and always positive. The current flow is showed in Figure 8.16.

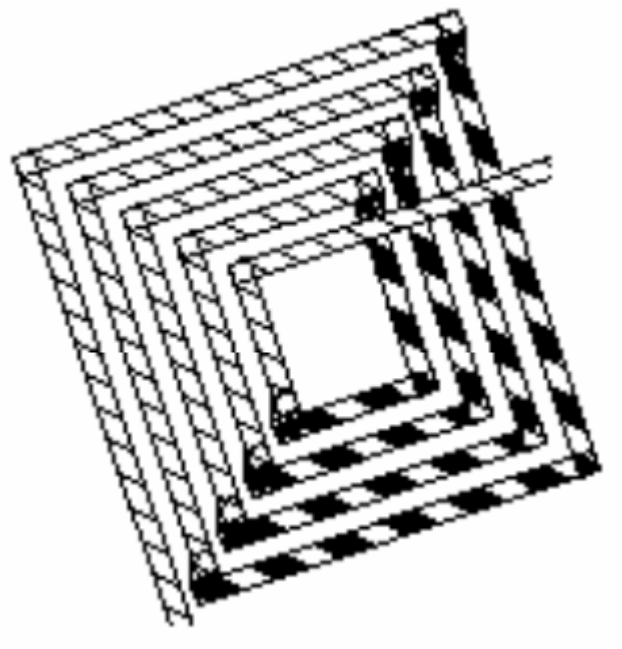


Figure 8.16: Current flow in novel inductor[8]

The advantages are reduced substrate losses, higher qualoty factor for a fixed size or fixed inductance specification which can be seen in Figure 8.17.

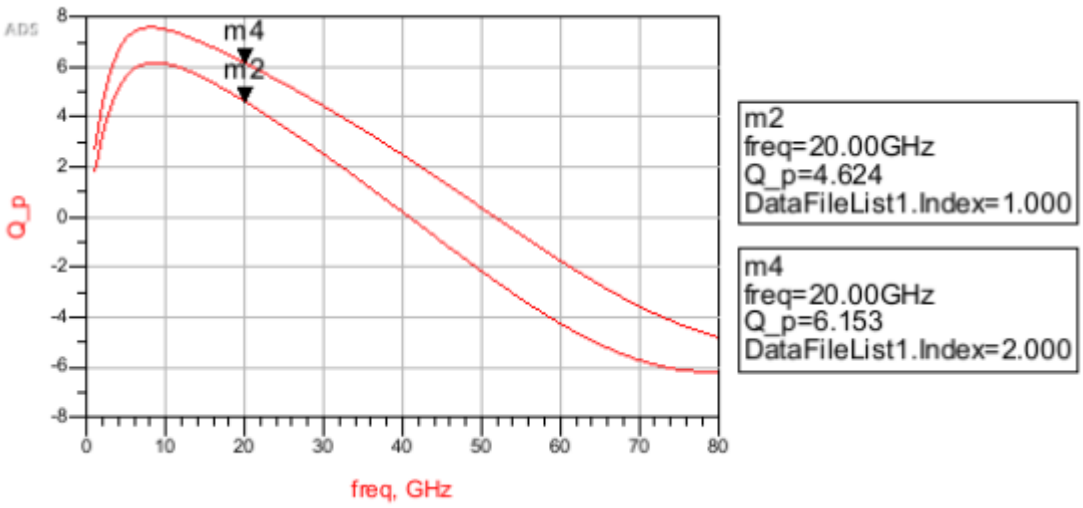
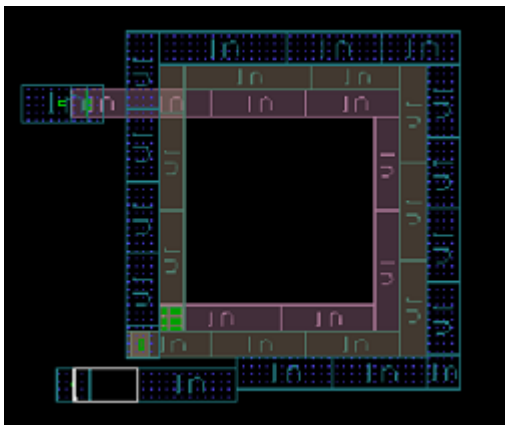


Figure 8.17: Comparison between Q of typical spiral and novel inductor

8.6.2 3D inductor

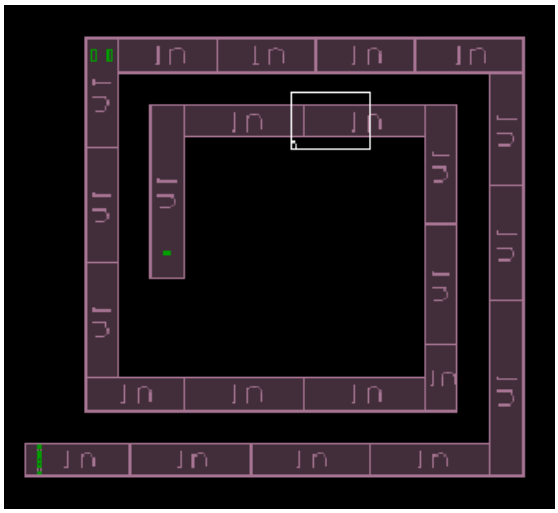
The layout showed in Figure 8.18 is generally called 3D inductor as each turn covers only one metal layer and are not stacked on each other.



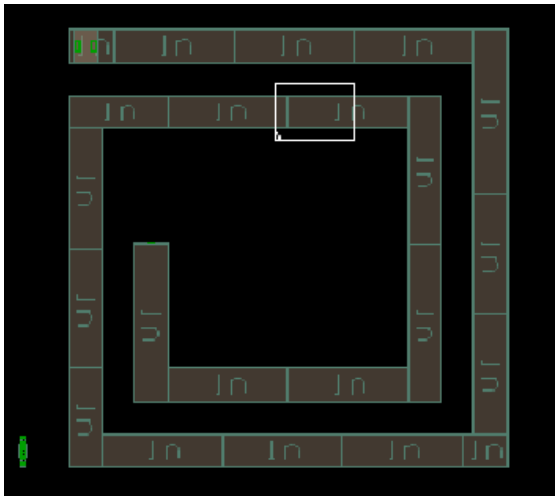
- Number of turns N = 3
- Number of metal layers used = 2
- Inner diameter $d_{in} = 40\mu$m
- Specific Spacing between tracks and width

Figure 8.18: 3D Inductor Layout

8.6.3 Multilevel Inductor

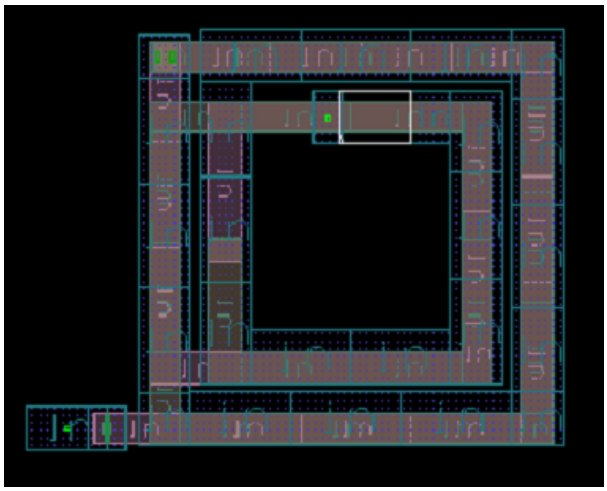


(a)



(b)

(c)



(d)

Figure 8.19: (a) lower most metal layer (b) Middle metal layer (c) Top most layer of three level inductor (d)Whole layout of multilevel inductor

The layout parameters are: Inner diameter $d_{in} = 40\mu$m

Specific Spacing between tracks and width

Number of turns N = 3

Number of metal layers used = 2

Chapter 9

Conclusion

The dynamic growth in wireless and RF portable electronics has driven the need of high performance on chip passive components. In this work a physical lumped model is represented to understand the characteristics of an on-chip inductor. we have presented three simple, approximate expressions for spiral inductors having different geometries. Various inductors have been designed and simulated. These results have been proven in ADS software for different inductors having different layout parameter values. A statistical study for a large number of different inductors was also performed.

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