Comparative Analysis And Evaluation Of Different CMOS Technologies

Submitted By

Ocean Godre

16MECV16

Department of Electronics & Communication Engineering
Institute of Technology, Nirma University
Ahmedabad-382481
May - 2018

Comparative Analysis And Evaluation Of Different CMOS Technologies

A Major Project Report

Submitted in Fulfillment of the Requirements
for the degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN

By

Ocean Godre (16MECV16)

Internal Guide	**External Guide**
Dr.N.M Devashrayee	Mahaveer Saptasagar
Professor, Nirma University	Staff Design Engg., ARM-Bangalore

Department of Electronics & Communication Engineering
Institute of Technology, Nirma University
Ahmedabad-382481

Certificate

This is to certify that The Major Project Report entitled **"Comparative Analysis And Evaluation Of Different CMOS Technologies"** submitted by **Ocean Godre** (**16MECV16**) in the partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design, Nirma University, is the record of work carried out by him under my supervision and guidance. The work submitted in our opinion has reached a level required for being accepted for the examination.

Prof./Dr. N.M. Devashryee
Guide and Professor,
Coordinator M.Tech - VLSI,
Institute of Technology,
Nirma University, Ahmedabad

Prof./Dr. D.K. Kothari
Professor and Head,
EC Department,
Institute of Technology,
Nirma University, Ahmedabad

Dr. Alka Mahajan
Director,
Institute of Technology,
Nirma University, Ahmedabad

Declaration

This is to certify that

1. The thesis comprises my original work towards the degree of Master of Technology in Electronics and Communication (VLSI Design) at Nirma University and has not been submitted elsewhere for a degree.
2. Due acknowledgement has been made in the text to all other material used.

- Ocean Godre (16MECV16)

Acknowledgment

I would like to thank Nirma University and ARM Embedded Technologies for providing this internship training. Let me take the opportunity to express my gratitude to my internal guide Dr.N.M Devashrayee ,manager Mahaveer Saptasagar and mentor Rakshith Chikkana for their suggestion and support. I extend my sincere thanks to Akhtar Alam and Sunnith Shrivastav for their help, guidance and constant encouragement during the training, ramping me up for my project work and inspiring me to put my best efforts.I would like to express my gratitude towards my colleagues and many who have rendered their help for various trainings , both explicitly and implicitly.

- Ocean Godre (16MECV16)

Abstract

Over the past decades perpetual shrinking of devices and circuits has led to semiconductor product improvements. A paralleling trend is that process variations and intra-die variability increase with each technology node and controlling the manufacturing process is very difficult. these fluctuations cause device and circuit characteristics to deviate from design goals and introduce significant device-to-device variability.The decrease in size of CMOS transistors leads to miniaturization of wires connecting these devices. However, there is a steep rise in the current density across integrated circuit. The increased current density eventually raises concern that VLSI chip reliability may be adversely impacted due to EM induced failures in the interconnects.Also,increasing design complexity, tighter design cycle time and performance requirements of advanced nanometer VLSI designs have made power/performance/area estimations at an early design phase critical design steps. So, accurate modelling of these early estimations, process variations and reliability issues has become critical to both foundries and circuit designers that seek optimal PPA balance.

To address time to market issue FOM (figure of merit) analysis is performed on different CMOS process which gives performance and leakage estimations at different PVT's ,VT/CL's very early in the design cycle. The impact of process and voltage variations has been analysed by running monte-carlo simulations on different technology nodes. Also, cell level variation is performed using regressive hspice simulations which gives us a estimate of manufacturing yield. Reliability analysis of different cells is performed with emphasis on electromigration estimation in power and signal lines. EM checks are performed to identify which cells satisfy the foundry EM and power on hours requirement.

Contents

Certificate **2**
Declaration 4
Acknowledgment 6
Abstract 8

Index **11**

List of Figures **11**

1 Introduction **14**

2 Early Estimations **16**
2.1 FOM(Figure Of Merit Analysis) 16
2.2 Deliverables 17
2.3 FOM Procedure 19
2.3.1 Parasitic Extraction 21
2.3.2 Extraction Flow 22
2.3.3 Overlay Analysis 23
2.3.4 Layout Proximity Effects 23
2.4 FOM Sample Results 25
2.5 Early Benchmarking 26

2.5.1 Early Benchmarking Results 27

3 Variation Analysis **28**

3.1 Types of Variations 28

3.1.1 Environmental,Temporal and Spatial 28

3.1.2 Systematic And Random Variations 29

3.2 Common Sources Of Process Variations 30

3.2.1 Lithographic variations 30

3.2.2 Random dopant fluctuation 31

3.2.3 Well-proximity effect 31

3.3 Variation Analysis Procedure 33

3.3.1 Vt(Effective Threshold) Calculation 33

3.3.2 Sample Vteff Results 34

3.3.3 Variation Between Different Domains 35

3.3.4 Cell Level Variation Using Solido 36

3.3.4.1 HSMC 38

4 Reliabilty Analysis **40**

4.1 Electromigration(EM) 40

4.1.1 Electromigration Flow 43

4.1.2 Electromigration Sample Results 44

5 Conclusion And Future Work **45**

5.1 Conclusion 45

5.2 Future Work 46

List of Figures

2.1 Trend Across Different Architectures 18

2.2 FOM Procedure 19

2.3 Table of expected characteristics of cells after analysis 20

2.4 Types Of Parasitics 21

2.5 Extraction Flow 22

2.6 LOD effect 23

2.7 Extraction Flow 24

2.8 Sample Overlay Results 24

2.9 FOM Results 25

2.10 Early Benchmarking Flow 26

2.11 Early Benchmarking Results 27

3.1 Illustration Of Different Process Variations. 29

3.2 Random Dopant Fluctuation. 31

3.3 Well Proximity Effect.High-energy dopant ions scatter at the well photoresist edge during well ion implantation and are reflected into the channel before the gate is formed 32

3.4 Threshold Voltage Calculation. 33

3.5 Vteff Flow 34

3.6 Sample Vt Results 34

3.7 Voltage Domain Variation 35

3.8 Sigma Coverage 37

3.9 Solido Flow 39

3.10 HSMC Results 39

4.1 Thermal Acceleration Loop During Electromigration 42

4.2 Electromigration Flow 43

4.3 EM Sample Results 44

Chapter 1

Introduction

Power consumption, delay and yield are on a top priority in modern integrated circuit (IC) design industry. A very good solution has been provided by the scaling to obtain low power dissipation, high packing density, reduced delay factor scaling had proved to be absolutely better and full proof method, scaling also provide better option for the performance improvement in the circuits. So, the major challenges become the function of gate oxide thickness, channel resistance, effective channel length and width of channel and threshold voltage for process variation. The continuous technology scaling gives tremendous performance enhancement but on the other hand, process variability in device parameters like channel length, channel width, threshold voltage, gate-oxide thickness and source-drain resistance has became major challenge.

Also ,the scaling down of the fabrication technology along with the race to meet time-to-market constraint results in hiccups in design and also susceptibility levels that reduce process yield and reliability.

The fixes required will again consume a lot of time.For this early PPA estimations during inital design phase can help to diagnose hiccups and will enable designers to meet the TTM.

Chapter 2 introduces two methodologies used for early estimations of PPA of particular process,the first is called FOM analysis and the second is Early Benchmarking.
Chapter 3 covers the impact of process and voltage variations on performance.Also cell level variation is analysed with the hrlp of solido tool which performs regressive monte-carlo simulations to estimate yield.
Chapter 4 covers the reliability analyses.EM checks are performed on different cells to identify whether they can pass the foundry EM requirements.

Chapter 2

Early Estimations

This chapter includes the methodology for early analysis of different CMOS process which effectively helps to reduce the design cycle time.

2.1 FOM(Figure Of Merit Analysis)

FOM analysis includes the following :

- Quantifying performance vs leakage tradeoff's without having resort to design cross sections.
- Calculation of average performance and leakage of different processes between same or different foundries:
  - Cell Level
  - Device Level
- Early estimation of the behavior of a particular process under different operation conditions
- Analysis of advantages and shortcomings of a process during early stages of design flow.

- Reduces debugging time.
- Benchmarking is generally used to deliver the actual results.

2.2 Deliverables

- Pre-library analysis and correlation with final implementation.
- Within process trend checks :
  - VT's
  - CL's
  - Voltage
  - Temperature
  - Architecture(Track,9Track)
  - Process Corners
- Between process trend checks.
- Autogenerate and validate FOM input data.

Figure 2.1: Trend Across Different Architectures

2.3 FOM Procedure

Below is the block diagram that depicts how the FOM analysis is carried out :

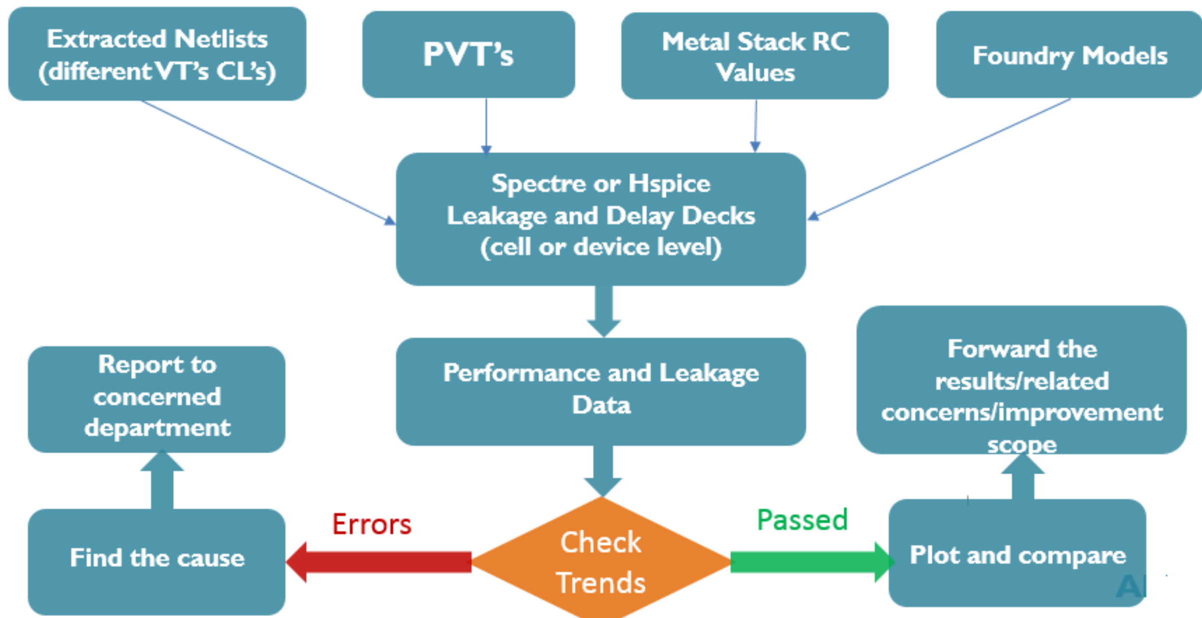


Figure 2.2: FOM Procedure

The general trend for expected characteristics of the cells after FOM analysis is given below

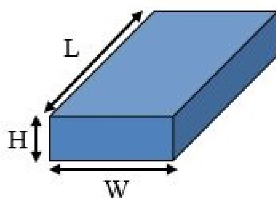
Characteristic	Performance	Leakage
Supply voltage Decreases	Decreases	Decreases
Channel length increases	Decreases	Decreases
Delay temperature increases	Increases	Constant
Leak temperature increases	Constant	Increases
Threshold voltage increases	Decreases	Decreases
Cornertype (corner, global, typical)	Increases	Decreases
Operating temperature decreases	Decreases	Decreases

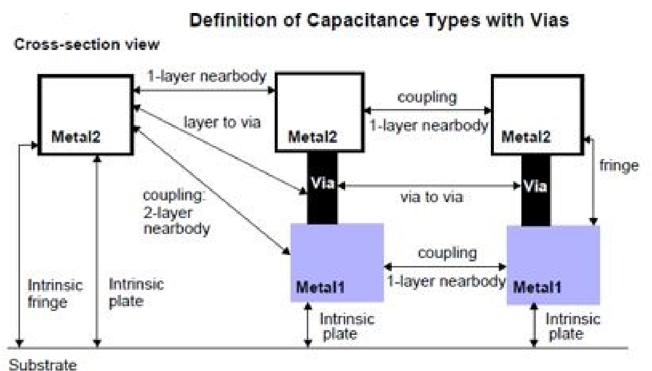
Figure 2.3: Table of expected characteristics of cells after analysis

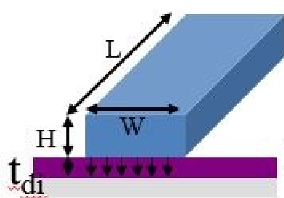
2.3.1 Parasitic Extraction

This section covers the flow for parasitic extraction to obtain the netlists used in the FOM flow. Parasitics give rise to a whole set of signal integrity issues as their scaling behavior differs from the active devices.

The major purpose of parasitic extraction is to create an accurate model of the circuit, so that detailed simulations can emulate actual digital and analog circuit responses.







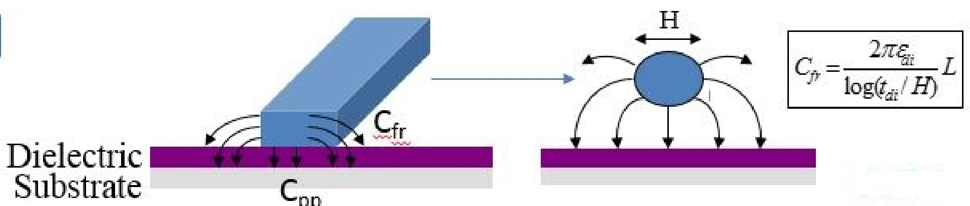


Figure 2.4: Types Of Parasitics

2.3.2 Extraction Flow

The below block diagram shows the Parasitic Extraction Flow:

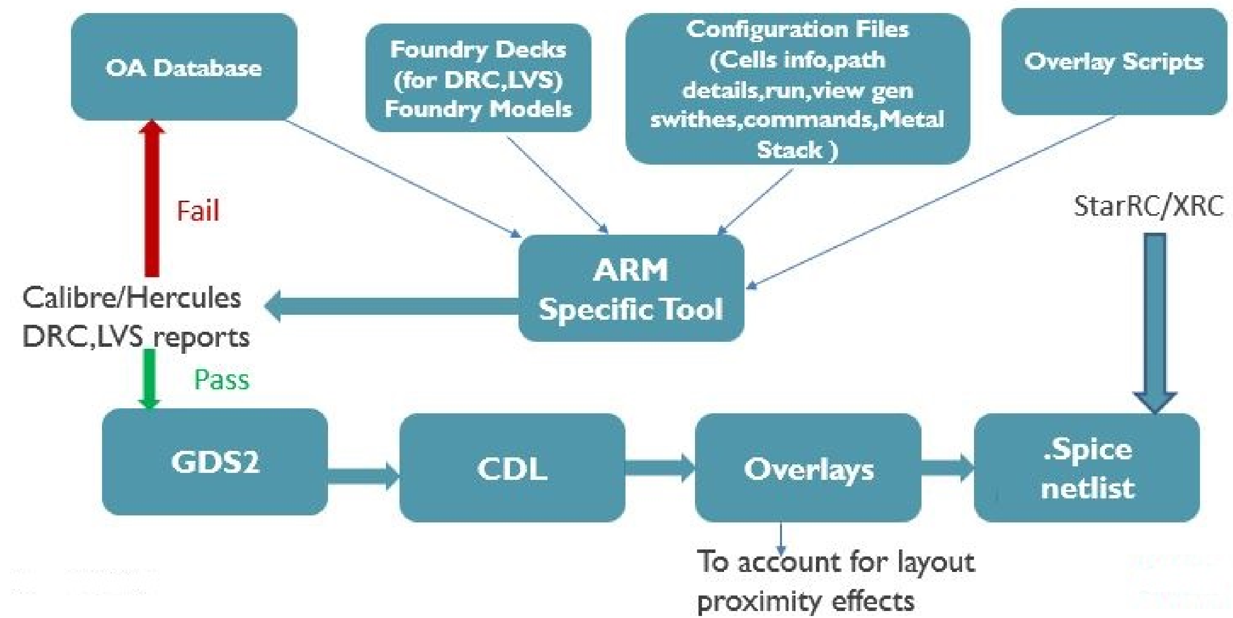


Figure 2.5: Extraction Flow

The netlists obtained from extraction are used as inputs to FOM analysis.

2.3.3 Overlay Analysis

This section will cover how the layout proximity effects (LPE) impact the performance and leakage of a design.Overlay analysis is done to account for these impacts of LPE on the actual silicon.

2.3.4 Layout Proximity Effects

- Unexpected mobility/Id/Vt variations making the circuit performance unpredictable.
- LOD

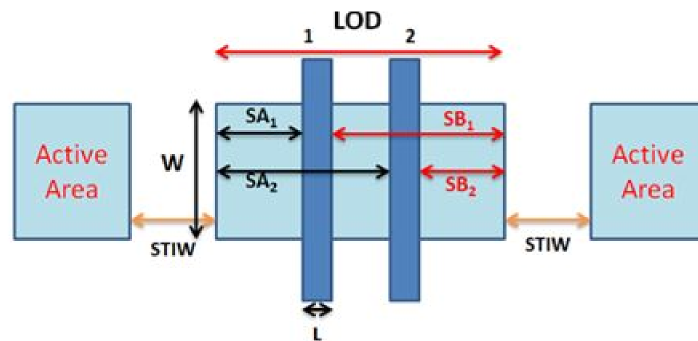


Figure 2.6: LOD effect

- **Effects**:
  - Can effect drive currents by 10
  - Compressive stress:NMOS mobility decreases with decrease in SA/SB ratio.
- WPE(well proximity effect)

WPE(well proximity effect)

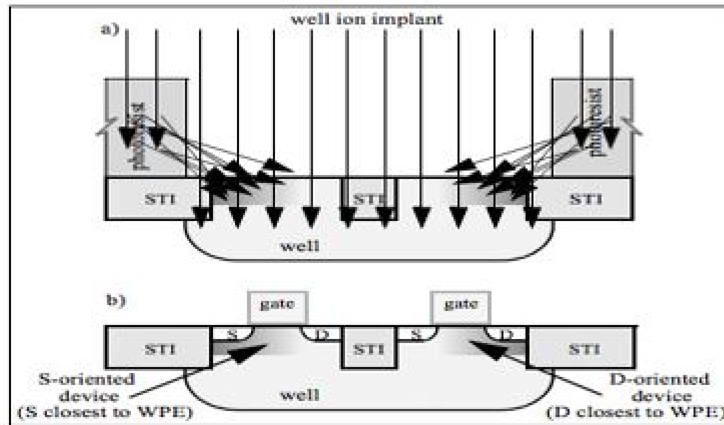


Figure 2.7: Extraction Flow

- **Effects**:Can shift Vt value in tens of mV.

OD Spacing				
Idsat	Dummy OD	Min(mA/um)	Max(mA/um)	Variation %
NMOS	With	0.4852	0.51371	5.88
	W/O	0.47707	0.50599	6.06
PMOS	With	0.20345	0.22089	8.57
	W/O	0.20663	0.22479	8.79

Overall Impact					
Process	Vth %	Idsat %	Ioff %	Delay %	Leakage %
40nm	2.88	8.3	20	15.39	30.48
28nm	3.91	11.5	2.18	3.73	0.163

Figure 2.8: Sample Overlay Results

2.4 FOM Sample Results

The below Table shows the comparison between 2 processes X and Y for different voltage domains ,channel lengths and different implants.

It can be observed that process X is around 7%-17% better in performance and 1.06x-2.00x leaky than process Y.

Ratio: [11nm Process X/ Process Y]						
Voltage Domain	VT	CL	Corner			
			Global-Corner		Typical - Corner	
			Performance	Leakage	Performance	Leakage
			SS/m40c	FF/125c	TT/25c	TT/25c
0.6V	LVT	C14	1.17	1.58	1.11	1.92
		C16	1.17	1.62	1.11	1.99
	RVT	C14	1.12	1.57	1.08	1.91
		C16	1.12	1.61	1.08	1.98
0.8V	LVT	C14	1.09	1.56	1.06	1.89
		C16	1.09	1.61	1.06	1.96
	RVT	C14	1.07	1.55	1.05	1.87
		C16	1.07	1.6	1.05	1.95

Figure 2.9: FOM Results

2.5 Early Benchmarking

In this section a improved methodology for perfomance estimates of a particular process is shown.It includes sequential elements such as flops and a combinational circuit between them derived from the becnchmarking result for a particular controller/processor core.The aim is to calculate the maximum frequency a process can support at different VT/CL/Arch/PVT's. The flow is shown in the following 2 figure :

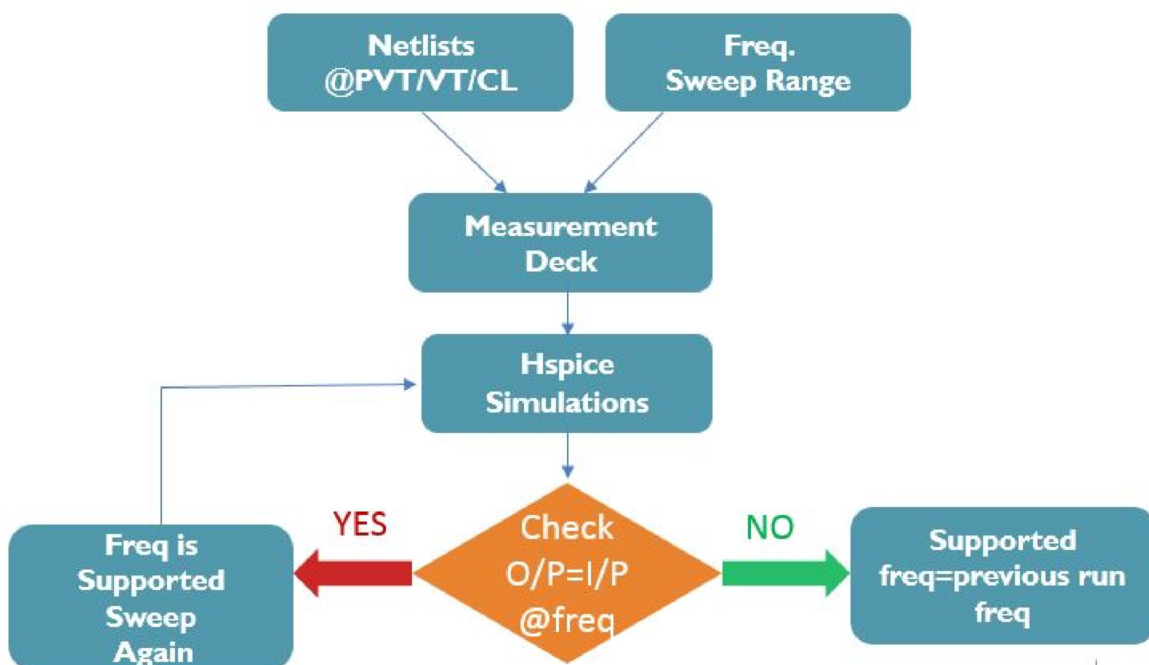


Figure 2.10: Early Benchmarking Flow

2.5.1 Early Benchmarking Results

The table below shows the results between actual and early benchmarking.By further improvements in combinational circuit choice we may see much better resemblance with the actual results .

40nm M-Core Results @TT/vnom/85c				
VT/CL	Track	Freq @Actual Benchmarking	Freq @Early Benchmarking	Ratio Early/Actual
LVT_C40	7T	398 Mhz	445 Mhz	1.12
	9T	514 Mhz	550 Mhz	1.07
RVT_C40	7T	314 Mhz	360 Mhz	1.15
	9T	363 Mhz	392 Mhz	1.08

Figure 2.11: Early Benchmarking Results

Chapter 3

Variation Analysis

This chaper will highlight how different kinds of variations effect the performance and yield of a CMOS process. A methodology is explained to account for the effect of these variations using monte-carlo simulations on different cells. Cell level variations are also analysed using high sigma monte carlo simulation which give a estimation of yield .

3.1 Types of Variations

3.1.1 Environmental,Temporal and Spatial

Environmental variations consist of variability in the surrounding temperature, power supply voltage, and even cosmic radiation.
Temporal variations as the name suggests, refer to device performance change over periods of time ranging from nanoseconds, for self-heating effect, to seconds or hours, for the negative bias temperatureinstability (NBTI), to years, for dielectric material deterioration after repeated programming and erasing operations in flash memories.
Spatial variations,are performance differences among devices that depend on

the distances between the devices or the locations of the devices on a chip. Typical spatial variations, such as line width or film thickness non-uniformity, universally exist across lots, across wafers, across chips and dies, and between circuit blocks and devices. As a result, the circuit performance of chips from wafers produced with the same design and process over a period of manufacturing time will never be the same.

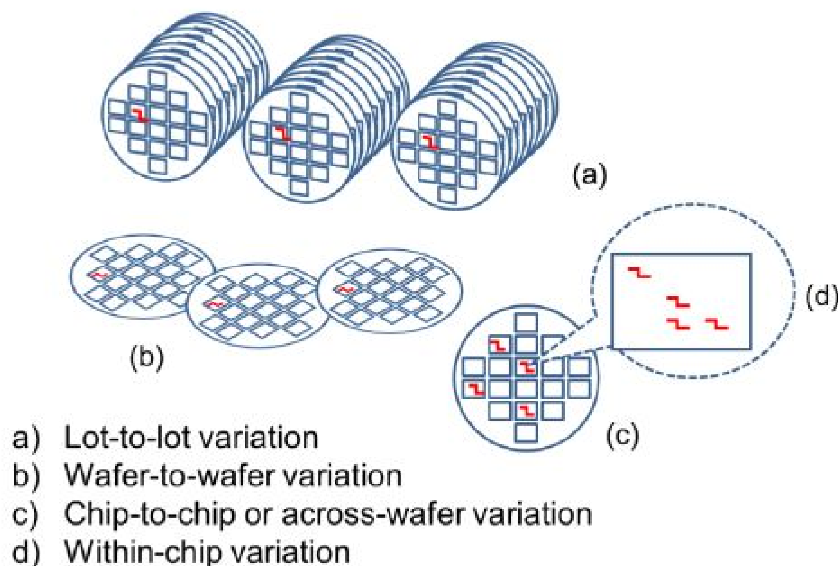


Figure 3.1: Illustration Of Different Process Variations.

3.1.2 Systematic And Random Variations

Systematic variations, also called deterministic variations, are repeatable deviations from nominal device characteristics depending on the device's spatial position on the die and on the wafer and/or the layout context surrounding the device being tested. Common sources of systematic variability include the non-ideality of the lithographic system, such as defocus, misalignment, and line-width roughness and various layout-dependent effects, such as WPE, optical proximity effects, strained silicon effects.

Random variations, or stochastic variations, are unpredictable components of device variability, such as non-uniformities resulting from random fluctuations in the fabrication process, microscopic fluctuations of the number and location of dopant atoms in the transistor channel,LER due to photoresist granularity, and atomic-scale oxide-thickness variation.

Systematic and random variations differ in how they impact device and circuit performance. Systematic spatial variation can cause large differences in performance among devices that are far apart on the die. From a modeling point of view, such an effect in the chips may directly contribute to the spatial correlation among transistors. Random variations, however, are usually treated as independent fluctuations at their corresponding spatial hierarchy level (lot level, wafer level, chip level, etc.).

3.2 Common Sources Of Process Variations

3.2.1 Lithographic variations

The uniformity of the printed feature sizes depends heavily on the control of the lithographic imaging system. It affects the two key requirements in integrated circuit manufacturing: the critical dimension (CD) and the overlay control. In a typical stepand- scan lithography stepper,the mask reticle and the wafer are simultaneously moving in opposite directions while a slit of light scans the whole mask and projects the image onto the wafer. Even tiny vibrations in the scanner system and variations of the movement speed of the wafer and reticle stage may lead to significant non-uniformities in the depth of focus (DOF) and the light-exposure dose. This can lead to non-uniformity of the critical dimension (CD) of printed lines and may vastly change the speed and leakage of CMOS

transistors.

3.2.2 Random dopant fluctuation

Random dopant fluctuation (RDF) refers to the random microscopic fluctuation of the number and location of dopant atoms in the MOSFET channel region. It causes fluctuations of the transistor electric parameters, such as the threshold voltage (Vt), short channel effect, and drain-induced barrier lowering (DIBL). With the gate CD scaling down to sub-100nm, the total number of dopant atoms under the gate is reduced to thousands or even hundreds,leading to significant variations in the threshold voltage and drive current.

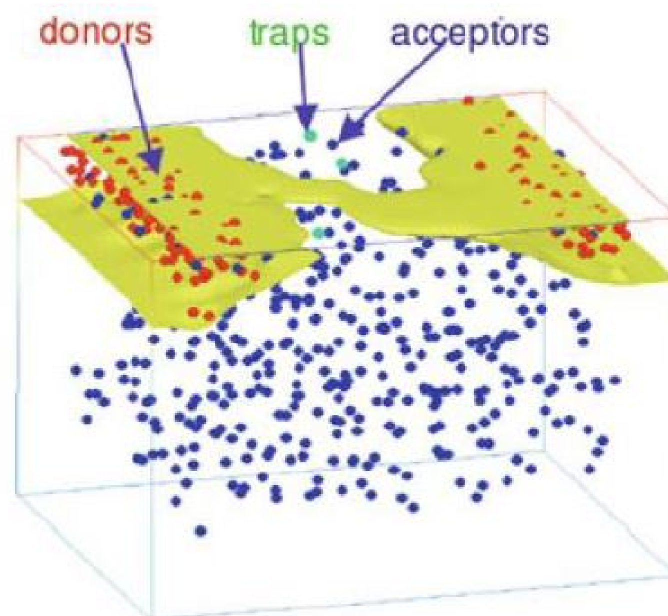


Figure 3.2: Random Dopant Fluctuation.

3.2.3 Well-proximity effect

The well-proximity effect is an important layout-dependent effect in the deep submicron manufacturing process. It originates from the lateral scattering of implantation ions during the well-implantation step. The incoming high-energy

ions collide with the edge of the photoresist on top of the shallow trench isolation (STI), and they get reflected into the channel area before the poly-silicon gate is actually formed. The closer the transistor gate is to the edge of the well, the higher the dopant concentration inside the channel. As a result, transistors with a smaller gate-to-STI distance will have higher threshold voltages.

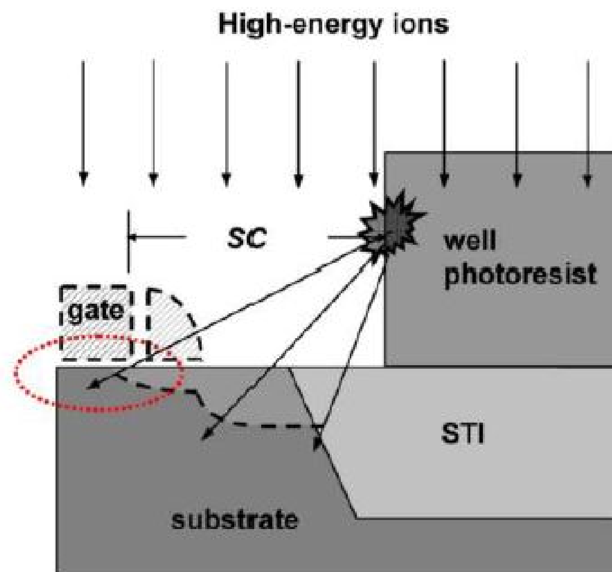


Figure 3.3: Well Proximity Effect.High-energy dopant ions scatter at the well photoresist edge during well ion implantation and are reflected into the channel before the gate is formed

3.3 Variation Analysis Procedure

This section covers the methodology for calculation of Vt and Variation between different domains.

3.3.1 Vt(Effective Threshold) Calculation

There are a number of methods to calculate the Vt out of which second derivative method is used here

Second derivative method is the most pessismistic method to calculate Vteff. It determines Vt as the gate voltage at which second derivative of current is maximum.

The method can we understood in the following figure :

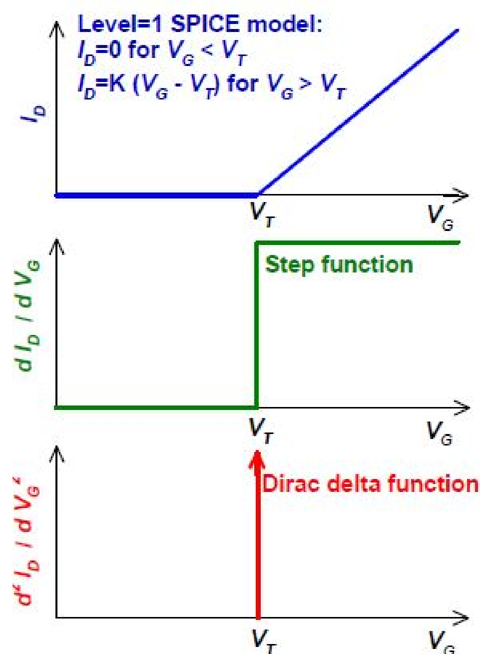


Figure 3.4: Threshold Voltage Calculation.

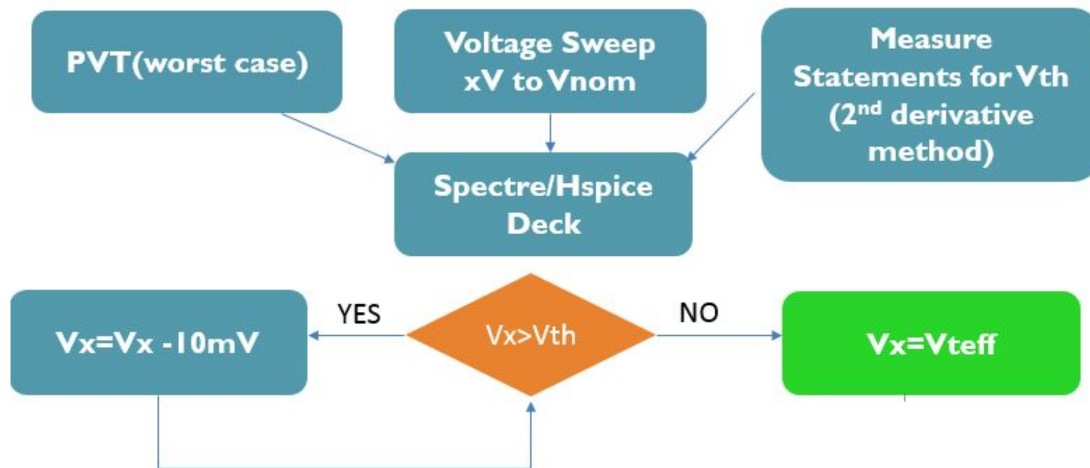


Figure 3.5: Vteff Flow

3.3.2 Sample Vteff Results

vsupply	processcorner	temperature	channellength	threshold	idsatnfet	idsatpfet	ioffnfet	ioffpfet	vtlingmnfet	vtlingmpfet
0.31	ss	-40	C30	ULVT	9.47E-06	6.15E-06	1.16E-09	7.28E-10	0.31	-0.31
0.32	ss	-40			1.17E-05	7.95E-06	1.22E-09	7.92E-10	0.32	-0.32
0.33	ss	-40			1.43E-05	1.01E-05	1.29E-09	8.60E-10	0.33	-0.33
0.34	ss	-40			1.72E-05	1.27E-05	1.35E-09	9.34E-10	0.34	-0.34
0.35	ss	-40			2.05E-05	1.57E-05	1.42E-09	1.01E-09	0.34	-0.35
0.36	ss	-40			2.43E-05	1.92E-05	1.49E-09	1.10E-09	0.34	-0.36
0.37	ss	-40			2.83E-05	2.32E-05	1.56E-09	1.19E-09	0.34	-0.37
0.38	ss	-40			3.28E-05	2.77E-05	1.64E-09	1.29E-09	0.34	-0.38
0.39	ss	-40			3.77E-05	3.27E-05	1.72E-09	1.40E-09	0.34	-0.39
0.4	ss	-40			4.29E-05	3.81E-05	1.81E-09	1.51E-09	0.34	-0.392

- 0.34V is the Vteff value for ULVT so supported domain can be ~0.40V.

Figure 3.6: Sample Vt Results

3.3.3 Variation Between Different Domains

For the variation between different domains monte-carlo simulations are performed at worst PVT on different cells at different voltage domains.The ratio of sigma values is taken.If the lower domain has not much increase in sigma then that domain can be used for that process thus saving the power.

The Voltage Variation tables is shown below :

Foundry X (w.r.t 0.90V Domain) (σ)					
Domain	Vjunc.	VT	INV	NAND	NOR
1.10V	0.99	ULVT	0.56	0.54	0.54
1.00V	0.9		0.72	0.7	0.71
0.90V	0.81		1	1	1
0.80V	0.72		1.59	1.64	1.63
0.70V	0.63		3.19	3.47	3.41
1.10V	0.99	LVT	0.57	0.56	0.52
1.00V	0.9		0.71	0.7	0.68
0.90V	0.81		1	1	1
0.80V	0.72		1.74	1.78	1.8
0.70V	0.63		4.28	4.6	4.73
1.10V	0.99	SVT	0.41	0.4	0.41
1.00V	0.9		0.6	0.59	0.59
0.90V	0.81		1	1	1
0.80V	0.72		2.13	2.19	2.23
0.70V	0.63		6.66	7.29	7.81
1.10V	0.99	HVT	0.31	0.3	0.32
1.00V	0.9		0.51	0.5	0.51
0.90V	0.81		1	1	1
0.80V	0.72		2.61	2.76	2.73
0.70V	0.63		10.91	13.14	12.79

Figure 3.7: Voltage Domain Variation

It can be observed from the below table that 0.7V and 0.8V domain suffers the highest variation.The domain that shows high sigma ratios will suffer very high delays and thus not recommended to be charcterized.So,a tradeoff between power and speed can be observed here.Using lower domain will help in power saving but will cause highest variation.

3.3.4 Cell Level Variation Using Solido

At advanced processes and low voltage, statistical variation has a big impact on standard cell delays and transition times – distributions skew from well-behaved Gaussian to extremely long tails. It is simply not sufficient to add a bit of margin for statistical variation or to use sloppy, inaccurate Monte Carlo techniques. To make libraries that are suited for low power design, it is essential to verify them thoroughly, and often to high-sigma, as many instances are placed on chips and they all need to work for a chip to work. Given the massive scope of standard cell verification and already exhausted CPUs and tool licenses, it is simply not feasible to do proper brute-force statistical analysis and meet production schedules.

Solido tool has effective and production-proven technology for accelerating statistical verification of standard cells .It is way faster, more accurate, and more resilient than traditional methods.

For example, a slow-slow global (SSG) corner typically bounds 3-sigma global variation for delays for nmos and pmos devices.. So what we really should be doing, if simulation were free, is running global and local statistical variation with 5K samples, and doing it at every PVT corner. That would actually be perfect information for 3-sigma designs, but it would take way too long to run. When targeting 4-sigma, as we often do for automotive parts or medical devices, it becomes even more impossible to do the right thing, as we need to run on the order of 1M samples to verify to 4-sigma correctly.

Solido Variation Designer delivers full statistical and PVT coverage with design-specific corners in just hundreds of simulations.

The main problems addressed by solido are :

- Non-Gaussian Distributions can be evaluated which are not practical with traditional monte-carlo simuations
- Provides estimate of full distribution
- Provides verifiable brute-force accurate high sigma results in just 1000's of simulations
  -4 sigma results are equivalent to 1 million simulations
  -6 sigma results are equivalent to 10 billion simulations

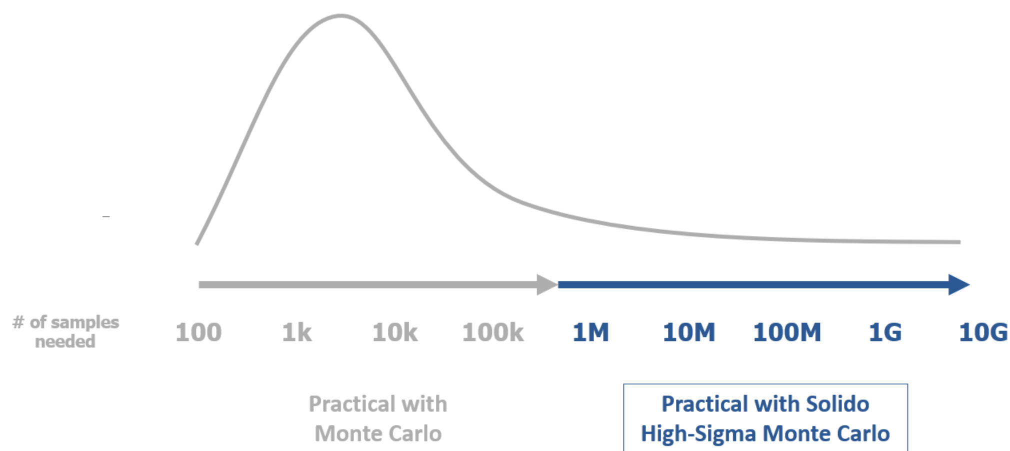


Figure 3.8: Sigma Coverage

Solido analysis is carried out in two stages :

- Worst PVT is found
- Regressive HSMC simulations are performed on worst PVT

3.3.4.1 HSMC

High-sigma parts are inherently difficult to verify because it is difficult to measure the effects of variation on high-sigma designs quickly and accurately. With only a few defects in a very large number of samples, Monte Carlo (MC) sampling takes prohibitively long to obtain accurate information in the extreme tail of the distribution where the defects occur. Other methods, such as extrapolating from fewer MC samples or importance sampling, have other drawbacks, such as long runtimes, poor accuracy, or that they are only effective for trivial examples and do not scale to the needs of production designs.
The result is that the actual sigma of high-sigma designs is often unknown, so designers add additional margin to compensate for this uncertainty. This in turn sacrifices power, performance, and area. Still, some designs may fail to meet their high-sigma goals, resulting in poor yields and expensive re-spins.

High-Sigma Monte Carlo (HSMC) is a advanced and production-proven technology for high-sigma analysis. HSMC includes technology that can do things we previously thought to be impossible like:

- Support trillions of samples: This gives HSMC the ability to deliver perfect Monte Carlo and SPICE verification to 7 sigma and beyond. Yes, it actually generates trillions of samples. And yes, it's still fast.
- Generate full PDFs: A single HSMC run can find not just the tail of the distribution with perfect Monte Carlo and SPICE accuracy, but the entire distribution, just as you would if you ran millions or billions of Monte Carlo samples in SPICE.

HSMC can be run for any measurement deck e.g delay , flop-margining etc.Below is the solido flow :

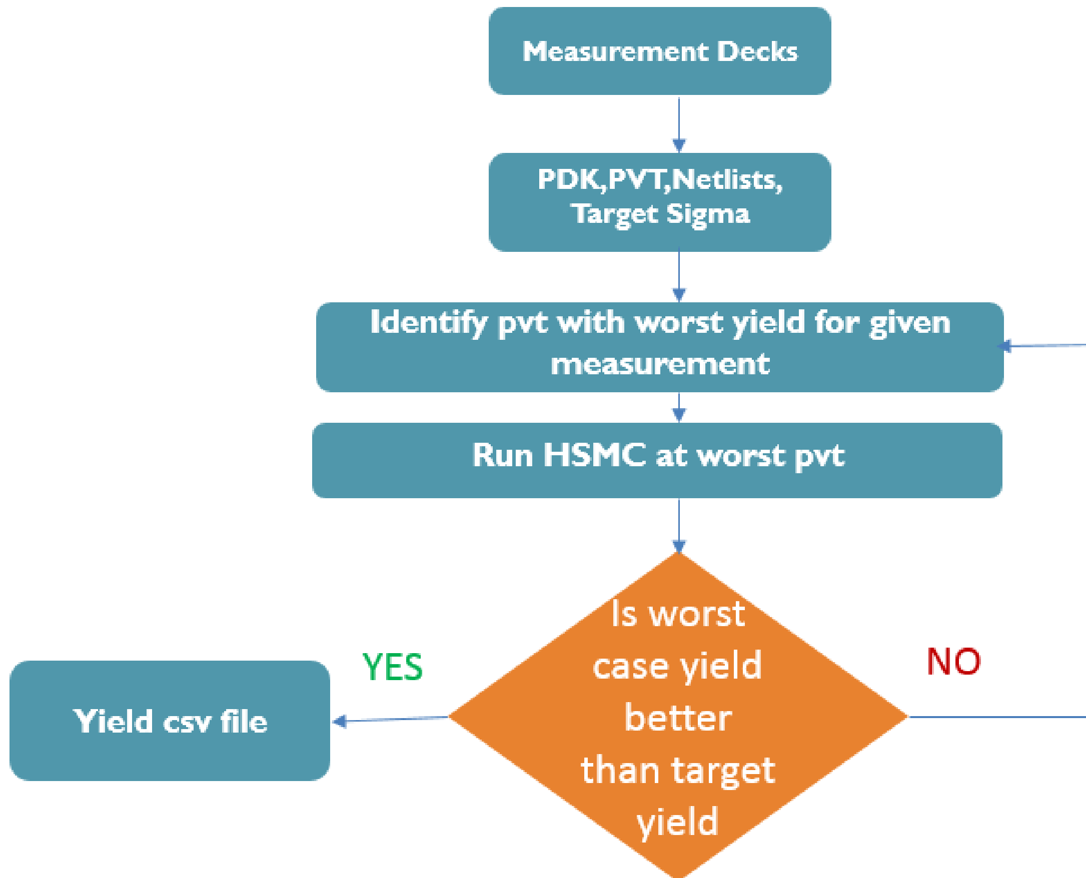


Figure 3.9: Solido Flow

HSMC			
FLOP	pvt	σ/yield	Pass/Fail
SDFF_flop1	fsg_cworst_0p6v_125c	4.1	Pass
SDFF_flop2	sfg_cworst_0p6v_125c	3.2	Fail
SDFF_flop3	sfg_cworst_0p6v_125c	4.8	Pass

Figure 3.10: HSMC Results

Chapter 4

Reliabilty Analysis

Reliability verification is a category of physical verification that helps ensure the robustness of a design by considering the context of schematic and layout information to perform user-definable checks against various electrical and physical design rules that reduce susceptibility to premature or catastrophic electrical failures, usually over time.
This chapter will focus on EM analysis which if not addressed properly can to reliability issues in a circuit.

4.1 Electromigration(EM)

Electromigration (EM) is a critical problem for interconnect reliability in advanced VLSI design. Because EM is a strong function of current density, a smaller cross-sectional area of interconnects can degrade the EM-related lifetime of IC, which is expected to become more severe in future technology nodes. Moreover, as EM is governed by various factors such as temperature, material property, geometrical shape, and mechanical stress, different interconnect structures can have distinct EM issues and solutions to mitigate them. Electromigration is generally considered to be the result of momentum transfer

from the electrons, which move in the applied electric field, to the ions which make up the lattice of the interconnect material. Modern semiconducting chips include a dense array of narrow, thin-film metallic conductors that serve to transport current between the various devises on the chip.
Electromigration causes several different kinds of failure in narrow interconnect. The most familiar are void failures along the length of the line (called internal failures) and diffusive displacements at the terminals of the line that destroy electrical contact. Recent research has shown that both of these failure modes are strongly affected by the microstructure of the line and can, therefore be delayed or overcome by metallurgical changes that alter the microstructure.

As integrated circuits become progressively more complex, the individual components must become increasingly more reliable if the reliability of the whole is to be acceptable. However, due to continuing miniaturization of very large scale integrated (VLSI) circuits, thin-film metallic conductors or interconnects are subject to increasingly high current densities. Under these conditions, electromigration can lead to the electrical failure of interconnects in relatively short times, reducing the circuit lifetime to an unacceptable level . It is therefore of great technological importance to understand and control electromigration failure in thin film interconnects.

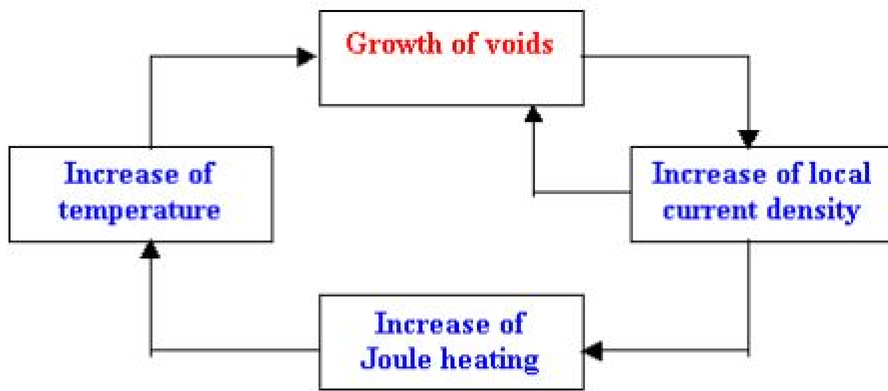


Figure 4.1: Thermal Acceleration Loop During Electromigration

4.1.1 Electromigration Flow

- Calculate the edge rates and load at worst pvt corner
- Create hit points on metal nets
- Calculate the currents(avg,peak,rms) at best pvt corner
- Compare the currents with the foundry limits

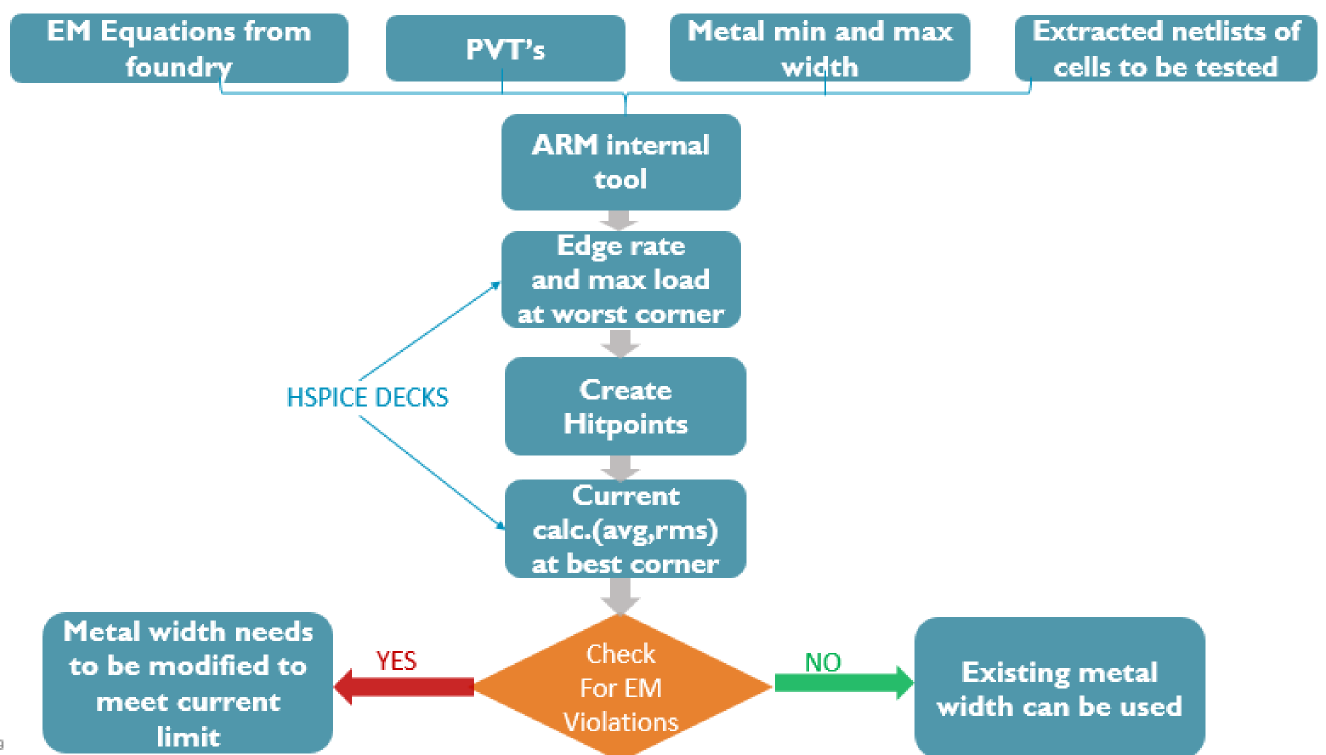


Figure 4.2: Electromigration Flow

4.1.2 Electromigration Sample Results

Power Bus Width Determination

INV Cell M1 Data							
Parameter	Current Limit (mA)	I - VDD (mA)	I - VSS (mA)	Max(I - VDD,I - VSS) (mA)	Max(I - VDD,I - VSS) (mA) CDF=0.471	%Ratio	%Ratio(with CDF=0.471)
Iavg	0.0977	0.148	0.148	0.148	0.069	151%	~70%
Irms	0.8061	0.426	0.499	0.499	-	62%	-

- Existing metal width = 50nm
- Required metal width=(50+50*51/100)=~75nm

Figure 4.3: EM Sample Results

Chapter 5

Conclusion And Future Work

5.1 Conclusion

Variation analysis accounts for all the variations that impact all level of designers directly or indirectly.The results obtained are useful to determine the appropriate voltage domain for a particular process.We can also observe how a process will behave at different domains.The variation values can be added to the standard cell libraries so that the libraries correlate with the silicon environment.This is done so that the circuit works regardless of where it falls in the process window.

FOM analysis gives us an early estimate of how the design will perform on the silicon.The leakage and performance values can be comapred across different processes or within the same process as well.It reduces the design cycle time as the bugs and discrepancies can be resolved at a very early stage of design.Overlay Analysis helps us to model the Layout Dependent Effects into out design so that it can correlate better with actual silicon environment.

Reliability Analysis helps us to check whether the cells created pass the reliability parameters like EM on actual silicon or not to ensure minimum failures.

5.2 Future Work

Future work consists of further improving the early benchmarking method for lower process nodes which will enable the designers to estimate how the process will behave and how can it be improved to achieve better performance.The ultimate goal will be to make the design better and reduce the TTM.

Bibliography

[1] www.wiki.arm.com

[2] Figures of merit for VLSI implementations of digital signal processing algorithms by J.S ward http://ieeexplore.ieee.org/document/4646053/

[3] Statistical modeling for efficient parametric yield estimation of MOS VLSI circuits by P.Cox http://ieeexplore.ieee.org/document/1484712/

[4] Performance and reliability analysis for VLSI circuits using 45nm technology by Ajit Kumar Yadav https://ieeexplore.ieee.org/document/7755590/

[5] Reliability- and Process-variation aware design of integrated circuits — A broader perspective by Kaushk Roy https://ieeexplore.ieee.org/document/5784500/authors