Implementation of SPI/I2C/Mux-Demux logic for MULTIDUT Setup for SoC Characterization

Submitted By

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INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

AHMEDABAD-382481

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Implementation of SPI/I2C/Mux-Demux logic for MULTIDUT Setup for SoC Characterization

Major Project

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology in Electronics & Communication Engineering (VLSI DESIGN)

Submitted By

Vaidya Chirag Hemantkumar

(16MECV27)

Guided By

Prof. Piyush Bhatasana

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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Institute Certificate

This is to certify that the major project entitled **"Implementation of SPI/I2C/Mux-Demux logic for MULTIDUT Setup for SoC Characterization"** submitted by **Vaidya Chirag Hemantkumar (Roll No: 16MECV27)**, towards the partial fulfillment of the requirements for the award of degree of Master of Technology in Electronics & Communication Engineering (VLSI Design) of Nirma University, Ahmedabad, is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project part-II, to the best of my knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Director,
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Industry Certificate

This is to certify that the Major Project entitled **"Implementation of SPI/I2C/Mux-Demux logic for MULTIDUT Setup for SoC Characterization"** submitted by **Vaidya Chirag Hemantkumar (16MECV27)**, towards the partial fulfillment of the requirements for the degree of Masters of Technology in Electronics & Communication Engineering (VLSI Design) of Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

Date: Place: Bengaluru

Mr. Halesh Halappanavar
Principal Engineer,
Digital Validation Team,
Broadcom Ltd.,
Bengaluru.

Statement of Originality

I, **Vaidya Chirag Hemantkumar**, Roll. No. **16MECV27**, give undertaking that the Major Project entitled "**Implementation of SPI/I2C/Mux-Demux logic for MULTIDUT Setup for SoC Characterization**" submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electronics & Communication Engineering (VLSI Design)** of Institute of Technology, Nirma University, Ahmedabad, contains no material that has been awarded for any degree or diploma in any university or school in any territory to the best of my knowledge. It is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. It contains no material that is previously published or written, except where reference has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

_____

Signature of Student

Date:

Place:

Endorsed by

Prof. Piyush Bhatasana

(Signature of Guide)

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- Vaidya Chirag Hemantkumar

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Abstract

Testing of product is a very vital role for any company before launching of the product. Half measure in testing can directly affect the trust of people on product and company. As time to market ratio also should be maintained by every company to get its product launch before any other company with the requirements customer needs.

MULTIDUT setup provides saving in time with validation testing for Bluetooth technology and reduce or almost kill the requirement to go to major chambers or labs to change the modules and do the testing. MULTIDUT Setup has its own controller as PSoC which controls CPLD to control the DUT and perform the operations. CPLD can control the blocks like DAC, EEPROM, etc. which is required for a DUT to control for the testing. PSoC controls CPLD to fire the commands and do the needed testing like Regression, PVT, etc. on the given DUT. Basic aim of the project is to reduce the human effort needed and giving the product to the customers with reduction of time of testing without compromising the quality of the product.

Abbreviations

MULTIDUT	Multiple Device Under Test
CPLD	Complex Programmable Logic Device
SRAM	Static Random Access Memory
DAC	Digital to Analog Converter
EEPROM	Electrically Erasable Programmable Read-Only Memory
SPI	Serial Peripheral Interface
I2C	Inter-integrated Circuit
PSoC	Programmable System-on-Chip
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver-Transmitter
DVT	Digital Validation Testing
MOSI	Master Output, Slave Input
MISO	Master Input, Slave Output
SCLK	Serial Clock
SS	Slave Select
CPOL	Clock Polarity
CPHA	Clock Phase
SDA	Serial Data Line
SCL	Serial Clock Line
TQFP	Thin Quad Flat Package
BLE	Bluetooth Low Energy
ASIC	Application Specific Integrated Circuit
FPGA	Field Programmable Gate Array
DMA	Direct Memory Access
GPIO	General Purpose Input Output
JTAG	Joint Test Action Group
SWDIO	Serial Wire Debug Input Output
BLE	Bluetooth Low Energy

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Chapter 1

Introduction

The Major role of testing is to know if system meets specifications or not, whether the output what we get is actually what the user needs. Basically by doing testing we cant prove that any errors are there or not but by doing testing we can detect the difference between required outputs and actual outputs.

Validation is sometimes referred as Pre Silicon Process and sometimes referred as Post Silicon Process. Nowadays Pre Silicon process is called as Verification and Post Silicon process is Validation. Where in Validation like pilot plot some countable number of chips manufactured before mass production of chips to test the correctness of all the functions which are given in the specifications. This process is usually done in lab setup using the pilot chips integrated in the board along with all other components/parts of the system for which the chip was designed for.

Validation will happen before it reaches to the customers where all the testcases will be checked with different temperatures & voltages also as per the given working requirement of the chip. Regression testing also comes under Validation only where it tests that the older programming still works fine with the changes made afterwards or not.

1.1 Motivation

Technology is increasing in very faster pace day by day and semiconductor device fabrication node is getting lower year by year. As 180 nm technology came in year 1999, 90 nm node technology came in year 2004 which has 6 years of difference. From 90 nm to 45 nm it took only 4 years. So to match up the speed companies are making machines, boards, SoCs which are made to give faster results for every task to be in the competition with other companies. And to do that one of the requirement of it is reducing testing time/power which happens while validating the chips.

As Validation will be the testing which will be done for pilot plot of chip which gets fabricated; after that testing if no failures are noticed fabrication companies will fabricate those chips in millions of lot as requested by the company. In Validation many Regression testing, Power Consumption testing with PVT comes whose setups are too big and those tests will also take too much time.

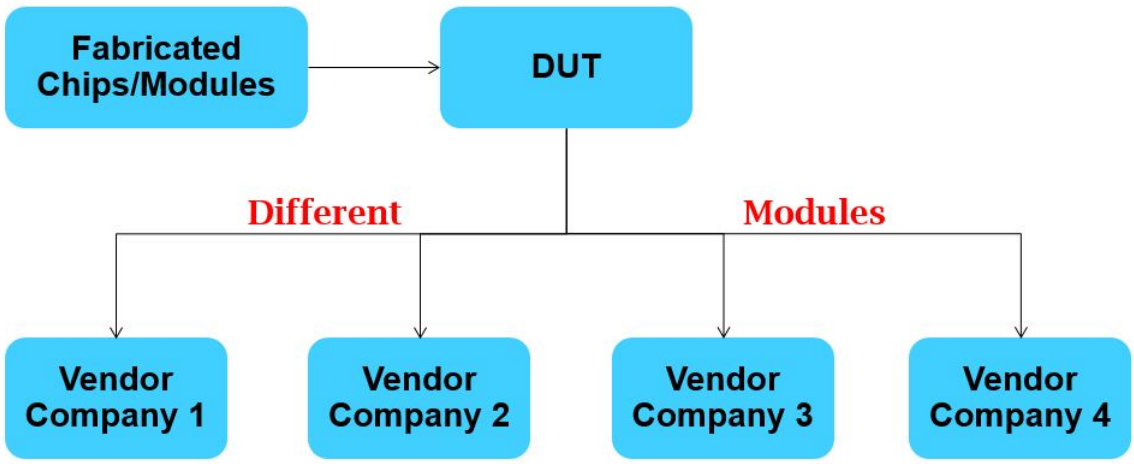


Figure 1.1: Motivation

Our main concern is to reduce the time and resources because of which in less cost and time the product can reach to the customer. Main purpose of the project is to make a board which can reduce the time. So that we came up with the idea of MULTIDUT Board which can have 4 DUTs (Device Under Test) so that we dont have to go to the

main chambers where Validation happens and change the modules.

We can have 4 totally different modules on each 4 DUTs and can do stress or PVT for whichever DUT we want to do.

Figure 1.1 shows the 4 different vendor companies different modules. For those modules we want to do the same kind of testing. We will get pilot fabricated chips from the Fabrication factory which will be attached to the modules to use for testing which is called as DUT (Device Under Test). MULTIDUT idea provides us the vision to minimize the physical changes we have to make to test the other modules with saving of time and power.

Chapter 2

Literature Survey

2.1 CPLD Research

Main aim to have CPLD which can operate at low voltages like 1.8V with multivoltage I/O operation. More number of macrocells and I/O banks were required for faster operations of CPLD. That's why we moved towards Coolrunner – 2 CPLD family which works for multivoltage I/O operations and has more number of I/O banks with less cost and high speed.

For MULTIDUT 1st time CPLD was chosen was XC2C256 which is having 256 macrocells and System frequency is also higher which is 256 MHz.
But after implementing CPLD code on XC2C256 for DUT switching and testing it was having problems of STA and less number of I/O banks was the main reason why testing was not happening.

	XC2C32A	**XC2C64A**	**XC2C128**	**XC2C256**	**XC2C512**
Macrocells	32	64	128	256	512
Max I/O	33	64	100	184	270
F–System (MHz)	323	263	244	256	179
$T_{PD}(nS)$	3.8	4.6	5.7	5.7	7.1
$T_{SU}(nS)$	1.9	2.0	2.4	2.4	2.6
$T_{CO}(nS)$	3.7	3.9	4.2	4.5	5.8

Table 2.1: Comparison of CPLDs of Coolrunner – II CPLD Family [1]

Given table shows comparison between following parameters. [1]

- Macrocells
- Max number of Input and Output
- Frequency of the system
- Time Delay for Tpd – Macrocell Input to Output Valid
- Time Delay for Tsu – Macro register setup before clock
- Time Delay for Tco – Clock to Output valid

MULTIDUT testing is done before also in industries but for those modules/ref cards which doesn't have any interference on each other while being tested.

MULTIDUT setup's main objective is to do reduce time and cost with increase in test speed but major point is at a time it can do only 1 module/ref cards/ testing.

As in Wireless communication protocols like Bluetooth and Wi-Fi can have interference problems when being tested for idealistic or practical situations.

That was one of the main reason MULTIDUT's power supplies also designed with switching characteristics which can give power to 1 DUT at a time only.

Chapter 3

MULTIDUT Setup

MULTIDUT stands for Multiple Device Under Test. This setup contains of one microcontroller who controls the CPLD (Complex Programmable Logic Device). For Validation testing whichever regression testing was done till now was on direct modules. But this setup provides more than 1 (In this setup 4) DUTs where every DUT can have different SoC contained module.

3.1 Block Diagram

Figure 3.1 shows the block diagram of the MULTIDUT setup. MULTIDUT is getting powered up from USB. PSoC is used for controlling the CPLD where PSoC stands for Programmable System on Chip. CPLD is connected all the DUTs. So CPLD is controlling DUTs and it is controlled by PSoC.

In this setup CPLD is used to control the DAC, EEPROM and the connections related to peripherals which can provide required speed to the DUT which will be in use at the point of testing. [2]

CPLD is selected for this project because setup requires more number of I/O banks with low power applications. CPLD provides low power applications with high speed and less cost. So all in all it provides overall system reliability. Clock divider and Multi voltage functionality gives the feature to have some flexibility for the setup to use it for different modules with different operating voltages and clocks also.

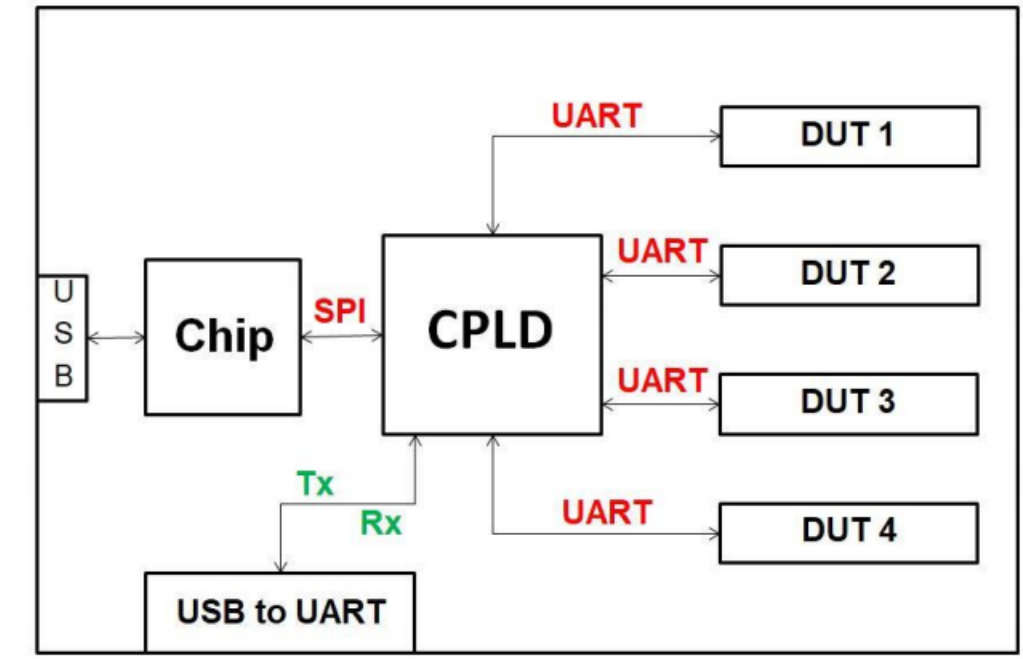


Figure 3.1: MULTIDUT Block Diagram

UART stands for Universal Asynchronous Receiver Transmitter. UART is generally used for converting the bytes (Data) it receives from the controller along parallel circuits in to a serial bit-stream for transmission. In the MULTIDUT setup which is fulfilled to do a parallel transmission of bits thats why UART is used for controlling all the DUTs through CPLD.

SoC to control the CPLD should be a programmable one as if any modifications for the future we want to do in the setup without changing the hardware it can be easily done. Thats why as a controller PSoC is selected. PSoC stands for Programmable System on Chip.

MULTIDUT board will have a similar look as shown in the block diagram where in the middle it will have PSoC and CPLD; at every periphery of the board it will have DUT connector; at one periphery it will have the power supply which will be USB to UART; another option for giving a power supply will also be there. DAC, EEPROM are also used for validating the SoC which will be there in the board. [2]

3.2 Flow of Project

As shown in the fig 3.2 validation testing needs and requirements were provided by the company which mainly had reduction in time, no need to go physically in the main chamber and change the DUTs; all of this with high performance. Because of which idea of MULTIDUT came into picture. Project is divided into 4 phases as shown in the figure.

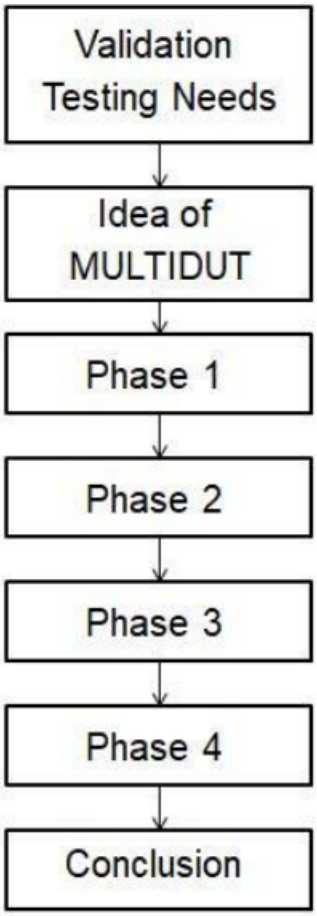


Figure 3.2: Flow of the Project

Knowledge Discovery Process Steps :-

- Phase 1

  Phase 1 contains selection of components like microcontroller, CPLD, which technology to use that can be implemented with minimal cost and high performance for the testing.

DVT Training, Tools training and which tool will be compatible for the MULTIDUT task to execute come in Phase 1.

- Phase 2

  Phase 2 contains the RTL integration part with respected to given specifications. SPI (Serial Peripheral Interface) protocol decided to run the MULTIDUT for the first time thats why implementation of it on the CPLD and checking whether that implementation is fitting onto CPLD or not. Meanwhile SoC is selected for controlling the CPLD. Basic Programming session started to implement the controlling code which can give commands to CPLD; Other task of fabricating the board.

- Phase 3

  At the starting of the phase 3 board's fabrication was almost done. In the meantime PSoC coding was being done to control CPLD with reference to given specifications. After that working of it was being checked on the hardware whether it is performing as expected or not.

- Phase 4

  Phase 4 contained the debugging of the MULTIDUT board to test if it works on PVT (In different temperatures and voltage combinations without getting effected on the functionality), Regression testing after PSoC code and CPLD implementation works as expected or not. After it passed for PVT and Regression testing more functions were added as per company/customer requirements (Main update was to run on not only Bluetooth but Wi-Fi also).

Chapter 4

SPI & I2C Interface

4.1 Serial Peripheral Interface

SPI is a protocol used for synchronous and serial communication between two main devices. It is used for short distance communication which has length less than a foot. SPI has Master Slave architecture which is using full duplex mode.

4.1.1 Interface

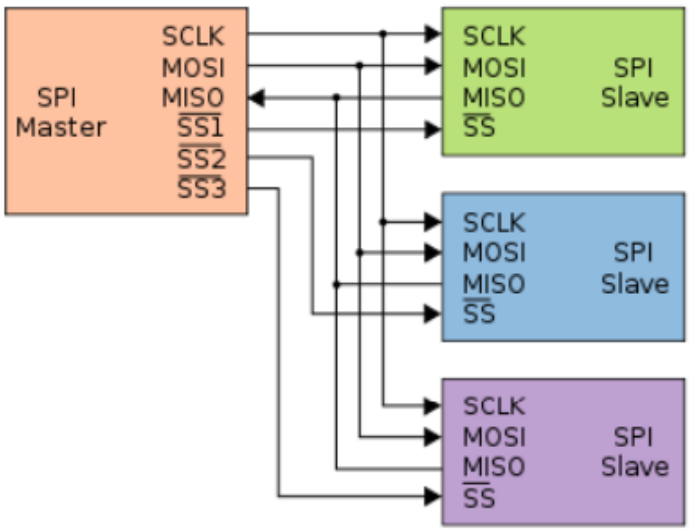


Figure 4.1: Single Master to 3 Slaves SPI Bus Example

SPI Bus has 4 logical signals which are given as below. [3]

- SCLK - Serial Clock (Output signal which comes from Master)
- MISO - Master Input Slave Output (Data Output signal from Slave)
- MOSI - Master Output Slave Input (Data Output signal from Master)
- SS - Slave Select (Output signal which comes from Master)

Serial Peripheral Interface is generally used to provide the communication between the operating device and peripherals. In this project SPI is used to control the peripherals like DAC (Digital to Analog Converters), EEPROM.

SPI can communicate with the peripherals with the stream of programmed length (2 to 16 bits) which can be shifted into the device or out of the device at a particular programmed bittransfer rate.

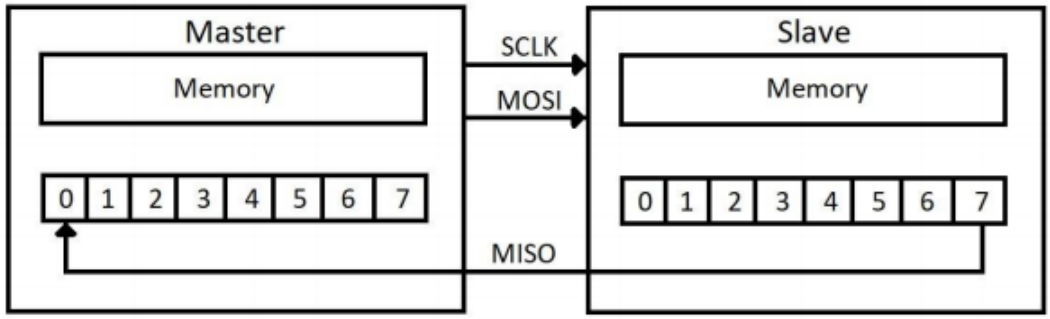


Figure 4.2: Basic Example – SPI as a Circuler Buffer

As shown in fig 4.2 [3]Master and Slave are communicating using SCLK, MOSI and MISO. Example of a circular buffer is shown where through SPI. Both the Master and Slave are having 8 bits of memory.

In each SPI clock cycle:

- The master sends a bit on the MOSI line, the slave reads it from that same line.
- The slave sends a bit on the MISO line, the master reads it from that same line.

4.1.2 Operation – Clock Polarity and Clock Phase

Fig. 4.3 Shows the Master/Slave transfer block diagram which contains a shift register, baud rate generator and all the SPI lines which are MISO, MOSI, SCK and SS. Slave select is an active low signal which is the only signal differs than the other SPI protocol signals.

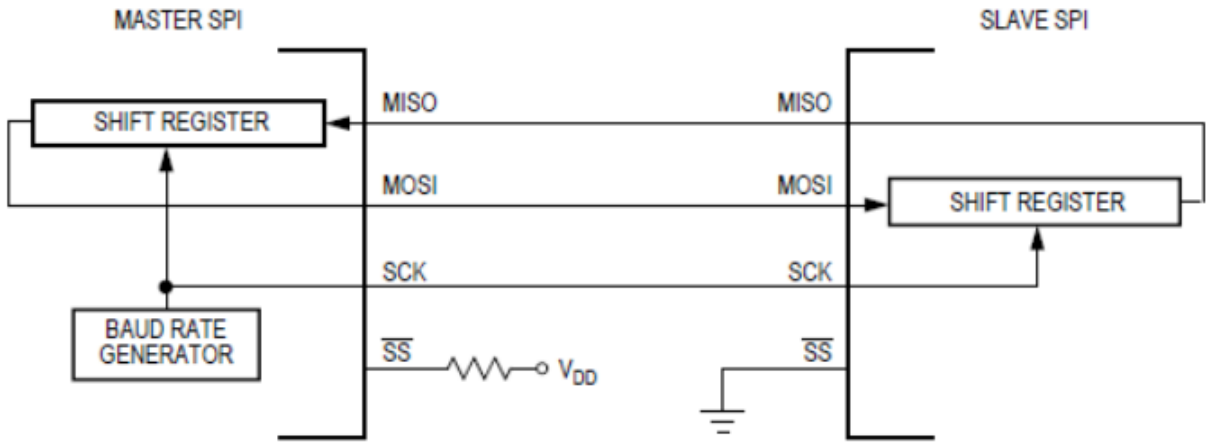


Figure 4.3: Master/Slave Transfer Block Diagram

A pair of parameters called clock polarity (CPOL) and clock phase (CPHA) determines the edges of clock signals on which data needs to be driven and/or sampled. Each of all parameters have two possible states, which allows four possible combinations, all of which are compatible with one another. So a master/slave pair must use the same parameter pair values to communicate. [3]

If multiple slaves are used that are fixed in different configurations, the master will have to reconfigure itself each time it needs to communicate with a different slave.

- CPOL = 1 indicates clock is HIGH at idle.
- CPOL = 0 indicates clock is LOW at idle.
- CPHA = 0 indicates sample on the first (or odd) clock edge from idle.

- CPHA = 1 indicates sample on the second (or even) clock edge from idle.

4.1.3 Advantages of SPI for Project

- SPI provides independent slave configuration for the slaves through slave select, which provides the flexibility to select the slave/peripheral with different clock frequency also so that we can connect different type of modules and run validation testing according to our will.

- Software implementation and hardware interfacing is simple compare to other protocols as it has less complexity.

- Lower power requirements compare to other protocols due to less circuitry.

- Higher throughput can be noticed as it has the capability to enable potentially high speed.

- Full duplex communication and in its default version of the protocol makes it comparatively better.

- Protocol flexibility for the data bits to transfer for the operations. For an example, it doesnt come with the limit of 8 bit words only; Plus we can make changes to the slaves according to our use as DUT 1 can have 8 bits of data transferring capability where DUT 2 can have 16 bits of data transferring capability too.

4.2 I2C Protocol

4.2.1 Interface

I2C stands for Inter Integrated Circuit. Compare to SPI it is a Multi Master, Multi Slave interface. It is also used for lower speed peripheral integrated circuits to P and C in shorter distances. It is a bidirectional interface which uses controller as master with the facility of having it more than one.

I2C bus consists of basically two bidirectional lines SDA & SCL.
SDA Serial Data Line
SCL Serial Clock Line

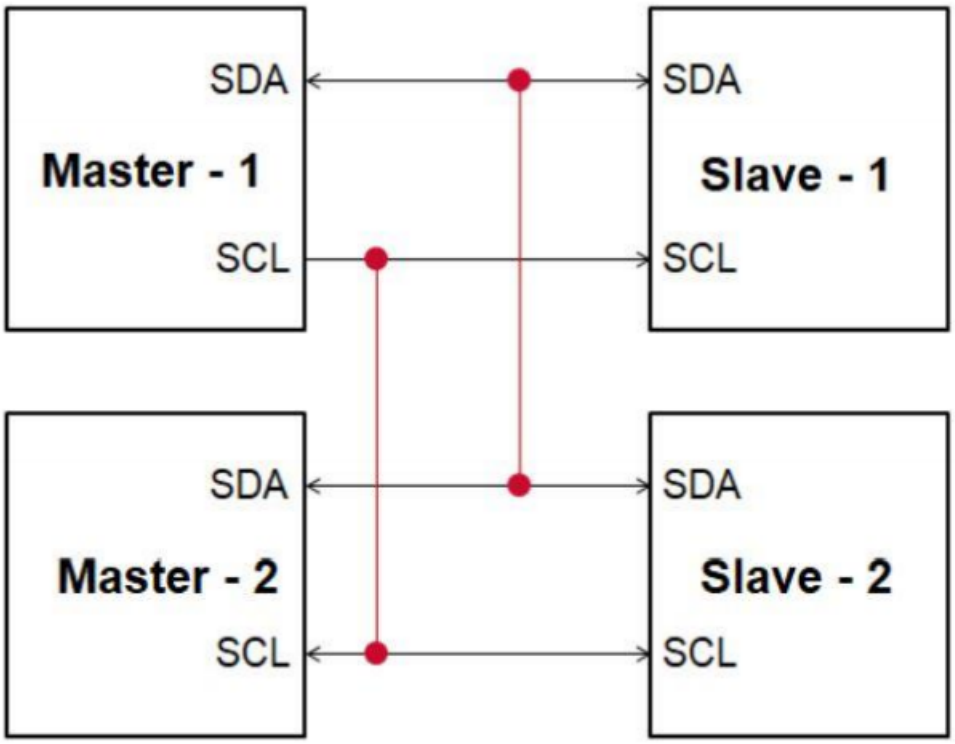


Figure 4.4: I2C 2 – Master Slave Example

As shown in the fig 4.4 I2C 2 Master Slave is taken for an example. From the figure we can see that both the masters share same clock frequencies (System clock) with the slaves where main master controller will give the clock to other master and slaves also.

Serial Data Line will be shared by every master and slave as I2Cs main protocol is that any master can control any slave thats why all the slaves will be connected to every master for the communication.

The Inter Integrated Circuit protocol is inherently Half-Duplex protocol compare to Serial Peripheral Interface which is a Full Duplex protocol which gives the scenario of speed difference between two protocols. It indicates that I2C will have less speed compare to SPI protocol.

I2C needs fewer lines for the communication thats why it is also called as 2 wire communication protocol. I2C mainly used in the applications like controlling low speed DACs and ADCs, System management for Computers, etc. It has a capability to control a network of device with 2 I/O pins available in it. Serial Clock Line (SCL) will be same for every master and slave to have same clock frequency; where for Serial Peripheral Interface it can have different frequency. [4]

I2C supports speed of transmission of data starting from 10 Kbps up to 3.4 Mbps as per the IEEE revision came of it. But if we compare the I2C protocol with SPI it will give less amount of speed comparatively.

4.2.2 Applications of I2C

- Accessing NVRAM (Non – Volatile Random Access Memory) and real – time clocks. (Main reason why I2C is used in too many projects and applications.)
- Elaborating connectable devices through small ROM configuration tables to enable operations like plug and play which can be used in EEPROMs.
- Controlling displays like LED or OLED.

- Accessing low – speed ADCs and DACs.
- With use of PCIe (Peripheral Component Interconnect Express) system management for PC systems.

4.2.3 Why SPI was chosen instead of I2C?

PSoC 5 LP will be the main controller of MULTIDUT setup who will be controlling XC2C512 CPLD also.

Major selection was to choose interface which will be there between PSoC 5LP and XC2C512 CPLD. And as shown in the title of project SPI/I2C are selected for the interfaces part. Main interface was taken as SPI over I2C because of the requirement fulfillment of the project which is given in below points.

- SPI supports 1 Master where in I2C supports Multi Master concept which was not required if we consider Low power side of the project.
- SPI is comparatively faster than I2C as it supports higher speed full – duplex communication.
- SPI is better when we talk about less distance communication interfaces. MULTIDUT setup will have PSoC and CPLD side by side having less distance only.
- SPI supports upto 10 Mbps speed which is less in I2C in comparison of 3.4 Mbps.
- We are using 4 DUTs in MULTIDUT setup so not that much of slaves will be required to control SPI if the DUTs would be in larger scale i.e. more than 10 then I2C would be better option but here is not the same case. That's why SPI was chosen for the main interface which will take place between PSoC and CPLD.

Chapter 5

PSoC & CPLD

5.1 PSoC

PSoC stands for Programmable System – on – Chip.

PSoC was chosen for the project because it was having in–built Bluetooth terms like

- Bluetooth Classic
- BLE (Bluetooth Low Energy)
- Bluetooth 4.0/4.1/4.2
- BLE Protocol Stack – A firmware that implements the Bluetooth 4.0/1/2 specification to provide BLE communication.
- BLE Profile – A Bluetooth specification that describes a set of operations & behaviors that devices use to interact with one another.

MULTIDUT setup is being made to ease the testing on Bluetooth with watching over major points like cost, area & time. PSoC gives that controlling element in setting up MULTIDUT Setup with Low Power, High Performance and more number of I/O paths which is the main requirement in the controller part.

5.1.1 Operation

PSoC has mixed – signal arrays of blocks like Digital and Analog peripherals which are configurable which makes PSoC different than other microcontrollers. PSoC also includes programmable routing and interconnect.

PSoC has 3 memory spaces.

- Paged SRAM – For Data.
- Flash Memory – For Instructions and fixed data.
- I/O Registers – For accessing and controlling configurable functions and logic blocks.

PSoC most closely relates a microcontroller having an additional blocks which are Programmable Analog & Programmable Logic Devices. Same as in microcontroller code is executed to have an intercommunication between components using APIs (Application Program Interface).

PSoC resembles ASIC and FPGA.

- ASIC :- Blocks are interconnected on – chip and have wide range of different functions but with no additional manufacturing process which required to make custom configuration; It saves time; one of the major point in designing chips.
- FPGA :- Like FPGA PSoC also needs to be configured on power up.

5.1.2 Configurable Digital & Analog Blocks

- Utilizing configurable digital and analog blocks, we can create & change mixed – signal applications which are embedded.
- Digital Blocks uses block registers; There are 2 types of Digital blocks given as below.
  - Digital Building Blocks
  - Digital Communication Blocks

- Digital Communication blocks have serial I/O user modules like UART, SPI, I2C, etc.

5.1.3 Programmable Routing and Interconnect

PSoC's flexible routing on mixed – signal arrays allows desingers to use I/O pins signal routing more freely compare to any other microcontrollers.

Programmable routing and interconnect allows user/designer to make improvements faster and easily with fewer changes in PCB redesigns compare to microcontroller having more fixed number of pins; which gives us flexibility to improve or update the functionality of MULTIDUT setup with addition of functionalities like testing modules or ref cards for not only Bluetooth but Wi-Fi also.

5.1.4 PSoC CY8C58LP Features

PSoC CY8C5LP features are given as below because of which it was selected for implementation of MULTIDUT. Selected PSoC 5 compare to any other lower end PSoC like PSoC3/4 as at the starting phase of project it was giving the features which we can later add and program it so need to do changes in the hardware; Changes in programming and additions in blocks like DACs, ADCs etc. can add on some more features which can be used for updating MULTIDUT. [5]

- Performance
  - 32 – Bit ARM Cortex – M3 Central Processing Unit is used
  - DMA(Direct Memory Access) controller with 24– Channel
- Operating Characteristics
  - Temperature range :- -40 to 85°C
  - Voltage range :- 1.71V to 5.5V
  - Power Modes
    - Active Mode :- At 6 MHz 3.1mA and At 48MHz 15.4mA

    * Sleep Mode :- 2 microampere
    * Hibernate Mode :- 300 – nA with RAM retention

- Digital Interfaces
  - SPI, I2C, UART, I2S interfaces
  - CRC (Cyclic Redundancy Check)
  - PRS (Pseudo Random Sequence) generators
  - Gate level logic functions
  - 16 – Bit Counter, Timer and PWM (Pulse Width Modulation) Blocks
  - 16 Rx, 8 Tx Buffers
- Memories
  - 2 KB EEPROM
  - Upto 64 KB RAM
  - Upto 32KB flash for ECC (Error Correcting Code)
- Analog Peripherals
  - 4 Comparators
  - 4 Opamps
  - 4 Programmable analog blocks to make
    * TIA – Transimpedance Amplifier
    * PGA – Programmable Gain Amplifier
    * Mixer
- I/O System
  - 1.2V to 5.5V interface voltages which can go upto 4 power domains
  - 2 USBIO pins which can be used as GPIOs
  - Routing of any analog or digital peripheral to GPIO which is easy and helpful if we want to make changes in it
  - Over voltage tolerance and Hot swap capability

- Programming and Debugging
  - 4 – Wire JTAG (Joint Test Action Group) used to program PSoC
  - Bootloader programming can done through SPI, USB, I2C, UAR
- Package used
  - 100 – Pin TQFP (Thin Quad Flat Package)
- Development Tools used
  - PSoC Creator Tool 4.0
  - PSoC Programmer 3.25.0
  - Firmware and Schematic Design Support

5.1.5 PSoC CY8C5LP's Architectural Overview

Major components used in PSoC CY8C58LP family is given as below.

- 32 – Bit ARM Cortex – M3 CPU Subsystem
- Programming, debug & test subsystem
- Analog Subsystem
- Digital Subsystem
- Inputs and Outputs
- Power Modes
- Clocking

PSoC 5LP is ulta low power with programmable flash System – on – Chip (SoC). Simplified block diagram of PSoC is given as below from which we can get to know about the seperate blocks' details. [5]

- Power Management System
- Analog System

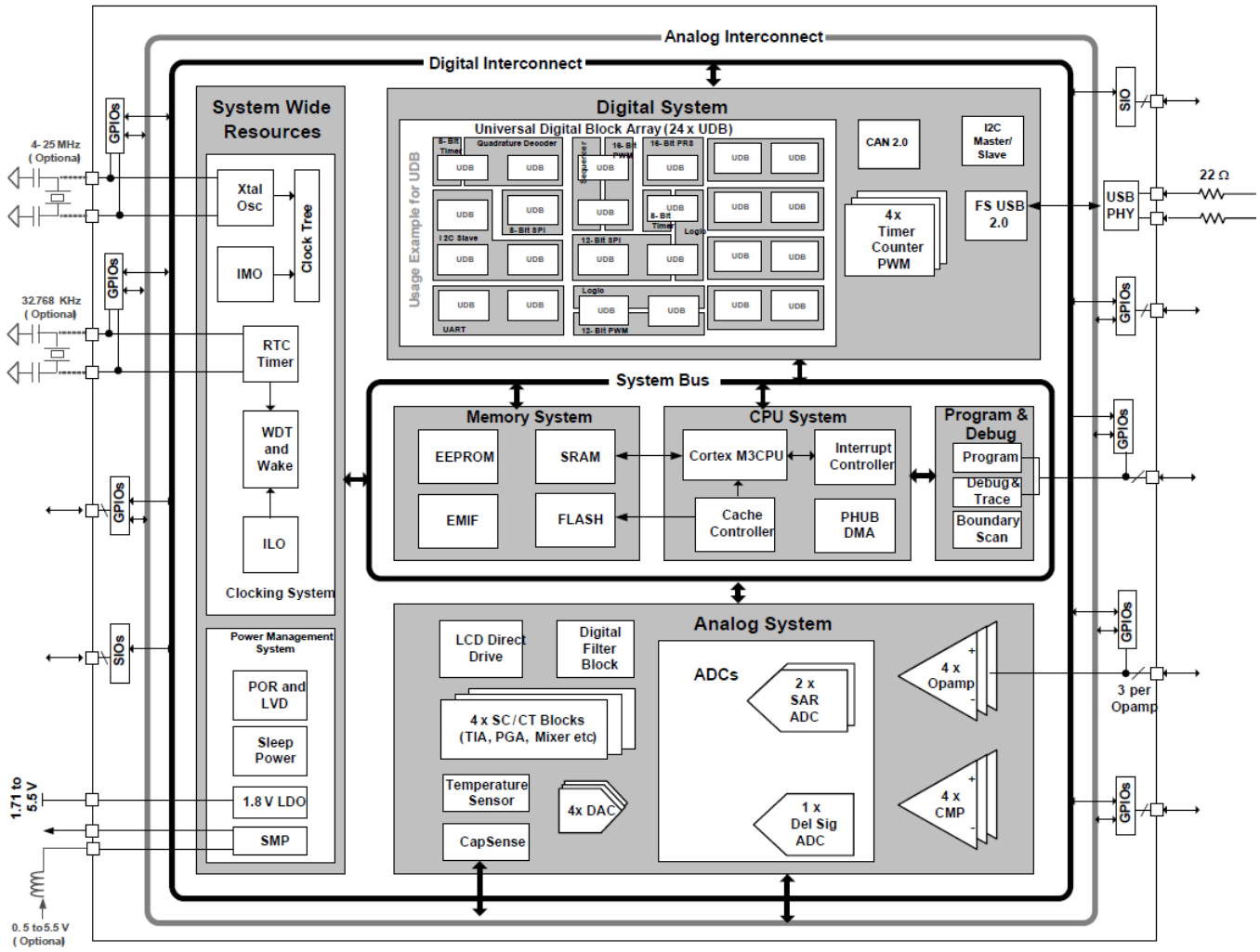


Figure 5.1: PSoC Block Diagram

- Digital System
- Memory System
- CPU System
- Program & Debug Block

For future purpose to implement code for Wi-Fi or any other technology more number of pin requirement was there. That's why 100 Pin TQFP (Thin Quad Flat Package) was used which is given in fig.5.2 as below. [5]

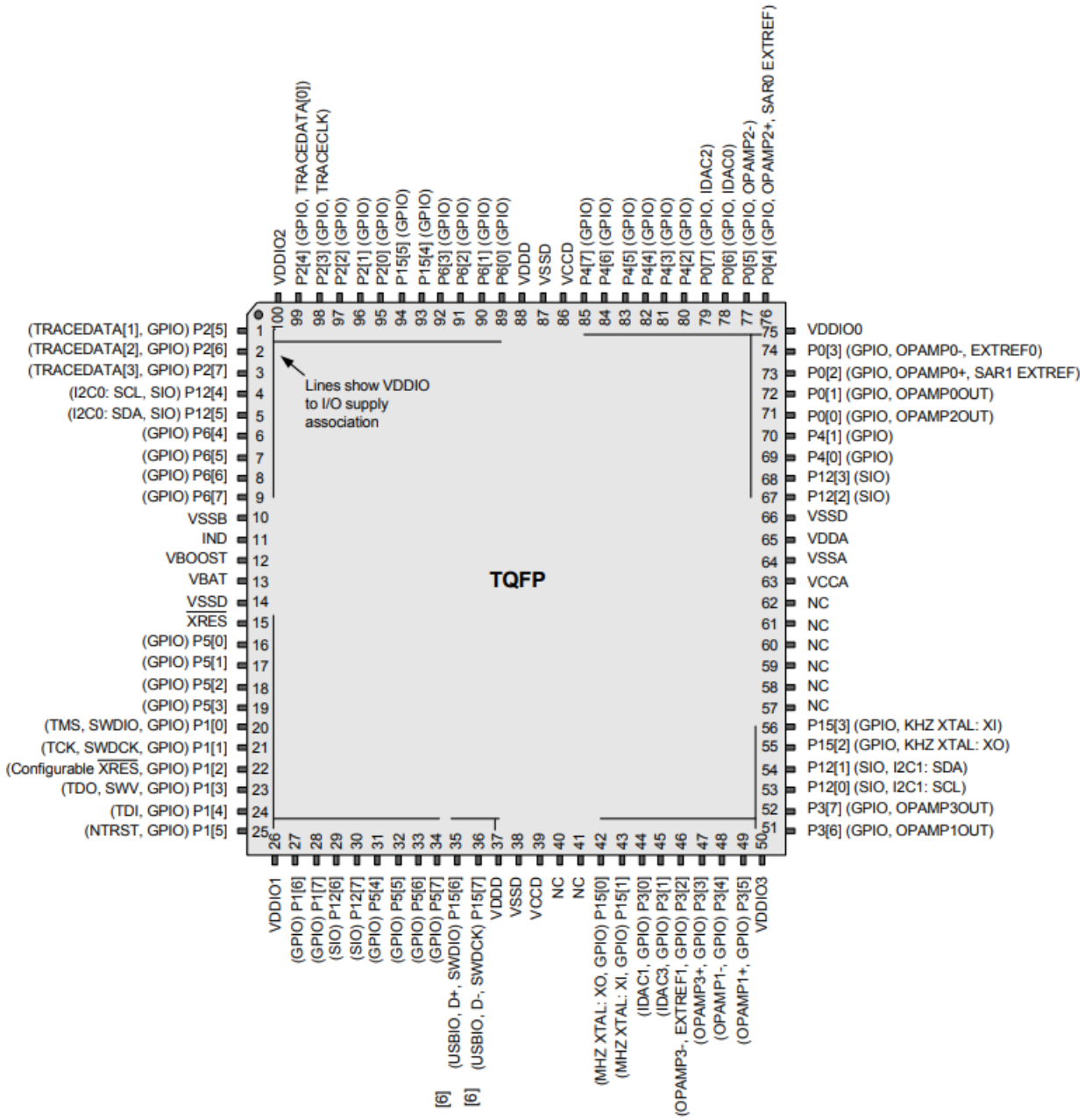


Figure 5.2: 100 – Pin TQFP used in project

Main pins which is used in MULTIDUT project for doing the programming through JTAG are given as below.

- SWDCK

  Serial Wire Debug Clock is used for programming the clock and debugging purpose

port connection.

- SWDIO

  Serial Wire Debug Input Output is used for Programming Input & output and debugging purpose port connection.

- TCK

  JTAG Debug port and Test Data In Programming.

- TDI

  JTAG Debug port and Test Data Out Programming.

- TMS

  JTAG Debug port and Test Mode Select Programming.

5.1.6 Memory

- SRAM – Static Random Access Memory
  - PSoC 5LP has 64 KB of SRAM which is used for temporary data storage. Because of more size of SRAM code execution speed is increased and fully utilizable.
- EEPROM – Electrically Erasable Programmable Read only Memory
  - EEPROM in PSoC is a non – volatile memory.
  - It is having 2 KB of memory which is used for storing the user data.
- Flash Program Memory
  - Flash program memory provides nonvolatile storage same like EEPROM but for specific blocks like
    - User Firmware
    - Bulk Data Storage
    - User Configuration Data
    - Optional ECC (Error Correcting Codes) data

- It has upto 32 KB of flash space for special use of ECC. But if it is not used for ECC we can use it to store bulk user data and device configuration data.
- ECC can detect 2 bit errors and can correct 1 bit error per 8 bytes of firmware memory.
- Interrupt can be given if an errors is detected.
- Flash output is of total 9 bytes where 8 bytes is of data and 1 byte is for ECC data.
- Flash program memory can do In–System programming also which is used for bootloaders which can be done using serial interfaces like SPI, USB, UART or any communication protocol.
- It is typically used for production programming through both the SWD and JTAG interfaces.

5.2 CPLD

CPLD stands for Combinational Programmable Logic Device.

CPLD was chosen for the project because its logic blocks are based on EEPROM which is non volatile. It means when program will be downloaded on CPLD after that we don't have to do programming again for power cycling it which is the major difference between CPLD and FPGA.

One of the major point is cost also as we have to make a MULTIDUT setup which reduces the cost, time and increase the speed that's why CPLD was a perfect fit for it compare to FPGA.

5.2.1 XC2C512 – Coolrunner – II CPLD Family

XC2C512 having 512 macrocells is designed for low power and high performance applications which improves the overall system's reliabilty.

XC2C512 CPLD was chosen for the project because of its capacity of more number of macrocells and I/O banks. Coolrunner – II CPLD family of CPLDs were perfect for our application purpose and cost-wise which was giving acceptable voltage range for VBAT & VIO with faster In – System programming JTAG inteface.

XC2C256 CPLD was chosen from the same CPLD family for project before selecting XC2C512 CPLD but it was having problems related to RTL integration because of less number of macrocells and I/O which is 256 and 184 respectively.

For MULTIDUT setup 4 DUTs will be there for implementation in an ideal situation while testing which should have more than 250 I/O pins according to RTL integration team.

System frequency of CPLD is less in XC2C512 compare to XC2C256 but it was not creating any problem for data to do switching from any working DUT to another DUT. This

is how XC2C512 CPLD was chosen at last for MULTIDUT setup and 2 major blocks were selected one was PSoC and another was CPLD.

5.2.2 CPLD Features

Major features of XC2C512 is given as below. [6]

- Optimized for Voltage 1.8V systems
  - Reduces quiescent as low as 14 microampere
  - Pin to pin delay is fast as 7.1 ns
- Advanced System Features
  - IEEE1149.1 JTAG BST (Boundary Scan Test)
  - Faster In system programming
  - Low Power Management
  - 4 Seperate I/O Banks
  - Flexible Clocking Modes
  - PLA (Programmable Logic Array) architecture
  - Input/Output voltages compatible with both 1.5V, 1.8V, 2.5V and 3.3V
  - Multivoltage I/O operation
- Programming in CPLD
  - Xilinx ISE 14.7 Suite is used for CPLD.
    - Programming data sequence is dowloaded in the CPLD device using Xilinx iMPACT tool.
- In System Programming
  - XC2C512 CPLD uses 1.8V (Internal Supply Voltage) which gives voltages and currents to pins on the part.

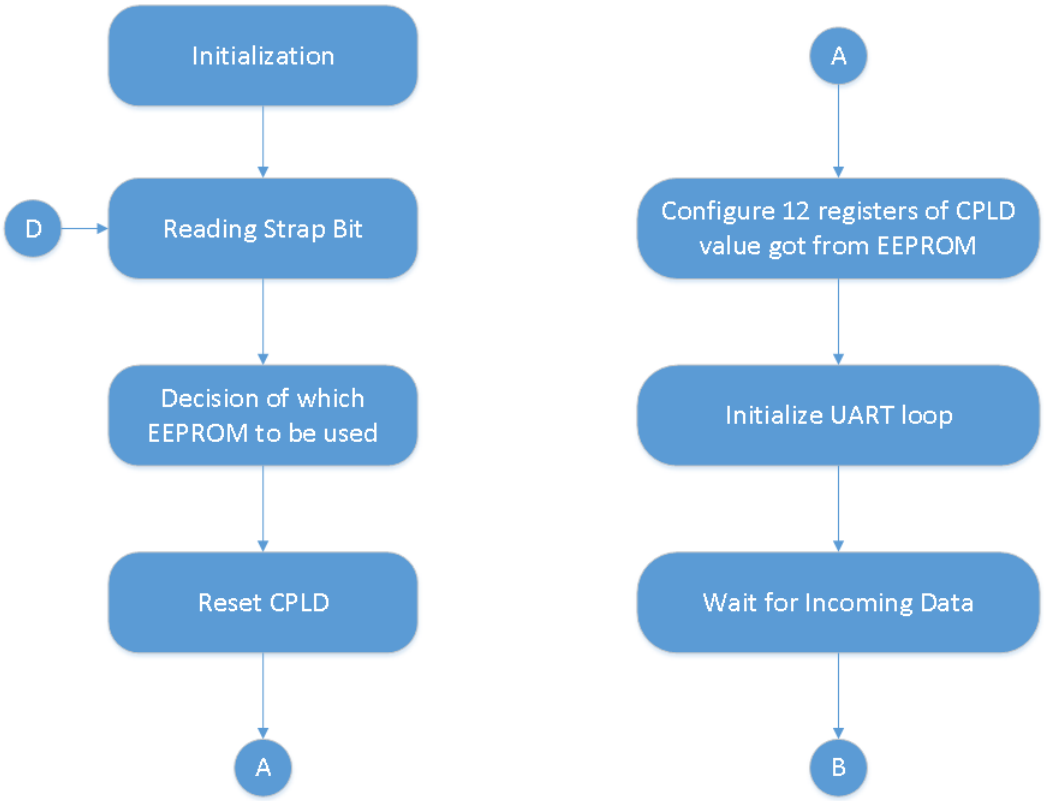
– Operating voltage for MULTIDUT is decided by the modules and ref cards we use for testing of the chips which is VBAT = 3.6V and VIO = 1.8V which can be derived internally through this that's why it's one of the biggest advantage of using this CPLD.

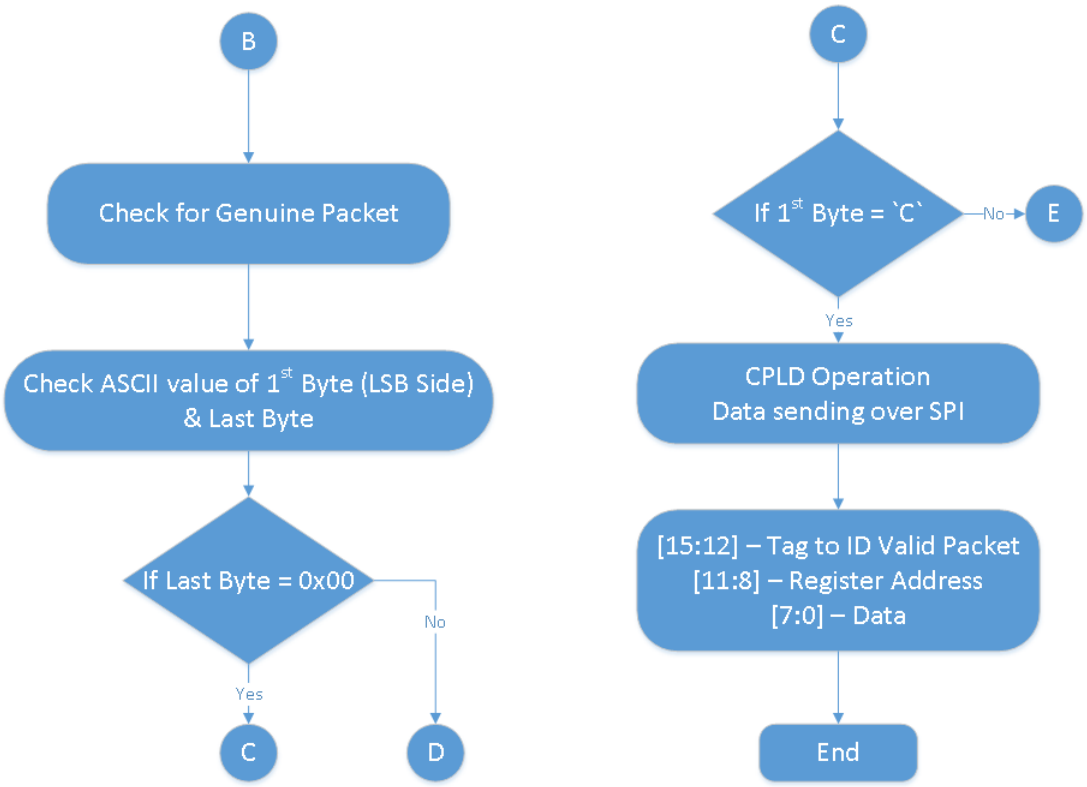
Chapter 6

PSoC & CPLD's Flow for MULTIDUT

6.1 Algorithm of PSoC Flow

PSoC's Code flow is given as below.



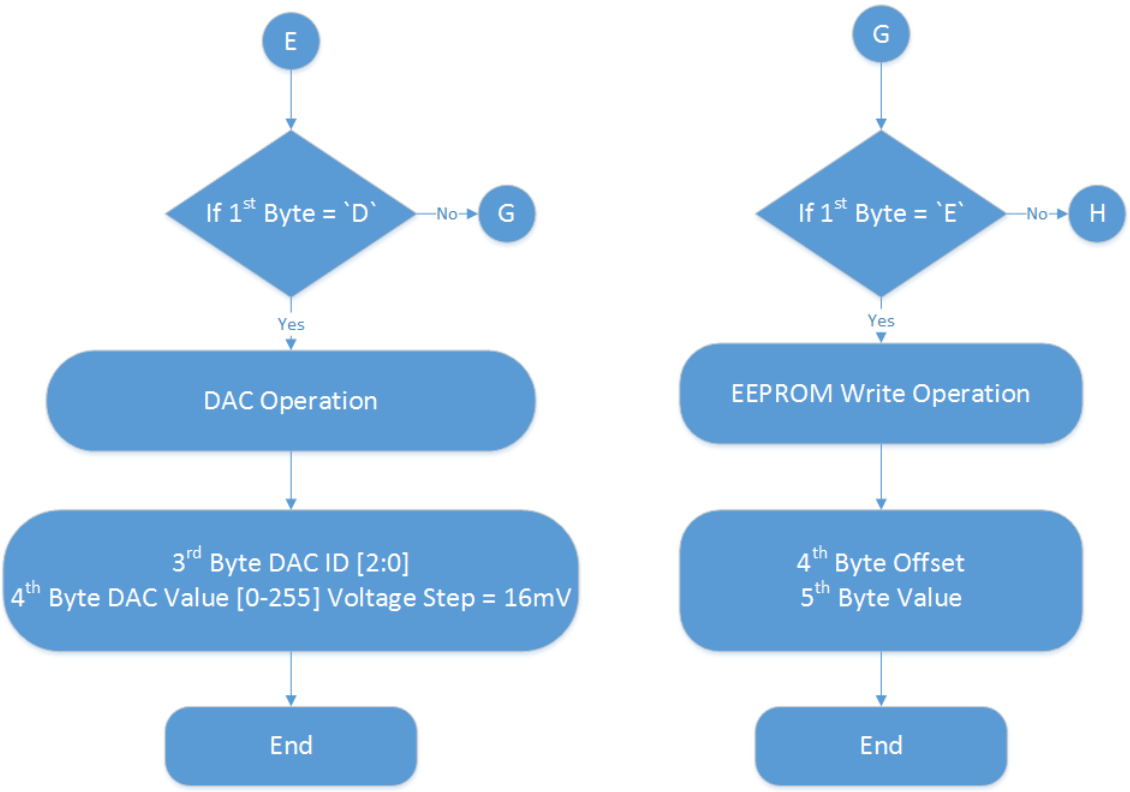


Main functions of PSoC [7]:-

- Send 16 – Bit of data to CPLD from PSoC via SPI Interface. (MOSI/MISO)
- Program DAC
- Read EEPROM
- Write EEPROM

Code Flow

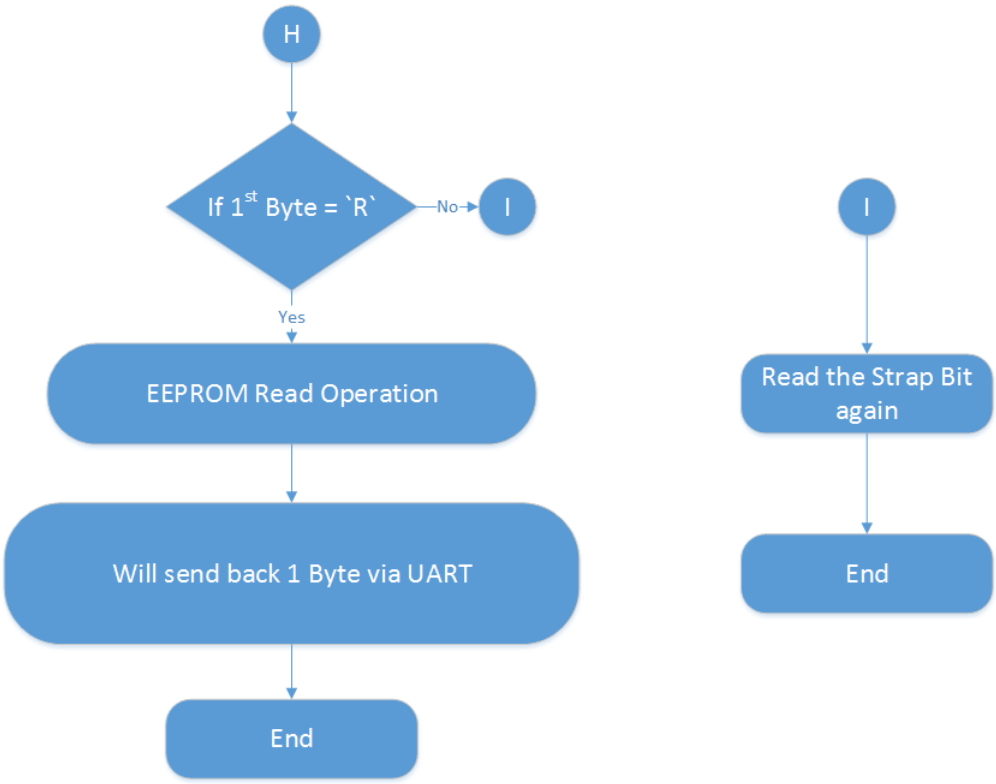
- Initialization
  - Read Strap Bit
  - Decide the EEPROM to be used
  - Reset CPLD
  - Configure 12 Registers for CPLD which helps in selection of DUT and switching also
  - Initialize UART



UART Loop

- Wait for Incoming data from PSoC
- After data is received, acknowledgement is sent.
- Check for Genuine packet
- First Byte should be from following
  - 0x43 – C
  - 0x44 – D
  - 0x45 – E
  - 0x55 – R
- Second Byte = Total length of packet + 2 (Payload + 1(length byte) + 1 (Header Byte))
- Last Byte should be 0x00 which only gives the acknowledgement back to PSoC
- If genuine packet is confirmed it will go for execution

- If 1st Byte is ‘C‘ : CPLD Operation
- Else if Byte is ‘D‘ : DAC Operation
- Else if Byte is ‘E‘ : EEPROM Write
- Else if Byte is ‘R‘ : EEPROM Read



CPLD Operation

- 3rd and 4th Byte are combined to get 16 - Bit Data
- 16 Bit of data is sent over SPI
  - Data [15:12] – Tag to ID valid packet
  - Data [11:8] – Register Address
  - Data [7:0] – Data

DAC Opeation

- 3rd Byte is DAC ID [0-3]
- Step Voltage of DAC = 16 mV

- 4th Byte is DAC value[0-255]

EEPROM Write

- 3rd Byte is Row number. (1st row is not used that's why actual row will start from +1)
- 4th Byte is Offset
- 5th Byte is value

EEPROM Read

- 5th Byte it will send back via UART for the reading operation
- Other bytes will be similar like EEPROM Write

6.2 Issues seen bringing up MULTIDUT

After MULTIDUT came from fabrication while bringing up MULTIDUT on bench setup some issues came which was causing failures in MULTIDUT. Issues were mainly seen in CPLD and PSoC.

6.2.1 CPLD related Issues

Problem in transferring the daata which was going through data lines from USB to UART in CPLD in MULTIDUT setup.

- Programming of HDL is done in Verilog in Cadence NCSim.
- Code was having problem because of creation of unnecessary latch which was causing problem og High impedance when data tries to go from USB to UART.
- 4 DUTs are there in MULTIDUT where each DUT contains total 16 – bit of data being transferred through USB to UART.
  - 2 Major Tx Lines and 2 Major Rx lines
  - Tx Lines
    - Tx Data towards CPLD

        * Tx Data from CPLD
    - Rx lines
        * Rx Data towards CPLD
        * RX Data from CPLD

- Because of this when MULTIDUT's CPLD is programmed DUT switching was not having any problem but when testing of the modules/ref cards' started because of data not going through fine testing was getting failures.

Solution of this problem was to rewrite the code and use Multiplexers which doesn't create any latches and we can not have the problem High Impedance.

6.2.2 PSoC related Issues

Bluetooth was tested and used till now on interface UART but as Wi-Fi was used in PCIe interface which is faster interfaces compare to UART. That's why some of the vednor companies required Bluetooth to be on same platform as Wi-Fi so that they can save the area on chip via using 1 interface for both and speed of Bluetooth can also be increased.

Shifting Bluetooth towards PCIe had its own problems for MULTIDUT testing which are given as below.

- Enumeration problems in PCIe for Soft reboot [7]
    - While powering up the station we have to give power to station, temperature chambler, brix, power supplies and MULTIDUT to initialize the testing. After powering up all the devices hard reboot (power cycling of all the devices) is not required.
    - Soft reboot is used as an option when DUT switching needs to be done when 1 DUT's testing is completed and needed another DUT's testing.
    - 60 - Pin PCIe interface is given in all 4 DUTs and while powering up where the testing happens. On powering up MULTIDUT no DUTs are selected because of this enumeration of the module/ref card was not happening which is required on powering up the station.

- Because of that reason module/ref card was not getting detected and soft reboot was needed so that PCIe device again rescans the interfaces for any module/ref card. This process is time taking as the whole setup needs to be soft rebooted.
- Time taken for whole testing increased because of this as we are dealing with PVT changes (Testing across Voltage/Temperature).

Solution to this problem was making DUT1 as selected from all 4 DUTs when powering up MULTIDUT which is controlled by PSoC. Giving DUT1 as default selection reduces the time which was taken by Soft reboot after every DUT switching and testing on it. So the PSoC code has been added with default DUT1 selection when power is given to MULTIDUT.

- Reading the data from modules having different interfaces (BToU/BToP)
  - Bluetooth module/ref card on UART inteface will not have any BDF (Base Data Function) address in PCIe but Bluetooth module/ref card on PCIe interface will have 1 BDF address thorugh which PCIe controls it.
  - In testing every possible combinations needs to be checked where 4 DUTs can have BToU and BToP scenarios which was giving in total 8 combinations.
  - 1 combination from it was failing which was when DUT1 is on UART and after testing is completed switching of DUT happens to any other DUT which is on PCIe it will have problem in initializing the testing sequence.
  - PCIe was not been able to detect the module/ref card in rescanning also that's why the test sequence was not starting.

Solution to this problem was adding removal of root complex in PCIe interface while DUT switching happens.

When DUT switching was happening it was removing the interface things only not root complex of PCIe which was needed. That's why after switching the DUTs rescan was not been able to give BDF required for the module/ref card.

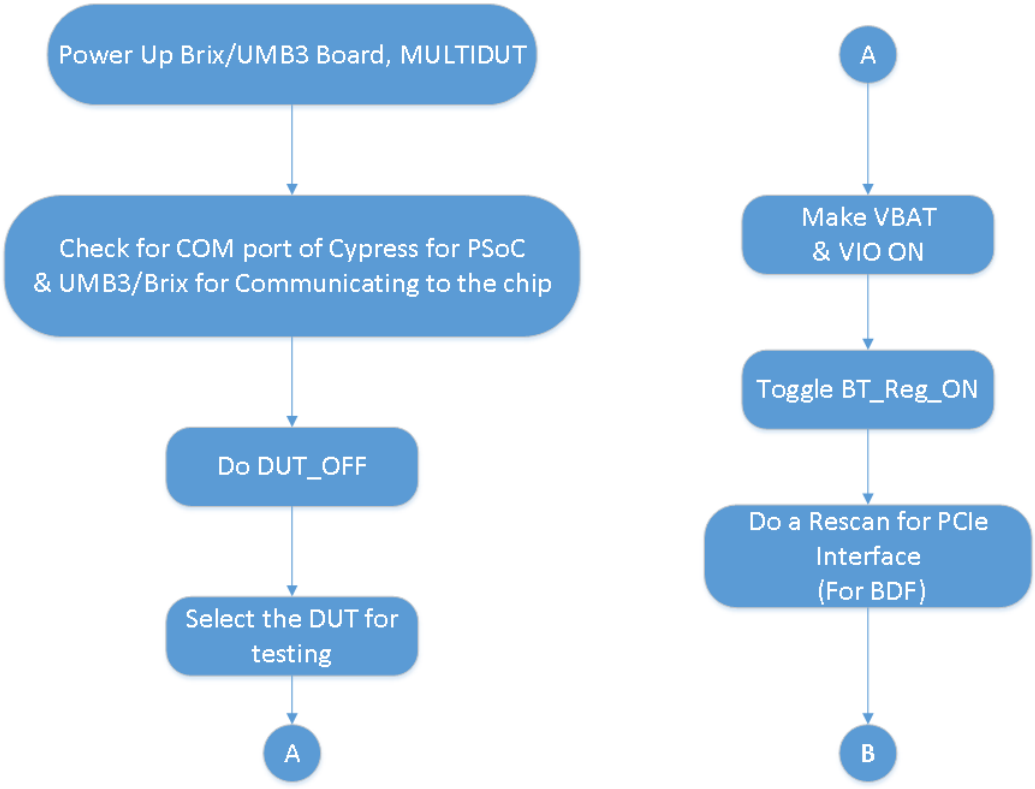
Removing root complex of PCIe and after that doing rescan gave the power cycle for PCIe which it required and could detect the BDF address which was needed for the testing.

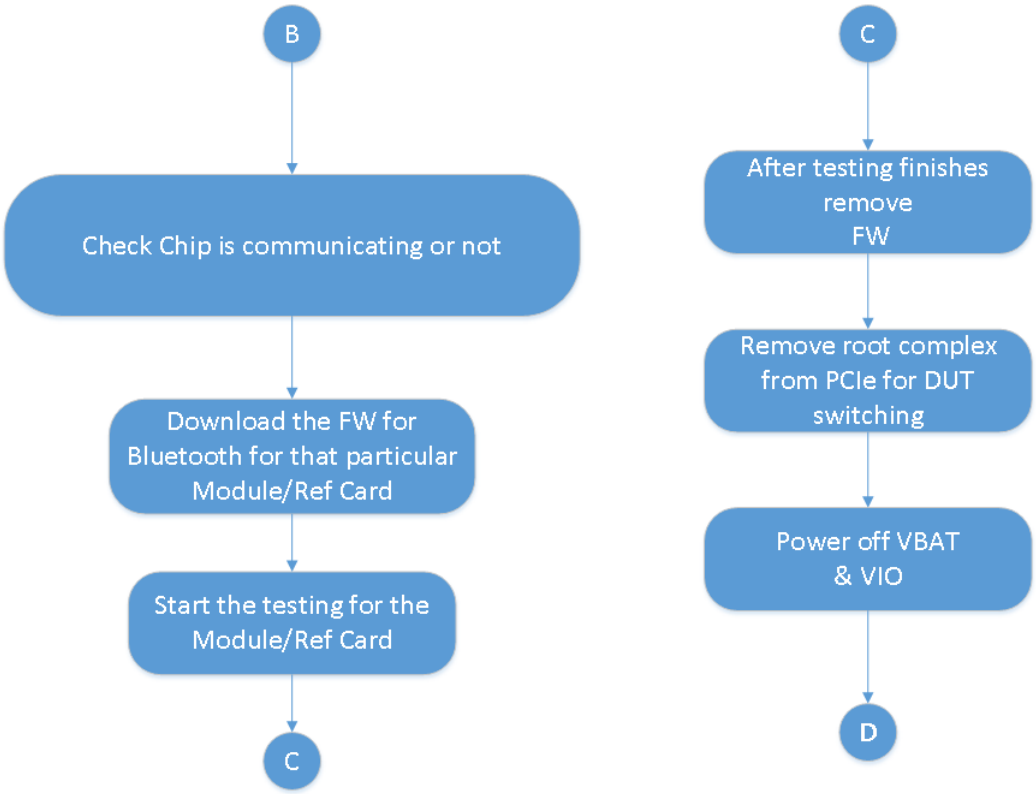
6.3 MULTIDUT Station Bring Up

As shown in the algorithm given below these are the steps to use MULTIDUT :-

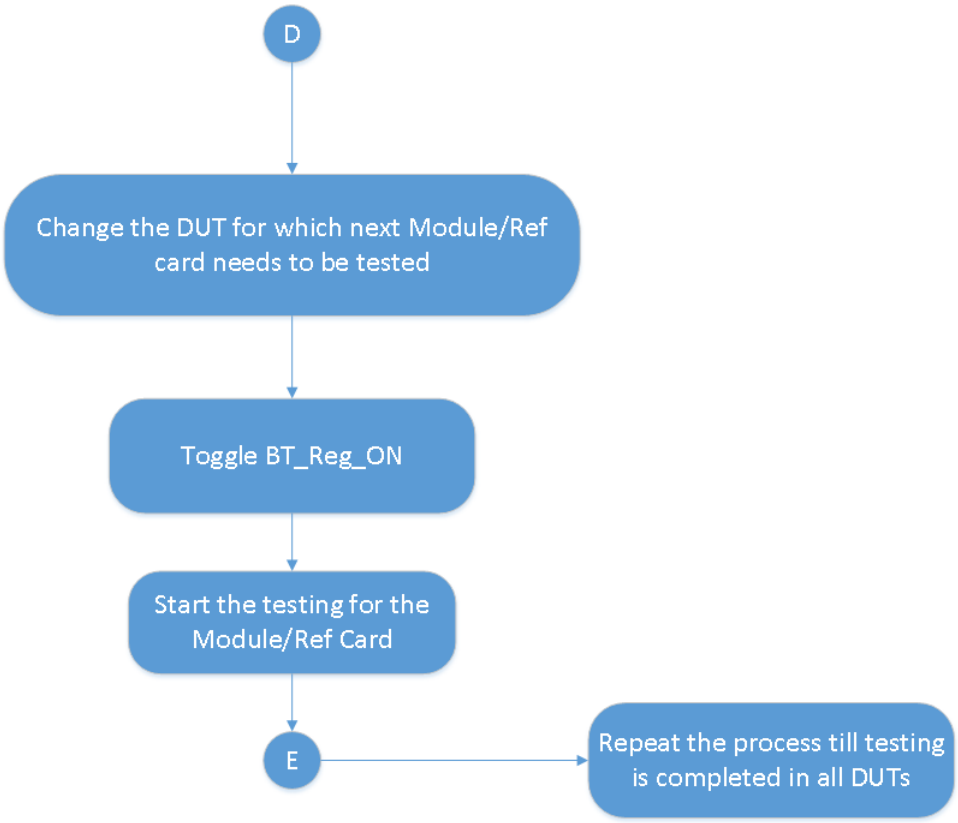
Important Note

- Whenever DUT – OFF is done make sure your power supply (VBAT & VIO) is OFF.
- All the DUTs batch files needs to be there in the machine.
- Always check for COM port first when you power up MULTIDUT and UMB3 for testing.
- Changes in Sequencing may fail the working of it.





- Power up the station with Brix/UMB3 and MULTIDUT in it.
- Check for COM ports for Brix/UMB3 and MULTIDUT PSoC for communication purpose.
- Do DUT – OFF first to make sure it doesn't have any garbage value.
- Select the DUT for testing from given 4 DUTs.
- Power on VBAT & VIO for giving the voltages to chip.
- After powering on VBAT & VIO do a BT–Reg–ON toggle (Must required for testing purpose).
- Check for the communication with the chip if it is working or not.
- Download the Firmware for Bluetooth for that particular Module/Ref card which is selected in DUT for testing purpose.
- Start the testing.
- After testing finishes remove the firmware which was downloaded for testing.



- Remove root complex from PCIe if module/ref card is BToP.
- Power off VBAT & VIO.
- Change the DUT for which next module/ref card needs to be tested.
- Toggle BT–Reg–ON (Again Must required for testing to not have any problem of continuity).
- Start the testing for another module/ref card.
- Repeat the process till testing is done in all the DUTs.

MULTIDUT will contain these major things for full PVT testing :-

- All 4 Modules/Ref cards to be tested on.
- Temperature Chamber in which MULTIDUT setup will be created.
- Power Supply (SMU – Source Measure Unit) to give VBAT & VIO to MULTIDUT setup.

  - VBAT - Battery Voltage
  - VIO - Interface Voltage

- Ref Dongle of Bluetooth with whom all 4 modules/ref card will do the testing.
- Controller which will connect all things (MULTIDUT, Temperature Chamber, Power Supply)
- Mini USB to UART cable for UMB3 Board.
- Macro USB to UART cable for MULTIDUT (PSoC).
- 12V Adapter which will power up MULTIDUT.
- RF cables for testing purpose.
- If Brix is used for testing it will require 19V adapter.

6.4 MULTIDUT Sanity Testing

As shown in the figure UMB3 (Universal Mother Board 3) or Brix machine which is used for testing the modules/ref card will be connected to MULTIDUT's 60 pin connector interface.

Steps how MULTIDUT will work

- 1st Voltage to power UMB3 Board/Brix will be given in form of VBAT and VIO.
- PSoC will boot up and make DUT1 ON automatically as programmed.
- DUT1's BDF (Base Data Function) address will be given in Brix machine for PCIe interface usage.
- For testing of the module CPLD will be used for Tx and Rx data paths along with whichever interface module is using like UART, USB, etc.
- After testing gets completed for switching the DUTs VBAT and VIO should get off first otherwise it can create glitch problem for MULTIDUT and board can fail because of power cycling issues.

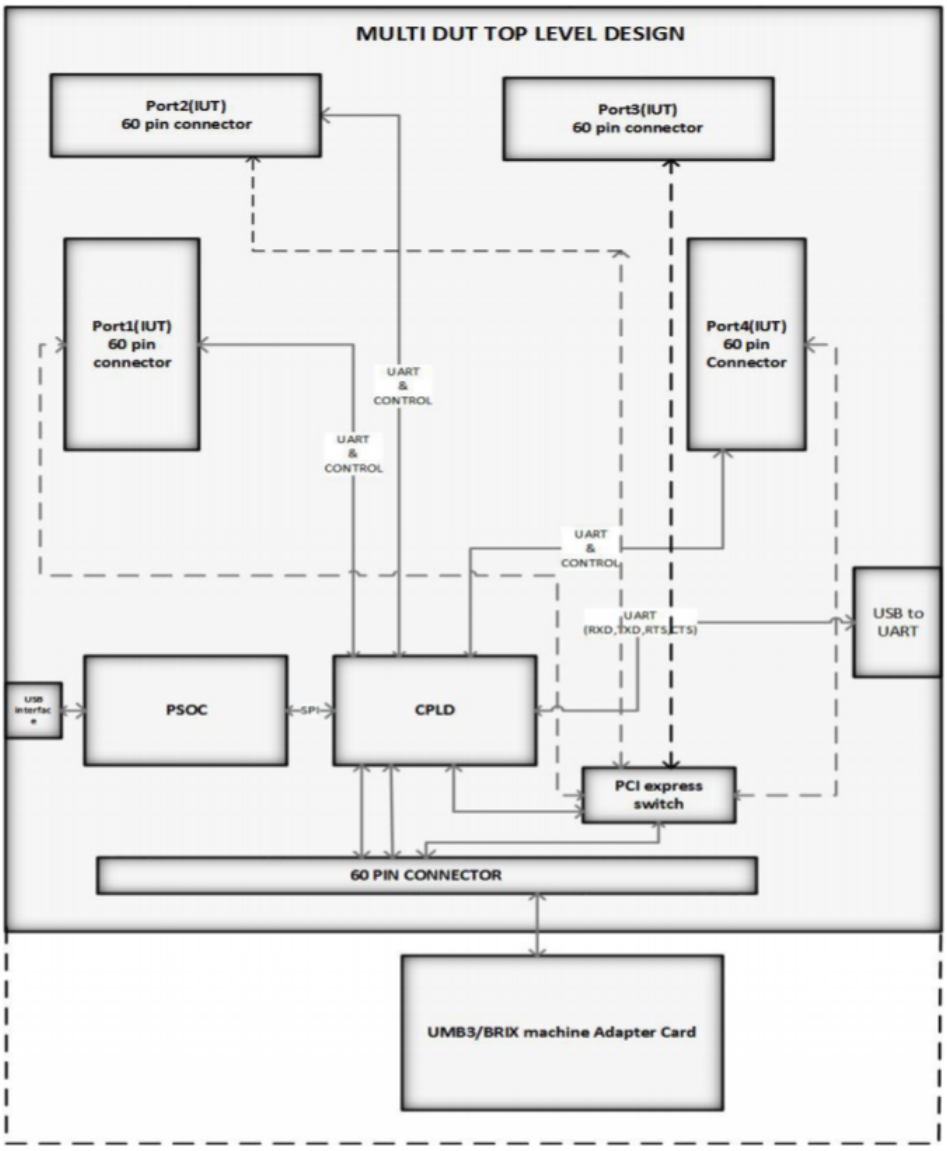


Figure 6.1: Top Level Design of MULTIDUT

- DUT should be switched to whichever number; It is not necessary that it can switch sequentially only. It can switch from DUT1 to DUT2/3/4 and vice versa.

Sanity Testing results are shown below with and without MULTIDUT setup.

As shown in the figure [8] we can see the difference in with and without MULTIDUT current measurement. Here same station, temperature and module/ref card is used for testing purpose so we can have accurate results and comparison can be done.

- 6 Testcases are selected for comparison for with and without MULTIDUT.

Testing			Without MULTIDUT		With MULTIDUT	
Voltage Setting			VBAT=3.6	VBAT=1.8	VBAT=3.6	VBAT=1.8
Test ID	Config Dowld	Range	VBAT (mA)	VIO (mA)	VBAT (mA)	VIO (mA)
Testcase 1	Default	0.1,0.1	2.0215	0.2370	1.9605	0.2396
Testcase 2	Default	0.1,0.1	0.0375	0.0623	0.0308	0.0723
Testcase 3	Default	0.1,0.1	0.0002	0.0130	0.0001	0.0118
Testcase 4	Default	0.1,0.1	29.7942	0.3015	27.6725	0.2872
Testcase 5	Default	0.1,0.1	26.8229	0.2997	26.2280	0.2856
Testcase 6	Default	0.1,0.1	7.3129	0.2888	7.1592	0.2787

Figure 6.2: Sanity Results

- Testcase 1 is one of the major testcase where FW download happens and chip behaves in idle state.
- Testcase 2 is one of the power saving modes used for the chip where we can see the power saving of almost 100 micro ampere when used MULTIDUT which is very good if we consider low power vlsi design.
- Testcase 3 is reset mode when no voltage is given in chip.
- Testcase 4 is for Bluetooth transferring Basic Data Packet Rate (BDR) Packet while transmitting the data.
- Testcase 4 is for Bluetooth transferring Extended Data Rate Packet (EDR) while transmitting data.
- Testcase 5 is for Bluetooth receiving the data packet which will have less current compare to what we need for transmitting the data packets.

Chapter 7

Conclusion & Future Work

7.1 Conclusion

This thesis aims to reduce the time and resource reduction for validation testing by means of MULTIDUT setup. After stydying and doing implementation on this following conclusions can be made :

- Creating MULTIDUT reduces TMT (Time to Market) ratio which is very crucial as too much of competition in industry is going on which requires solution like this.
- Cost Reduction – Cost taken for total 4 temperature chambers, power analyzers, Brix/UMB3 machine requires more money where MULTIDUT uses only 1 of it which is the major point industry is in need of.
- By giving algorithm in MULTIDUT whenever 1 DUTs' testing is completed it will automatically switch to another DUT which automation is required wherever manual testing is used.

7.2 Future Work

Future work consists of making MULTIDUT up with Wi-Fi (Wireless Fidelity) technology also with proper change in the firmware and Hardware. With that upgrade MULTIDUT can be used for both leading technologies which are getting used in communication industry.

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