Analysis and Design Validation of Standard Cells Library

Major Project Report

Submitted in fulfillment of the requirements
for the degree of

Master of Technology
In
Electronics & Communication Engineering
(Embedded System)
By
Aman Kumar
(17MECE01)

Electronics & Communication Engineering Department
Institute of Technology
Nirma University
Ahmedabad - 382 481
December, 2018

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Under the Guidance of

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Declaration

This is to certify that

1. The thesis comprises of my original work towards the degree of Master of Technology in Embedded System at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgment has been made in the text to all other material used.

Aman Kumar
(17MECE01)

Disclaimer

Certificate

This is to certify that the Major Project entitled **"Analysis and Design Validation of Standard Cells Library "** submitted by **Aman Kumar (17MECE01)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in Embedded System, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this Major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

Dr. Sachin Gajjar   Dr Nagendra Gajjar

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Head, EC Department   Director, IT - NU

Date :   Place : Ahmedabad

Certificate

This is to certify that the Project entitled "**Analysis and Validation of Standard Cells Library**" submitted by **Aman Kumar (17MECE01)**, towards the submission of the Project for requirements for the degree of Master of Technology in Embedded System, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

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(17MECE01)

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Abstract

A standard cell library is a collection of low-level electronic logic function such as AND, OR, INVERTER, flip-flops, latches, and buffers. These cells are realized as fixed-height, variable-width full-custom cells. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The cells are typically optimized full-custom layouts, which minimize delays and area. So Standard cells plays a vital role in the SoC. The objective of project is to design the layouts of the standard cells as per the required specifications of customer, and to check the yield we have to check the design under various real world scenarios and in order to do that we check performance of design through various PVT (Process, Voltage and Temperature)corners with an aim that the circuit should be able to reliably operate at all the extreme conditions For that Monte carlo, cross corner, High sigma analysis is done. standard cell libraries have to be deliver on time. So in less time full packed library has to be created in which every cell has to be DRC and DFM clean. Standard cell libraries offer specific cells designed for various applications, balanced cells (inverters, buffers, flip flops), metastable flip flops (for synchronizer circuits), level shifters. So all these cells are created depending upon the need of customer which requires different processes.

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List of Abbreviation

SoC   - System on Chip

ASIC   - Application specific integrated circuit

DRC   - Design Rule Check

LVS   - Layout v/s schematic

GDS   - Graphical Discription of System

CDL   - Circuit Description Language

MC   - Monte Carlo

CC   - Cross Corner

IP   - Intellectual Property

CBIC   - Cell Based Integrated Circuit

SPR   - Synthesis Place and Route

VLSI   - Very Large Scale IC

HDL   - Hardware Discription Language

DFT   - Design For Testablity

PVT   - Process Voltage Temperature

Chapter 1

Introduction

1.1 Role of standard cell library

Phenomenal advances in photolithography process has enabled feature sizes to shrink from 500 nm in 1990 to as low as latest 10/14 nm process, these advances have played crucial role in keeping Moores law alive from past fifty years. Process below 100nm are referred as Ultra Deep Sub-Micron technology nodes. As the technology shrinks, the chip becomes denser and complex, therefore manual creation of the digital modules of the design become more difficult. To simplify and speed up the design process, synthesis and place-and-route tools are used to automate the design flow and to reduce turnaround time for multimillion gate SoC with the use of Standard cell based ASIC design (CBIC) or semi-custom methodology. Standard cells are basic building blocks for the ASIC design and hence categorized as Foundation IP in the company IP portfolio[6].

A standard cell is a group of transistor and interconnect structures that provides a Boolean logic function (e.g, AND, OR, inverters) or a storage function (flipflop or latch). The simplest cells are direct representations of the elemental NAND, NOR, and XOR Boolean function, although cells of much greater complexity are commonly used (such as a 2-bit adder or muxed D-input flipflop). A standard cell library usually contains multiple implementations of the same logic function, differing in area and speed. This variety enhances the efficiency of automated synthesis, place, and route (SPR) tools. Indirectly, it also gives the designer greater freedom to perform

implementation trade-offs (area vs. speed vs. power consumption). You just need to pick the one you need for your parameters and one designer need to focus on the high-level (logical function) aspect of digital design, while another designer focuses on the implementation (physical) aspect. Along with semiconductor manufacturing advances, standard cell methodology has helped designers scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate SoC devices. In semiconductor design, standard cell methodology is a method of designing Application Specific Integrated Circuits (ASICs) with mostly digital-logic features. Standard cell methodology is an example of design abstraction, whereby a low-level VLSI-layout is encapsulated into an abstract logic representation (such as a NAND gate). Cell-based methodology (the general class that standard-cell belongs to) makes it possible for one designer to focus on the high-level (logical function) aspect of digital-design, while another designer focused on the implementation (physical) aspect. Along with semiconductor manufacturing advances, standard cell methodology was responsible for allowing designers to scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate devices (SoC). Standard Cell is a glue logic i.e., it helps in the communication of different blocks present on chip[5]. It is a Basic building block of all digital design which acts as an interface between different blocks.

Fig.1.1.1 represents a broad level ASIC design flow. Based on the specifications, an RTL code is written for the intended functionally using Hardware Description Language(HDL).This RTL code is verified for the functionality though rigorous verification strategy. The next step in the flow is synthesis step. From this step, the standard cell library involvement comes in the picture[4]. ASIC synthesis tool transforms the HDL code into the Boolean network, the Boolean network is optimized for log minimization and in the final step of the logic synthesis process the technology independent.

Boolean network is mapped to network of logic picked from the technology library file (.lib) of the foundry specific standard cell library used for the synthesis. Standard cell library provides wide set of basic combinational and sequential logic functionalities such as basic gates, multiplexer, latch, flip-flop etc. in multiple cell architectures and different drive-strengths. Based on the timing, power and area characteristics specified in technology library file for each cell of the library, the synthesis tool selects suitable cells from the library to meet the specified de-
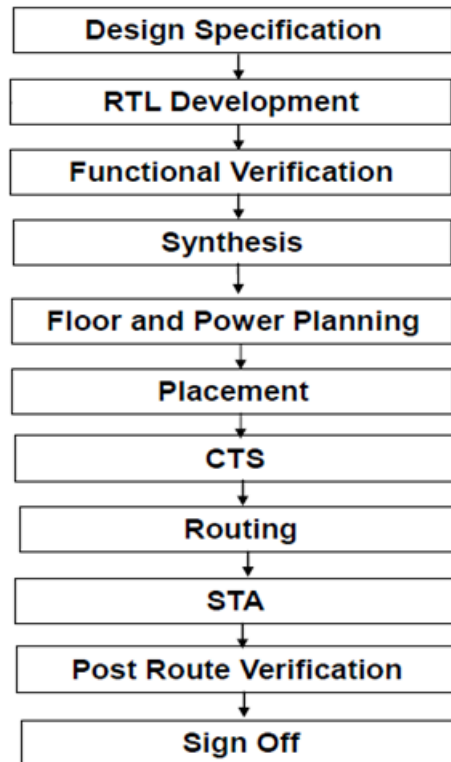
2

Figure 1.1.1: ASIC Design flowchart

sign constraints as an input to the synthesis tools[2]. Once synthesis is done, the next phases in the flow are associated with the physical design implementation. Power network planning and chip level block/macro placement strategy is decide in floor planning and power planning phase. In the placement phase the layouts of the cell developed in the library are placed in chip based on the cell selected by the synthesis tools from the library. Routing phase deals with taking connection out of these standard cells to connect one cell input-outputs with another one through the use of higher metal level global interconnect network. Timing analysis is carried out both before and after clock tree insertion and before/after routing to check whether the design is meeting timing constraint of the chip. During the physical design phase the CAD automation tool uses some cells like decoupling capacitor cells, filler cell, well tie/substrate cells etc.from the standard cell library. After routing physical verification is performed to check chip compliance to the process rules. Sign-off and validation checks are carried out to ensure bug free design before delivering it to the foundry. The standard cell library also provides cells required for implementing various objective specific phases such as design for testability(DFT)
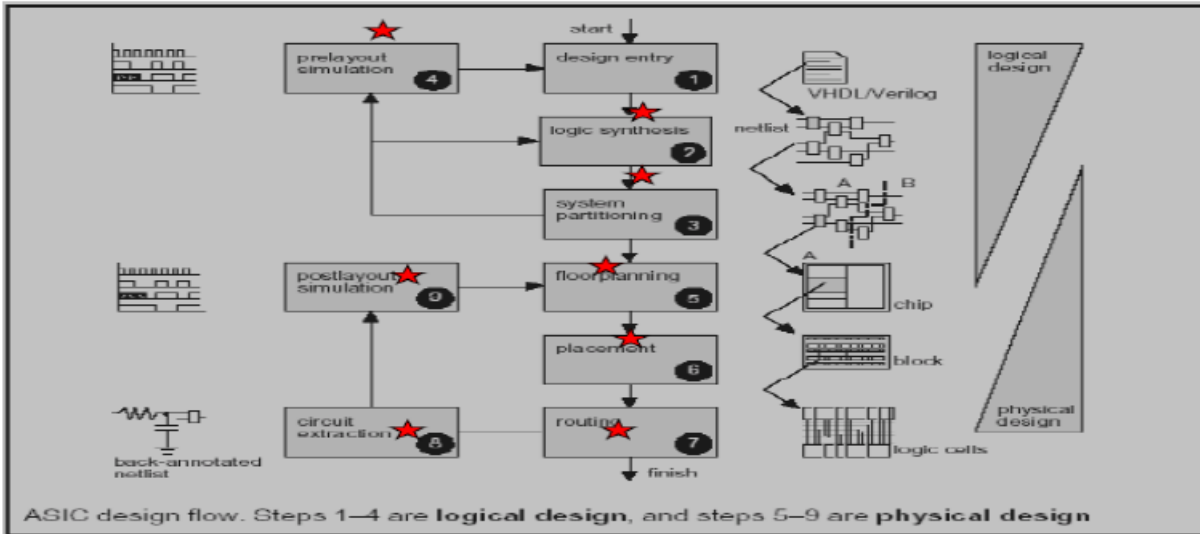
Figure 1.1.2: ASIC Design flow

like scan flip-flops, Low power techniques implementation-level shifters, isolation cells, Engineering Change order (ECO) flow-mask programmable cells, Clock tree Synthesis(CTS)-clock gating cells etc[4].

1.2   Process variation

This variation is due to deviations in the semiconductor fabrication process. Usually process variation is considered as a percentage variation in the performance. Variations in the process parameters could be impurity in concentration densities, oxide thicknesses (tox) and transistor diffusion depths. These are effect of non-uniform conditions during depositions process AND/OR during diffusion of the impurities in device. This introduces variations in the sheet resistance (Rs) and transistor parameters such as threshold voltage (VT). Variations are in the dimensions of the devices, generally subsequent from the narrow resolution of the photo lithographic process[4]. This causes (W/L) variations in MOS transistors. Process variations are cause of variations in the manufacturing conditions like a temperature, pressure and material dopant concentrations.

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1.3   Motivation

At lower technology nodes, bulk CMOS process has increased leakage current and exhibits issues related to short channel effect, process variability and the consequences are the gate is losing control over the flow of electron in the channel. Therefore, lot of other novel devices with good scalability are looked for as a potential replacement candidate for the conventional bulk CMOS process. STMicroelectronicss Ultra-Thin Body and Buried oxide (UTBB) Fully depleted Silicon on Insulator (FDSOI) device is one promising candidate with fully qualified high volume production process available from 2012.

ST Microelectronics, Samsung Foundries, Synopsys, Global Foundries, ARM, cadence, Sony and many more companies are building a strong eco-system to promote FDSOI to develop next generation chips with FDSOI technology with companies having started migrating their IP portfolio to FDSOI.Therefore, a versatile range of foundation IP portfolio like standard cell library, memory, I/O IPs are required to cater high performance SoC design enablement in FDSOI technology. ST Microelectronics being key player with the process foundry support is committed to develop extensive FDSOI foundation IP portfolio with wide range of standard cell libraries available for high performance, low power, low leakage, high density requirements of ASIC/SoC design in FDSOI technology. The motivation behind the project is to add a new high density standard cell library in 28nm FDSOI technology foundation IP platform to cater low area requirement.

1.4   Objective

A highly optimized library for given application would yield best synthesis results and the design constraints would be perfectly met for the overall chip level area, power and delay requirements, hence choosing the right library for the specific design constraints from the vast libraries available for different vendors is very crucial for the overall chip because vendors have extensive range of library portfolio of speed, power and area optimized libraries with different low power solutions such as poly bias, body bias, multi threshold voltage embedded for speed/power optimization.From the foundation IP development companys perspective,[5] The

aim is to deliver:

- A perfectly optimized cell library with strong cell offer with good cell utilization numbers and best in the class benchmarking results for the particular power, speed, density requirements.

- Increased process manufacturability and lithography related issues at lower technology nodes demands a robust library with clean design for Manufacturability (DFM) by construct providing good yield numbers is key for the success of the library.

- To validate the behaviour of the cell at different process corners, temperature and voltage.

- To validate that whether the cell is implementing the same logic that we expect form it or not.

1.5   Overview of the Thesis

In this thesis,

Chapter 2 is the Literature Survey where there is discussion about the basic overview of standard cell library. about template and its routing grid and some standard calculation and also cell template structure.

Chapter 3 discusses about Functional validation, in which discussion about monte carlo and cross corner along with its use and need is described.

Chapter 4 contains conclusion and Future work.

Chapter 2

Literature Survey

This chapter describes the detailed approach and methodology followed for standard cell library development at different technology nodes. The chapter also gives the overview of the structure of the standard cell library and various flavors available for customer offering depending upon the usage specifications.

2.1 Standard cell library template

Standard cell library is a collection of basic building logic functions available for synthesis/-Place and route CAD automation and reuse enabling quick ASIC turnaround. The most prominent feature of the standard cell library is that all logic functions are of same cell height and different width.[6] Keeping cell height constant enables standardized placement and routing of the cell at SoC level and provides design uniformity.Therefore, standard cell libraries are designed using fixed cell template which is frozen at very early stage before starting actual development based on the library specification and aimed usage.

2.1.1 Cell template definition

This sub-section gives idea about various aspects looked upon to arrive at the cell template for the library. The standardization of the cell template is achieved by using a standard grid which enables ease in overall place and route by CAD tool at SoC level. The grid ensures the fact that
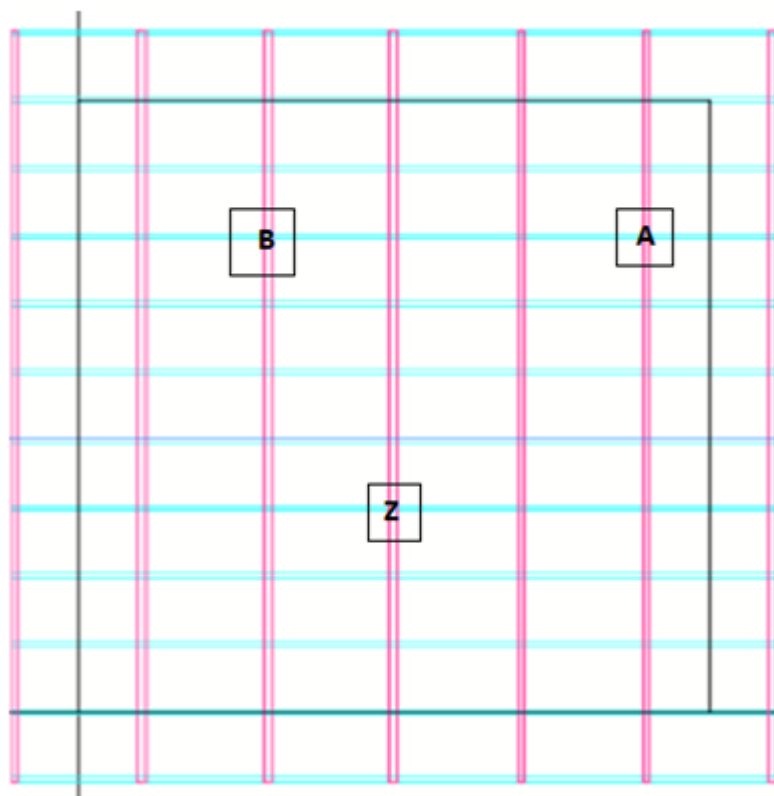
Figure 2.1.1: standard cell template routing grid

if grid alignment and rules are taken care by the designer during design than the design will be correct irrespective of tools routing decision. Routing and placement grid is used in standard cell library development because the algorithms followed by CAD automation tool use grid based routing and placement strategy.[6] The rectangular box at origin is called place and route boundary and it is a bounding box describes the cell boundary in both horizontal and vertical direction. Horizontal green lines represent center to center distance between two metal. This is a technology dependent and foundry specific parameter and is called metal pitch or metal track. Total no. of metal pitches/tracks or horizontal metal routing grid within the cell PR boundary is called total tracks or cell height. This parameter is fixed for entire library and gives basic characteristic name to the library. This factor tells maximum number of metal routings can be done to connect various transistors and nets within the individual cell.

Red vertical lines in fig.2.1.1 are drawn for pin accessibility at chip level, wherever red and green lines intersect input output pin of the cell can be placed there to provide chip level access through higher metal. At chip level, cell pin routing with other cell is done through higher metal
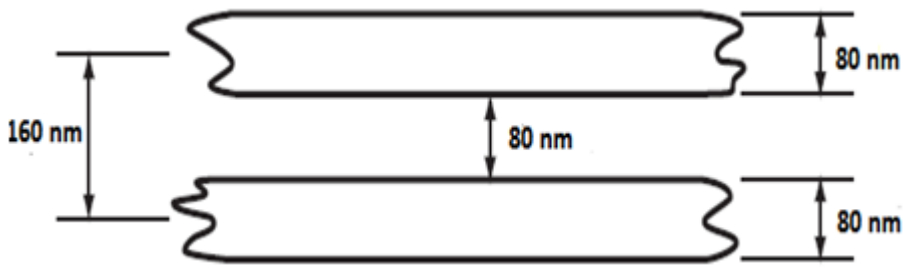
Figure 2.1.2: horizontal metal routing grid calculation

layers and power mesh network. Conventionally, metal1 acts as a local interconnect in the cell and can run in both horizontal and vertical direction but higher metal layers like metal2 and metal 3 and so on based on available device technology metal stack, are global interconnects and are used for chip level interconnection and power mesh formation hence fixed for running at a particular direction either horizontal or vertical for ease of chip level routing and guaranteed cell accessibility. The red and green line intersection is called pin hit point, this approach ensures the part of the metal used for pin formation runs totally on the grid for required distance so that the global interconnect network strictly running on routing grid formed by CAD tool can decide the possible routing strategies for accessing the pins inside the cell., this kind of arrangement reduces the possibility of congestion at chip level. Suppose metal 1 width and spacing for x nm technology is 80 nm, so total distance for two parallel metal 1 at minimum width and spacing requires 240 nm.Center to center routing grid or the metal pitch is of 160 nm in template for x nm technology as in Fig.2.1.2

 Fig.2.1.3 shows standard cell placement grid where thin red rectangular bounding box is PR boundary. It should coincide with the vertical white lines so the cell width is aligned with the white line spacing. This grid used by tool during cell placement Vertical white lines represent center to center distance of polysillicon layer-a layer used to draw the NMOS and PMOS transistors in the layout. This parameter is called as poly pitch and it depends on the process technology and foundry. The individual cell width of all cells in the library are integer multiples of the poly pitch with the constant height represent by the track number. So, the dimensions of the cells and library can be summarized as follows:

Width of the cell = n (variable) X poly pitch in nm Height of the cell = no of tracks (constant) X metal pitch in nm = constant number for the entire library
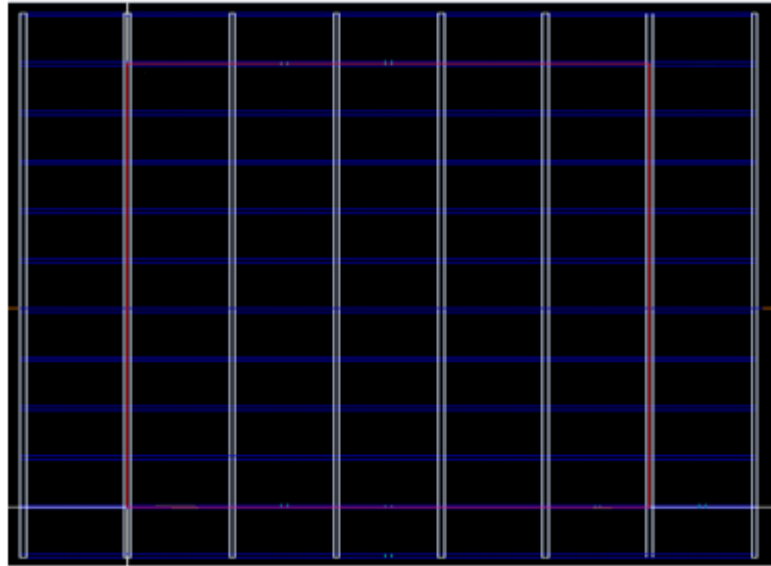
Figure 2.1.3: standard cell template placement grid

2.1.2 Cell template structure

Along with the grid standard cell library is developed using a fixed template across all the cell, the characteristics of the template is discussed here. Firstly, the template has fixed width of VDD and GND rail. VDD is at the top and GND is kept at the bottom of the cell. Power rail is width is fixed higher than the normal metal routing width to cope up with electromigration and reliability issues because VDD and GND rail carry high current density due to the fact that when cells abut the power rails becomes continuous running for the large distance across the entire cell row.[4] Electromigration effect causes eventual loss of metal connection, causing opens over period of time due to momentum exchange between ions and metal atoms.Metal usage strategy M1 or M2 or both or other- for power rail is decided based on elctromigration effect and the rail metal width is also constrained by process rule.[3] Power rail width and metal number selection also depends on the maximum allowable IR drop or maximum allowable current for unit power rail width and is determined using the sheet resistance of different metal numbers from the design rule manual. Thick higher metal rail gives more protection for electromigration effect,but in case if higher metal used than via placement strategy also needs to be fixed and the chip level global interconnect network metal number strategy changes accordingly. The cells get abut in both vertical and horizontal direction and both rails should merge or overlap during

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abutment across different rows, therefore it is good practice keep half of the total metal width decided for power rail in one cell and half width outside the PR boundary. The vias placed on the power rail in case of higher metal number usage must get aligned or superimposed in accordance with the process via placement rules during row to row abutment.[6] Cell library is a collection of low-level electronic logic functions such as AND, OR, INVERT, flip-flops, latches, and buffers. These cells are realized as fixed-height, variable-width full-custom cells. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The cells are typically optimized full-custom layouts, which minimize delays and area A typical standard-cell library contains two[6] main components:

- Library Database : Consists of a number of views often including layout, schematic, symbol, abstract, and other logical or simulation views.

- Timing Abstract : Generally in Liberty format, to provide functional definitions, timing, power, and noise information for each cell.

The implant layers, marker layers and other overlapping layers at the time of abutment, are fixed to be drawn for the particular distance from the PR boundary during the template fixture phase to maintain standardization across the cells and to facilitate ease of abutment as given in Fig.2.1.4. A represents the VDD and GND power rail width. B gives N well dimensions for all the cell across the library and F marks N well extension length. C shows the P implant length and E depicts the extension of the implant layer from the PR boundary. D represents N implant length, N implant is also extended by distance E to maintain uniform structure. G describes the rail extension from the cell boundary done for the rail abutment purpose. x and y are the standardized grid coordinates superimposed on the layouts. This cell architecture is documented in product release notes along with the exact dimension and other physical layers information. Since PMOS in connected to VDD and NMOS is connected to GND, PMOS is formed at the top and NMOS layers are drawn at the bottom in the layout.Because of this fact a common continues N well is used in the library, The reason behind this approach is the fact that N well spacing rules require more space between N well as compared to active devise to devise rules as shown in Fig.2.1.5.
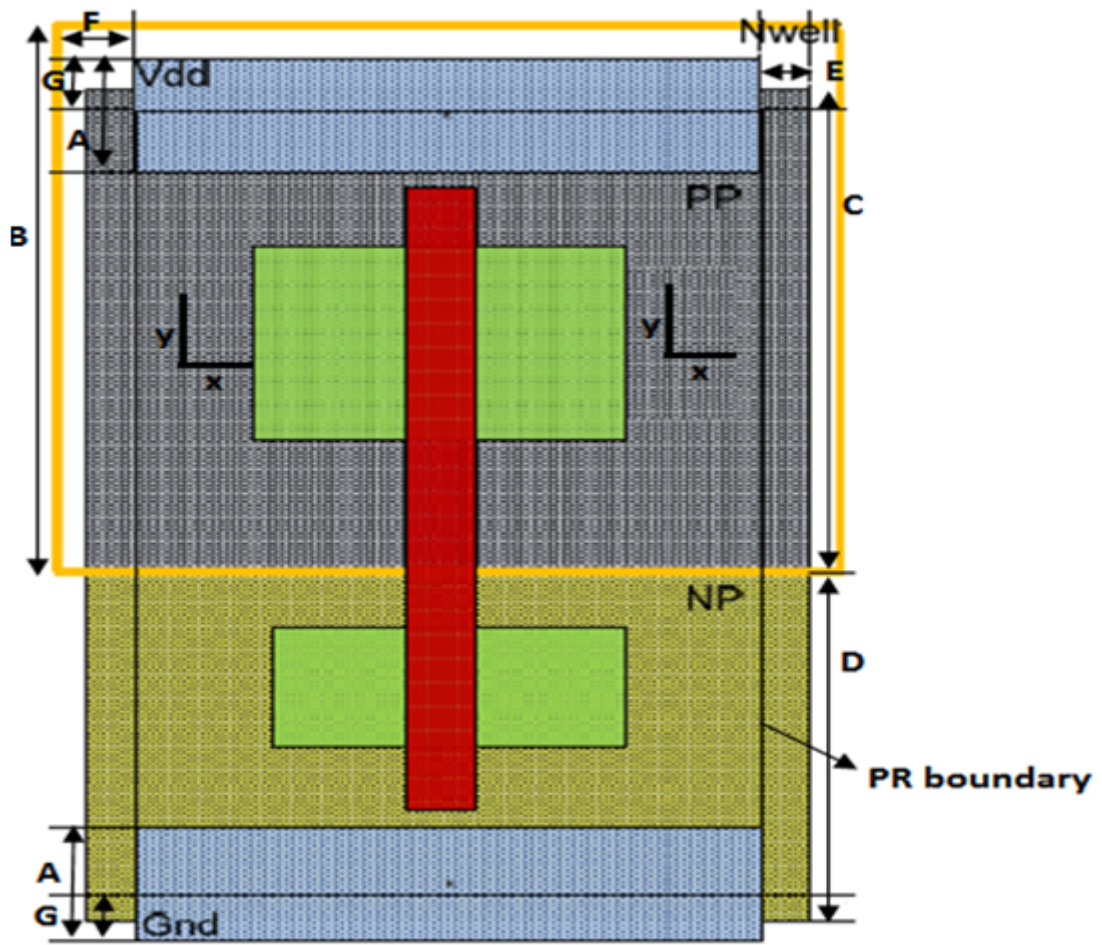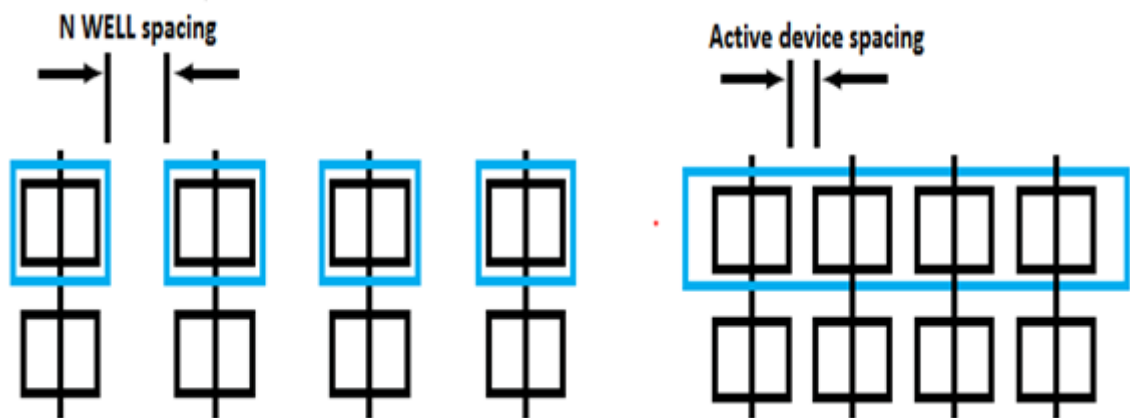
Figure 2.1.4: Standard cell library template

Figure 2.1.5: common continuous N well approach

2.2 Standard cell library offering

Based on technology along with power, performance and area requirements library design companies offers wide range of cell libraries as a part of their library IP portfolio. The section describes various types of library offerings and classifications.

Intended application based library offering classification

Based on the intended chip level usage i.e. power, speed and area requirements libraries are classified as follows:

- High performance/speed library

- High density library

- Ultra high density library

High performance libraries are used in speed critical requirements and usually designed with higher number of metal tracks with higher transistor width at around 12 track, 14 track etc. High density library is intended to be used in mainstream application and offers good balance between speed, density and power designed for 9,10 tracks.[4] Ultra high density libraries are designed for smallest cell heights among the entire portfolio and used for area and cost critical applications, typically designed in 6 track or 7 track etc.As leakage power has become very critical issue for lower technology nodes along with extreme need for low power, various low power techniques such as multi-Vt, multi-channel, poly bias, body bias techniques are embedded as a part of standard cell IP solutions strategy by companies. Threshold voltage flavors such as High Vt (HVT), Regular Vt (RVT), Low Vt (LVT) along with multi-channel, multiple gate length options are used for designing the library to achieve efficient speed leakage optimization[6].

Library classification based on function

Based on the functionality classifications are:

- Core library

- Clock library

- Place and route library

- ECO library

- Low power cell library

- Special purpose flip-flop library

Core library: core library is the basic library consisting various combinational logic cell such as inverter, buffer, basic gates, multiplexers, different complex logic functions from the AOI and OAI family, latch, flip-flops, full adder, half adder etc. with different drive strength and different cell specific architectures for speed, power and area optimization. Clock library: It consists of special cells design for the use in clock trees with balanced delays, balanced buffers and inverters for set up and hold time optimization, various architectures of clock gating cells.[3] Place and Route library: this library is used by CAD tool during physical design phase and consists of filler cells and decoupling capacitor cells.

ECO library: Engineering change Order (ECO) is methodology facilitate cost effective design changes for the timing optimization before the masks are made, the library consists of mask programmable cells with floating input outputs to make any logic functions.

Low power Library: with different lower power techniques such as multi-vdd, multi threshold techniques being implemented at chip level special cells like power switches, isolation cells, retention flip-flops, level shifter cells are required .The low power library consists of these cells with different architectures based on specific requirements.[2] Special purpose flip-flop Library: flip-flops are used in higher utilization factor at chip level, so wide range of flip-flop architectures such as dynamic flip-flops, bank flip-flops, radiation hardened flip-flops, multiple types of flip-flop architecture for setup and hold fix, flop synchronizers for metastability fixes are provided in this library.

2.3 Design approach

The width of the NMOS and PMOS devices are constrained by the cell height of the library. The maximum device width for the cell is known and multi fingered cells are made to facilitate

high load drives. Usually for inverter and buffers more drive options are provided along with that the basic logic gates like NAND,NOR,AND,OR are provided with more drive strength because of their higher utilization factors at SoC level. Complex logic functions can be efficiently realized by different configuration of multi-level logic as compared to realization using basic logic gates, the logic includes AO (and-or), AOI (and-nor), OA (or-and) OAI (or-nand) logic where multiple gates packaged as one gate, effectively reduces the delay .Logic optimization tools widely use these cells to realize sum of product (SOP) and product of sum(POS) forms faster and with reduced area as compared with basic gates[4].there are total 56 different logic configurations available for these four types of logic family,based on the utilization the configurations to make are decided. Apart from these cells various basic gates flavors with inverted inputs such as two input NAND with inverted input A, three input NOR gate inverted B and C inputs and other similar configuration are given in design offer aimed at performance, power and area optimization through increased cell picking efficiency of the synthesis tool. Some cells are made with more than on variant for the same drive strength intended for various power or performance or area optimization. XOR cell can be made in more than one architecture based on Boolean optimization, so speed optimized variant of the cells can be offered. Power optimized version of various cells are made using device width reduction with a slight penalty in terms of delay. Area optimized versions of some cells are made using layout level routing tweaking along with reduced device widths or by using lesser transistor architecture. Speed, Area and power optimized cell version are cell logic specific and is not present across all the cells in the library. There are two approaches to make higher drive strength cells using multiple transistor fingers:

- Finger approach: In fingered approach higher drive logic cells are made just by multiplying the device width by a constant factor, i.e. by adding constant parallel devices of the same widths for all the device in the cell schematic. So, n number of fingers addition for all the transistors of the cell gives x drive. This approach requires more area for higher drive cells for some logic functions as compared to buffered approach.

- Buffer approach: . In buffered approach, 1 or 2 finger cell logic is followed by higher finger buffer to obtain the x drive. Significant area saving is obtained because higher drive

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buffers requires less number of transistors as compared to multi fingered logic functions where all the transistors required to design the cell are multiplied by constant number. For some cells buffered approach gives more delay with good area saving, thus the better approach among two is entirely cell logic specific.

A stage ratio between 2-3 is followed for designing the schematics for better speed optimization.Therefore, two staged circuits such as AO12C have x width of NMOS/PMOS in the first stage followed by 2x width in the second stage where in first stage output is given as input to one of the transistor of the second stage. Even inverters and buffers used in 2nd stage of the higher drive have 2x fingers than first stage. For example, 6 finger AND two input structure has 3 finger two input NAND followed by 6 finger inverter.

Chapter 3

Statistical analysis

Depending on the threshold voltage every MOS can be Slow, Typical, or Fast. Here the lesser threshold voltage requirement corresponds to fast and opposite to that for slow. Typical is a state where we consider room temperature or behaviour at standard condition. We use this analysis to validate the outcome at different condition to check the behaviour of Mos at different condition which gives us a large amount of data for each and every delta change in possible input and condition. From that Gaussian graph can be plotted which shows its deviation from nominal value and how much can be tolerated is defined from that.

3.1   CMOS Inverter

Given below is a CMOS inverter, we'll take this inverter into consideration and try to understand validation.

3.2   Transistor behaviour

If we think about the quality of transistor with respect to it's performance we find that "A transistor with smaller oxide thickness, smaller length, smaller threshold voltage" The variations cause a small shift in the switching threshold, but that the operation of the gate is not affected. Process variations (mostly) cause a shift in the switching threshold.[1]
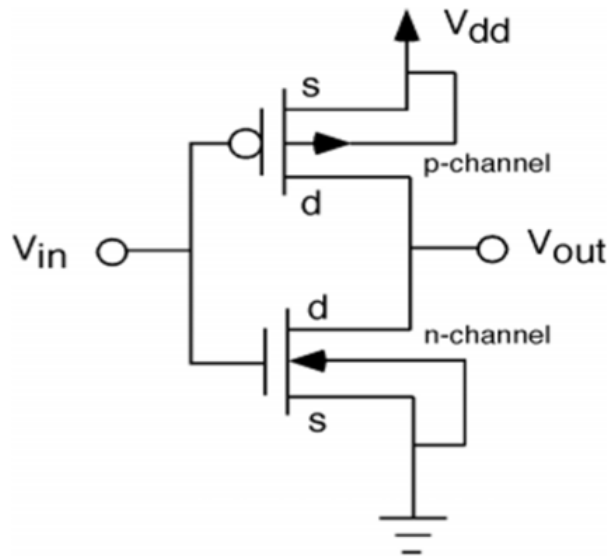
In MOSFET, following parameter can vary

Figure 3.1.1: CMOS inverter

- Oxide thickness.

- Doping concentration because of that Vt (threshold voltage) can vary.

As we know that A CMOS is made up of PMOS and NMOS. In CMOS inverter nMOS and pMOS can be fast or slow or typical.

- SnFp - SF

- FnSp - FS

- FnFp - FF

- SnSp - SS

3.3 Monte Carlo Analysis

The small random variations (Device Mismatch) in the characteristics of identically designed devices, occur during the manufacturing of ICs. These mismatches result in behavior change of ICs. It is difficult to predict the behavior of a circuit due to the combination of the mismatch errors of individual devices. The impact of these random parameter variations on circuit behavior
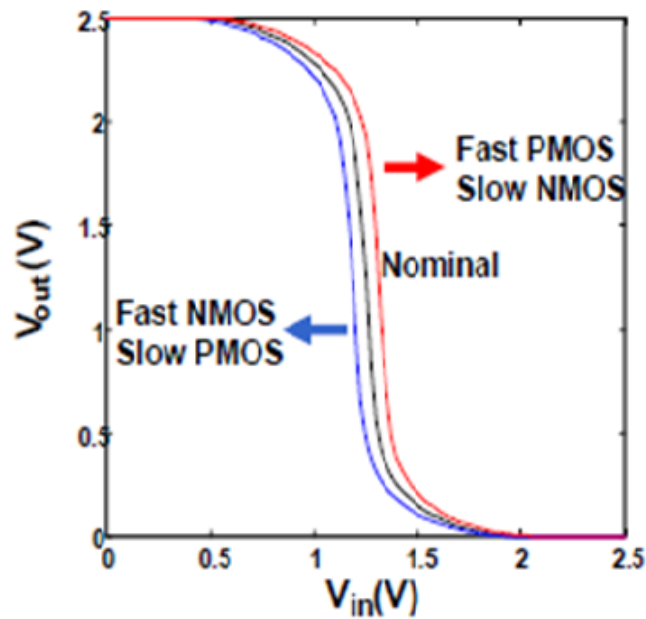
Figure 3.2.1: V-I Graph

can be studied with Monte Carlo simulation by analyzing a large set of circuit instantiations with randomly varied devices. As technology is scaled down to leading edge nodes (28nm/14nm or below), chip design engineers face numerous challenges in maintaining the historical figures of performance improvement and the density increase.[2] Performance of the chip, its lifetime and the product yield cannot be determined accurately at the design stage since the chip parameters-such as impurity doping and oxide thickness- cannot be precisely resolute. Process variation is one of the perilous aspect of semiconductor fabrication which impacts the chip performance, yield and the reliability. Process variation is basically defined as the variance in the intended design parameters and the actual (fabricated) design parameters of a circuit and hence reduce the reliability and yields of chip designs. The relationship between parameter variation and the yield can be viewed in this figure. It shows the Gaussian distribution of a particular specification with standard-deviation "" around the mean "" with the specification limit of (68.3% pass range) 3 (99.7% pass range). Beyond the specification limits, the shaded portion represents the failure range. It is important to use such design methodologies which consider the impact of process variation, environmental variation and the uncertainty in temperatures on the chip performance. To ensure the functionality of the design on silicon one must be able to replicate
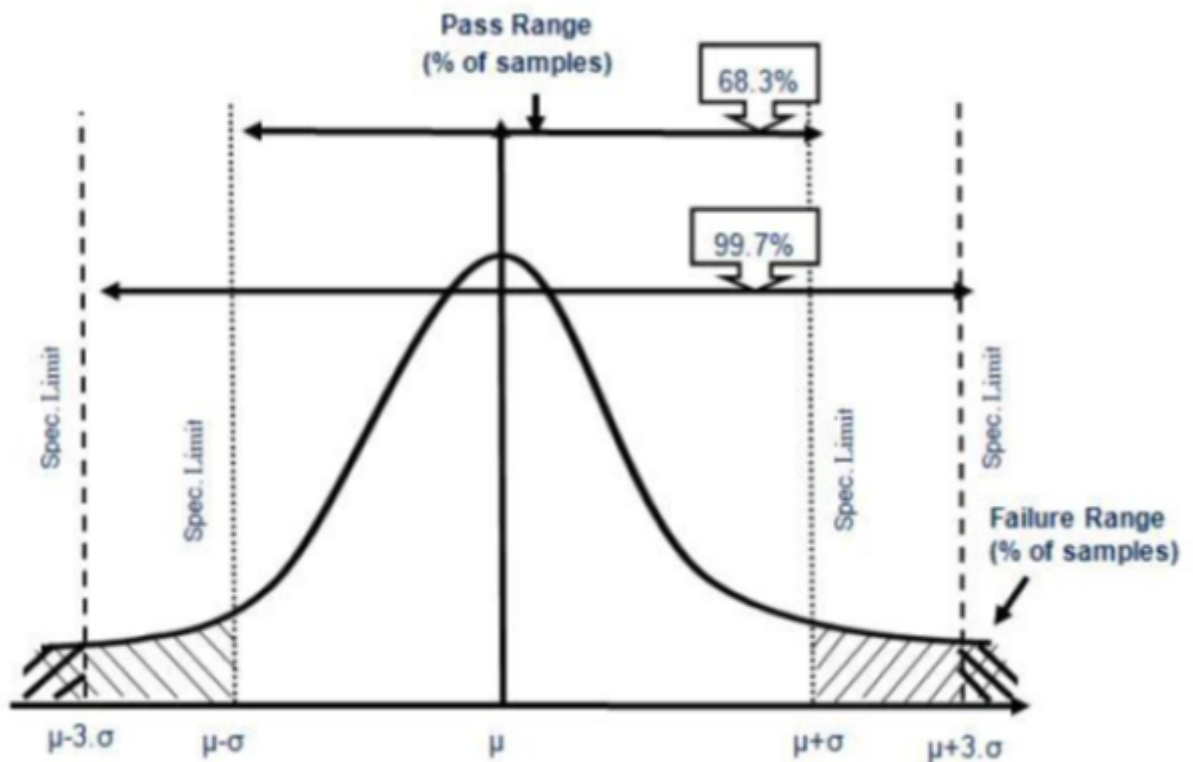
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Figure 3.3.1: Relationship between parameter verification and yield

the variability on CAD tools in order to predict the yield. In other words, the design tools and the methodologies from system level down to physical level have to embrace variability impact on VLSI chips which requires "Statistical-analysis". For advanced processes, number of corners have expanded which leads to increased design efforts and prolonged time-to-market. Pre-defined corner simulations cannot predict the product yield as they characterize worst case corner only and are pessimistic in nature.

Monte-Carlo analysis is one of the efficient technique of statistical analysis.[2] The main aim of Monte-Carlo simulation is to determine the dubiety in the circuit performance owing to random variation of the input circuit parameters. It focuses on how the vulnerability of input parameters propagates through the computations in the circuit and impacts its performance. In process variation, device mismatch plays a key role and can be only considered by monte-carlo simulation in any kind of analysis. The input parameters for Monte-Carlo simulation are process parameters, environmental conditions and the various design parameters. The circuit performance can be defined as a measure that is .extracted from the circuit simulation. Considering Monte Carlo

(MC) analysis, designers have to run a large number of simulations in order to guarantee the functionality of a design and thus yield on silicon. MC simulations are complex to run with true SPICE due to time complexities. To ensure the execution of MC analysis more practical to make the circuit validation process more robust, there is need for a solution that provides faster performance with reasonable good accuracy.[3]

In VLSI circuit design during simulation, we run the design through various PVT (Process,voltage and Temperature) corners with an aim that the circuit should be able to reliably operate at all the extreme conditions. These PVT variations can be generalized as,

- Temperature from as low as -40 to as high as 125C.

- Voltage 10% variation from its nominal value

- Process This is generally two letter convention where first letter is the behavior of NMOS and second letter is of PMOS. TT, SS, FF, SF and FS are the corners generally used. Letter T stands for Typical (Nominal VT), F for Fast (Low VT) and S for Slow (High VT).

Why do we need monte carlo?

Running the design over different PVT corners cover the environmental variations (voltage and temperature) as well as manufacturing variations (process). A very common figure to illustrate the process corner is shown here,Now we can't guarantee the functionality of silicon across all condition by simulating the design across PVT corners." Its the manufacturing variations introduced during fabrication of the chip. here we have covered the manufacturing variations in the process corners (TT, SS, FF, FS and SF), but thats not enough.[4]

Now we consider a scenario, where we have a design which has 1000 NMOS and 1000 PMOS. Lets say we are running this design at FS corner, considering all the 1000 NMOS are identically FAST and all the 1000 PMOS are identically SLOW. This is not true in real silicon where no two transistors are identical due to Systematic and Random variations. So even after running the design across process corners we are leaving behind the corner case where there is variations across different transistors in the same process corner.

This is where Monte Carlo comes into picture. It aids in introducing the randomness into the

transistors by changing its VT in different directions such that all the 1000 NMOS/PMOS are different at a time, depicting the real silicon behavior. Industry-wide, the MC corner files itself are different than the usual process corner files for the reason that the variations at MC corners are different than the process corners hence one should avoid the mistake by running the MC at process corner, which will not be able to hit the worst case for above mentioned reasons.

How does it work?

The Monte Carlo simulations can be done in two ways for any given design, Global Monte and Local Monte. Again the corner files for these two will be different. These are:

- Global Monte: We can think of this Monte run as unconstrained in a way that the variations in this case can span over different process corners.
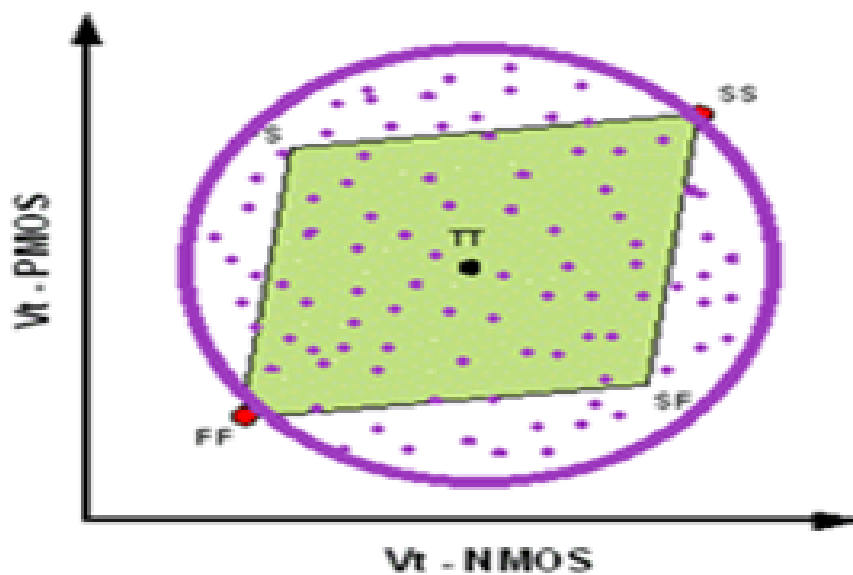
Figure 3.3.2: Dot represents one Monte Carlo run

In the figure 3.4.1, each dot represents one Monte Carlo run and as we can see it will spread the variation by introducing a VT change in its every single run. The span of the variations in this global Monte run is spread across the process corners as its name also suggests, Global MC.

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- Local Monte: This Monte run is constrained to a particular process corner. In general, first step is to run the design at various PVT coroners to find the worst one. Then second step is to run the Monte on this particular corner to see the functionality on worst of worst corner. Let us say the worst corner in the first step was found to be SS then the Monte variations will look something like this fig.3.4.1, this is Local Monte as the scope of variations is limited to a particular corner.[5] Both the methods have their own set of
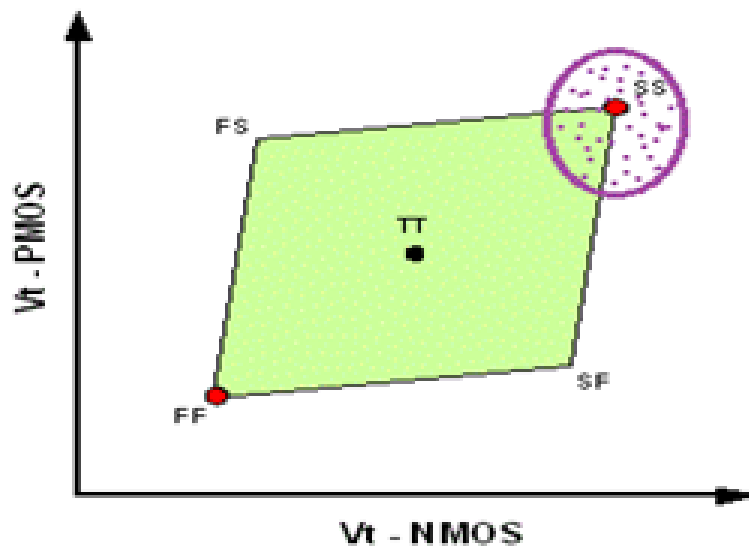
Figure 3.3.3: Vt - graph for Local Monte

applications and used across industry to emulate the silicon behavior during simulation and have a working silicon in one go.

3.4 Cross Corner

Corners Analysis is performed to simulate your circuit's performance against a set of parameters belonging to extreme manufacturing variations. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does

not function at all at any of these process extremes the design is considered to have inadequate design margin. In order to verify the robustness of an integrated circuit design, semiconductor manufacturers will fabricate corner lots, which are groups of wafers that have had process parameters adjusted according to these extremes, and will then test the devices made from these special wafers at varying increments of environmental conditions, such as voltage, clock frequency, and temperature, applied in combination (two or sometimes all three together) in a process called characterization.

Corner-lot analysis is most effective in digital electronics because of the direct effect of process
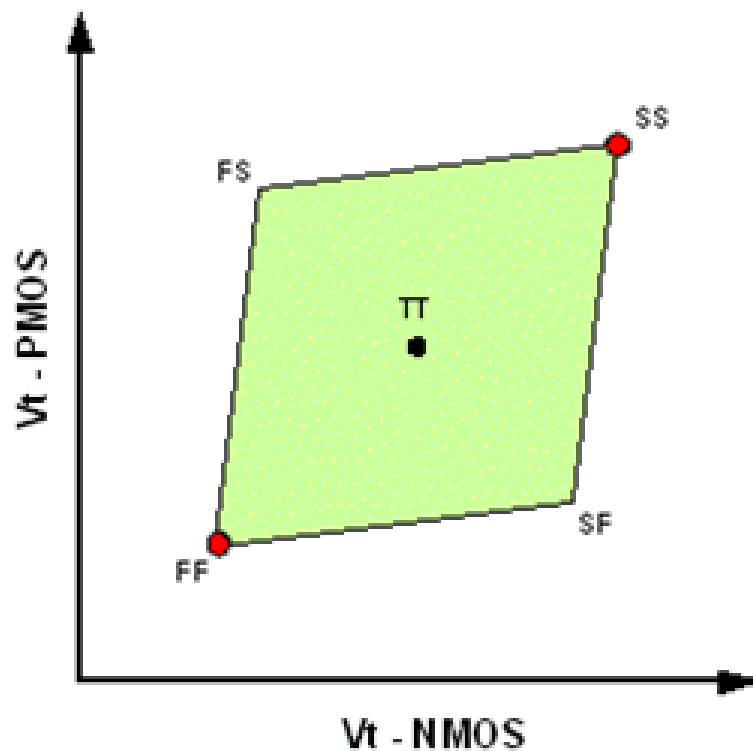
Figure 3.4.1: NMOS vs PMOS Graph

variations on the speed of transistor switching during transitions from one logic state to another, which is not relevant for analog circuits, such as amplifiers. In Very-Large-Scale Integration (VLSI) integrated circuit microprocessor design and semiconductor fabrication, a process corner represents a three or six sigma variation from nominal doping concentrations (and other parameters) in transistors on a silicon wafer. This variation can cause significant changes in the duty cycle and slew rate of digital signals, and can sometimes result in catastrophic failure of

the entire system.[4]

Variation may occur for many reasons, such as minor changes in the humidity or temperature changes in the clean-room when wafers are transported, or due to the position of the die relative to the center of the wafer.
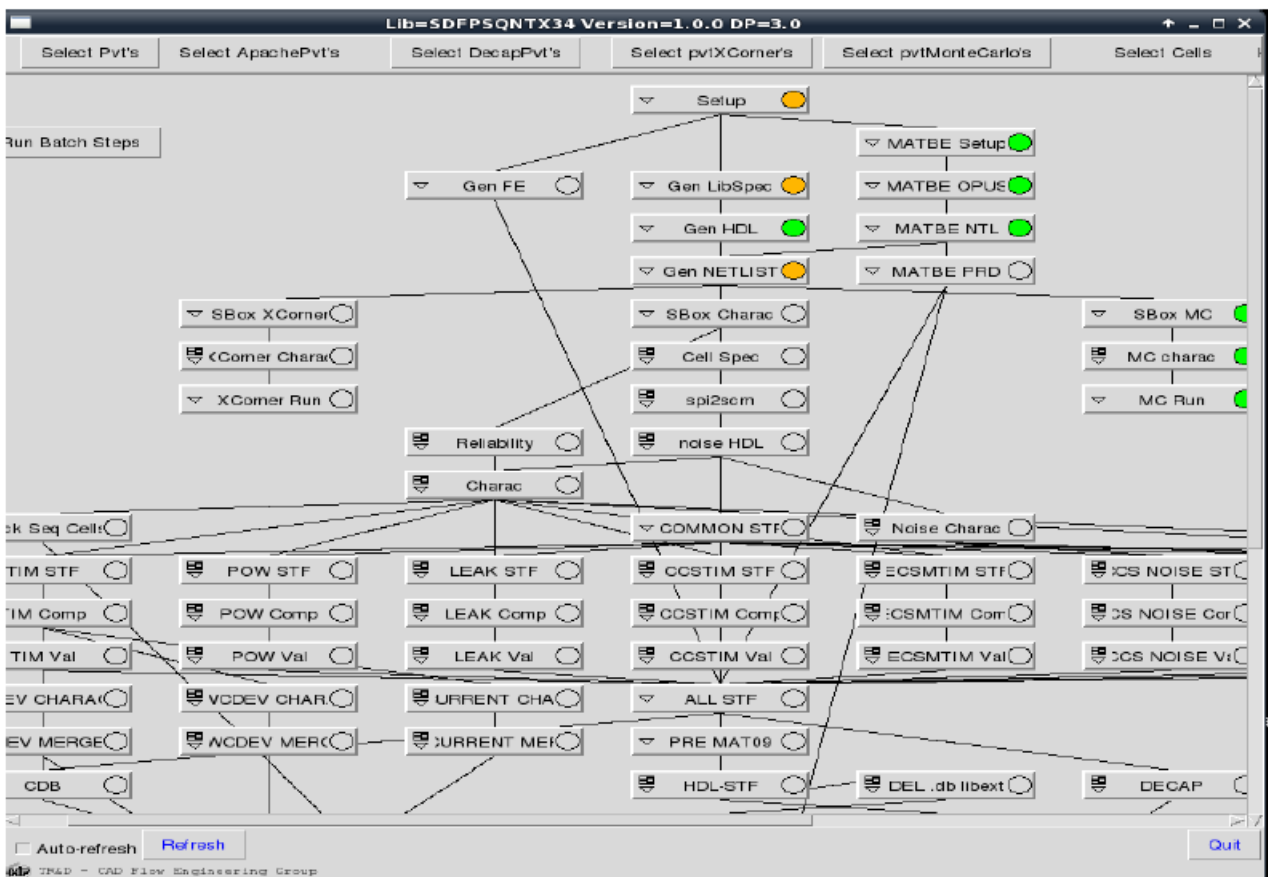
3.5   Tool used in simulation

3.5.1   Weblib

Figure 3.5.1: Weblib Gui

It requires the folowing file for weblib [6]

- Input directory : It contain the input files that required in the weblib.

- Weblib.conf : It will set all the path of input file.

- Command : bsub -J weblib -q lowjobs -R "rusage[mem=10000]" -P weblib -oo weblib.log -eo weblib.err weblib -maxGmakeProcs 50

  - -J : Job name

  - -q : Queue for Job

  - -R : Reverse swap memory for weblib

  - -P : Project name

  - -oo: Create weblib log file

  - -eo: Create weblib error file

  - -maxGmakeProcs : Maximum parallel process execute

Chapter 4

On chip process monitoring

4.1 Process monitoring box

When we check the behaviour of design on a post layout netlist then we consider the behaviour of cell on different prosess corner (FF,SS,SF,FS,TT). But at the time of fabrication it is obvious that the threshold of any two MoS can never be equal due to fabrication variation in width of cell, In this case we have to analyze that the process corner of the cell is same as we expected or not due to this variation in fabrication.[6]

4.1.1 Overview

In order to verify this we use PMB (Process monitoring box) where we try to make use of group of cell to make an oscillator and then from this chain we try to find out frequency and from that frequency output we decide that this frequency belongs to which process corner.

4.2 Working

the below given diagram in Block diagram of Process monitoring box. as we can see this block diagram includes two oscillator [6] 1. Logic ring to measure logic speed. 2. Logic + interconnect ring to measure logic and interconnect speed.
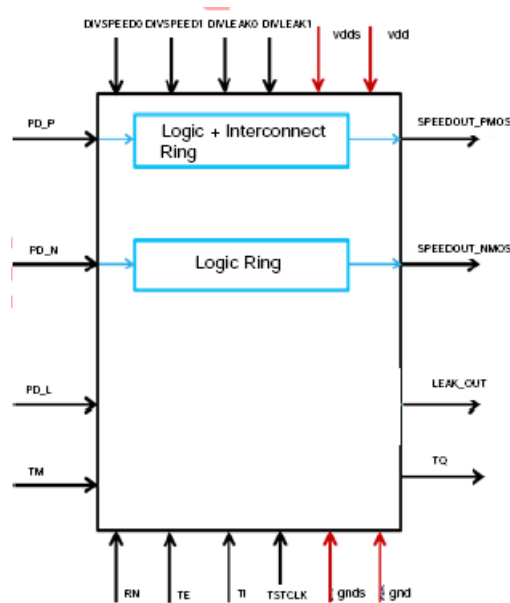
Figure 4.2.1: Block Diagram of Process Monitoring Box
[6]

4.2.1 Cell chain and MOS structure

In order to find the frequency, we need to make oscillator from that cell which is under test eg:- if we want to find out frequency to detect process corner of a NAND gate we need to make oscillator from that gate and arrange it in series as shown in diagram. From this type of arrangement we can monitor process and interconnect of 28nm FDSOI platform. [6]
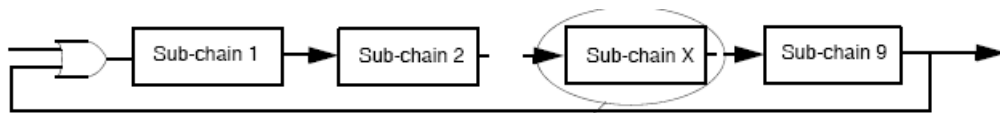

Figure 4.2.2: Cell chain

In the given Mos structure P1 and P3 becomes ON when we give '1' as IN and it charges the capacitor but when we give '0' both the nMos becomes ON and they discharges the charged capacitor and this process goes on and it start this charging and discharging process again and

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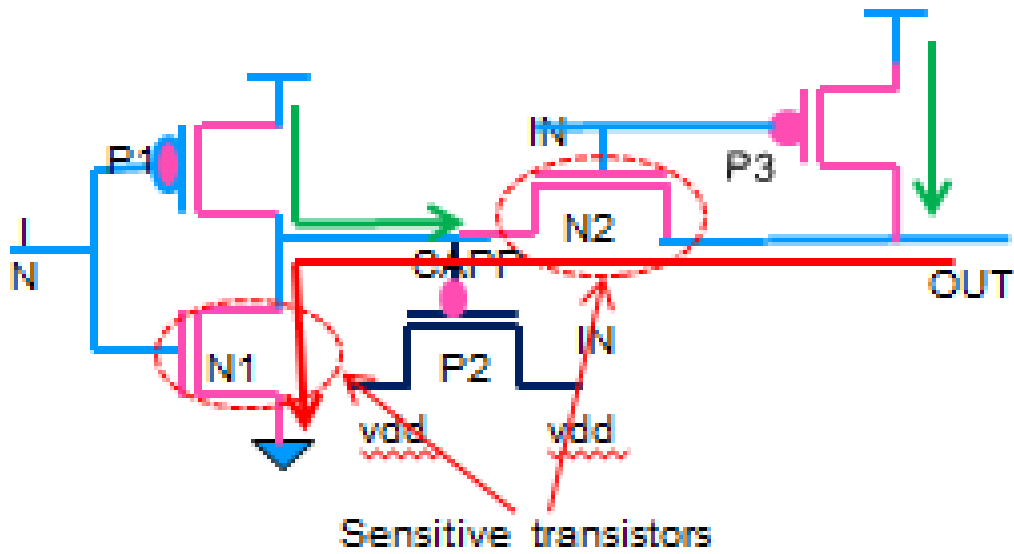again which makes it works like an oscillator.

Figure 4.2.3: MOS structure

4.3   Function of arrangement

The above given Mos structure is used in the place of Logic Chain of functional diagram which works as an oscillator which one output is connected to one pin of NOR gate and the other pin PD_N is connected to active low to enable the logic ring.

which gives us frequency output SPEEDOUT_NMOS.[6] And after plotting this output we can make decision about working process corner of the cell.
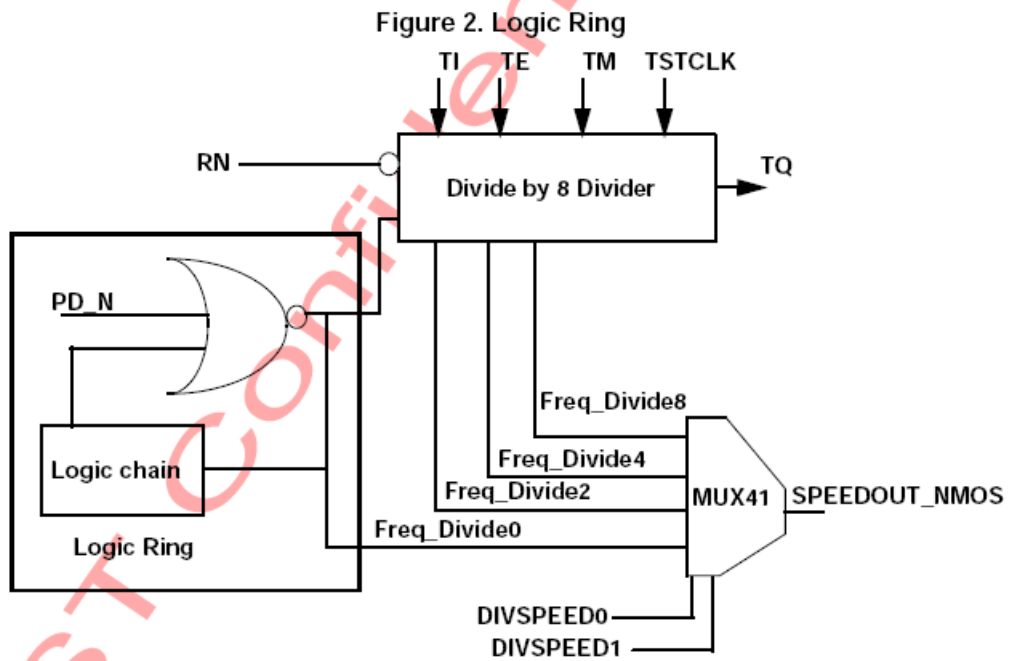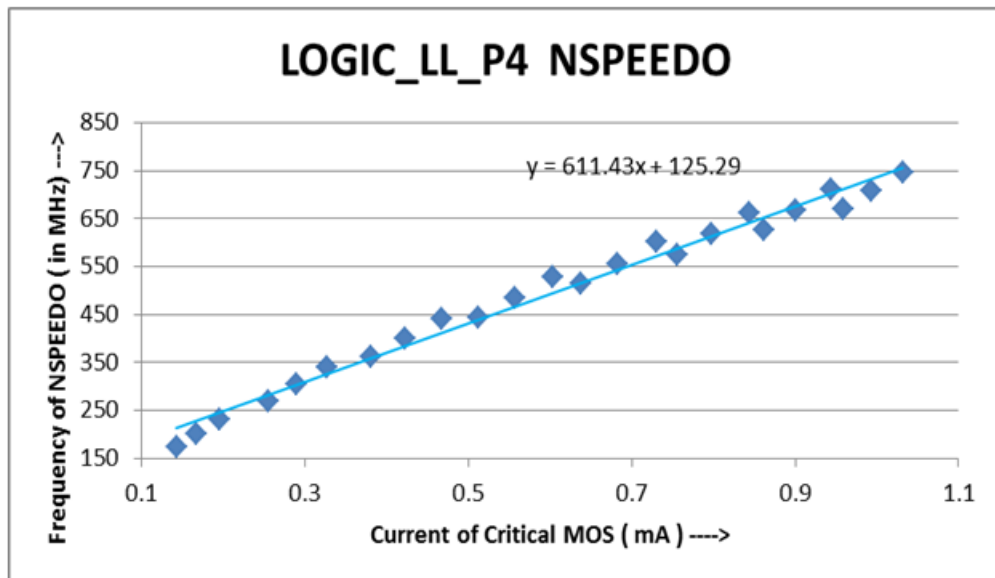
4.3.1   Result

Figure 4.3.1: Functional diagram
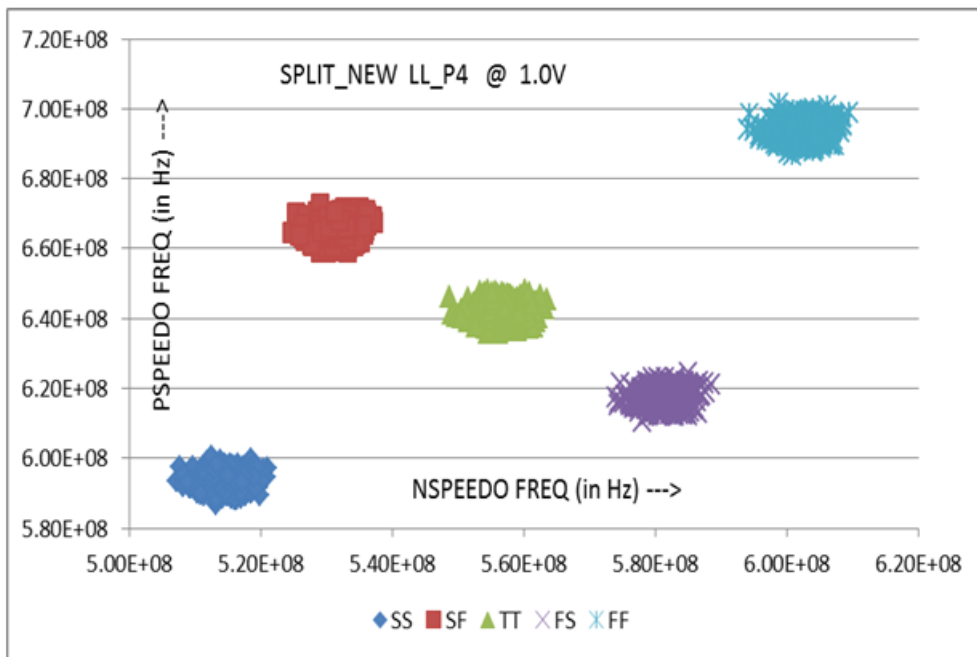

Figure 4.3.2: Frequency from PMB

Figure 4.3.3: Process corner corresponding to Frequency

Chapter 5

Conclusion

5.1 Conclusion

Hence, we know that validation of standard cell library is an important part of SoC synthesization. The semi-custom based approach is most widely used design approach for ASICs. the standard cell libraries are the heart of semi-custom ASIC design. The creationof standard cell libraries was the objective of this work. The library creation involves two major steps i.e. characterization of standard cells and packaging them in the form of .lib along with documents. The complete characterization and packaging is analyzed. Also the methodologies used for delay, power, input capacitance, etc. are analyzed. SOC.It is required to have multiple variants of standard cell optimized for particular aspects.We need to design as per customers requirement(i.e. power,area).Process variation plays important role on chip performance.In order to improve yield of product we need to observe effect of process variation and need to compensate it. Here we have used monte carlo,The main aim of Monte-Carlo simulation is to determine the dubiety in the circuit performance owing to random variation of the input circuit parameters. It focuses on how the vulnerability of input parameters propagates through the computations in the circuit and impacts its performance. For Cross Corners Analysis is performed to simulate your circuit's performance against a set of parameters belonging to extreme manufacturing variations. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly.

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[6] ST Microelectronics document., "Cell Library Layout Basics ASIC Work Flow".