Improvement of Project Turn-Around Time using In-design IR/RV Analysis

Major Project Report

Submitted in fulfillment of the requirements
for the degree of

Master of Technology
in
Electronics & Communication Engineering
(Embedded Systems)

By

Chandrika Pande

(17MECE03)

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May-2019

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Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in Embedded Systems at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Chandrika Pande

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Disclaimer

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Certificate

This is to certify that the Major Project entitled **"Improvement of Project Turn-Around Time using In-design IR/RV Analysis"** submitted by **Chandrika Pande (17MECE03)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in Embedded Systems, Nirma University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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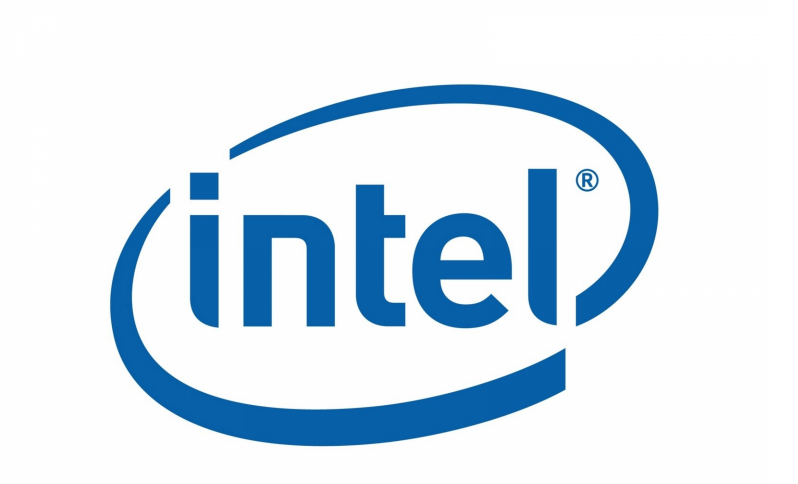

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Abstract

With ever increasing emphasis on project time lines, it is imperative to identify design cycles which take majority of time and find an innovative solution to the problem. One such issue is Volatge Drop/Reliability Verification (IR/RV) signoff which can potentially delay the tape-out by weeks. In general, the total time taken to generate layout from synthesized netlist is around 4 to 5 days and thereafter to generate IR Voltage Drop (IR), Electro-Migration (EM) violation report is around 2 to 3 days. These violation reports are analyzed to fix the design and generate the new layout. Each such cycle takes approximately 1 week. A violation free layout of the design is generated after multiple such cycles. To reduce this turn-around time, we are trying to enable the IR/RV analysis from within the Place and Route (PNR) tool, called as In-Design tool. This will help designer to get violations at any/every stage in the design. This tool will help designer to debug and fix violations in the design stage by stage, completing the layout and its IR/RV signoff in 4 to 5 days as compared to multiple weeks. For enabling IR/RV analysis from within the PNR tool, the newer version of PNR tool having inbuilt IR/RV analysis tool is correlated with standalone IR/RV analysis tool. This allows designer to do IR aware Placement as well as IR aware routing by doing IR/RV analysis before and after placement as well as routing. This reduces the design turn-around time helping designer to meet project deadline.

Abbreviation Notation and Nomenclature

IR/RV Volatge Drop/Reliability Verification

RV Reliability verification

PNR Place and Route

GDS Graphic Database System

IR IR Voltage Drop

EM Electro-Migration

SH Self Heating

SoC System on Chip

ASIC Application Specific Integrated Circuit

IP Intellectual Property

UPF Unified Power Format

SDC Synopsys Design Constraint

DEF Design Exchange Format

SDEF Scan DEF

RC Parasitic Capacitance

CTS Clock Tree Synthesis

IC Integrated Circuit

FT Feed Through

IO Input Output

FC Full chip

VR Virtual Route

QoR Quality of Report

CTO Clock Tree Optimization

DRC Design Rule Checking

LVS Layout Versus Schematic

SI Signal Integrity

DFM Design for Manufacturability

STA Static Timing Analysis

PG Power/Ground

GPO Greedy-Pareto-Optimal

TTF Time-To-Failure

LEF Library Exchange Format

GSR Global Specification Requirement

VLSI Very Large Scale Integration

CMOS Complementary Metal-Oxide Semiconductor

ICC II IC Compiler II

GUI Graphical User Interface

ASCII American Standard Codes for Information Interchange

SPEF Standard Parasitic Exchange Format

PT Prime Time

TW Timing Window

WNS Worst Negative Slack

TNS Total Negative Slack

NVE Number of Violating Endpoints

TCL Tool Command Language

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Chapter 1

Introduction

1.1 Motivation

In the process of designing System on Chip (SoC), sign-off is a crucial step. The tool that do reliability verification is known as IR/RV analysis tool. Signing off on IR/RV takes a lot of time falling in the critical path and delaying the tape out. The time required for editing the design with PNR tool for the removal of IR and EM violations adds on to the delay in taping out the design. This leads to the requirement of an In-Design tool that does reliability verification at every stage of the designing process, meeting the project timelines.

1.2 Objective

The main objectives of the project are as follows:

- To reduce potential delay in tape-out by improving project turn-around time
- To reduce the efforts, time and resources required by the design team and signoff team
- To reduce the time required to debug and resolve the IR and EM violations.

- To ensure that the reports generated by IR/RV analysis tool match with those generated by In-Design tool.
- To provide confidence to the SoC designers for using In-Design tool

1.3 Requirements

The development and implementation of the project at Intel Technologies, requires knowledge of Very Large Scale Integration (VLSI) Physical Design flow, Automatic Place and Route flow, Reliability Verification process, Power Distribution network, Tool Command Language (TCL) scripting.

1.4 Problem Statement

Till now SoC designers have followed traditional method of designing the SoC. This method takes a lot of time (approximately 4 to 5 days) in layout generation from a synthesized netlist followed by reliability verification (taking approximately 2 to 3 days). The designer analyses the violation reports and fixes the design to generate a new layout. This cycle repeats until the design is ready for tape-out. As, the generation/correction of layout and reliability verification are carried out in two different tools one after another, each cycle takes approximately 1 week, causing delay in tape-out, missing project timelines.

1.5 Scope of Work

The In-Design tool is designed in such a way that, the PNR tool can invoke the IR/RV analysis tool from within on request. Designer can run the verification checks after every stage of layout design. The violation reports for the completed stage are available inside the PNR tool. The designer can correct the design stage-by-stage

using the same tool, within a week. This saves a lot of time and efforts of the designer.

1.6 Thesis Outline

- **Chapter-1** contains the brief information about motivation and objective of the project, along with the problem statement and scope of work.
- **Chapter-2** describes the literature survey done in order to pursue the project by providing the overview of Application Specific Integrated Circuit (ASIC) Physical Design Flow and the problems faced during IR and EM analysis.
- **Chapter-3** discusses about the Reliabilty Verification steps, Static IR analysis. The inputs required and outputs generated by Static IR check, its requirement, steps for calculation and the problems faced.
- **Chapter-4** gives a detailed information about the In-design IR/RV Analysis Tool.
- **Chapter-5** discusses the Simulation results of Static IR analysis in standalone IR/RV analysis tool along with correlation results of the standalone and In-Design IR/RV analysis tool. It also contains the results of IR aware placement and routing stages.
- **Chapter-6** concludes the project report and provides the future scope of the tool.

Chapter 2

Literature Survey

This chapter provides overview of ASIC Physical Design flow and the literature review done to study and reduce the effect of IR drop and improve the reliability in the chip designing.

2.1 Introduction to ASIC Physical Design

ASIC Physical Designing of a circuit is a process which is done before fabricating the circuit. Physical designing refers to all steps of synthesis starting from logic design and till step before fabrication. These are logic partitioning, floorplanning, placement, and routing. In Physical Designing process synthesized netlist is converted into physical layout which can be manufactured called as Graphic Database System (GDS). Physical Designing process is done in PNR tool.

The performance of the circuit, it's area, yield, and reliability depend critically on the way phisical designing of the circuit is carried out. In an Integrated Circuit (IC) layout, metal and polysillicon are used to connect two points that are electrically equivalent. Both metal and poly lines introduce wiring impedance. Thus a wire can prevent a signal from traveling at a fast speed. The longer the wire, the larger the wiring impedance, and longer the delays introduced by the wiring impedance. When a connection is implemented partly in metal layer 1 and partly in metal layer 2, via

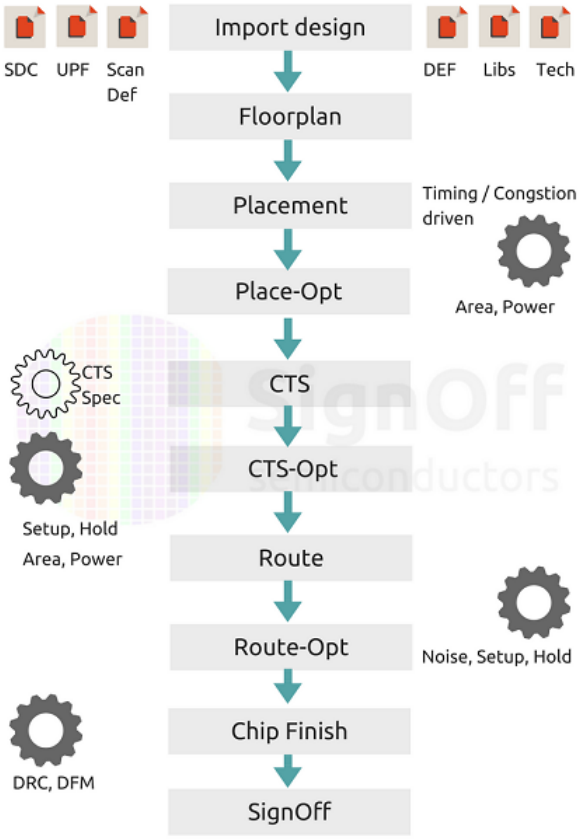


Figure 2.1: ASIC Physical Design flow [1]

is used at the point of exchange. Similarly, if a connection is implemented partly in poly and partly in metal, a contact becomes necessary to perform the layer change. Contacts and vias introduce a large amount of impedance, contributing to delay in signals.

The reliability of the chip is also influenced by the layout. For instance, vias are source of unreliability, and a layout which has a large number of vias is more likely to have defects. Also, the width of a metal layer must be chosen appropriately by the layout program to avoid EM. If a thin metal wire carries a large current, the excessive current density may cause wearing away of metal, tapering the wire slowly, resulting in an open circuit [2].

2.1.1 Import Design

This is the primary step of Physical Designing process. In this tool reads all necessary inputs and data. For importing design, inputs required are logical and physical views of standard cell, gate level netlist along with Intellectual Property (IP) used in the design, Synopsys Design Constraint (SDC) timing constraints, Unified Power Format (UPF) power intent, Floor-plan Design Exchange Format (DEF) and Scan DEF (SDEF), Technology file and Parasitic Capacitance (RC) Co-efficient files.

2.1.2 Floor-plan

Floorplanning is defined as considering all macros of the design, memory, IP cores and there placement needs along with routing possibilities and the area of complete design. Design area and speed are the two factors which can be compromised for one another. If the design is optimized for minimum area, then the designer can only few resources thus, escalating the system. A good floor plan can make implementation process of Placement, Clock Tree Synthesis (CTS), Routing and timing closure cake walk. Similarly, a bad floor plan can create all types of problems in the design such as timing, congestion, noise, routing issues and IR. A bad floor plan blows affects reliability, power, IC lifetime, and increases area along with overall IC cost. Floorplanning methods used in Physical Designing are

- Abutted floorplan
- Non-abutted floorplan
- Mix of both

In Abutted floor plan all inter block pin connections are done by Feed Through (FT) whereas, in Non-abutted or channel based floor plan all inter block pin connections are routed in channels. The mix type floor plan are partially abutted with with some channels.

Some of the steps followed in floor planning are

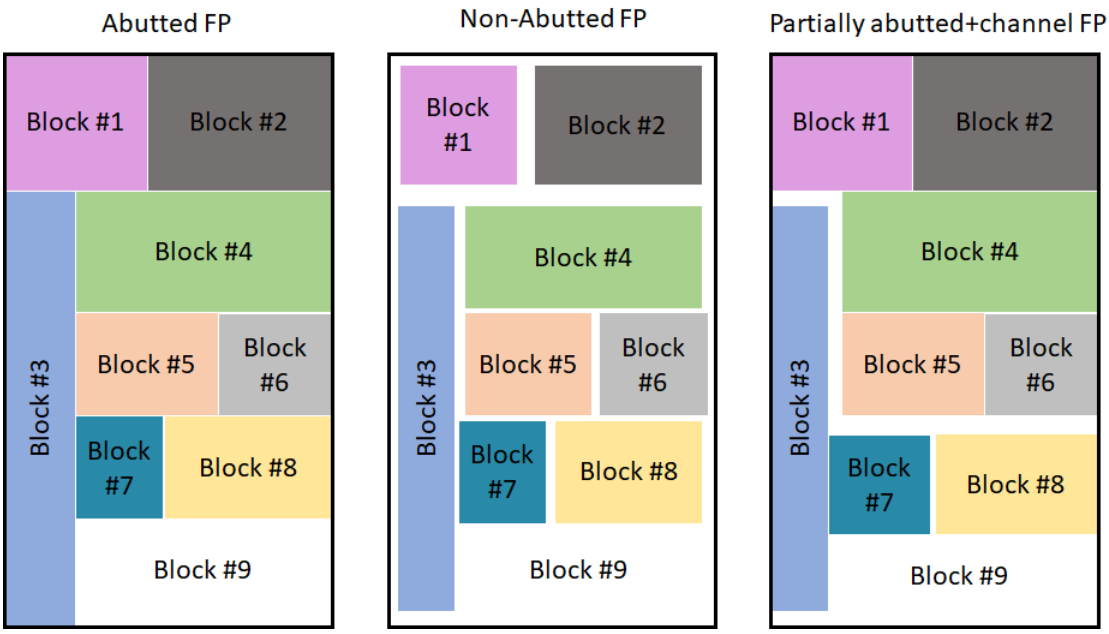


Figure 2.2: Floor plan Techniques

- Size and shape of the block
- Creation of voltage area (power domains)
- Input Output (IO) placement
- Creation of standard cell rows
- Macro placement
- Addition of routing and placement blockages
- Addition of power switches (Daisy chain)
- Creation of power mesh
- Addition of physical cells
- Placement of pushdown cells
- Creation of bounds/plan groups/density screens [3].

2.1.3 Placement

Placement is the step of placing standard cells in the rows created at the floor planning stage.The goal is to minimize total area and interconnect cost. The quality of routing is highly determined by placement.

Placement is a critical step in VLSI design flow. It largely determines the length and hence, the delay of interconnect wires which can consume as much as 75% of clock cycles in advance design. Thus, placement is a key factor in determining the performance of a circuit. A well constructed placement solution will have less routing demand that is, shorter total wire length, and will distribute the routing demand more evenly to avoid routing hotspots. Placement also decides the distribution of heat on a die surface. An uneven temperature profile can lead to reliability and timing problems. It can also reduce the capacitive load because of wires, by having shorter wire and larger separation between adjacent wires. Hence, the switching power consumption can be reduced.

Some of the steps followed in placement are:

- Global Placement
- Legalization
- Detailed Placement [4].

2.1.4 Place-Optiomization

Placement Optimization is performed in four steps:

- **Pre placement Optimisation**

  In this process, optimization is done before netlist is placed and high-fan out nets are collapsed shrinking the cells.

- **In placement Optimization**

  In this process, logic is re-optimized according to the Virtual Route (VR).

Cell bypassing, cell moving, gate duplication, buffer insertion, etc. can be preformed in this step.

- **Post placement Optimization**
  Netlist is optimized with ideal clocks before CTS. It can fix setup and hold violations. Optimization is done based on global routing.

- **Post placement Optimization after CTS optimization**
  Optimization is performed after CTS optimization is over using propagated clock. It tries to preserve the clock-skew.

2.1.5 CTS

CTS is one of the most important stage in PNR. CTS Quality of Report (QoR) decides timing convergence and power. In most of the ICs clock consumes 30 to 40 percentage of total power. So, efficient clock architecture, clock gating and clock tree implementation helps to reduce power.

The goal of CTS is to reduce the skew and insertion delay to minimum. Clock is not propagated before CTS. If clock is divided, then separate skew analysis is done. Global skew achieves zero skew between two synchronous pins without considering logic relationship and local skew achieves zero skew between two synchronous pins while considering logic relationship. If clock is skewed intentionally to improve the setup slack then it is known as useful skew [3].

2.1.6 CTS-Opt

Clock can be shielded so that noise is not coupled to other signals. But shielding increases area by 12% - 15%. Clock Tree Optimization (CTO) is achieved by buffer sizing, gate sizing, buffer relocation, level adjustment and high-fan out net synthesis. Setup slack is improved in pre-placement, in-placement and post-placement optimization before CTS stages while neglecting hold slack. But in post-placement

optimization after CTS hold slack is improved. As a result of CTS lots of buffers are added [4].

2.1.7 Route

Routing is the done after CTS Optimization where actual path for the interconnection of all standard cell, macro and IO pin are determined. Also, electrical connections are created using metal in the layout which are defined by the logic connection present in the netlist.

The tool takes the placed cells, blockages, clock tree buffers and inverters, IO pins information from CTS, once these are available, to complete electrical connections that are defined in the netlist. The tool does this in such a way that there are minimal Design Rule Checking (DRC) violations during routing. When the design is fully routed with minimum Layout Versus Schematic (LVS) violations then, there are minimum Signal Integrity (SI) related violations. There must be then no or minimum congestion hotspots, the timing DRC are met and the timing QoR is good.

Routing is performed in various steps. They are:

- Global routing
- Track assignment
- Detailed routing
- Search and repair

2.1.8 Route-Opt

Routing optimization is a step performed after detailed routing in the flow. Inaccurate modelling of the routing topology may cause timing, SI, and logical design constraint related violations. This may cause conditions wherein fixing a violation

would create other violations and many such scenarios may cascade to make it very difficult for timing closure with no timing DRCs. Hence, it is necessary to fix and optimize the routing topology.

Routing optimization involves fixing timing violations, fixing LVS, fixing DRC, fixing timing DRC, finding and fixing antenna violations, area and leakage power recovery, fixing SI related issues and redundant via insertion.

2.1.9 Chip finish

Chip finish is a stage after post-route optimization where filler cells and metal fills are added to meet the DRC rules. Filler cells are used for rail continuity and to fill up gaps between standard cells in the rows thereby reducing the DRC violations created by the base layers. It is also possible to reduce the IR drop by inserting de-cap filler cells but this comes at a cost of higher leakage currents. The metal fills are small floating metal nets inserted after post-route optimization in order to maintain uniformity in metal layer density in empty spaces in the design [1].

2.1.10 SignOff

In the automated design of ICs Signoff checks is the collective name given to a series of verification steps that the design must pass before it can be tapped out.

Various verification steps are

- **DRC** It is also calle as Geometric Verification where verification is done to check if the design can be reliably manufactured by giving current photolithoghaphy limitations. In advanced process nodes, Design for Manufacturability (DFM) rules are upgraded from optional to required.

- **LVS** It is also called as Schematic Verification which is used to verify that the placement and routing of the standard cells in the design has not altered the functionality of the constructed circuit.

- **Formal Verification** In this verification, the logical functionality of the post-layout netlist is verified against the pre-layout, post-synthesis netlist.
- **Voltage drop analysis** It is also called as IR drop analysis. This check verifies if the power grid is strong enough to ensure that the voltage representing the binary high value never dips lower than a set margin below which the circuit will not function correctly or reliably due to the combined switching of millions of transistors.
- **SI analysis** In this, noise due to cross talk and other issues are analyzed and its effect on circuit functionality is checked to ensure that capacitive glitches are not large enough to cross the threshold voltage of gates along the data path.
- **Static Timing Analysis (STA)** Slowly superseded by statistically STA is used to verify if all the logic data paths in the design can work at the intended clock frequency, especially under the effects of on-chip verification.
- **EM** Lifetime checks, used to ensure a minimum lifetime of operation at the intended clock frequency without the circuit succumbing to EM [5].

Amir H. Ajami describes in his paper the requirement of reducing the static IR and dynamic IR drop. Also, the effect of Power/Ground (PG) network is shown with the advancement in the technology. IR drop might introduce the significant amount of skew in the design, which might lead to timing issues. In this paper, the author describes various fixes how the Static IR drop can be reduced by reducing the power supply glitches and ground bounce. Similarly, the effect of Dynamic IR on a circuit can be reduced by adopting various fixes. The task here is that the cells in the design should not toggle simultaneously. If they are toggling at the same time, grid robustness will decrease. The metal grid is used to carry current from power pads to the standard cells. If IR drop is coming on a metal layer, it means the amount of voltage required by the standard cell to operate will not reach there,

so the cell will not work thus it will disturb the complete logic of the circuit, thus the chip will not function properly, so we can say the power distribution is very important in the chip design. In this paper, the author has referred the power grid planning criteria in order to reduce the IR drop [6].

Minghui Han describes in his paper the study of how increase in resistance in a specific part of the supply grid can lead to the increase in the Static IR drop in that region. If the circuit components start toggling at the same time, it leads to Dynamic IR drop. The Aim of reducing the IR drop either Static IR drop or Dynamic IR drop is to make the grid more resistive and robust enough. Designer might come across different challenges while reducing the Static IR drop or Dynamic IR drop. Optimization can be done for these issues by finding a way such that we can make a trade-off between the two. The author describes how we can reduce their drop at different levels. Reducing IR drop is also related to reducing the impedance at the package level. In short, we can say that different factors are there at different levels to reduce the drop.

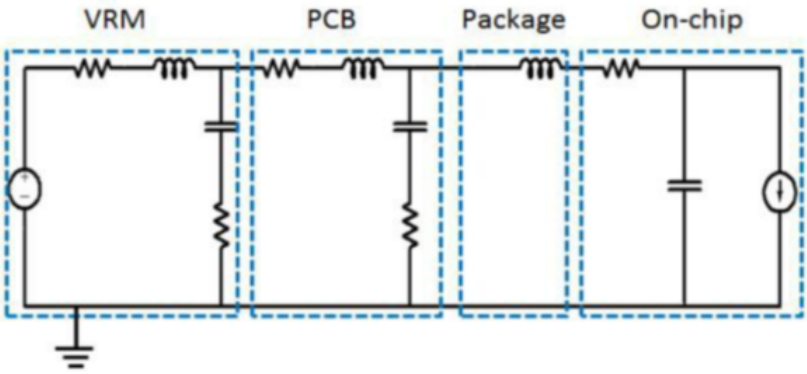


Figure 2.3: Network behind SoC

At the chip or block level, the factor is resistance i.e. making the grid robust enough by reducing the resistance. At the package level, there comes impedance. Again at the PCB level, different factors like resistance, inductance plays a significant role as shown in Figure 2.3 [7].

Tsu-wei Tseng et al. explained in his paper about the IR drop coming after

routing stage. After floorplanning and placement stage, few routing area will be left in the design. It becomes a challenging task to reduce the IR drop. Because of the lack of routing area, Engineering Change Orders (ECO) are a crutial part of the designing. It might require to re-synthesis the whole design. Thus, it will result in a long process again. The author has suggested few methods by which we can solve our problem and implement the fixes in the design. The author has suggested a technique named Greedy-Pareto-Optimal (GPO), in which we can reduce the IR drop of the chip with less routing area also. By using this technique, the author has reduced the IR Drop at the post-routing stage from 9.34% to 3.84%. This reduction is almost 58.9%. This is how the IR Drop is improved in the design without affecting the routing congestion [8].

Valeriy Sukharev et al. explained in their paper the voltage drop is increasing beyond the threshold value then it causes the voltage drop to increase beyond the limit that the PG grid can sustain. This also causes EM violations to occur. The author has described a technique to calculate the stress distribution inside the multi-branch interconnect tree i.e. the stack of metal layers. Lowermost metal layer will be having the highest resistance while topmost layer will be having the lowest resistance. The author has described about Time-To-Failure (TTF) and various factors affecting the EM phenomenon occurring in the chip. The method suggested by the author accounts for the redundancy of the power grids, assuming that the circuit will definitely fail if it will not function properly [9].

Chapter 3

Reliability Verification (RV)

IC switches on and off million times during its operational life. Reliability ensures IC performs its functions properly in its operational life. It checks for device and interconnect aging. Interconnect aging is driven by change in material properties, application profile and environment. Every cell in design requires fixed voltage at pins for proper functioning. High current densities lead to EM.

Reliability Verification is used to prevent premature wire failures and transistors. It mainly checks for the following

- Interconnect failure (EM/Self Heating (SH))
- Device failure
- IR drop (Static, Dynamic)[10]

3.1 Interconnect Failure

A reliability verification violation (EM/SH) exists whenever a wire's actual current,I_{actual}, exceeds its max safe current,I_{max}

$$\frac{I_{actual}}{I_{max}} > 1 \tag{3.1}$$

A given wire has a maximum safe current limit, I_{max}, as specified by the process design rules. At the same time, the circuit in which the wire is used draws a certain actual current, I_{actual}, through the wire. If the ratio is equal to or less than 1, the wire meets or exceeds the design rule requirements for reliability. Any ratio above 1 signifies a violation [11].

EM Every atom in wire is effectively stuck in one place and does not move under normal circumstances. If an electron bumps into an atom, the atom will wiggle (i.e. heat up) but not move from its basic location.If the atom is hit repeatedly from the same direction, it will slowly be pushed in the direction of electron flow. Wires experience electromigration only under direct current condition. Electromigration causes :

- Creation of Holes (also called as voids) in metal wires that increase wire resistance,
- Creation of Voids which completely breaks wire, causing open circuits,
- Regions where accumulated metal (also called as hillocks) can crack surrounding layers and squeeze through, resulting in short circuits to adjacent wires as shown in Figure 3.1. EM can be mathematically defined as

$$\text{EM} = \frac{J}{J_{max}} \tag{3.2}$$

  where, J is the actual amount of current flowing in that area whereas, J_{max} is the maximum allowed current in that area.

Electromigration is very sensitive to temperature. If wire is pre heated, that is if its atoms are already in strongly vibrating condition then these atoms are more likely to be moved from its place by electron wind. The risk of EM failure is directly proportional to temperature. If temperature increases then EM failure risk also increases and vice-verse.

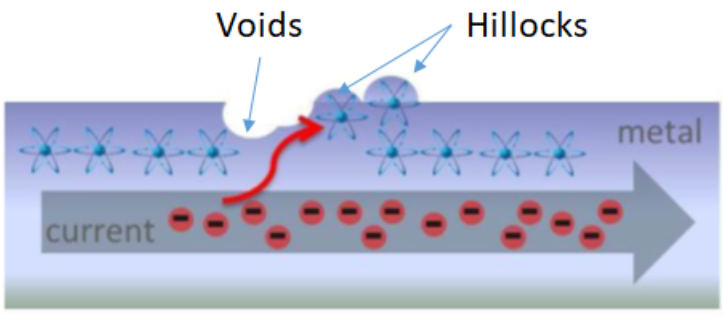


Figure 3.1: Electromigration in metal wire

Self Heating Temperature is a measure of the kinetic energy in the atom. If the object is hot and it's atoms are vibrating vigorously around their resting positions then as the current flows through the wire, the electrons carrying the current get kinetic energy. These moving electrons bump into (more or less) stationary atoms. The kinetic energy of the electrons is transferred to the atoms which start vibrating strongly and the wire heats up. Wires experience self-heating irrespective of current direction (i.e. under AC or DC).

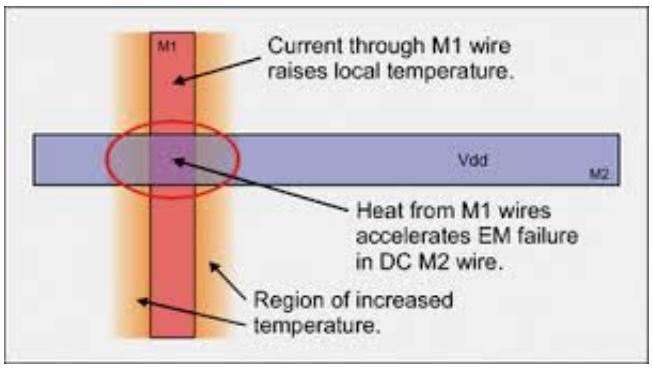


Figure 3.2: Self heating in metal wire

As shown in Figure 3.2, metal wire 1 carries current causing local heating. The increase in temperature accelerates the electromigration mechanism in DC carrying metal 2 wire. EM failure of the metal 2 wire becomes more likely [12].

3.2 Device Failure

Device fails due to SH caused by high device current density, higher integration of transistors on chip and poor conduction of heat. On high-power chips, transistor junction temperatures may reach more than threshold and may break the transistor[11].

3.3 IR Drop

IR drop can be defined as voltage drop occurring in metal wires that make up the power grids before the voltage reaches the V_{DD} pins of the cells. If in a region, there are cells requiring high current or having high switching activity then, voltage drop occurs which in-turn causes setup and hold violations due to delaying of cells. Hold violations cannot be corrected once chip is fabricated. There are two types of IR drop analysis:

- Static IR drop
- Dynamic IR drop

3.3.1 Static IR Drop Analysis

Metal grid used to distribute current to the standard cells has some finite resistance. According to Ohms law,

$$V = I * R \tag{3.3}$$

thus some drop will occur called as Static IR drop.

Inputs and Outputs of IR/RV Analysis Tool

The above flowchart describes the inputs required to perform the static IR analysis and also describes the outputs generated from these analysis. The inputs which are

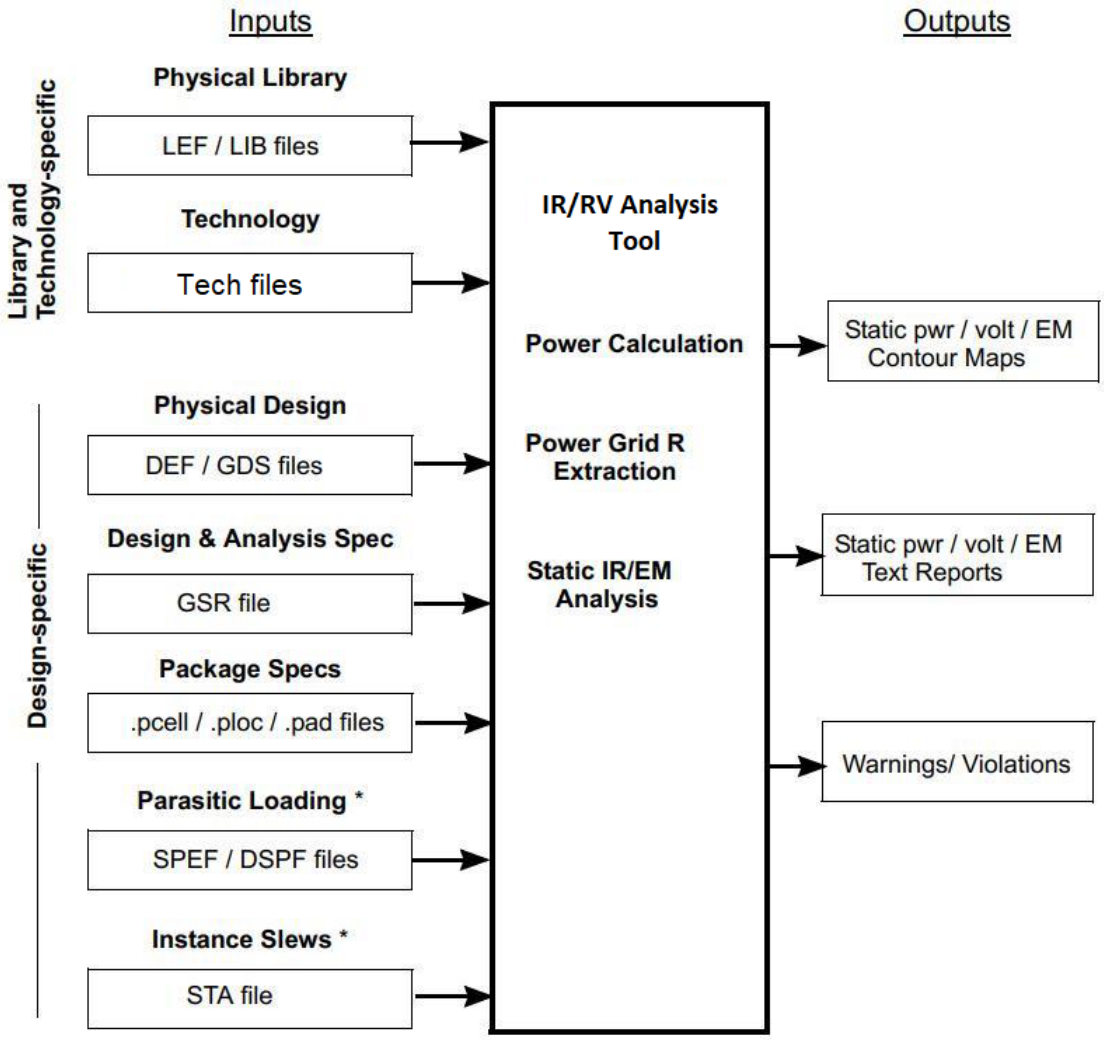


Figure 3.3: Inputs and Outputs of IR/RV analysis tool

shown with asterisk sign are optional for performing the static IR analysis. The description of various inputs are as:

- **DEF** This is a standard format file used to read the design. This file contains the information about the design like physical description of instances, power and ground network, and other circuit elements. If in a design, we have multiple def files then we need to specify every DEF file with top extension at partition level. DEF file is created by PNR tool like ICC or ICC2 from Synopsys.

- **Library Exchange Format (LEF)** These files contain the physical information about the library cells like Layer, Type, Width and Routing. LEF file is also a standard format file used to run the simulations.
  These two files are used to read the design. By default, the tool will be able to read all these files in zipped format.

- **Global Specification Requirement (GSR)** This is a file which is created by the tool, which acts as an input file for the simulation. It contains all the files required by the tool. In short, we can say that the tool will take this file as input file. This file contains DEF file, LEF file and all other files required by the tool.

Calculation Steps of Static IR Drop

Following are the key steps

- Prepare design data files.
- Import design data using the automated setup script or the GSR file.
- Perform power calculation.
- Perform power grid extraction for R network.
- Evaluate power/ground grid weakness.
- Define pad and package constraints.
- Perform static IR drop voltage drop and EM analysis.
- Perform static IR/EM summary reports and evaluate what other information is needed from the analysis.
- Explore solutions to reduce excessive static IR drop with the IR/RV analysis tool's power grid Fixing and optimization tool.

Necessity of Static IR drop Estimation

Static IR drop is the due to the average current flowing through the device. The figure below describes the I-V characteristics curve of the device.

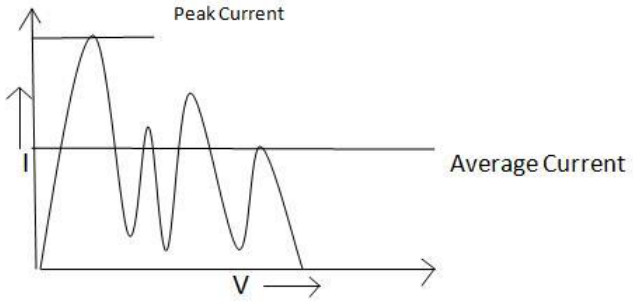


Figure 3.4: I-V Characteristic Curve

Static voltage drop means that we consider that on an average how much the current is flowing the device multiplied by the resistance value. According to Equation $V = I * R$, average current flowing in the circuit depends upon the requirement of the circuit based on the functionality of the circuit. Power bumps are used to provide current to the standard cells. If more power bumps are there, then more current will flow through the metal interconnection. So, average current will increase. This is called glitch in the power supply. But, while calculating Static IR drop, ground bounce is also considered. It also plays a vital role in Static IR drop.

Calculation of Static IR Drop

Static IR drop estimation is not a difficult task. It depends on Ideal voltage, Glitch in power supply and ground bounce.

Glitch in the power supply It is defined as the voltage drop occurring due to current flowing through the parasitic inductance associated with the package wire bonding due to sudden charge and discharge of capacitance with respect to V_{DD}. It can be defined as the change in the supply voltage assumed to reach in the standard

cell and the voltage actually reaching there.

$$\text{Glitch in supply voltage} = \text{ideal voltage reaching cell - actual voltage reaching cell} \tag{3.4}$$

Ground bounce It is defined as the difference between the ground voltage i.e. 0V and the actual ground voltage reaching there. It is actually supposed to go to ground level but it bounces and creates some spikes.
Static IR can be calculated as

$$\text{Static IR drop \%} = \frac{\text{Glitch in power supply - Ground bounce}}{\text{Ideal voltage}} \text{ X } 100\% \tag{3.5}$$

Finding the Minimum Resistive Path

Static IR drop is due to average current flowing in the metal grid. As the grid is made up of copper, it has some resistance value. Therefore, when power is applied to the grid through some IO peripherals then, due to resistance of the metal, voltage drop occurs. Nothing can be done with metal resistance, which is the default value. But the effective resistance of the instances can be reduced in the design and thus, tool can decide the minimum resistive path of the current flowing through it.

In all previous work, people have explained different ways in which they can reduce the drop. But practically, it becomes tough to fix these issues with the growing technology node. In Deep-sub-micron technology, fixing one IR issue might cause other disturbance in the circuit, like DRC, timing issue, etc. Sometimes, due to routing congestion also, reduction of normalized resistance becomes difficult.
The normalized resistance can be calculated as:

$$R_{norm} = \frac{R_{inst} - R_{min}}{R_{max} - R_{min}} \text{ X } 100\% \tag{3.6}$$

Where, R_{inst} is the effective resistance of the PG arc with some max value and min

value, R_{min} is the minimum value of the R_{inst} and R_{max} is the maximum value of R_{inst}.

Static IR drop can also occur due to weakly connected instances to the PG mesh. Via on a metal layer act as a current divider. Therefore, more vias on a metal means it divides the current into more paths. More current paths lead to smaller length of the segment having current flowing through it thus, reduces resistance and hence voltage drop reduces. Because of via-to-via DRC issue, again more vias on the metal cannot be added. Thus, by increasing the resistance of minimum resistive path Static IR drop also increases.

Power Summary

Different types of cells are present in a design. Every cell in a design is not intended to operate at same frequency, so different cells in a design must be having different frequencies, again based on these frequency values, leakage power, internal power, switching power and total power will vary.

Power has components Static component and Dynamic component. As the name suggests that the static component is defined by the leakage current in the design, and Dynamic IR component is defined by the internal power and switching power of the design. More is the value of these components, more will be the power dissipation. For least Static IR drop, leakage power should be less and for least Dynamic IR drop, internal and switching power should be less.

Types of Issues Faced

- **Weak Grid**

  In the case of higher current flowing through the metal, due to resistivity of metal involved, will cause more IR drop. The best solution to avoid this type of issue is providing more paths for the current to flow. Thus, it will reduce the current flowing through the device, then it will definitely cause the IR drop to reduce.

- **High Impedance of the Path**

  The increased impedance of path is something unpredictable type of issue. During placement and routing, it can be predicted that the value of impedance of the path will be more. This issue can be resolved in various ways depending on the maximum resistance difference occurring on a metal and pin. This can be resolved by adding vias or providing more paths as more number of parallel wires reduce resistance.

- **High Package Parasitic**

  Package Parasitic is also a critical part of analysis. It includes all the power locations in the design. If more than required power is coming in the design, it will definitely cause voltage drop. Also, there might be some power hungry devices in the design, which may require more power. So, sufficient amount of power locations are required. Both count of power pads and location of power pads play important role in Static IR analysis [10].

3.3.2 Dynamic IR drop Analysis

The Reason for the Dynamic IR Drop is the fast toggling of the standard cells. When these fast toggling cells are sitting near, then it will increase the peak current flowing through the device. This peak current gets multiplied to the resistance of the metal grid, causing higher Dynamic IR Drop. The Reason for Dynamic IR is that the grid is not robust enough to carry the current caused by the high toggling cells in the design. Sometimes cluster of high toggling cells results in Dynamic IR but single high toggling cell in the design can also result in Dynamic IR Drop.

Factors on which Dynamic IR depends

Dynamic IR depends on three factors, which are described below:

- **Toggle rate**

Dynamic IR drop is mainly depending upon the toggle rate. More cells are placed near to each other in a cluster having more toggle rate will cause more Dynamic IR drop. This is because, if cells are toggling at higher rate, then the peak current will be more. Hence, more drop will be observed.

As, we can see from Figure 3.5, the I-V characteristics curve, when the toggle rate of a cell is high, then peak current is high because of high rise time and high fall time.

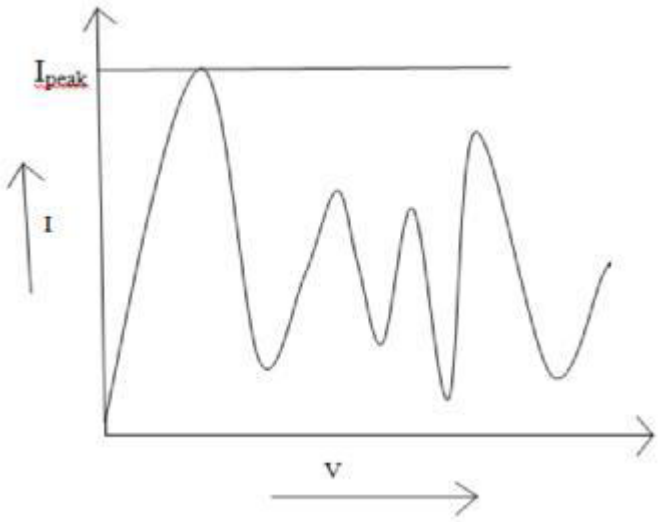


Figure 3.5: Peak current

The other alternative is to add Decap cells in the design because of their functionality. Decap cell is nothing but decoupling capacitor, which will not allow DC to flow. Decap cells act as a capacitor which will get charged when more current is flowing through the device is more and will get discharged when the current is not sufficient in the design.

- **Frequency**

  In the design, if the frequency of the standard cells is higher, then it means that the time period to charge and discharge the load capacitance related is

small. As current and frequency are directly proportional to each other, thus it will result in more drop and hence, higher power dissipation.

- **Load capacitance**

  The load capacitance also plays an important role in dynamic IR calculation. If the load capacitance is more, then the rise time and fall time will be steep, hence, the peak current will be more. This will result in dynamic IR drop. Also, more is the load capacitance, current requirement will be more through that cell, which will ultimately result in higher drop.

There are three types of power dissipation in Complementary Metal-Oxide Semiconductor (CMOS) design leakage power dissipation, short-circuit power dissipation and Dynamic power dissipation. Leakage power dissipation and short-circuit power dissipation depends on the fact that how we fabricate them. While dynamic power dissipation is due to charging and discharging of the load capacitance. If the capacitor charges and discharges immediately, then the peak current will be high. If peak current is more, then the dynamic IR drop will be more. Dynamic power dissipation is given by

$$P_{dynamic} = \sum_{i=1}^{k} \frac{C_{Li} * V_{DD}^2 * T_{Ri}}{2 * T} \tag{3.7}$$

where, $P_{dynamic}$ is the dynamic power dissipation, V_{DD} is the operating voltage of the design, K is the total number of nodes, T_{Ri} is the toggle rate of the ith node, C_{Li} is the load capacitance of the ith node, T is the time taken by the clock period.

Power dissipation at the circuit level depends upon toggle rate only. This is because out of other factors, few will be constant, depending on design or fabrication. High toggle rate will result in higher peak current. If the metal grid is not robust enough to carry that current then, the Standard cells might not work, if they are not able to get the sufficient operating voltage. Thus, design will not work properly and hence, IR Drop is of more concern.

Relationship between Timing and IR drop

IR drop and Timing issues are closely related to each other. By Timing issue, we mean here Setup and Hold Violations. Any Circuit in VLSI has two types of path in the circuit, Clock path and Signal path. High IR drop on Clock path causes Hold violations whereas High IR drop on Signal path causes setup violations. Out of setup and hold violations, hold violation is bad for chip designing. Fixing hold violations is more critical because hold violations are coming due to high IR drop on Clock path. Timing issues can be resolved by adding buffer in between the timing critical paths. Again, addition of buffer in the long route will not reduce the amount of current flowing through the circuit but it will reduce the current flowing in that area. This, it will reduce the IR drop coming on that particular net [11].

3.4 Electromigration

EM is a very critical part in VLSI design. It is the property of metals on which lifetime of a chip depends. If we meet our criteria then only we can make the chip to work for that particular time period. EM is the property of metals that helps in finding the temperature effect in metal. So, we can say that in order to meet the EM criteria, we need to have knowledge of current per unit area (or current density) in that metal.

Till date, we have so many hand-held devices in our home, work-place and public-place, etc. We have seen that in small hand-held devices, the major issue is heating up of the device. This is because of small area of the chip means if there is a large current injection at one place, then current per unit area will increase. This may lead to increase in local temperature which can further lead to EM effect in that metal and also in other metal straps. So, we can conclude that there are two types of nets while calculating the EM:

- **Aggressor** As the name specifies, the net which will cause more current to

flow through a particular unit area is called Aggressor. This net will cause increase in local temperature.

- **Victim** The other nets which get affected by the increase in local temperature of the aggressor net which is causing them to increase the local temperature, are called Victim nets. It is always compulsory to fix Aggressor nets, but the Victim nets will depend upon the change in temperature.

3.4.1 Factors affecting EM

Electromigration depends on a number of factors, which are as follows:

- **Rise in Temperature**

  The temperature of the metal is the main factor in electromigration. Due to the flow of electrons in the metal wire, it has some temperature. If more current starts flowing in this metal, then the temperature of the metal gets increased. If the rise in temperature is more, then the aggressor and victim nets also need to resolved. Thus, increase in local temperature results in increase in electromigration effect. This increase in temperature can be mathematically expressed as

  $$\triangle = \text{T2 - T1} \tag{3.8}$$

  In this above Equation, T1 is the actual temperature of the net, T2 is the temperature of the net after the aggressor net comes into picture and, $\triangle$ is the change in the temperature. Thus, we can conclude that for better reliability of the chip, $\triangle$ should be less. The reason is that the rise in temperature of one of the net may rise the global temperature of that area thus, it may increase the temperature of the nearby nets.

- **Frequency**

  Frequency is a method to measure how fast our device or chip is responding.

Lesser the slew rate, faster the device works. With more functionality incorporated in a chip, requirement of zero or positive slew increases. Thus, with this scenario, the toggling rate of the cells should be more, which will further impact frequency of the chip. By default, the toggle rate (in percentage) of the signal coming on the net should be 100% and toggle rate (in percentage) coming on the signal should be 200%. It means, data will toggle only once in a clock period and as clock frequency is half than the signal frequency, so it will toggle twice. If any signal or clock toggle rate is coming more than this value, then it is called as violation. Thus, the frequency issue is very critical issue in the design.

- **Load capacitance**

  Load capacitance is one of the key factor responsible for EM. If a cell or instance is placed somewhere such that the load capacitance is high, then those load capacitances or those cells will try to draw more and more current from the driver cell.The driver cell will not be able to supply them with sufficient amount of current, so it will try to provide current to the load cells, which will cause increase in current density, thus will cause EM. For better reliability of the chip, it is good choice that number of loads which driver cell will driving should be made according to the capacity of the driver cells. For more loads to carry, more strong the driver cell needs to be. Thus, up-sizing the driver size or splitting the load is the optimal solution if the load capacitance is higher for a particular standard cell [12].

3.4.2 Mathematical Calculation of EM

EM is nothing but the factor of current flowing through the metal and current limit allowed to flow through the device. Depends on the chip, we can set the value to some random number, then, according to that, we can decide the violation.

Mathematically EM is calculated as:

$$\text{EM} = \frac{I_{rms}}{I_{limit}} \tag{3.9}$$

Where I_{rms} is the current flowing in actual in the metal and I_{limit} is the max amount of current which is allowed to flow in that metal. For different chips, based on different logic and functions, this ratio will vary. In order to calculate EM in percentage, we simply need to multiply this ratio with 100. Then we will get % EM.

In Real Scenarios, it is always difficult to fix the EM coming on a net or metal. The design is deprived of EM issue with newer technology nodes. Its always a challenge to fix them. Different criterias are followed by different people to fix them.

3.4.3 Real Scenarios based on EM

- **Long Route**

  In a design, if a cell is driving another cell then, it is not an issue because, in that case, output load is not high. So, it will not create any kind of EM issues. But, if the route between the two cells is long, then the current flowing per unit area (i.e. current density) will increase. Thus, EM % will increase. To reduce this we can apply some technique which can divide the current flowing through the metal. For this we can add buffer somewhere in the route.

- **High Load at the output**

  If a cell or driver is driving many cells, then the load capacitance of the cell will be high. The EM basically depends on the input transition and output capacitance. If the output capacitance is more, then the driver cell will have to provide more current in order to support the functionality of the load cells. But, as we know that capacitance and current are both directly proportional to each other. Thus, more is the output capacitance, more will be the current

flowing per unit area, this will result in the rise in default temperature of the net in the form of power dissipation (heat). To avoid this, we can split the load. This will reduce the output capacitance.

- **High Frequency of the standard cells**

  Higher is the frequency, higher is the amount of current flowing through the metal hence, current density increases. This again increases the EM % on the net. In order to deal with high frequency, we need to check few criteria like length of route, load capacitance, addition of parallel path, via laddering, etc. If this is a real issue, then addition of parallel path or addition of via ladder is of greater help if load capacitance is fine and also the length of the route is not much long [13].

Chapter 4

In-design IR/RV Analysis Tool

4.1 Overview

This chapter describes how to use the In-design IR/Reliability verification (RV) analysis tool feature to perform rail analysis in the PNR environment. The RedHawk (standalone IR/RV analysis tool) power integrity solution is integrated with the IC Compiler II (ICC II) (standalone PNR tool) implementation flow through the RedHawk Analysis Fusion (In-design IR/RV analysis tool) interface. RedHawk Analysis Fusion feature are used for rail analysis at different points in the physical implementation flow after power planning and initial placement are completed. This enables detection of potential power network issues before performing detail routing and thus significantly reduce the turnaround time of the design cycle. When placement is complete and the PG mesh is available. RedHawk Analysis Fusion is then used to perform voltage drop analysis on the power and ground network to calculate power consumption and to check for voltage drop violations. Voltage drop analysis can also be performed at other stages in the design flow, such as after detail routing. When chip finishing is complete, RedHawk Analysis Fusion is used to perform PG electromigration analysis to check for current density violations.

RedHawk Analysis Fusion rail analysis supports gate-level rail analysis capabilities,

including both static and dynamic rail analysis. RedHawk Analysis Fusion can be used to perform the following types of checking and analysis in the ICC II environment:

- Missing via and unconnected pin shape checking
- Voltage drop analysis
- PG EM analysis
- Minimum resistance analysis

Depending on the type of analysis run, the tool generates visual displays (maps) of the results that can be viewed in the IC Compiler II Graphical User Interface (GUI), as well as error data that can be displayed in the IC Compiler II error browser. These maps and error data help to discover problem areas and determine corrective action without leaving the IC Compiler II environment. When analyzing a multicorner-multimode design, RedHawk Analysis Fusion analyzes only the current scenario. Figure 4.1 shows where these analysis capabilities can be used in a typical design flow.

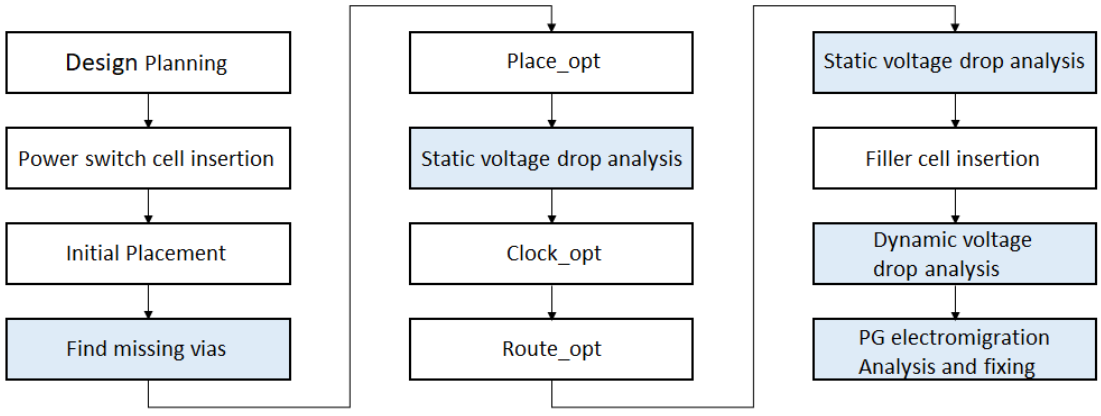


Figure 4.1: Using Redhawk Analysis Fusion in IC Compiler II design flow

4.2 Redhawk Analysis Fusion Data Flow

The RedHawk Analysis Fusion feature allows to perform rail analysis during the implementation stage. With the required input files, the IC Compiler II tool creates the RedHawk run script and the GSR configuration file for invoking the RedHawk tool to run PG net extraction, power analysis, voltage drop analysis, and PG electromigration analysis. When analysis is complete, the IC Compiler II tool generates analysis reports and maps using the results calculated by the RedHawk tool. Hot spots can then be checked graphically in the IC Compiler II GUI. Error data and American Standard Codes for Information Interchange (ASCII) reports are also available to check for locations where limits are violated. Figure 4.2 illustrates the data flow when using RedHawk Analysis Fusion to perform rail analysis in the IC Compiler II environment.

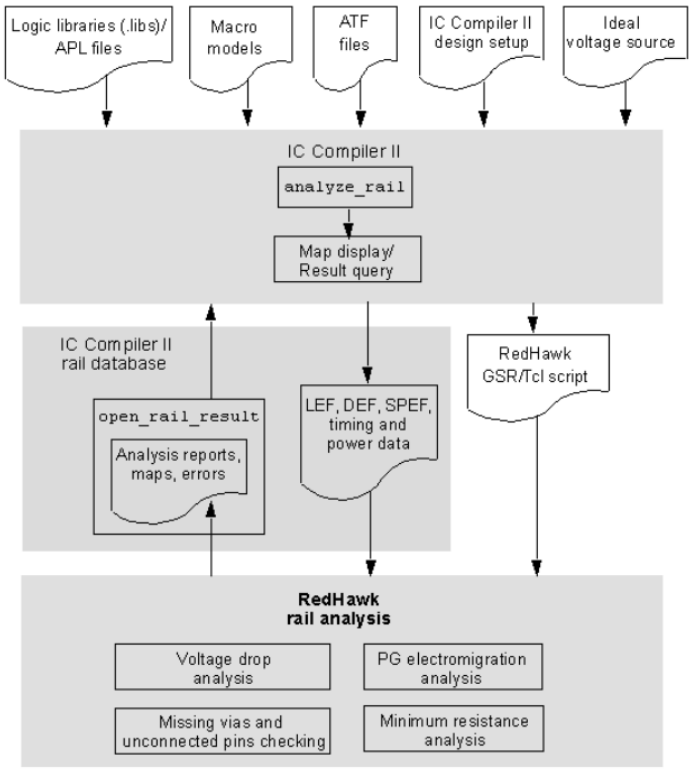


Figure 4.2: Redhawk Analysis Fusion data flow

4.3 Redhawk Analysis Fusion Analysis Flow

When the necessary input and design data are specified, voltage drop and PG electromigration analyses on the design can be performed. Figure 4.3 illustrates the steps in a basic static rail analysis flow.

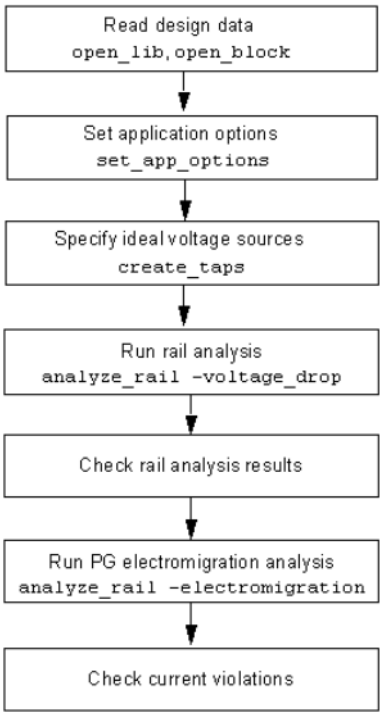


Figure 4.3: Required steps for a basic rail analysis using Redhawk Analysis Fusion

4.4 Prerequisites for Redhawk Analysis Fusion

Before invoking the RedHawk tool to perform power analysis, PG net extraction, or voltage drop analysis in the IC Compiler II environment, following input files are required:

- Liberty logic library (.lib)
- Apache technology file (*.tech)

- Apache macro models
- Apache power library (APL) files
- Tap files (or RedHawk pad location files)
- LEF/DEF files (When not provided, the IC Compiler II tool generates these files by using the data in the design library.)
- Static timing window (STA) file
- Signal Standard Parasitic Exchange Format (SPEF) files

Before analyzing voltage drop and current density violations in a design using the RedHawk Analysis Fusion capability, set_app_options command is used to specify the location of the libraries and the required input files. Table 4.1 lists the application options for specifying design and input data for running RedHawk rail analysis within the IC Compiler II environment.

4.5 Setting up Executables

To run RedHawk Analysis Fusion features, we need to enable the features and specify the location of the RedHawk executable by setting the rail.enable_redhawk and rail.redhawk_path application options. By default, the rail.enable_redhawk application option is set to true. For example

```
icc2_shell> set_app_options -name rail.enable_redhawk -value true
icc2_shell> set_app_options -name rail.redhawk_path \
          -value /tools/RedHawk_Linux64e5_V19.0.2p2/bin
```

Figure 4.4: Setting up executables

Table 4.1: Application Options

Application Option	**Description**
rail.lib_files	Specifies the RedHawk library files in .lib format.
rail.tech_file	Specifies the Apache technology file for performing PG extraction and PG electromigration analysis.
rail.apl_files	Specifies the Apache APL files, which contain current waveforms and intrinsic parasitics for performing dynamic rail analysis.
rail.switch_model_files	Specifies the RedHawk switch cell model files for performing dynamic rail analysis.
rail.macro_models	Specifies the RedHawk macro model files.
rail.lef_files	Specifies a list of LEF files. When not specified, the IC Compiler II tool generates one using the data in the design library.
rail.def_files	Specifies a list of DEF files. When not specified, the IC Compiler II tool generates one using the data in the design library.
rail.pad_files	Specifies a list of RedHawk pad location files. When not specified, you need to specify the ideal voltage sources by running the create_taps command.
rail.sta_file	Specifies the RedHawk static timing file (STA), which contains the final slew and delay information. When not specified, the IC Compiler II tool generates the static timing window information using the data in the design library.
rail.spef_files	Specifies a list of SPEF files, which contain the detailed parasitic resistive and capacitive loading data of the signal nets. When not specified, the IC Compiler II tool generates the SPEF file using the data in the design library.
rail.effective _resistance_instance _file	Specifies the instance file, which lists the cell instances for effective resistance calculation.

4.6 Specifying Redhawk Working Directories

During rail analysis, RedHawk Analysis Fusion creates a working directory to store the generated files, including analysis logs, scripts, and various output data. By default, the RedHawk working directory is named RAIL_DATABASE. To use a different name for the RedHawk working directory, the rail.database application option is used.

RAIL_CHECKING_DIR is the directory where RedHawk Analysis Fusion saves report files on the missing information during rail analysis.

RAIL_DATABASE is the directory where the tool saves and retrieves results and log files that are generated during power calculation and rail analysis. This directory contains the following subdirectories:

- **in-design.redhawk** This directory contains the **design_name.result** where RedHawk saves the analysis result files.
- **design_name** The directory where RedHawk writes analysis results for the IC Compiler II tool to retrieve for map display and data query. For example, running the open_rail_result command loads the data in this design_name directory for displaying maps in the GUI.

4.7 Specifying Ideal Voltage Sources as Taps

Taps are used to model the external voltage source environment in which the device under analysis operates; they are not part of the design itself, but can be thought of as virtual models of voltage sources. The locations of the ideal voltage sources and the ideal power supplies in the design are required to achieve accurate rail analysis results. To create a tap,the create_taps command is used. The -top_pg option is used when the block does not have physical pad or bump information available.

4.8 Performing Redhawk Voltage Drop Analysis

To invoke the RedHawk tool for calculating voltage drops of the specified power and ground networks, we use the analyze_rail command with the following options:

- **-top_pg** to specify the analysis mode.
- **-voltage_drop** to specify the analysis mode.
  - **static** Performs static voltage drop analysis
  - **dynamic** Performs static voltage drop analysis
- **-all_nets** to considers all the switched or internal power and ground nets
- **-power_analysis** By default, the tool uses the RedHawk power analysis feature to calculate the power consumption of the specified power and ground network. If we prefer having the IC Compiler II tool generate the necessary power data for rail analysis, we set the -power_analysis option to icc2.
- **-extra_gsr_option_file** By default, the analyze_rail command automatically generates a GSR file for running RedHawk rail analysis. To specify an external GSR file to append to the GSR file generated in the current run, the -extra_gsr_option_file option is used.

```
icc2_shell> analyze_rail -voltage_drop static -nets {VDD VSS} \
   -extra_gsr_option_file add_opt.gsr
```

Figure 4.5: analyze_rail command example

4.9 Writing Analysis and Checking Report

When the checking or analysis is complete, run the report_rail_result command to write the analysis or checking results to a text file. The power unit in the report file is watts; the current unit is amperes; and the voltage unit is volts.

Chapter 5

Results

In this chapter,Analysis and Simulation results of Static IR drop using standalone and In-design tool for a partition of SoC is shown.

5.1 Static IR Simulation Results

Figure 5.1 shows the histogram of 86,600 cells (also known as instances) connected to a specific PG net named vccvssaon having voltage drops ranging between 0mV to 3mV.

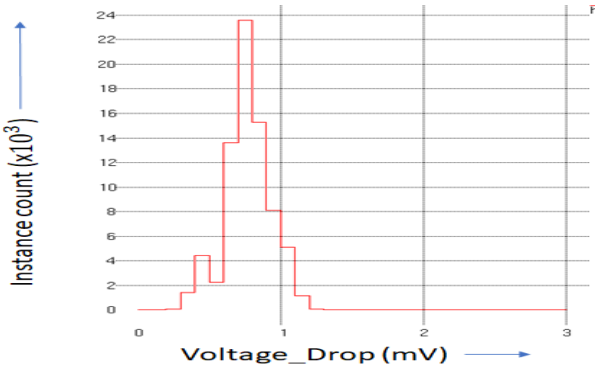
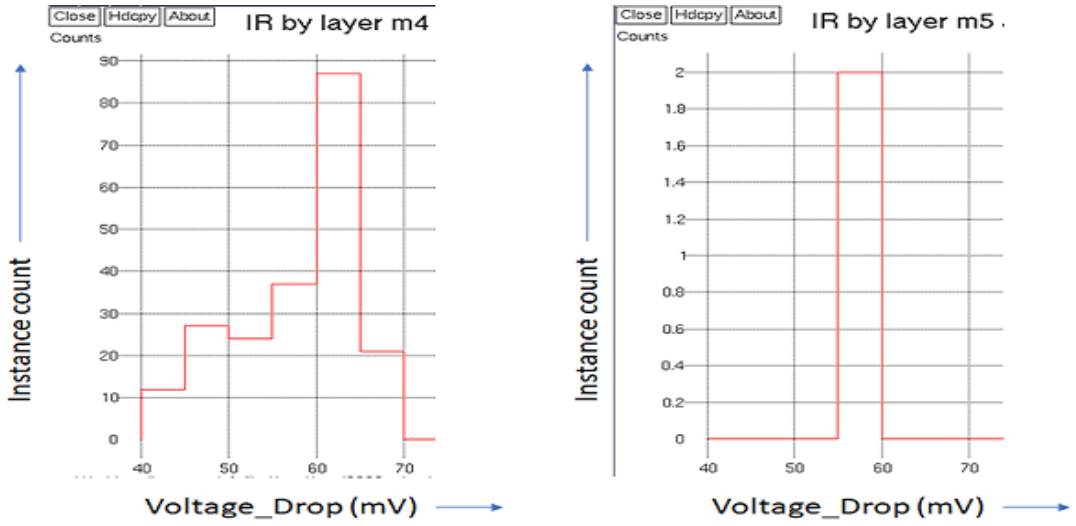


Figure 5.1: Histogram of instances having drop upto 3mV

The ideal voltage of PG net vccvssaon is 0.89V and the maximum allowed voltage

drop is 5% (i.e., 44.5 mV). All cells having voltage drop more than 5% are said to fail Static IR drop check.

Figure 5.2 (a) and Figure 5.2 (b) show Histograms of cells connected to Metal layer



(a) Metal 4 (b) Metal 5

Figure 5.2: Histograms of instances having drop beyond 44.5mV on metal 4 and 5 respectively

4 and Metal layer 5,respectively, of PG net vccvssaon, failing Static IR check using IR/RV analysis tool.

Histogram shows, around 200 cell are connected to metal layer 4 whereas, only 2 cells are connected to metal layer 5. Figure 5.3 shows the Summary report generated by the IR/RV analysis tool for Static IR check. The report shows that there are total 67 cells failing due to Static IR drop of more than 5%, 51 cells having more that 6% whereas, 30 cells having more than 7% static IR drop. The worst Static IR drop of these failing cells is 7.53%.

Figure 5.4 (a) shows the area of design where Static IR drop is more than 5% (red colored cells). We can see from the figure that all the instances failing 5% static IR criteria are connected in series to the same PG net.

Blue and violet color denote the region where Static IR drop is $<$ 1.667% and

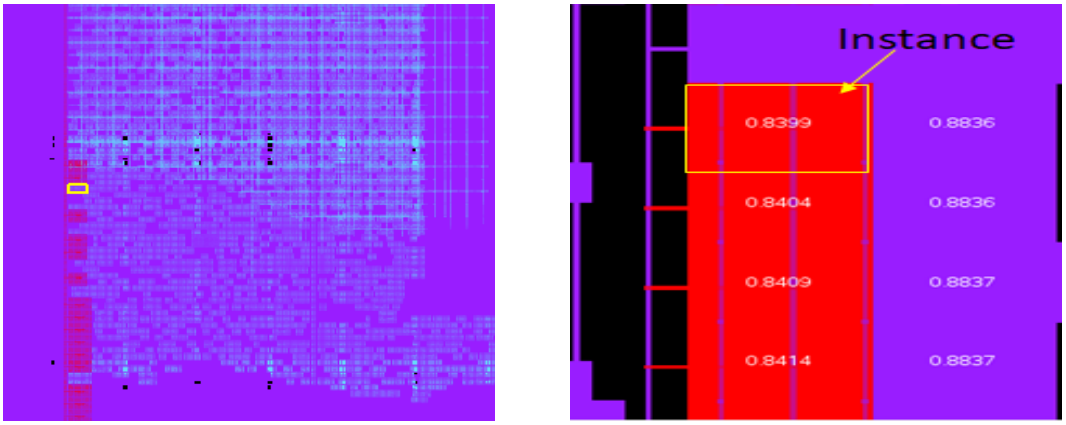
```
Worst Drop%              >5%              >6%              >7%


0.17%                    0                0                0
7.53%                    67               51               30
0%                       0                0                0
0%                       0                0                0
1.07%                    0                0                0


Worst Static IIR Drop :  7.53%


Total Static failing cells > 5% :  67
```

Figure 5.3: Summary report of Static IR Drop before fixing design



(a) (b)

Figure 5.4: (a) Static IR Drop in design, (b) Cells having Static IR Drop violation

$< 0.833\%$ respectively, which means majority of the cells are satisfying the static IR drop criteria. The design is zoomed and shown in Figure 5.5. The figure shows one of the Instance connected by metal layer 5 through layer 4 which is failing 5% static IR drop criteria. It also shows the actual voltages reaching the instances.

When the design is opened in PNR tool, as shown in Figure 5.5, it can be seen that for the PG net vccvssaon, the metal interconnect i.e., via 4 is missing. This is causing the cell to drive voltage from lower metal layers having higher resistance value, causing higher voltage drop. This fault can be corrected by using the PNR

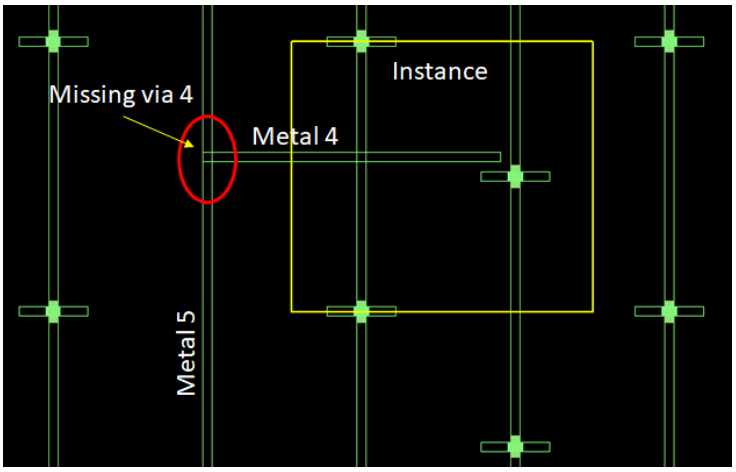


Figure 5.5: Missing via4 of instance having max voltage drop

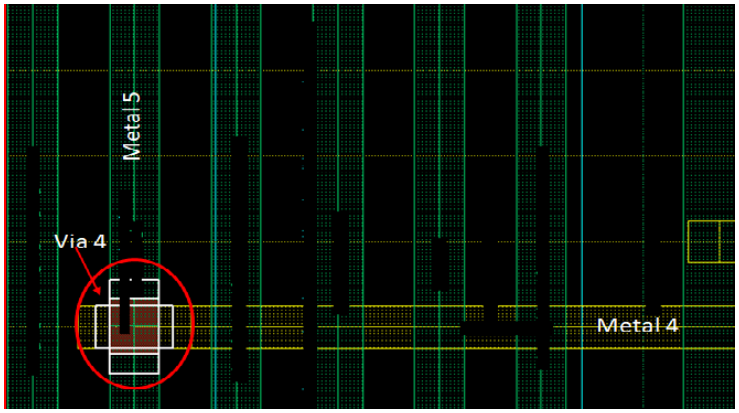


Figure 5.6: Placed via4 between metal4 and metal5 in PNR tool

tool and adding the missing via at the required points as shown in Figure 5.6. After placing the missing vias at the required points, the design is reloaded in IR/RV analysis tool. The Static IR check is run again on the new layout and the report is generated as shown in Figure 5.7.

The report shows, now no more cells are failing Static IR drop $> 5\%$ criteria. The design then looks clean as shown in Figure 5.8. The report also shows that the Static IR violation is reduced down to 1.06% by adding missing vias between metal layer 4 and metal layer 5. In this way the current is prevented from flowing through lower metal layers whic have high resistance due to lesser wire width.

```
Worst Drop%              >5%              >6%              >7%


0.18%                    0                0                0
0.67%                    0                0                0
0%                       0                0                0
0%                       0                0                0
1.06%                    0                0                0


Worst Static IIR Drop :   1.06%


Total Static failing cells > 5% :   0
~
```

Figure 5.7: Summary report of Static IR check after placing missing via4 in design

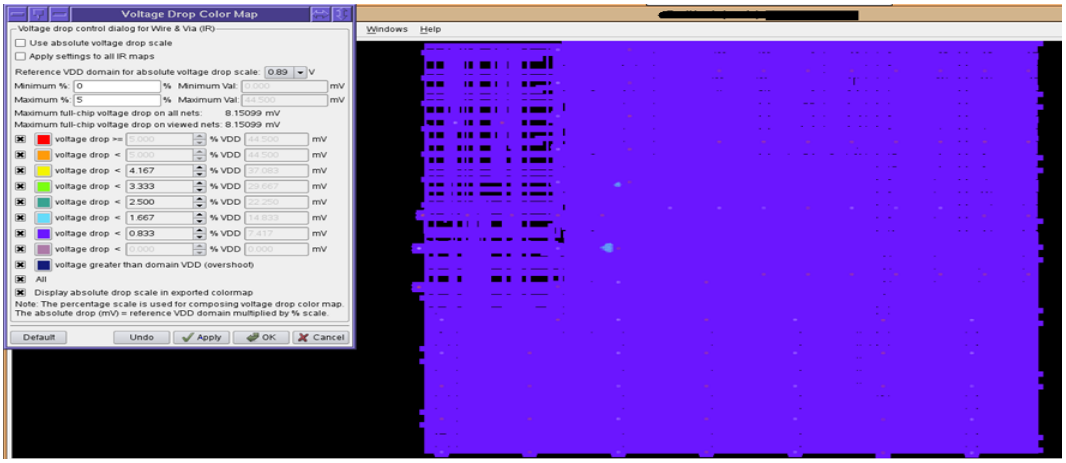


Figure 5.8: Design after cleaning Static IR violation

Hence, we conclude from the simulation results that a partition of SoC failing Static IR check of 5% limit due to missing vias at 67 places is corrected by adding just 4 missing vias at instances with maximum Static IR drop. The partition's IR signoff was found to be clean, successfully completing the evaluation of standalone IR/RV and PNR tool.

5.2 Correlation of In-design with Standalone IR/RV Analysis Tool

For correlation of In-design IR/RV analysis tool with standalone IR/RV analysis tool we need to compare analysis results of both the tools. In order to correlate we need to set all the required app_options (rail.redhawk_path, rail.tech_file, rail.switch_model_files, rail.lib_files, rail.macro_models and rail.databases) in IC Compiler II shell. The current in the design is supplied from the top power ground grid through taps that are created using "create_taps -top_pg" command. In-design tool has two power analysis engines. One is ICC2 and the other is Redhawk power engine which is invoked by default on giving analyse_rail command.

5.2.1 Static Voltage Drop Analysis

In In-design IR/RV analysis tool, designs layout is loaded in order to do its static IR analysis. After creating taps, using the Redhawk power engine, power_summary report(power numbers) are generated for static voltage drop analysis using command "analyze_rail -voltage_drop static -all_nets". This power_summary report contains summary of the power consumed by different frequency, clock roots, VDD domains, and cell types. In standalone tool also, power summary report for static analysis is generated. On comparing these power numbers with those generated by standalone IR/RV analysis tool, we see power numbers of some frequencies (1.84E+02 MHz) are missing in the power summary report of In-design IR/RV analysis tool as can be seen form Figure 5.9 and 5.10.

Also, the deviation of power numbers of different VDD domains, clock roots and cell types generated by In-design tool were seen to be large from that generated by standalone tool. The reason behind the deviation was the difference between the Timing Window (TW) files taken as input in both the tool. The Prime Time (PT)

STANDALONE

Power of different frequency (MHz) domain in Watt:

Frequen	total_p	leakage	interna	switchi	%_total	#inst_c
0.00E+00	5.76E-03	5.76E-03	0.00E+00	0.00E+00	7.11E+00	32420
4.77E+01	2.70E-05	6.92E-06	8.21E-06	1.18E-05	3.32E-02	140
7.07E+01	4.32E-03	1.49E-03	1.91E-03	9.23E-04	5.33E+00	21981
7.12E+01	7.67E-06	1.39E-06	2.64E-06	3.65E-06	9.46E-03	34
1.84E+02	2.24E-03	6.21E-04	9.50E-04	6.70E-04	2.76E+00	13572
1.84E+02	9.79E-04	2.52E-04	7.27E-04	0.00E+00	1.21E+00	9923
1.91E+02	2.76E-03	7.74E-04	1.25E-03	7.33E-04	3.40E+00	15736
7.36E+02	2.08E-02	6.85E-03	8.28E-03	5.69E-03	2.57E+01	107841
9.21E+02	2.60E-05	7.98E-06	1.14E-05	6.61E-06	3.20E-02	206
9.60E+02	4.29E-02	1.23E-02	1.66E-02	1.40E-02	5.29E+01	241002
9.77E+02	6.06E-04	2.07E-04	2.38E-04	1.61E-04	7.47E-01	3993
9.80E+02	5.25E-04	1.96E-04	2.22E-04	1.06E-04	6.47E-01	1898
1.00E+03	9.27E-05	4.09E-05	2.94E-05	2.25E-05	1.14E-01	294

Figure 5.9: Standalone IR/RV analysis tool's Static Power summary for different frequencies

IN-DESIGN

Power of different frequency (MHz) domain in Watt:

Frequer	total_p	leakage	interna	switchi	%_total	#inst_c
0.00E+00	7.29E-03	7.29E-03	0.00E+00	0.00E+00	1.99E+00	42208
4.77E+01	2.04E-05	6.92E-06	6.05E-06	7.43E-06	5.56E-03	140
7.07E+01	4.44E-03	1.49E-03	1.99E-03	9.64E-04	1.21E+00	21981
7.12E+01	3.36E-06	1.39E-06	7.39E-07	1.23E-06	9.14E-04	34
1.84E+02	3.61E-03	6.21E-04	1.89E-03	1.10E-03	9.82E-01	13572
1.91E+02	5.03E-03	7.74E-04	2.82E-03	1.43E-03	1.37E+00	15736
7.36E+02	9.86E-02	6.86E-03	5.58E-02	3.59E-02	2.69E+01	107841
9.21E+02	2.55E-04	7.98E-06	1.34E-04	1.13E-04	6.94E-02	206
9.60E+02	2.39E-01	1.26E-02	1.32E-01	9.46E-02	6.51E+01	241002
9.77E+02	4.64E-03	2.07E-04	2.96E-03	1.47E-03	1.26E+00	3993
9.80E+02	3.82E-03	1.96E-04	2.13E-03	1.49E-03	1.04E+00	1898
1.00E+03	3.24E-04	4.13E-05	1.54E-04	1.29E-04	8.83E-02	294

Figure 5.10: In-design IR/RV analysis tool's Static Power summary for different frequencies

tool generates the TW file which contains the timing data of the design, i.e. signal arrival time, slew rates, setup and hold time of each and every cell in the design. Standalone tool uses the PT generated TW file called as STA file whereas, in-design tool generates its own TW file which it gives as input to Redhawk engine for static IR analysis. Also, the frequency set in gsr of both the tools was different as can be seen in the comparison table shown in Figure 5.11.

To ensure that the reason of the deviation is the difference in TW file and frequency, the gsr file generated by in-design tool having frequency set as 1.84e+08 MHz and

	ICC2-RH Fusion .gsr	RH standalone .gsr
RC Tech file	Same	Same
RV Tech file	Not set	Set by RH
LEF	ICC2 generated	RH generated
DEF	ICC2 generated	RH generated
LIB	Copied from RH gsr	Set by RH
Switch_model	Copied from RH gsr	Set by RH
GDS cells	Copied from RH gsr	Set by RH

Power net definitions	VDD_NETS {
	vccsa_lv 0.650000
	vccst_lv 0.650000
	vccstg_lv 0.650000
	vccsagnpk 0.650000
	vccsagnpkaon 0.650000
	}
		VDD_NETS {
		vccsa_lv 1.050
		vccst_lv 1.050
		vccstg_lv 1.100
		vccagsh_ehv 1.800
		vccstg_fabric_lv 1.050
		}

Ground nets	0.00	0.00
Frequency	1.84094e+08	976.562e06
Temperature	108	100
PAD	ICC2 generated	Set by RH
STA	ICC2 generated	Set by RH
SPEF	ICC2 generated	Set by RH

Figure 5.11: Comparison of In-design tool's generated gsr with that of standalone tool for static IR drop analysis

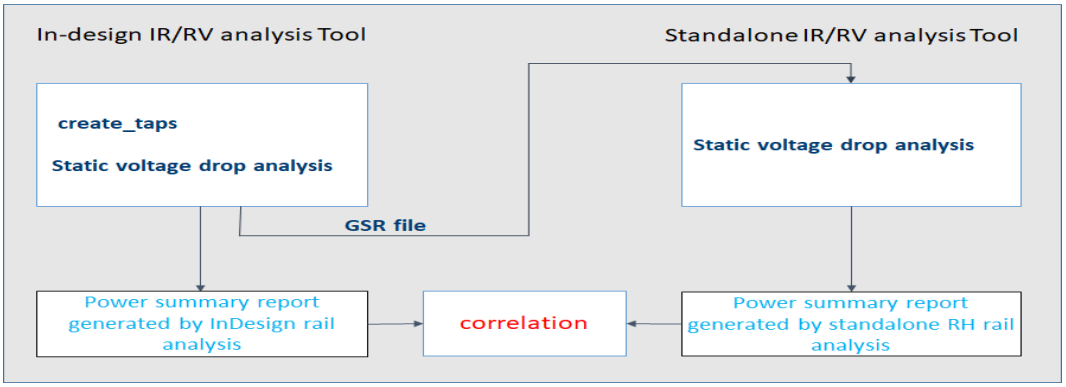


Figure 5.12: Data Flow for static analysis correlation of in-design and standalone IR/RV analysis tool

IC Compiler II generated is fed as input in the standalone tool as shown in Figure 5.12.

Power summary reports generated by the standalone tool using in-design tools gsr is compared with that generated by in-design tool. Results were similar to the previously conducted experiment as shown in Figure 5.13 and 5.14. As can be seen, power numbers for frequencies 70.7 MHz and 977 MHz is missing in standalone tools generated power report which confirms that the deviation is due to the above stated reason. Hence, The PT generated TW file is fed in in-design tool by storing

the files path in a new file and including this file as extra_gsr_option_file in analyse_rail command. Also, using the setapp_options, frequency is set to 976.56 MHz

IN-DESIGN

Power of different frequency (MHz) domain in Watt:

Frequenc	total_pw	leakage_	internal_	switchin	%_total_	#inst_c
0.00E+00	7.29E-03	7.29E-03	0.00E+00	0.00E+00	1.99E+00	42208
4.77E+01	2.04E-05	6.92E-06	6.05E-06	7.43E-06	5.56E-03	140
7.07E+01	4.44E-03	1.49E-03	1.99E-03	9.64E-04	1.21E+00	21981
7.12E+01	3.36E-06	1.39E-06	7.39E-07	1.23E-06	9.14E-04	34
1.84E+02	3.61E-03	6.21E-04	1.89E-03	1.10E-03	9.82E-01	13572
1.91E+02	5.03E-03	7.74E-04	2.82E-03	1.43E-03	1.37E+00	15736
7.36E+02	9.86E-02	6.86E-03	5.58E-02	3.59E-02	2.69E+01	107841
9.21E+02	2.55E-04	7.98E-06	1.34E-04	1.13E-04	6.94E-02	206
9.60E+02	2.39E-01	1.26E-02	1.32E-01	9.46E-02	6.51E+01	241002
9.77E+02	4.64E-03	2.07E-04	2.96E-03	1.47E-03	1.26E+00	3993
9.80E+02	3.82E-03	1.96E-04	2.13E-03	1.49E-03	1.04E+00	1898
1.00E+03	3.24E-04	4.13E-05	1.54E-04	1.29E-04	8.83E-02	294

Figure 5.13: Standalone IR/RV analysis tool's Static Power summary for different frequencies using in-design tools gsr

STANDALONE

Power of different frequency (MHz) domain in Watt:

Frequency	total_pw	leakage_	internal_	switchin	%_total_	#inst_c
0.00E+00	2.25E-02	2.25E-02	0.00E+00	0.00E+00	1.77E+01	308485
4.77E+01	6.12E-06	3.15E-06	2.47E-06	5.13E-07	4.84E-03	73
7.12E+01	1.20E-03	3.51E-04	7.61E-04	8.53E-05	9.46E-01	4463
1.84E+02	7.14E-04	1.12E-04	4.98E-04	1.03E-04	5.64E-01	2766
1.91E+02	4.74E-03	1.49E-03	2.86E-03	3.94E-04	3.75E+00	14476
7.36E+02	2.64E-02	1.77E-03	1.99E-02	4.82E-03	2.09E+01	35791
9.21E+02	8.45E-05	3.31E-06	6.99E-05	1.12E-05	6.67E-02	66
9.60E+02	7.02E-02	3.87E-03	5.08E-02	1.56E-02	5.55E+01	81911
9.80E+02	7.33E-04	5.13E-05	5.36E-04	1.46E-04	5.79E-01	799
1.00E+03	3.95E-05	4.05E-06	1.79E-05	1.76E-05	3.12E-02	75

Figure 5.14: In-design IR/RV analysis tool's Static Power summary for different frequencies using in-design tools gsr

as used by the standalone tool. In order to avoid supplying STA file externally in extra_gsr_option_file, TW file generated by PT IC Compiler II Fusion is proposed. PT IC Compiler II Fusion is a new another In-design STA tool that invokes PT tool from within IC Compiler II to generate TW file. From Figure 5.15 and 5.16, it can be seen that now all the frequencies are same and the power numbers so generated are also same resulting in zero deviation.

STANDALONE

Power of different frequency (MHz) domain in Watt:

Frequenc	total_pw	leakage_	internal_	switching	%_total_	#inst_
0.00E+00	2.25E-02	2.25E-02	0.00E+00	0.00E+00	1.77E+01	308485
4.77E+01	6.12E-06	3.15E-06	2.47E-06	5.13E-07	4.84E-03	73
7.12E+01	1.20E-03	3.51E-04	7.61E-04	8.53E-05	9.46E-01	4463
1.84E+02	7.14E-04	1.12E-04	4.98E-04	1.03E-04	5.64E-01	2766
1.91E+02	4.74E-03	1.49E-03	2.86E-03	3.94E-04	3.75E+00	14476
7.36E+02	2.64E-02	1.77E-03	1.99E-02	4.82E-03	2.09E+01	35791
9.21E+02	8.45E-05	3.31E-06	6.99E-05	1.12E-05	6.67E-02	66
9.60E+02	7.02E-02	3.87E-03	5.08E-02	1.56E-02	5.55E+01	81911
9.80E+02	7.33E-04	5.13E-05	5.36E-04	1.46E-04	5.79E-01	799
1.00E+03	3.95E-05	4.05E-06	1.79E-05	1.76E-05	3.12E-02	75

Figure 5.15: Standalone IR/RV analysis tool's Static Power summary for different frequencies using PT TW and 976.56 MHz frequency

IN-DESIGN

Power of different frequency (MHz) domain in Watt:

Frequen	total_pv	leakage_	internal_	switching	%_total_	#inst_
0.00E+00	2.25E-02	2.25E-02	0.00E+00	0.00E+00	1.77E+01	308485
4.77E+01	6.12E-06	3.15E-06	2.47E-06	5.13E-07	4.84E-03	73
7.12E+01	1.20E-03	3.51E-04	7.61E-04	8.53E-05	9.46E-01	4463
1.84E+02	7.14E-04	1.12E-04	4.98E-04	1.03E-04	5.64E-01	2766
1.91E+02	4.74E-03	1.49E-03	2.86E-03	3.94E-04	3.75E+00	14476
7.36E+02	2.64E-02	1.77E-03	1.99E-02	4.82E-03	2.09E+01	35791
9.21E+02	8.45E-05	3.31E-06	6.99E-05	1.12E-05	6.67E-02	66
9.60E+02	7.02E-02	3.87E-03	5.08E-02	1.56E-02	5.55E+01	81911
9.80E+02	7.33E-04	5.13E-05	5.36E-04	1.46E-04	5.79E-01	799
1.00E+03	3.95E-05	4.05E-06	1.79E-05	1.76E-05	3.12E-02	75

Figure 5.16: In-design IR/RV analysis tool's Static Power summary for different frequencies using PT TW and 976.56 MHz frequency

5.2.2 Dynamic Voltage Drop Analysis

Similar to Static IR analysis, in In-design IR/RV analysis tool, designs layout is loaded in order to do its dynamic IR analysis. After creating taps, using the Redhawk power engine, power_summary report(power numbers) are generated for dynamic voltage drop analysis using command "analyze_rail -voltage_drop dynamic -all_nets". In standalone tool also, power summary report for dynamic analysis is generated. On comparing these power numbers with those generated by standalone IR/RV analysis tool, we see power numbers of different cell types generated by

standalone tool are three times greater than that generated by In-design IR/RV analysis tool. This is because Redhawk is very pessimistic whereas, ICCompiler II is optimistic. Redhawk takes into account the worst timing scenario whereas, ICCompiler II takes the best timing scenario into account.

STANDALONE

Power of different cell types in Watt:

cell_type	total_pwr	leakage_p	internal_p	switching_	%_total_p	#inst_co
combinational	4.82E-01	1.51E-02	1.91E-01	2.75E-01	6.41E+01	384735
decap	1.10E-05	1.10E-05	0.00E+00	0.00E+00	1.47E-03	3647
I/O	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
latch_and_FF	2.12E-01	6.38E-03	1.80E-01	2.54E-02	2.82E+01	52418
memory	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
misc_seq	5.73E-02	1.38E-03	4.38E-02	1.22E-02	7.63E+00	3915
Total	7.51E-01	2.28E-02	4.16E-01	3.13E-01	1.00E+02	444715

Figure 5.17: Standalone IR/RV analysis tool's Dynamic Power summary for different cell types

IN-DESIGN

Power of different cell types in Watt:

cell_type	total_pwr	leakage_	internal_p	switching_	%_total_pv	#inst_co
combinational	2.46E-01	2.34E-02	9.81E-02	1.25E-01	6.70E+01	384733
decap	3.17E-06	3.17E-06	0.00E+00	0.00E+00	8.62E-04	1042
I/O	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
latch_and_FF	1.03E-01	5.60E-03	8.79E-02	9.87E-03	2.81E+01	58901
memory	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
misc_seq	1.76E-02	1.13E-03	1.39E-02	2.64E-03	4.80E+00	4229
Total	3.67E-01	3.01E-02	2.00E-01	1.37E-01	1.00E+02	448905

Figure 5.18: In-design IR/RV analysis tool's Dynamic Power summary for different cell types

5.2.3 Electromigration

Similar to Static and Dynamic IR analysis, in In-design IR/RV analysis tool, designs layout is loaded in order to do its Electromigration analysis. After cre-

ating taps, using the Redhawk power engine, power_summary report(power numbers) are generated for Electromigration analysis using command "analyze_rail -electromigration -voltage_drop static -all_nets".

In standalone tool also, power summary report for Electromigration analysis is

STANDALONE

Power of different cell types in Watt:

cell_type	total_pw	leakage_	internal_	switching	%_total_	#inst_c
combinational	1.41E-01	3.09E-03	5.04E-02	8.80E-02	6.30E+01	76379
decap	2.55E-05	2.50E-05	4.58E-07	0.00E+00	1.13E-02	13035
I/O	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
latch_and_FF	5.64E-02	2.10E-03	4.64E-02	7.88E-03	2.51E+01	9965
memory	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
misc_seq	2.68E-02	4.00E-04	1.07E-02	1.57E-02	1.19E+01	1041
Total	2.25E-01	5.62E-03	1.08E-01	1.12E-01	1.00E+02	100420

Figure 5.19: Standalone IR/RV analysis tool's EM Power summary for different cell types

IN-DESIGN

Power of different cell types in Watt:

cell_type	total_pw	leakage_	internal_	switching	%_total_	#inst_c
combinational	7.62E-02	3.09E-03	2.16E-02	5.15E-02	5.82E+01	75162
decap	2.15E-05	2.12E-05	2.92E-07	0.00E+00	1.64E-02	2270
I/O	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
latch_and_FF	3.67E-02	2.10E-03	2.96E-02	5.00E-03	2.80E+01	9965
memory	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0
misc_seq	1.80E-02	4.00E-04	6.57E-03	1.10E-02	1.37E+01	1041
Total	1.31E-01	5.61E-03	5.77E-02	6.75E-02	1.00E+02	88438

Figure 5.20: In-design IR/RV analysis tool's EM Power summary for different cell types

generated. On comparing these power numbers with those generated by standalone IR/RV analysis tool, we see power numbers of different cell types generated by standalone tool are twice of that generated by In-design IR/RV analysis tool. As stated above this is because Redhawk is pessimistic whereas, ICCompiler II is optimistic.

5.2.4 IR Aware Placement and Routing

In the normal design flow, IR/RV sign-off is carried out after completing the design's detailed placement and routing (4 to 5 days), which takes a significant amount of time (2 to 3 days). To improve this project turn-around time (1 week), IR/RV sign-off is carried out during the process of designing called as IR aware placement and routing. The improved design flow is shown in the Figure 5.21.

Following the IR aware design flow, the floorplan database is used for global place-

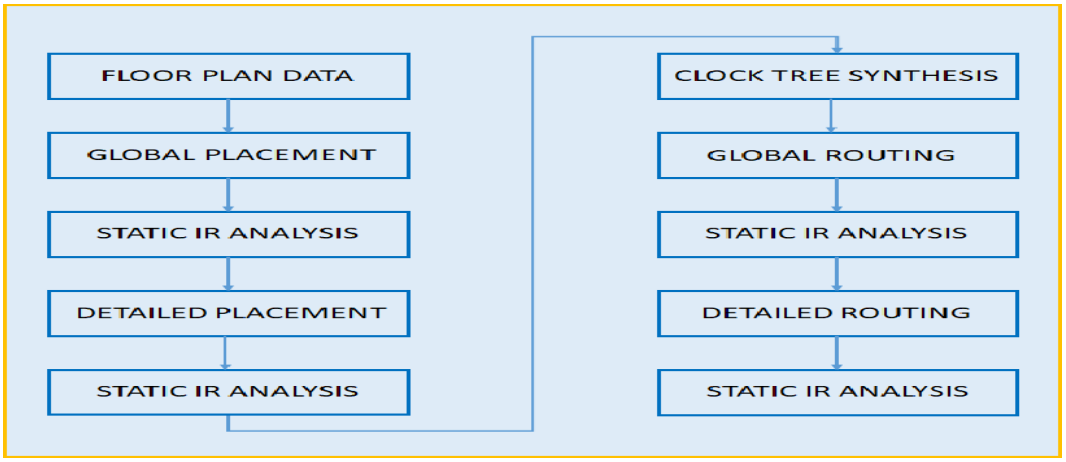


Figure 5.21: IR Aware Design Flow

ment followed by legalization for removing the placement violations, after which the resulting design is checked for static IR violation with a minimum threshold value of 4% and maximum 5%. The maximum threshold value is selected such that only 1% of cells should have static IR violation above 5%. The minimum threshold is set by the foundry for a given project. Once the static IR analysis is completed the globally placed and legalized database is used for detailed placement where the tool improves the legalized placement in an iterative manner by rearranging a small group of modules in a local region, keeping all other modules fixed. Detailed placement database is now again check for static IR violation. During detailed placement the tool takes into account the cells falling in 4% to 5% criteria in order remove static IR violation. Hence, any violations caused due to placement are removed in parallel

with design flow. It can be justified by comparing the timing report from QoR of detailed placement database of normal flow (before IR aware) with that of IR aware flow (after IR aware). As shown in Figure 5.22, the Worst Negative Slack (WNS), Total Negative Slack (TNS) and Number of Violating Endpoints (NVE) of the design after IR aware has reduced significantly from that before IR aware.

Also. it can be justified from Figure 5.23 which shows the cell count falling in 4%

	BEFORE IR AWARE			AFTER IR AWARE		
Context	**WNS**	**TNS**	**NVE**	**WNS**	**TNS**	**NVE**
func_max_highvcc (Setup)	-223.34	-44695.4	860	-40.11	-565.09	72
func_max_lowvcc (Setup)	-223.34	-44694.3	860	-40.11	-565.09	72
func_max (Setup)	-223.34	-47780.9	954	-40.11	-565.09	72
Design (Setup)	-223.34	-47781.9	954	-40.11	-565.09	72

Design (Hold)	--	0	0	--	0	0

Cell Area (netlist)	164651.6			164117.7		
Cell Area (netlist and physical only)	175377.2			174843.3		
Nets with DRC Violations	2446			1183		

Figure 5.22: Comparison of Timing report with and without IR aware placement

BIN	BEFORE IR AWARE	AFTER IR AWARE
4	1349	2
4.1	1180	1
4.2	1342	3
4.3	1067	1
4.4	852	0
4.5	687	3
4.6	148	0
4.7	25	1
4.8	3	0
4.9	1	1
5	1	0
5.1	2	2
5.2	0	2
5.3	0	1
5.4	0	1
5.5	1	1
5.6	0	1
5.7	2	0
5.8	1	1
5.9	0	0
cell with drop > 4%:	**6678**	**53**

Figure 5.23: Number of cells falling in 4% to 5% static IR violation range

to 5% static IR violation criteria. Without IR aware total 6678 cells were failing

static IR whereas, With IR aware placement only 53 cells are violating. Figure 5.24 shows the graph for the same which further justifies that IR aware placement reduces the static IR violation significantly during the placement itself. The red line in the graph show the static IR violating cell count when placement is done without checking for static IR drop whereas, the green line indicates the the cell count when placing the cells after checking static IR violations. Y-axis of the graph gives the cell count in multiples of 1000 whereas, X-axis gives the static IR percentage drop values.

Clock tree synthesis is done on the new placement database, once the IR aware

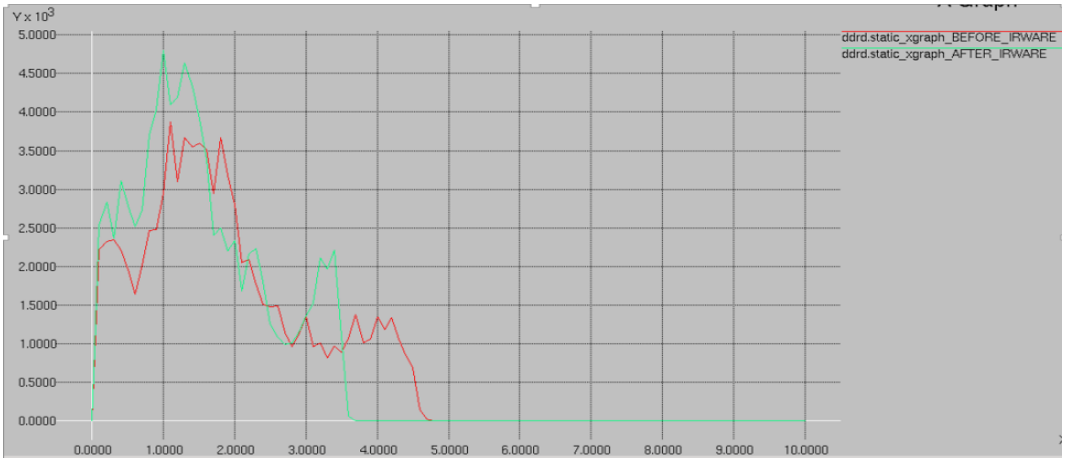


Figure 5.24: Graph of static IR violation with and without IR aware placement

placement is completed. After doing global routing on CTS database again static IR analysis is done, now taking the minimum threshold value 3% and maximum threshold value of 4%. Using this criteria, the cells following in this range are taken into account while doing detailed routing which is followed by static IR analysis.

Comparing the timing data from QoR of detailed routing database of normal flow (before IR aware) with that of IR aware flow (after IR aware), as shown in Figure 5.25, we can see that the WNS, TNS and NVE of the design after IR aware has reduced significantly from that before IR aware.

Again,it can be justified from Figure 5.26 which shows the cell count falling in 3%

Timing	BEFORE_IRAWARE			AFTER_IRAWARE		
Context	WNS	TNS	NVE	WNS	TNS	NVE
func_max_highvcc (Setup)	-1478.2	-258007	4156	-439.45	-35602.1	624
func_max_lowvcc (Setup)	-1478.2	-258071	4156	-438.25	-35007.7	627
func_max (Setup)	-1478.2	-262784	4192	-438.25	-35371.2	685
Design (Setup)	-1478.2	-262785	4192	-439.45	-36146.4	685
Design (Hold)	--	0	0	--	0	0

Figure 5.25: Comparison of Timing report with and without IR aware routing

BIN	BEFORE_IRAWARE	AFTER_IRAWARE
3	1134	1923
3.1	889	1964
3.2	1299	2194
3.3	1177	1919
3.4	1209	489
3.5	1177	14
3.6	1515	2
3.7	1511	1
3.8	1295	0
3.9	1125	1
4	567	0
cell with drop > 3%	**12938**	**8551**

Figure 5.26: Number of cells falling in 3% to 4% static IR violation range

to 4% static IR violation criteria. Without IR aware total 12938 cells were failing static IR whereas, With IR aware routing only 8551 cells are violating. Figure 5.27 shows the graph for the same which further justifies that IR aware routing reduces the static IR violation significantly during the routing stage itself. The red line in the graph show the static IR violating cell count when routing is done without checking for static IR drop whereas, the green line indicates the cell count when routing the cells after checking static IR violations. Y-axis of the graph gives the cell count in multiples of 1000 whereas, X-axis gives the static IR percentage drop values. Hence we conclude that IR aware placement and routing improves the design turnaround

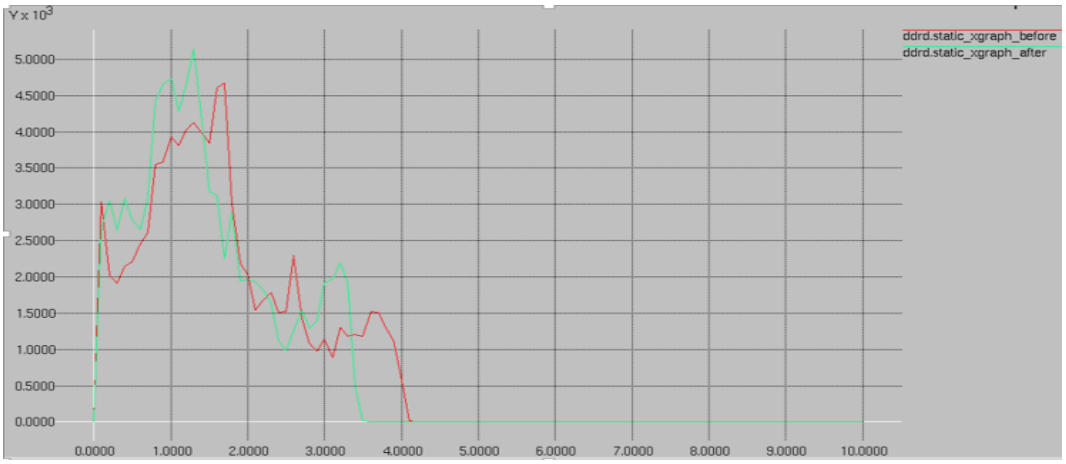


Figure 5.27: Graph of static IR violation with and without IR aware routing

time by reducing it from weeks to approximately 4 to 5 days.

5.2.5 Conclusion

Table 6.1 shows comparison of time taken to generate placement database following traditional design flow vs IR aware flow.

As we can see from the table, IR aware flow consumes the same amount of time as

Table 5.1: Flow runtime comparison table

Stage	**Runtime of Tradition Flow**	**Runtime of IR Aware Flow**
import_design	00:04:35	00:04:35
init_floorplan	00:06:34	00:06:34
setup_timing	00:12:48	00:12:48
floorplan	02:15:23	02:15:23
pre_place	00:17:03	00:16:58
place	02:20:19	02:56:02
place_refine	01:45:29	01:11:12
Total	**07:02:18**	**07:03:32**

the normal flow but it completes the static IR checks during the flow thus, saving the time taken by the designer to analyze the design for static IR and other RV check after generating the layout. Any necessary correction can be done according to the IR/RV analysis results during the flow itself.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Analyzing the violation with standalone IR/RV analysis tool and fixing them with PNR tool, typically takes more than a week to complete. In the above mentioned tools, PNR tool alone takes minimum of 4 days to generate layout whereas, standalone IR/RV analysis tool takes minimum of 2 days for IR/RV analysis of the layout. Following normal design flow, to generate IR violation clean layout, it takes approximately 2 to 3 week. To overcome this huge overhead of time required to complete one cycle of analysis and fixation of violation, In-Design IR/RV analysis tool is employed.

From the results, taking into account only a part of Physical Design flow, i.e. Floorplanning and Placement, we have seen that the Traditional flow alone takes 7 hours to complete Placement. On the other hand IR aware flow completes IR violation check as well as Placement in approximately same time. Thus, we conclude that In-design tool reduce potential delay in tape-out by improving project turn-around time from 2-3 weeks to 1 week to generate IR violation clean layout, helping the designer to meet the project deadlines with less effort.

6.2 Future Scope

The Intel Technologies will keep on providing the new platforms with increased performance and better functionality by breakthrough innovation and cutting-edge technology development.

By proving the correlation between the standalone and the In-Design IR/RV analysis tool, the overall project designing time at Intel can be significantly reduced. Presently, the violations are being fixed by the designer manually but fixing manually is prone to human errors, so, we plan to automate this fixing of violations such that the tool can automatically fix the violations at any stage, whenever it encounters. This will save a lot of time of the designer, increasing the productivity of the company.

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