SPI Analysis and Voltage Level Translator Selection

Major Project Report

Submitted in fulfillment of the requirements
for the degree of

Master of Technology
in
Electronics & Communication Engineering
(Embedded Systems)

By

Venoo Jadav

(17MECE06)

Electronics & Communication Engineering Department
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May 2019

Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in Embedded Systems at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Venoo Jadav

17MECE06

Certificate

This is to certify that the Major Project entitled **"SPI Analysis and Voltage Level Translator Selection"** submitted by **Venoo Jadav (17MECE06)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in Embedded Systems, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

Dr Tanish Zaveri	Dr N. P. Gajjar
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Head, EC Dept.	Director, IT - NU
Date :	Place : Ahmedabad

Statement of Originality

I, **Venoo Jadav**, Roll. No. **17MECE06**, give undertaking that the Project Report on "**SPI Analysis and Voltage Level Translator Selection**" submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electronics and communication (Embedded System)** of Institute of Technology, Nirma University, Ahmedabad, contains no material that has been awarded for any degree or diploma in any university or school in any territory to the best of my knowledge. It is the original work carried out by me as part of on-going research work in ARM embedded technology Pvt. Ltd. and I give assurance that no attempt of plagiarism has been made. It contains no material that is previously published or written, except where reference has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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Date:

Place:

Endorsed by

Dr. Tanish Zaveri

Acknowledgement

I would like to express my gratitude and sincere thanks to **Dr. N.P.Gajjar**, PG Coordinator of M.Tech Embedded Systems and **Dr. Tanish Zaveri** for their guidance during the review process.

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- Venoo Jadav

17MECE06

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Abstract

Multiple integrated circuits are used in designing a system to meet better power and performance demands. These devices operate at different voltages and so has different logic levels which necessitate the use of voltage level translators between them. This report gives a brief understanding of voltage level translators aimed at choosing the best device as per design requirements. In addition, the report also highlights a study on asynchronous and synchronous serial protocols which will be used as a communication medium between devices and logic translator along with a comparison between features of the serial protocols. Results show research on various level translators available in the market with respect to the design requirements of the system.

Abbreviation Notation and Nomenclature

SoC ..... System on Chip
SPI ..... Serial Peripheral Interface
UART ..... Universal Asynchronous Receiver Transmitter
I2C ..... Inter-Integrated Circuit
VLT ..... Voltage Level Translator
MOSI ..... Master out slave in
MISO ..... Master in slave out
SS ..... Slave Select
PCB ..... Printed Circuit Board
TTL ..... Transistor Transistor Logic
CMOS ..... Complementary Metal Oxide Semiconductor

Chapter 1

Introduction

1.1 Motivation

With ever increasing demand for efficient power, increased performance and time-to-market constraints, several methodologies and manufacturing technologies are invented for the transistor to be as small as possible. Due to this SoC works at way lesser voltage but gives faster and better performance. But this enhancement also has consequences in terms of board designing. Design Engineers now need voltage level translators for interfacing integrated circuit devices to SoC since SoC work at lower voltage levels than its peripherals.

1.2 Problem Statement

There has been numerous different types of technological inventions in the field of semiconductor manufacturing which has in turn allowed those semiconductors to occupy less real-estate and to be able to work at a lesser voltage such that their performance can be increased with decrease in power consumption. [1] Now to make use of these semiconductors with its peripherals on board, voltage level translators become essential. Voltage translators facilitate communication between these two devices. They connect two devices with different voltage levels or logic levels to each

other and make the connection possible. This report focuses on understanding level translators, its types available in market and its characteristics to compare with its application, also SPI protocol has been compared and analyzed with other protocols to understand its frequent use in today's applications.

1.3 Approach

Understanding and comparing SPI protocol with other synchronous and asynchronous protocols to understand its advantages and disadvantages with respect to using other protocols. Understand the need for level translators in circuit design, understanding types of translators and their use case environment and finally using all this knowledge to solve a real time issue in a project shown in results.

1.4 Scope of Work

This report is divided into two parts, first being the study of SPI and other synchronous and asynchronous protocols and a comparison of them. Here concept of asynchronous protocols is discussed first. Their use case and then the problem associated with using asynchronous protocols is discussed. Then comes in depth study of SPI protocol and at last a comparison between UART and I2C is discussed. In the second part of the thesis voltage level translators are discussed. Starting with use case of level translators and the problems that came with not using them in circuit design. Then various types and methods of voltage translators are discussed. Then various parameters which taken into consideration while selecting level translators are noted. At last a table is shown in which shows an actual use case where various translators are compared which were selected for an actual project.

1.5 Outline of Thesis

This report covers the work presented and used for selecting voltage level translator in a circuit design. Selecting VLT involved taking care of several design constraints of the circuit. The chapter two covers study of asynchronous and synchronous protocols and SPI, QSPI, UART and I2C protocols are explored. The chapter three covers use-case of VLT, problems associated without using VLT, types and methods of VLT. The chapter four covers electrical characteristics of VLT. The last chapter describes comparison of various VLT for their characteristics.

Chapter 2

SPI Analysis

2.1 Introduction

In the world of ever improving and increasing multimedia contents, data processing increases and for this embedded application have evolved them selves to cope up with this demand by adding more features to their systems. These extra features have several demands and often limited my the resources on the system. These leads to adding extra resources to the system for example adding more memory to resolve memory size limitations. This compromises the pin count that SoC is having leads to the design being more complex. So to face these requirements SoC has an external interface named Quad-SPI which enables interfacing with external memory. This can be used for applications like data transfer which can enable system to reach the requirement level necessary [2].

2.2 Everything Wrong with Serial Ports

A serial protocol usually has two lines for its data transfer operation named Tx(Transmitter) and Rx(Receiver). The reason for calling them asynchronous is that there is neither any synchronization between sender and receiver nor is there

any control over the data that is transmitted on transmission line. Now normally computers are synchronized with one another on one clock-signal coming from a source now this becomes an issue if two devices are receiving clock from difference source.[2]

To solve this problem asynchronous serial connections have came up with adding extra bits called start-bit and stop-bit with every byte so that the receiver can synchronize with transmitter. Also both sides agree in the beginning a set speed at which communication has to happen. Still there are some slight differences in data transmitted and received but that can be handled because receiver re synchronizes at the beginning of each byte.[2]

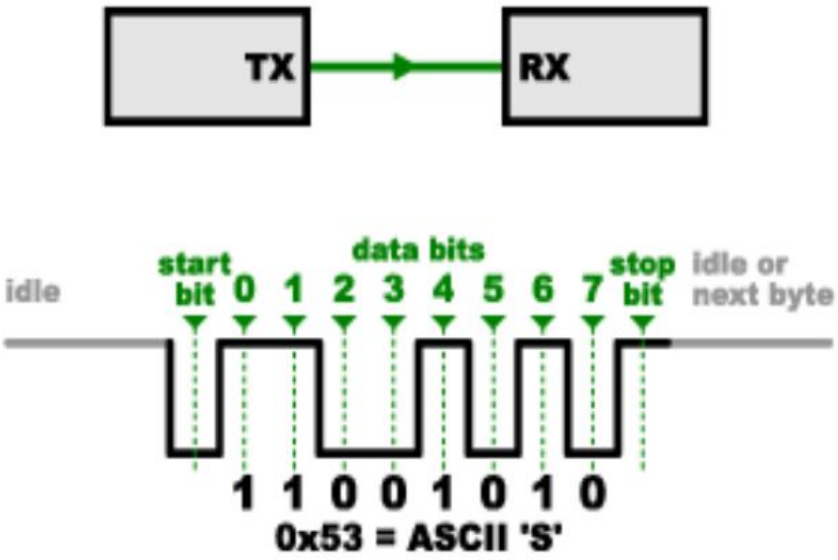

Figure 2.1: Asynchronous Protocols
[2]

Asynchronous protocols works nicely but have overhead in terms start and stop bits which is sent with every byte, and the hardware which is required is complex to send and receive data. If both sides are not operating at equal speed, than the

received data will be garbage. This is because receiver is checking for the bits at predefined period of time.[2]

2.3 A Synchronous Solution

Now comes SPI which works differently than other protocols. SPI is also known as synchronous protocol because it has separate lines for data and clock. This helps in keeping communication between transmitter and receiver in sync. The clock here tells when to sample data on the bus. This could be rising or falling edge of the clock. When the receiver detects the predefined edge to see, it will immediately look at the data line to read next data. Speed need not be defined in this scenario. [2]

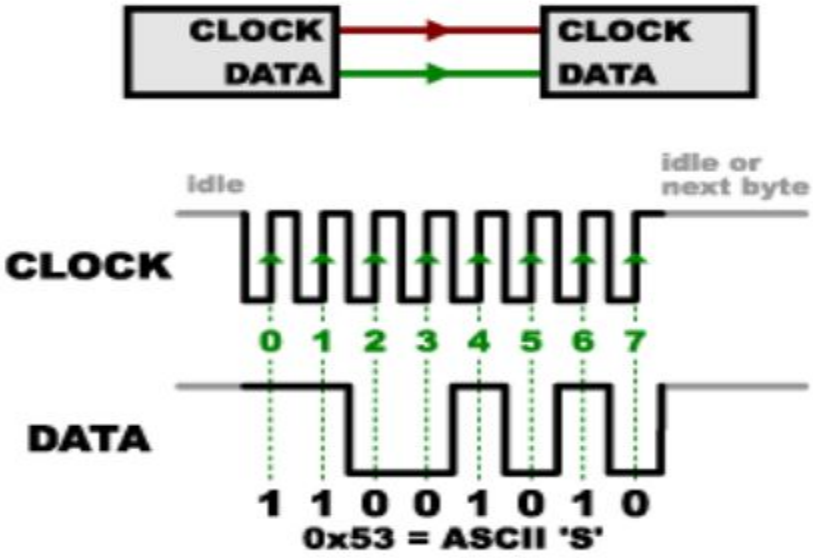

Figure 2.2: Synchronous Protocols
[2]

2.4 Receiving Data

In SPI, CLK signal is generated by only one side i.e. master. The other side is called the slave. There is always only one master, but there can be multiple slaves. There are two other lines in SPI called MOSI and MISO.When data is sent from the master to a slave, it's sent on a data line called MOSI which refers to Master Out Slave In. If the slave needs to send a message back to the master, it continues to generate clock and data is send into the bus at specific intervals on the line called MISO which refers to Master In Slave Out .

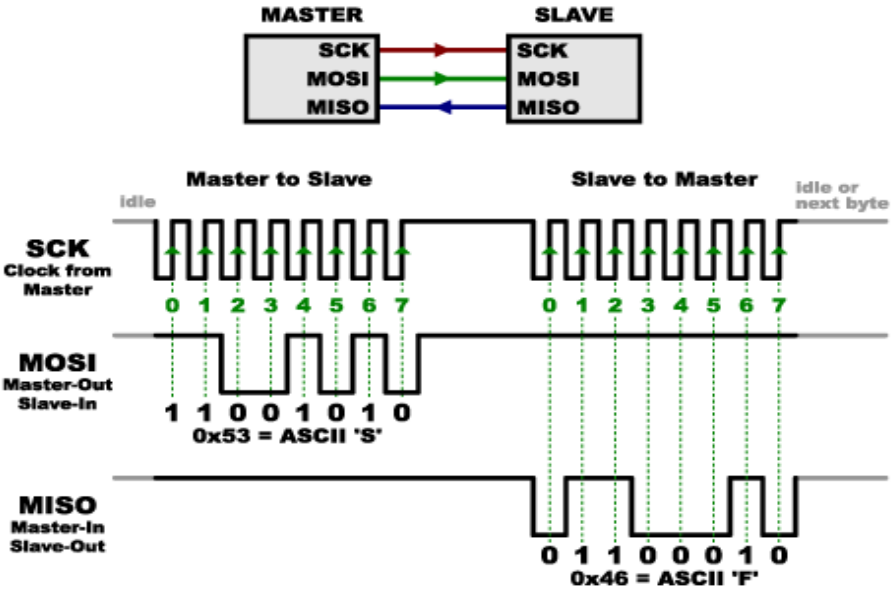

Figure 2.3: Receiving Data
[2]

Here master is the one who always generates the clock but it needs to know the amount of data that slave needs to return and the instance at which slave wants to communicate. In asynchronous communication is was not the case as random amount of data was send in either direction at any time. In regular use this isn't a problem, as SPI is generally used to talk to sensors that have a very specific com-

mand structure. For example, if a command is send to read data, it is known how much data will the receiver send. There also are cases where receiver wants to send variable amount of data, then it first sends the length of the data to be send and then lets master retrieve full data. SPI is Full Duplex which means that transmission and reception of data can be done at the same time.

2.5 Slave Select

The fourth line is SS(Slave Select). This line is used to wake up or select the slave that master wants to talk to and is also used when multiple slaves are there of that master can select specific slave to talk to. Normally SS line is held high which actually keeps the slave disconnected from the bus and gets connected only when the line is turned low. This type of logic is called active low logic. When transmitter wants to talk to slave, its SS is brought low and slave is activated. After the transmission is completed, the line is again held high so that slave gets disconnected from master. But there is a limit to the amount to data transfer that than be done with SPI.

2.6 Advantages of SPI

a. It is faster than asynchronous serial communication protocols.

b. Receiver hardware is very simple like shift register.

c. SPI can support multiple slaves.

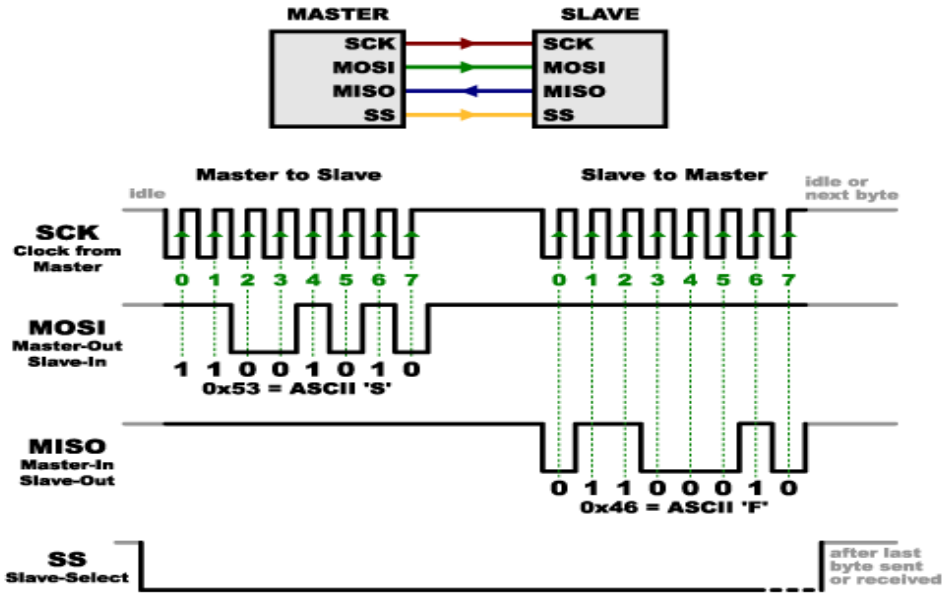

Figure 2.4: Slave Select
[2]

2.7 Disadvantages of SPI

a. More serial lines are required compared to other protocols.

b. Cannot send random data so communication must be predefined first.

c. Only master can control all the communication on bus i.e. slaves cannot talk to each other directly.

d. It is required that each slave connected to master needs a separate SS line so if there are numerous slaves than it becomes difficult for master to connect to all of them.

2.8 QSPI

QSPI (Quad-SPI) is a synchronous serial protocol which super seeds SPI in terms of data transfer speeds. QSPI in quad mode consists of four data transfer

lines(MISO, MOSI, IO3, IO4), one clk line(SCK) and one slave select line(CS/SS). The Quad SPI also supports traditional SPI as well as dual SPI where communication happens on two lines. Quad mode in SPI is way faster than normal mode in terms of data transfer because data can be transferred from four lines instead of two or one. Quad SPI multiples the throughput by four time compared to classical SPI.[3]

2.8.1 Main benefits of Quad-SPI interface

Benefits	**Comments**
Low pin count	Single mode, Double mode and Quad-SPI mode are supported. Six pins are used in Quad-SPI and four pins are used for single or dual SPI. Saves GPIOs to be used for other purposes.
PCB design is easy	Faster and better PCB design is possible
Save space for smaller size applications	Footprint is smaller comparatively. memories.
Save cost	Easier and faster design allows a lower development cost.
Executable	Memory found in internal chip can be extended using QSPI by connecting external memory. seen as an internal memory. Code can be executed from external memory using flash.
High performances	Throughput is multiplied by four versus traditional SPI. Perfect for graphical applications.
Supports all Quad-SPI memories available in the market	Flexible and highly configurable frame format is there.

Table 2.1: Benefits of using QSPI

2.9 Comparison with other protocols

Features	**UART**	**I2C**
Full Form	Universal Asynchronous Receiver Transmitter	Inter-Integrated Circuit
Pin Designations	TxD : Transmit Data To RxD : Receive Data From	SDA: Serial Data SCL: Serial Clock
Data rate	This being asynchronous, the two devices that are communicating should be at equal rate. Data rate which is maximum is supported of about 230 Kbps to 460kbps	I2C has 100 kbps, 400 kbps, 3.4 Mbps of data transfer speeds.
Distance	Less, about 50 feet	More than UART
Type of communication	Asynchronous-Communication	Synchronous-Communication
Number of masters	NA	single or more
Clock	There is no single clock for both devices, independent clocks used.	Clock is single only and common between devices.
Hardware complexity	lesser	more
Advantages	Widely popular due to UART being supported in many 9-pin modules.	Masters that can be connect are more than one. Needs only 2 wires for communication. Data ;ine addressing is comparatively simple.
Disadvantages	Data transfer can be done between two devices. Works only at a pre-defined data transfer speed.	Complexity of circuit is more when I2C is used in terms of slaves and masters. I2C works on half-duplex.

Table 2.2: Comparison with other protocols

Chapter 3

Voltage Level Translator Selection

3.1 Introduction

Several advances and improvements have been made in manufacturing and fabrication processes which enabled us to have smaller footprint of components in circuit designing and also that they can operate at lower supply voltages. This development is done to support many high performance and low-power applications. There has to be something which can help in connecting different components working at different logic levels in a circuit design.[1]

The technologies that are used in today's circuit design dictate the high and low logic threshold levels that the devices can achieve. So due to this level translators become essential in circuit design.[1]

3.2 What does a voltage translator do?

Voltage translator is a circuit which can help translating from one logic level to another which would in turn allow both sides to be compatible to each other, such as TTL or CMOS. In today's circuit design level shifter is often used to bridge low-

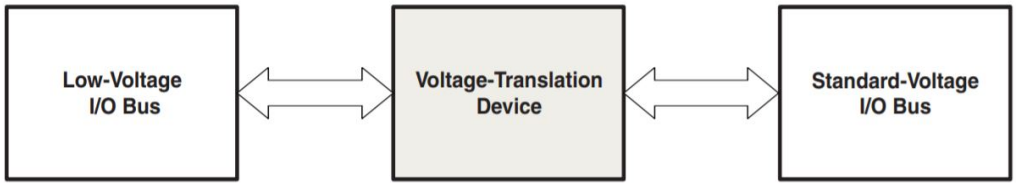

Figure 3.1: Flexible Voltage-Translation Application
[5]

powered SoC with its peripherals running at higher voltage than SoC. [5]

Latest technology which is used to manufacture today's components actually determine the logic threshold levels of those devices. So when these devices are connected to each other on a circuit design, level translators becomes essential. There are certain rules when designing a circuit which level translators. They are:

a. Output high voltage (VOH) of driver device during transmission has to be greater than input high voltage (VIH) to the receiver device.

b. Output low voltage (VOL) of driver device during transmission has to be less than input low voltage (VIL) to the receiver device.

c. There is a certain tolerance of the receiver and I/O voltage from driver should not exceed it.

3.3 Problems Occurring Without Voltage-Level Translation

When two devices are equipped with different supply voltages, level translators are necessary. There could be two conditions where level translators are necessary:[1]

a. A high-voltage device might have to drive a low-voltage device.

b. A low-voltage device might have to drive a high-voltage device.

If the high voltage device is what is driving the circuit than it can operate smoothly if following conditions are met:

- Receiving device should be such that it could tolerate logic levels of high voltage device.
- The receiver logic levels must pass through the VIL and VIH logic level range specified by the receiver device.

In case driver is a device with a low voltage than the circuit design might not function correctly without a voltage translator. Here voltage difference is too big for the circuit to operate. In this case, the device with low voltage might not provide enough voltage to make receiver to work, this makes the system non-functional.

3.4 Types of VLT

a. **Unidirectional**: Translation happens only in one direction i.e. from high-to-low or low-to-high.

b. **Bidirectional with dedicated ports**: Translation happens in both directions but data direction of a pin does not change.

c. **Bidirectional with External Direction indicator**: Translation can happen in both directions and the direction is controlled via a direction pin. When triggered, inputs become outputs and vice versa.

d. **Bidirectional Auto sensing**:Translation happens bidirectionally without external stimulus from a dedicated direction controlled pin.

3.5 Methods of Voltage Level Translation

There are various methods through which voltage level translation can be performed. The devices to be selected and placed in designing a circuit are chosen by checking following parameters like

- Consumption of power
- Logic levels of the device
- Device's capability to source current

First preference for level translation method is the use of bidirectional level translators or dual supply level translators. These can benefit circuit design in translating voltages bidirectionally as the name suggests. They help in translating from a device with low input voltage to a device with high output voltage as well as from a device with high input voltage to a device with low output voltage. Consumption of power is lower in these devices compared to others.[1]

Second option for level translation is to use open drain devices. These devices can do a voltage level translation between variety of devices. As shown in figure output can be measured with respect to voltage VCCB. This can be higher compared to high input voltage logic level also known as up-translation or lower compared to high input voltage logic level also known as down-translation. However power consumption of circuit designed is determined depending on the configuration of circuit, which is usually higher than other methods. Figure below shows the circuit with open drain outputs.[1]

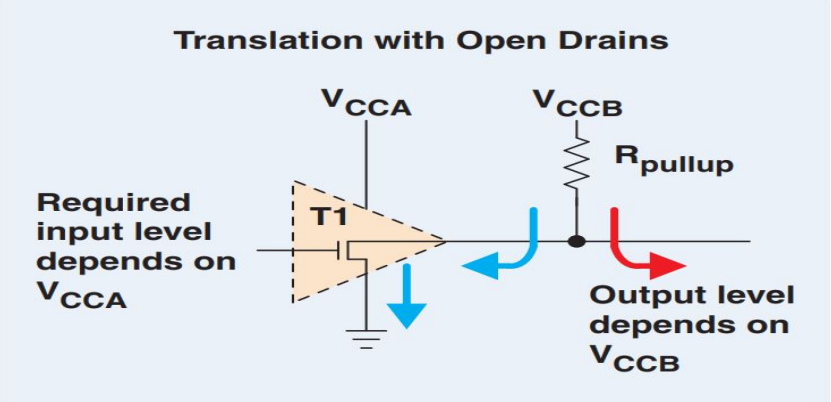

Figure 3.2: Open-Drain Outputs
[1]

There is also a third option of using unidirectional translators. These devices can do the translation only in one direction. For example devices with over voltage tolerant inputs. These can work with input voltage levels that are higher than the supply voltage of interfaced device. Voltage translation from high to low is suitable for these devices. Power consumed by these devices is comparatively less and they need a single supply voltage only. Device families with offer over these kind of devices are AHC, AUC, AVC, LV-A, and LVC. When these devices are used for logic translation slow edges coming on duty cycle on input voltages will have an affect on the duty cycle of output voltages. Also switching levels of any circuit design is always constrained by VCC. So these devices are not used where duty cycle is critical.[1]

Fourth option is to use auto bidirectional voltage level translator devices. These devices help in improving connections between newer generation components and its peripherals. With auto directional level shifter there is no need for a direction control pin which are usually found in other types of level shifter. They offer following things:

- Lesser power consumption

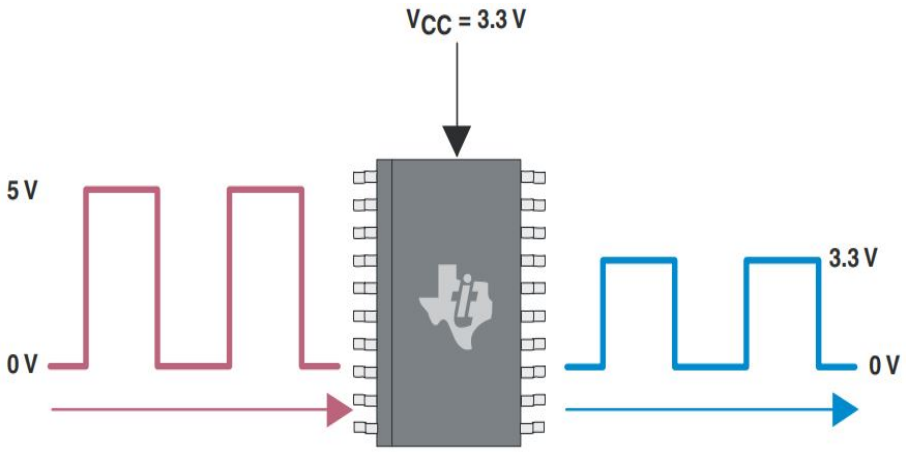

Figure 3.3: Down logic translation With Over-Voltage-Tolerant Inputs [1]

- Isolation of VCC
- Power down mode of operation which is done partially

Field Effect Transistor(FET) Switches are also used as logic translator devices. The advantage that they offer is faster propagation of signal. Some FET switches can only do down translation, while others could be configured to do bidirectional translation. Device families like CBT, CBTD and TVC families can offer level-translation solutions like these. [1]

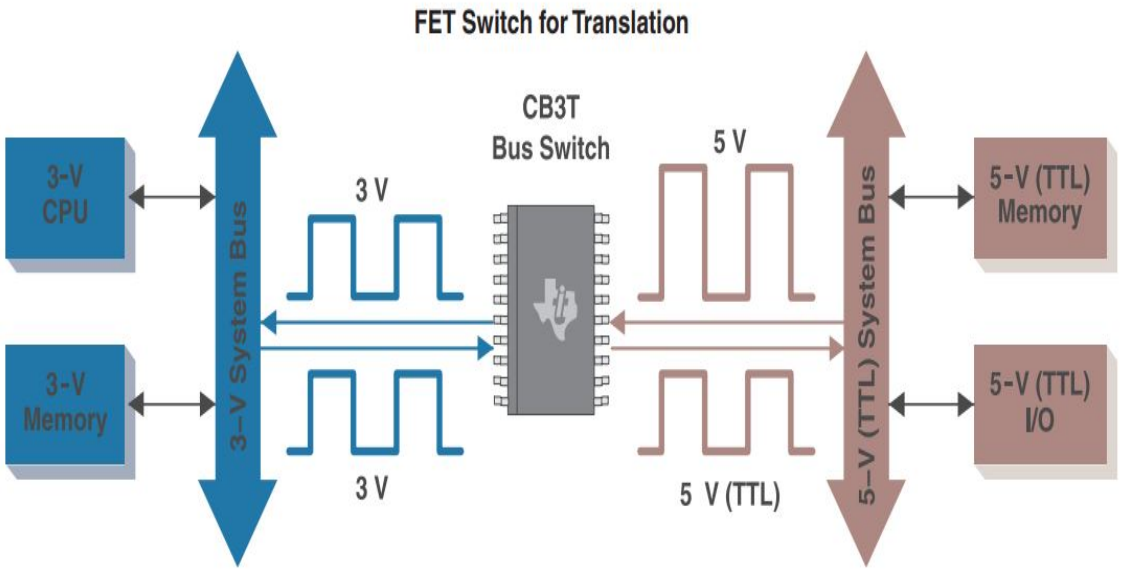

Figure 3.4: Level Translation With FET Switches
[1]

Chapter 4

Basic Characteristics of Translators

Following are some of the important characteristics of Translators.

4.1 Electrical Characteristics

Following are common terminologies used for recognizing voltage values. For a High logic gate driving a second gate, we define the following referring to Figure 5.1:

- Voh (min), output high voltage, the minimum voltage that a driver will produce as logic 1.
- Vih (min), input high voltage, the minimum voltage that a driver will recognize as logic 1.
- Ioh, output high current, under logic 1 of the driver, the current that flows out from output.
- Iih, input high current, under logic 1 of the driver, the current that flows in from input.

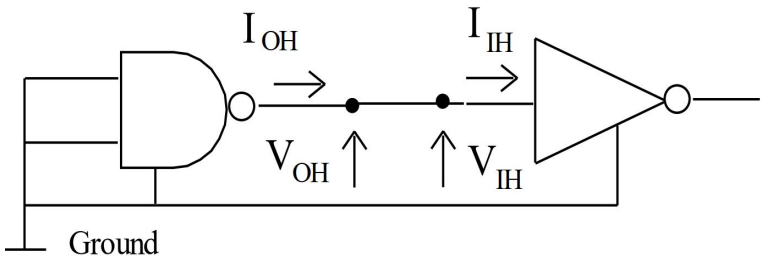

Figure 4.1: High logic gate driving a second gate

For a Low logic gate driving a second gate, we define the following referring to Figure 5.2:

- Vol (max), output low voltage, the maximum voltage that a driver will produce as logic 0.
- Vil (max), input low voltage, the maximum voltage that a driver will recognize as logic 0.
- Iol , output low current, under logic 0 of the driver, the current that flows out from output.
- Iil , input low current, under logic 0 of the driver, the current that flows in from input.

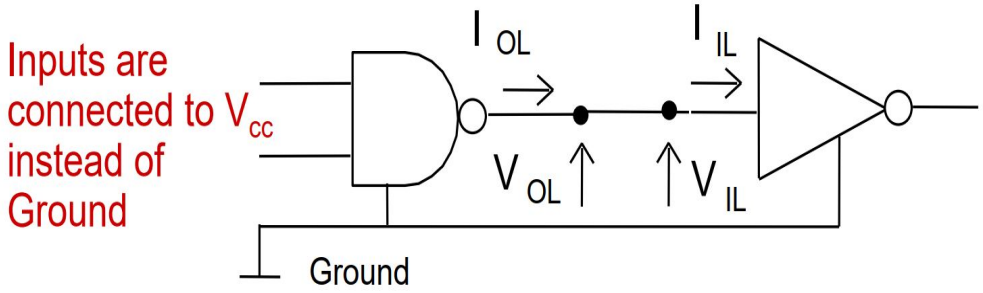

Figure 4.2: Low logic gate driving a second gate

4.2 Logic Level and Voltage Range

There are a certain range of voltages which are acceptable as logic level 1 and logic level 0 as shown in Figure 5.3. For the outputs to be predictable and the circuit to operate normally, the voltage levels should be between this range only. If not than output will be unpredictable in the intermediate range. It is useful to know voltage levels of the logic family in use so that the system can be validated with correct inputs. Respective voltage ranges of the logic families must be known to choose appropriate voltage translators.

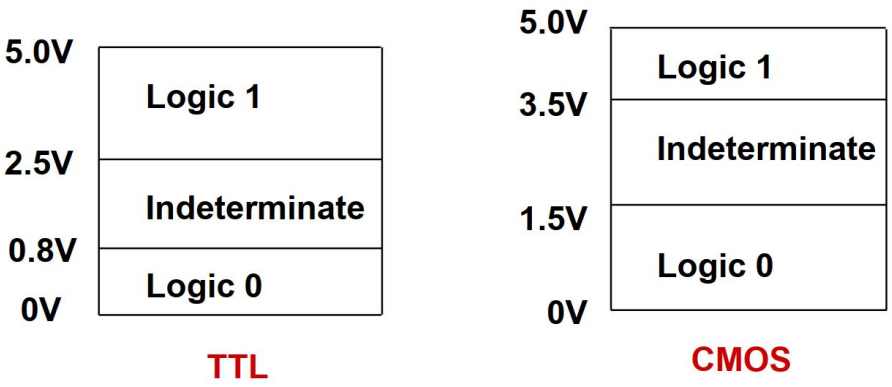

Figure 4.3: Logic Level and Voltage Range

4.3 Propagation Delay Time

Propagation delay is the time it takes for a state of a gate to change from high to low or from low to high. It is also the time it takes for a signal to propagate from input pin of a device to when signal arrives as output at the output pin of the device. It should be as small as possible ideally.As shown in Figure 5.4 Tphl-time taken by output to go from high logic to low logic and Tplh-time taken by output to go from low logic to high logic. In the figure a simple inverter is taken as an example.

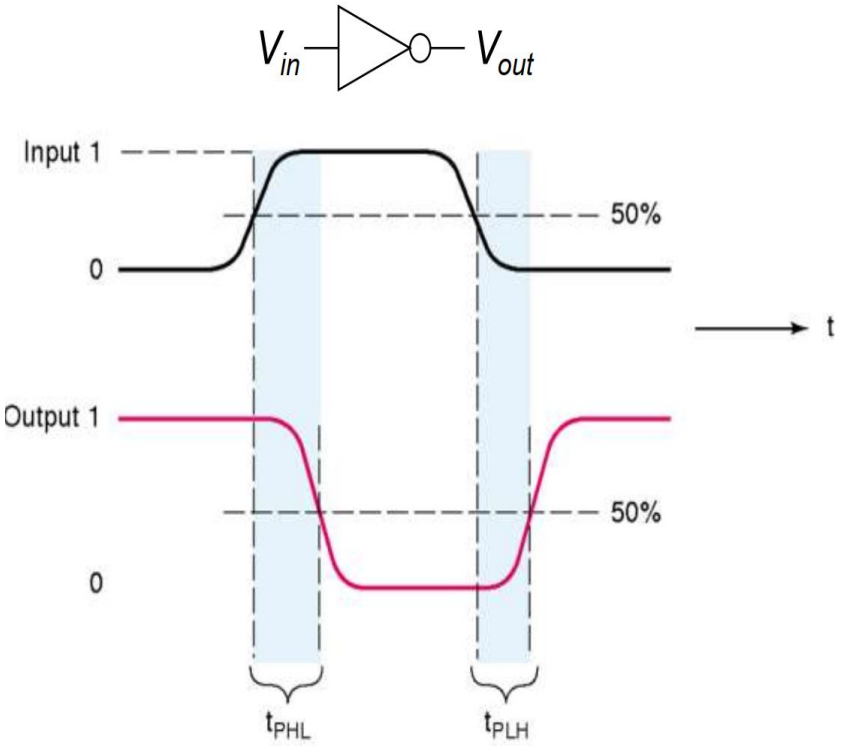

Figure 4.4: Propagation Delay

4.4 Noise Margin

The measure of a circuit to resist noise without changing output voltage is termed as noise margin. If noise is higher in the circuit than the output values can go to invalid regions or can change the logic 1 to logic 0 and vice versa. Noise margin of a device should always be as high as possible. As shown in Figure 5.5 when a signal has to translate from logic low to logic high, there is an undefined region(in yellow) where signal can be called neither high nor low. This is considered noise margin.

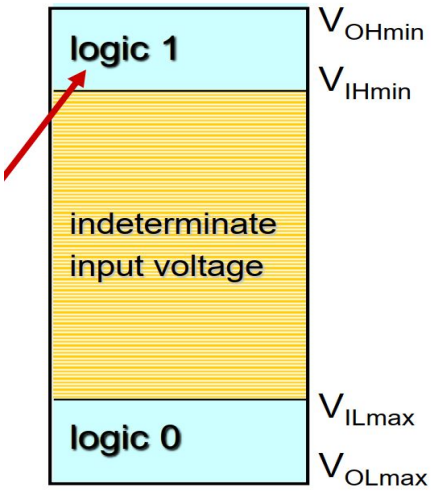

Figure 4.5: Noise Margin

4.5 Current Sourcing

There is a certain amount of current required to be handled by a translator so that efficient data transfer can be possible. As shown in Figure 5.6 when output of a driving gate is at high level, it drives Iih current to the load gate which in turn acts as a resistance to the ground. Here gate 1 acts as source of current for gate 2.

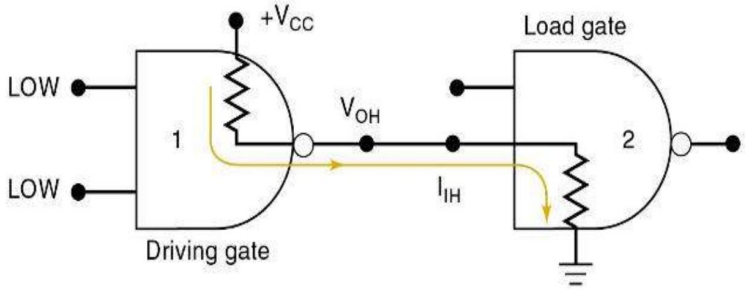

Figure 4.6: Current Sourcing

4.6 Current Sinking

Same as current sourcing, a certain amount of current sinking is also required by translators. As shown in figure when output of gate 1 is low, and input of gate 2 is tied to VCC, a current Iil will flow from input of gate 2 to output of gate 1 to ground. Here gate 1 must be able to sink current from gate 2. Both current Sourcing and Sinking play a major role in making communication successful between two devices.

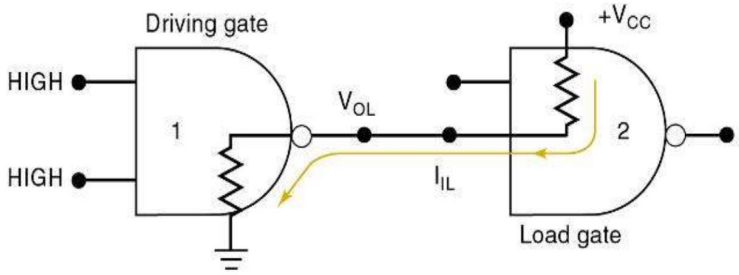

Figure 4.7: Current Sinking

4.7 IC Packages and Real Estate on Circuit Board

These features are often overlooked when selecting electronic components but are very important. Several packages are offered by manufacturers which differ majorly in terms like electrical, mechanical, thermal, economic characteristics.

The pins that come out of the package of chip have different electrical properties than the routing done on printed circuit board. Differing properties like resistance, capacitance and inductance come into picture. So both structure and materials used should be taken into consideration.

Mechanical and thermal aspects of the package are responsible for keeping it

safe from heat and mechanical stress occurring in the chip. Packages must resist humidity from entering, should be airtight if necessary and should also prevent the chip from breakages. Special care is taken when designing dimensions of chip so that better thermal dissipation can be done.

There are always cost constraints while a chip is developed. Using better materials will make the chip mode durable and more resilient to external factors but also will increase its cost. So appropriate balance is found between cost and quality.

Chapter 5

Results

5.1 Results

SPI Interface on SoC dye is powered by a 1.0V rail and the SPI NOR devices available are in 1.8V or 3.3V powers supply. So for communication between these two sets of devices, a bidirectional level shifter is necessary. A level shifter is a circuit used to translate signal from one logic level to another and thus allowing compatibility between different ICs with different voltage requirements. A bidirectional level shifter facilitates communication in both direction, for example: from SoC to SPI device or from SPI to SoC.[6]

Now to propagation delay of bidirectional level shifter is very large when compared to the requirement. This slows down speed of the whole operation. SPI interface on SoC is capable of running at 50MHz. But with the use of bidirectional level shifter, SPI NOR device would have to run at much lower speed. When the speed is reduced, it has a negative impact on the boot time of the system.[6]

Time required to read 16KB of flash descriptor is shown in following figure. **Note**: Only 16KB of flash descriptor is required to be read.

Frequency	Code Size	Single Mode	Quad Mode
50MHz	16KB	2.62ms	0.66ms
40MHz	16KB	3.28ms	0.82ms
33MHz	16KB	3.97ms	0.99ms
20MHz	16KB	6.55ms	1.64ms

Table 5.1: Time Required to read Flash

Following are all the explored solutions:[7]

a. **Use Bidirectional level shifter at 50MHz**

(1) TI TXB0304 - 4-bit device - need two devices; Large propagation delay (20ns)

(2) TI TXB0108 - 8-bit device; Level shifting from 1.2V to 3.3V (no 1.0V support); Large propagation delay

(3) Pericom PI4UL5V106 - 8-bit device; Sink current issue to 3.3V level shifting;

(4) Pericom PI4ULS3V504 - 4-bit device; 10ns propagation delay

(5) TI LSF0102/0108 - 8-bit device; 2.2ns propagation delay

Comments: With Bi-directional level shifter, if passive, it is difficult to get a balanced pull-up resistor value which achieves 3.3V levels for Flash when driven from CPU and stay within VIL limits during logic LOW if active; the TPD are way high to allow 50 MHz operation.

b. **Use Uni-directional level shifter at 50MHz**

(1) NXP 74AVCH4T245 - Single bit mode only which will impact the boot time

i. Time required to read flash descriptor at 50Mhz - 2.6ms

ii. Time required to read flash descriptor at 20Mhz - 6.55ms

Comments: This defeats the very purpose of Quad SPI feature in SOC because the time it takes is too large.

c. **Run Bidirectional Passive level shifter at lower speed**

(1) NXP 74AVCH4T245 - Single bit mode only which will impact the boot time

i. Boot time will be impacted which is undesirable.

Comments: Not able to achieve even 25MHz with Passive level shifter.

d. **Use Bidirectional level shifter with SPI LOOPBACK CLK**

(1) Need an additional pin on the package.

Comments: Places constraint on Routing of the Clocks + Return Loopback Clock.

e. **Use 1.8V SPI NOR devices with Pericom PI4UL5V106**

(1) No current sink issue.

(2) Need a LDO on the board just for 1.8V.

Comments: Adding an LDO will eat up real-estate and will also increase BOM Cost.

Chapter 6

Conclusion

This report showcases a study on level translators and the design requirements that should be met while selecting them. The integration of voltage level translators into the circuit design enables efficient communication between devices operating at different logic levels. Scaling down components for lower power and higher performance applications is now possible. Depending on circuit design certain types of level translator are better than others as they have their own properties.

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