Customized Routing Optimization Flow To Fix Timing Violations in Ultra Deep Sub Micron Technology

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Omkar Deshkar

17MECV05

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

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Under the guidance of

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Certificate

This is to certify that,

1. The thesis comprises my original work towards the degree of Master of Technology in Electronics and Communication Engineering at Nirma University and Intel India Pvt. Ltd. and has not been submitted elsewhere for a degree.

2. Due acknowledgment has been made in the text to all other material used.

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This is to certify that the Major Project entitled **"Customized Routing Optimization Flow To Fix Timing Violations in Ultra Deep Sub Micron Technology"**submitted by **Omkar Deshkar (17MECV05)**, towards the partial fulfillment of the requirements for the degree of Masters of Technology in VLSI Design Engineering, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge, havent been submitted to any other university or institution for award of any degree or diploma.

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Abstract

In ultra-deep submicron technology, Routing has become challenging due to the ever-increasing number of metal layers, distinct layer thicknesses, new design rules and design complexity. Due to increase in congestion with lower technology nodes designer has to predict during floor plan weather routing is possible with meeting timing constraints. It is not enough to route only but need to route with DRC clean and without degrading post layout timings. Due to area reduction with lower node technology, routing congestion increases on chip and in that scenario need to route the different topologies for the single net. Best topology need to be routed and for that topologies timings are calculated for that path and if it is not meeting there are some methodologies in Layout which will fix the timing violations for the routed net.

This thesis will discuss about routing a net with different routing topologies and from all those we can select the best topology which meets our timing violations and DRC requirements.Flow is developed which will select the best topology from available topologies on the basis of different criteria and which will be routed automatically with given metal layers.Once it is routed, It will also fix the timing violations on the net with different layout solutions.

Keywords : Routing,Floorplan,Algorithm,Timing violations,DFM

Abbreviations

DRC	Design Rule Check
LVS	Layout Vs Schematics
Fub	Functional Unit Block
VIA	Vertical Interconnect Access
SLO	Section Layout Owners
IC	Integrated Circuits
CTS	Clock Tree Synthesis
DFM	Design For Manufacturability
ECO	Engineering Change Order
PnR	Placement and Routing
OCV	On Chip Variation
IP	Intellectual Property
GDS	Graphic Data System
DEF	Design Exchange Format
LEF	Library Exchange Format

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Chapter 1

Introduction

With todays newer fabrication technology improvements following Moores law, integrated circuits (ICs) are continually shrinking with creating many new challenges for the place and route flow. We face a lot of problems in converging during the place and route flows. Each flow stage impacts downstream steps in the flow,making later stages like routing and post-route more challenging, it is hard to successfully route a design during the routing stage, and it has become even harder to re-route after disturbing it during the post-route stage. Thats why we have to control and minimize the optimization disturbance.

With increases in on-chip packing densities, routing congestion has become a major problem in chip design. Due to area decrease also routing congestion increase with space violation. The problem is especially acute as interconnects are also the important performance parameter in integrated circuits. The solution lies in judicious resource management. This involves intelligent allocation of the available interconnect resources, up-front planning of the wire routes for even wire distributions, and transformations that make the physical synthesis flow congestion-aware.

1.1 Company Profile

Intel Corporation works in the design, manufacture, and sale of computer products and technologies. Intel is the world's one of the largest and most valued semiconductor chip makers based on revenue.Inventor of x86 series of microprocessor. Intel supplies processors for computer system manufacturers such as Apple,Lenovo etc.Intel also manufactures motherboard chip sets, network controllers , system on chips and integrated circuits, flash memory, graphics chips, embedded processors and other devices related to communications and computing. Intel's innovation in cloud computing, data center, Internet of Things, and PC solutions is powering the smart and connected digital world we live in.

1.2 Group Profile

Core IP Group (Big Core) is responsible for designing processor cores for Intel's client and server products. Big Core is the group which is designing cores from Intel's Pentium generation processors.

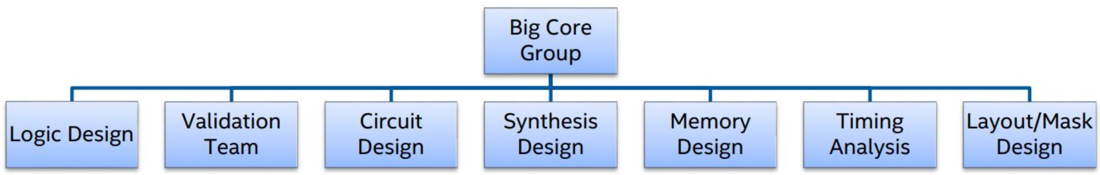

Figure 1.1: Big Core Teams

1.3 Backend Design Flow

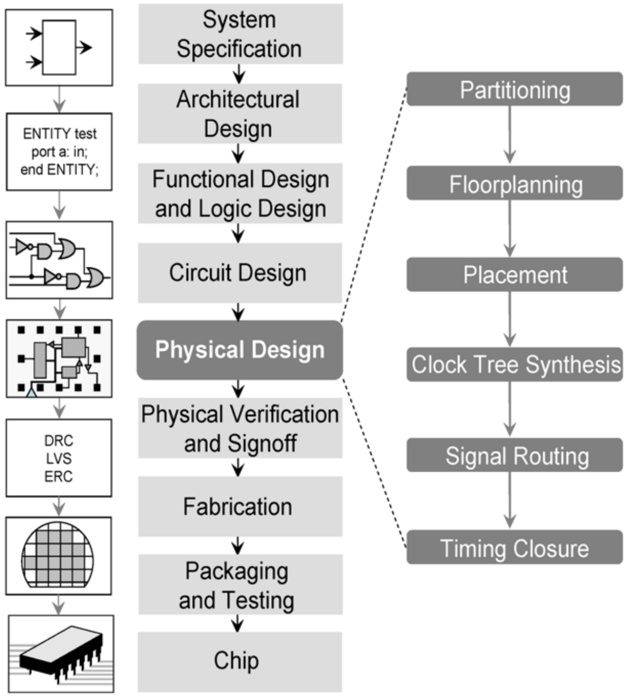

Figure 1.2: Back-end Design Flow

1.3.1 Partitioning

Partitioning of a complex system into smaller subsystems.Each subsystem can be designed independently speeding up the design process.Partition scheme has to minimize the interconnections among the subsystems. Partitioning is carried out hierarchically until each subsystem is of manageable size.[1]

1.3.2 Floorplan

A floor planning is the process of placing blocks/macros in the chip/core area as per the connection with another blocks in the core. While all this thing is being executing floor plan of the design is taking place in parallel from the past experience or the knowing behavior of its all Functional unit block and their connectivity.Floor planning is done by the layout people.Floor plan decides the area of the core.[2]

1.3.3 Placement

Placement is the process of placing standard cells in the rows created at floor-planning stage. The goal is to minimize the total area and interconnects cost. The quality of routing is highly determined by the placement.Placement is the stage where all the functional unit blocks are placed inside the floor plan of the core.

1.3.4 Clock Tree Synthesis

Clock Tree Synthesis is a process which makes sure that the clock gets distributed evenly to all sequential elements in a design to minimize the skew and latency. The clock tree constraints will be Latency, Skew, Maximum transition, Maximum capacitance, Maximum fan-out, list of buffers and inverters etc. The clock tree synthesis contains clock tree building and clock tree balancing. Clock tree can be build by clock tree inverters so as to maintain the exact transition (duty cycle) and clock tree balancing is done by clock tree buffers (CTB) to meet the skew and latency requirements.

1.3.5 Routing

Routing is an important step in the design of integrated circuits (ICs). It generates wiring to interconnect pins of the same signal, while obeying the manufacturing design rules.After reading the netlist which will show the pin to pin connectivity to route metal between those pins.Two approaches are used i.e. Global and Detailed routing. Global routing first partitions the routing region into tiles and decides tile-to-tile paths for all nets while attempting to optimize some given objective function (e.g., total wire length and circuit timing). Then, guided by the paths obtained in global routing, detailed routing assigns actual tracks and vias for nets.[3]

1.3.6 Physical Verification

In the layout,It need to check all the Design Rule Check which are specified by the foundry for the fabrication process.So cleaning of different DRCs are needed after the routing it is called the physical verification. below are the some examples of DRC

- Shorts
- spacing violations

1.4 Introduction to Section Layout

Design of any System on Chip is hierarchical design. The Hierarchy is as shown in below figure.From Figure 1.2 we can see that it consist of Transistor as basic element, gates are made up of transistors. Standard cell are made up of gates. Functional unit block are made up of standard cell.This Functional Unit block had some specific logic built inside it with the help of standard cell.Functional unit blocks are integrated inside Section. Section is made up of lot more number of Functional unit blocks. Combining all this section Full chip is created.

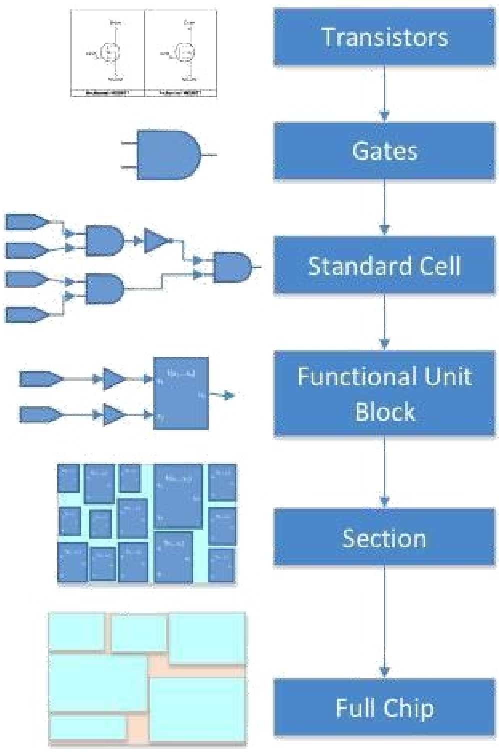

Figure 1.3: Hierarchical Design of SOC

1.4.1 Fub Integration

Functional unit block integration is the process of integrating functional unit block inside section.functional unit blocks have routed in lower metal layers while section has routed in the higher metal layers.Functional unit blocks had information of pin terminal and its lower metal layer. This will be transferred to section and from the netlist information nets will be connected. Than DRC (Design Rule Check) process will started and cleaning will be done manually.

Figure 1.4: Fub Integration FLow

1.4.2 Clock Integration

Clock had its own structure and it will be transferred to all the part of section from global driver.Global drivers are used to boost the clock signal which will maintain the slop for the clock signal. Functional unit block has clock port this needs to be integrated separately with considering max delay allowed to reach the clock to their terminal.

1.4.3 Timing Convergence

Timing convergence at section level is also one of the important task in Layout.Sometimes it might possible for the functional unit blocks some blocks have the paths which are not meeting timings in that scenario it is necessary to fix those timing paths from the section level.There are different ways to improve the timings in layout for the given net.

Chapter 2

Problem Statement

2.1 Motivation

To integrate many functional unit blocks inside the section level and cleaning all the DRCs is very critical and time consuming task.It is very difficult to check and fix the timing violations for each and every net with DRC clean routing.While doing the Routing on the section level there are many different topologies available for the routing a single net.But It need to be select best topology in terms of timing closure considering open length,shorts and RC delay on that net.

Also when there is congestion in any specific metal layer in specific region,we need to be upgrade or downgrade metal layers in that region and which needs to be DRC clean.Current mode of work is to remove routing from congested area manually and doing whole routing again with meeting timing constraints.

2.2 Objective

Flow to be developed to optimize the routing choosing best topology from different available topologies and to fix timing violations with DRC free routing with achieving quick integration time to reduce manual intervention. Developed utility will fix up all the routing with timing violation at section level and target is to reduce 60% of manual efforts in DRC free routing on every metal layer in a short time.

Chapter 3

Literature Survey

3.1 Introduction to Routing

Routing is one of the most important step in the design of integrated circuits after the floor plan and placement.Routing is nothing but connecting wires from pin to pin as per the netlist.While doing routing need to check manufacturing design rule checks.As we are moving towards Nano meter technology age,foundries are fabricating billions of transistors on a single chip and it might possible it will grow drastically in upcoming future.This increasing complexity will be the big challenge for back-end design.[4]

VLSI has very grand domain of research and in which routing has received much attention in the literature. As specially in ultra deep sub micron technology routing is one of the most complex challenges in physical design.To make if feasible , routing is done with two approach,

- Global routing
- Detailed routing

In Global routing, partitioning of the routing region is done into the tiles and tile to tile paths are routed.It will try to optimize some objectives of routing (i.e. total wire length and circuit timing).After global routing paths detailed routing is done.Detailed routing will assign actual metal layer routing and via for the net.

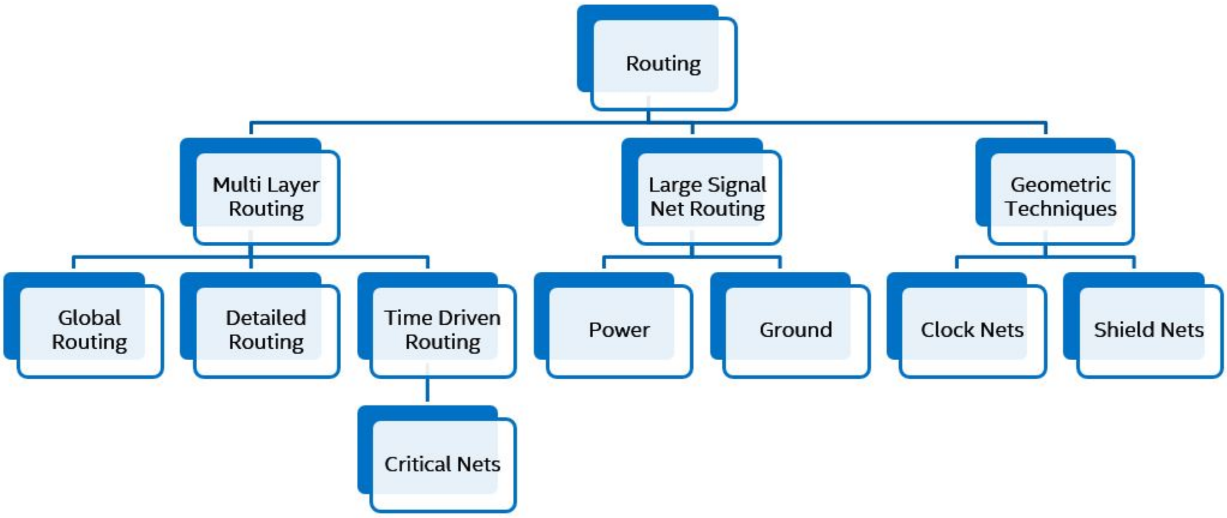

Figure 3.1: Different Routing structures

3.2 Global Routing

Global routing is done at the start of the back end design routing part.Input to the global router will be floor plan and locations of blocks which might me fixed or flexible which contains logical cells inside the blocks.Global routing will provide instructions to detailed router for the routing of each and every net.

The input to the global router is a floor plan that includes the locations of all the fixed and flexible blocks; the placement information for flexible blocks; and the locations of all the logic cells. The goal of global routing is to provide complete instructions to the detailed router on where to route every net. Global routing emphasizes on:

- Minimizing the interconnect length.
- Maximizing the probability that the detailed router will complete the routing.
- Minimizing the path delay which are critical in timing.

3.2.1 Sequential Routing

In this approach for global routing picks up each net and calculates the shortest length path using tree's algorithms also known as Sequential routing.In this algorithm it might possible that some gutters will get more congested because there might be more number of nets routed there. There are two ways to solve this problem,

- Order independent

- Order dependent

As the global router routes each net independent of congestion in that gutter.Selection of net is independent of routing order but gutter alignment will be same.Once all the nets are assigned to any specific channel global router will return to those channels which are very much congested and try to route some of the nets in the less congested channels of that metal layer.

Alternatively, in the another approach a global router can consider the number of interconnects already routed in various channels as it starts routing. In this scenario the global routing is done order dependent, Still the routing is sequential, but now the order of routing the nets will affect the results.There might be little bit improvement in the solutions of order dependent and order independent methods.

There are some popular net-ordering approaches :

- Order the nets in the ascending order according to the number of pins within their bounding boxes.
- Order the nets in the ascending or descending order of their lengths if routability is the most critical issue.
- Nets are routed on the basis of their timing criticality.

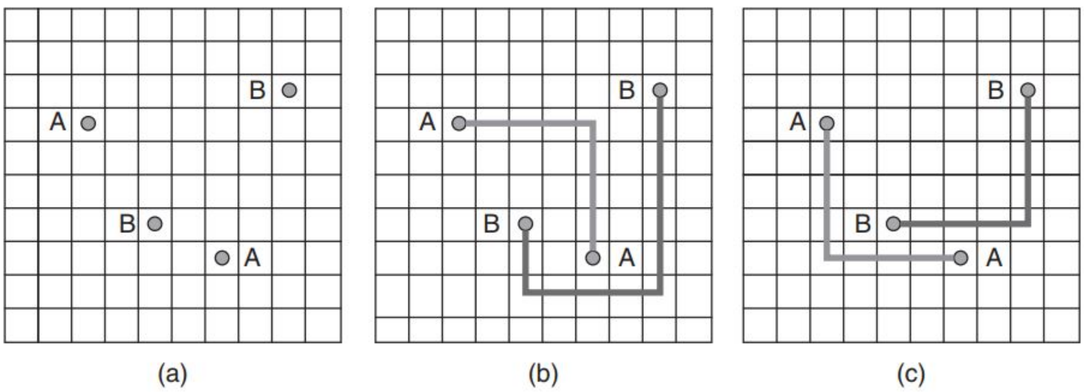

Figure 3.2: Routing based on net orderings: (a) A one-layer routing with two two-pin nets A and B. (b) One solution routed by the net ordering of A followed by B. (c) Another solution routed by the net ordering of B followed by A.

Figure.3.2(a) shows a one-layer routing case with two two-pins nets 1 and net 2. If one choose net ordering as routing 1 followed by 2, net 2 may be blocked by net 1 and requires long wire length for complete routing (Figure.3.2(b)). If routing of net 2 is done first followed by net 1, better result with shorter length can be obtained (Figure.3.2(c)).

3.2.2 Concurrent Routing

One of the major disadvantage of sequential routing approach is that it will try to route with net ordering issue.It is very difficult to route the nets which are processed latter in net ordering scheme as that routing will get more blockages for further routing.If the sequential routing fails to find the proper solution, it might be because of no any other solution is existing there or might be poor net selection bu the router.Routing from the sequential router might be optimal or not also.

One popular concurrent solution is to formulate global routing as a 0-1 integer linear programming (0-1 ILP) algorithm. There are new or improved routers developed for global routing NTHU-Route, FGR , MaizeRouter, BoxRouter, Archer, FastRoute, and NTUgr.

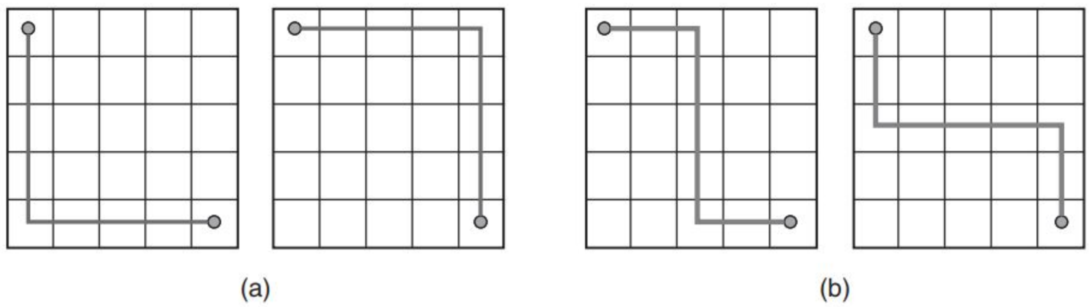

Figure 3.3: types of different Patterns of routing: (a) L-shaped routes (b) Z-shaped routes

3.3 Detailed Routing

This type of routing will route the nets determining the exact tracks and vias for the nets.There are two types Detailed routers,

- Channel routing

- Full - chip routing

In previous process technologies there were maximum 2-3 metal layers are used to route the nets and wires are routed without that much congestion. But in the modern age technologies , there are 6 - 10 metal layers for the fabrication and it might increase also as technology advances.Area is also decreasing with modern technology nodes with increase in congestion.Routing region will become more channel less region.In this scenario full chip method routing is needed.

3.3.1 Channel Routing

Channel routing is a case of the routing problem in which wires are connected within the routing gutters. To apply channel routing, a routing region is usually decomposed into routing gutters. Note that there are often various ways to differentiate a routing region. For example Figure.3.4 shows two ways of decomposition for the T-shaped routing region. The routing region is decomposed into one horizontal channel (channel 1) and one vertical channel (channel 2), The routing region is decomposed into two horizontal channels (channels 1 and 2) and one vertical channel (channel 3).

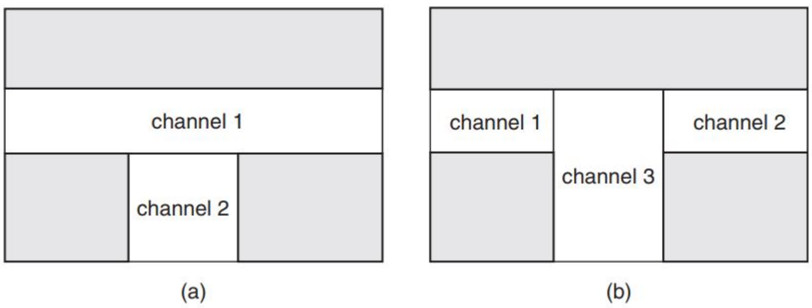

Figure 3.4: Two ways of routing region differentiate : (a) The routing region is with two channels. (b) The routing region is with three channels.

3.3.2 SwitchBox Routing

In this type of routing horizontal and vertical channels are intersecting with each other.Because of fixed dimension of switch box routing , it shows less flexibility and very complex to route.It is very difficult to find routes inside the switch box. Switchbox is the rectangle area where we can route in circuit blocks which are connected to each other.There are two types of routing regions in switch box routing.

- Track - Horizontal wire
- Column - Vertical wire

Width of the switch box is decided by the number of tracks in particular region.Pins are routed all around the switch box which are connected to circuit blocks.

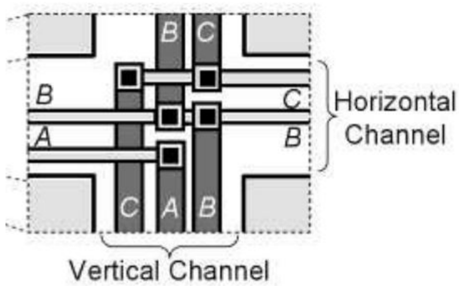

Figure 3.5: Switchbox routing for horizontal and vertical channels

3.4 Router Models

Modeling of the routers are based on the global routers and the detailed router routing graphs.Graph search techniques is used to model routing.[5] There are two major type of graph search technique,

- Maze routing
- Line - search technique

Above both the algorithms can be applied to global routing and detailed routing.So it is called general purpose routing algorithm also.

3.4.1 Maze Routing

Maze routing was invented by Lee in 1961 so it is called Lee's algorithm also.Main purpose of the maze routing is finding the path between two pins.Breadth first search techniques is used in maze routing technique.There are two phases in maze routing technique,

- filling
- retracing

Filling is the process like wave propagation.It start with the source node S and on the grid adjacent grid cells are labeled one by one till the target node it reaches.So the wave-front will travel from source to target in grid.Figure.3.6.a and 3.6.b illustrates the wave propagation when the labels of wave fronts reach 2 and 3, respectively. Once wave is reached to the target it starts retracing till the source again with the shortest path.Best property of the Lee's algorithm is it will surely routes with shortest path and the path which is exist with no obstacles.Disadvantage of the Lee's algorithm is that it is slow and very memory consuming due to retracing target to node.

Because of the disadvantage of Lee's maze-routing algorithm and its long time and space complexity, many methods have been invented to reduce routing running time and memory consumption. These popular optimization methods can be classified into three major categories:

- coding scheme

- search algorithm
- search space

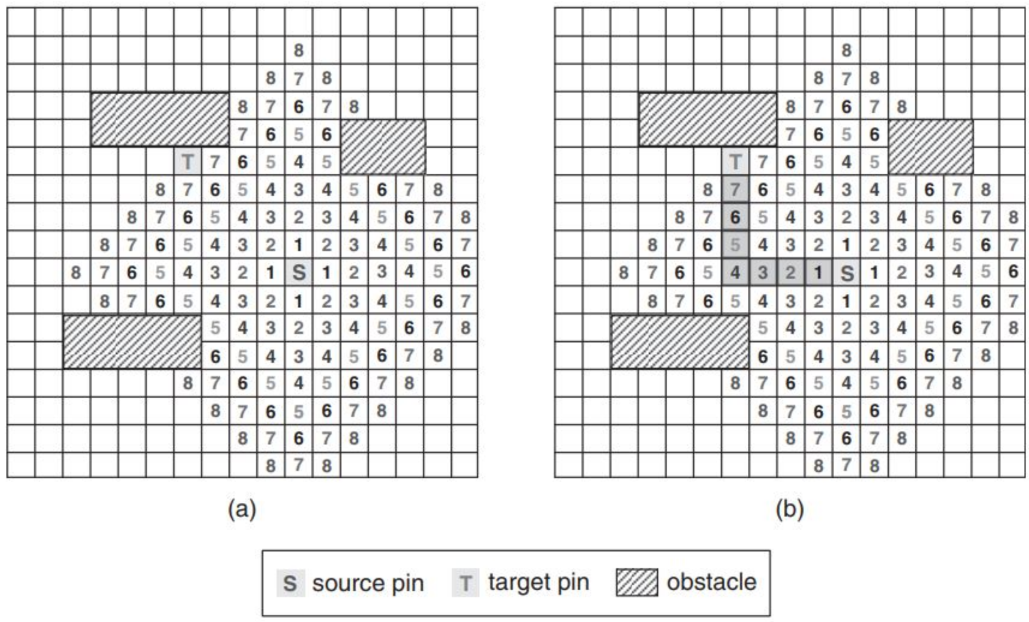

Figure 3.6: Maze routing algorithm: (a) Propagation phase (b) Retracing phase.

3.4.2 Line Search Routing

The major disadvantage of the maze-routing algorithm are the high memory consumption and long running time. The line-search algorithm overcomes these disadvantages with the use of line segments which represent the routing space and paths at the cost of solution.

The first Line-Search algorithm was invented by Mikami and Tabuchi which is also known as Line probe routing. Line search algorithm also starts with depth first search manner.Line search algorithm first search for source S and target T base points and then generates the four segments (two vertical and two horizontal) which are passing through the source and target.This segments are extended till the boundary of the design grid.for each line segment in each grid point sets the new base points and from which new base point new perpendicular line segment is generated.This process is repeated till the segments generated from the source and segment generated from the target intersected.And connection is found from the source to target by retracing intersection points from source and target both.

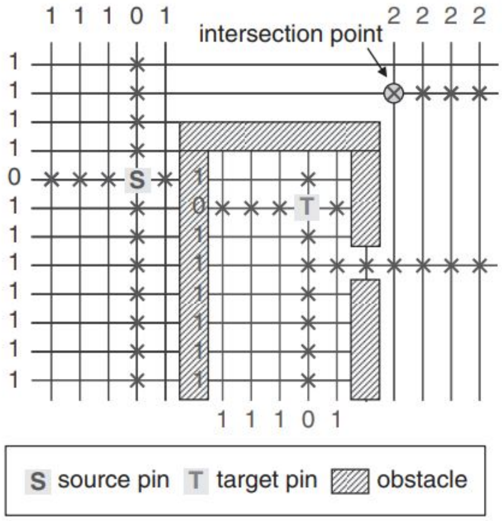

Figure 3.7: line-search algorithm.

3.5 Routing Constraints

Routing constraints are the obstacles which are affecting to route in layout.The routing constraints can be classified into two categories:

- Design rule checks for the technology
- Performance constraints (Timing and power constraints)

For the specific fabrication technology design rules are decided and for the chip manufacturing it is important to satisfy all the design rule checks.Design rules are directly affecting manufacturing yield of the chip.There are different fabrication process which decides design rules which need to be taken care in layout design.in the 45-nm technology, the physical limitations of an optical lithography system would impose a constraint on a wire such that its width cannot be smaller than 45 nm.

A set of design rules, It defines the minimum widths of wires and vias, the minimum wire-to-wire spacing, and the minimum via-to-via spacing of a layer. The distance

between two wires or routing tracks of the grid-based model is often called wire pitch. Other design rules of the manufacturing process, such as resistance and capacitance of each layer, are also included.
The most common DRC rules are :

- Minimum Spacing
- Minimum Width
- Minimum edge length
- Via cut to cut
- Via to Via
- Via coverage enclosure
- Via overlap
- Shorts

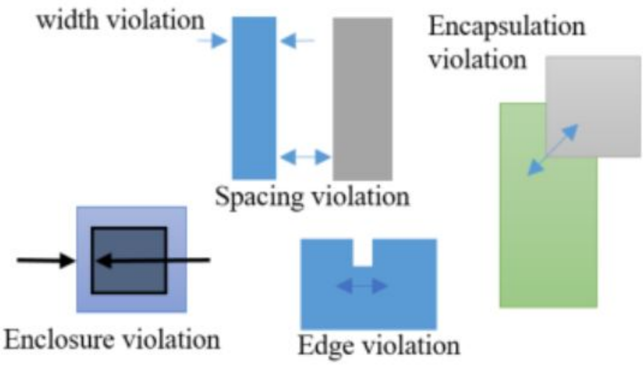

Figure 3.8: Different Design Rule Violations

The objective of the performance constraint is to make the layout routing meet the performance (timing and power) specifications provided by chip designers. For example, most important performance parameter is Timing in post layout design.The performance of the chip is decided by the critical timing net comparing with other nets timing budget.To meet the timing constraints for the critical net it is necessary to route the net with proper routing topology with proper metal layer.[6]

For the specific net/path slack must be positive.If calculated slack is negative for the path,It shows timing violations are there for the path.In that scenario need to use different layout solutions to improve timings for the path.

To Meet the timing constraints at section level need to route the net with proper width and spacing with proper metal layer as per the timing requirements.

Power is also one performance constraints in layout design.VCC and VSS are spreaded over the core.IR drop is also reduced using proper width and spacing of power trail routing.

3.6 Routing Congestion

Routing congestion occurs when there are no tracks available in single power gutter to route the net.It means when no resources available in specific region to route.[7]

3.6.1 Routing Metal Layer Stack

Wider wires on higher metal layers enable signals to travel faster and further (and without as many buffers) than for wires on thinner metals and help offset the reduced benefits from scaling, albeit at the cost of fewer available routing tracks.Figure.3.9 shows an example of a possible layer stack available for technologies between the 130nm and the 32nm node. If one considers M as single wide 1x metal, then C, B, E, U and W correspond to 1.3x, 2x, 4x, and 10x, and 16x metal, respectively. The 90nm node was the first to offer two different metal thicknesses: thin wires for the first five metal layers and 2x wires for the top two metal layers.[8]

The top metal layers have fewer wiring resources but superior performance characteristics which are typically utilized for clock and power distribution; however, some cross-chip signal nets also utilize the widest metal layers. We expect some designs in the 32nm node to have between four and six different metal widths, using up to 15 metal layers.

With the lower technology nodes transistor size shrinks.But wire size does not shrink with the same transistor scaling.Because shrink in the size of wire width will increase the resistance of the wire which will automatically gain in RC Delay.AS per the research,wire resistance per unit length gets double with each technology node while capacitance will be same for the each node.If there is 70% of transistor size scaling for any technology node, wire lenth decreases still the RC Delay will be same as resistance will increase.So here situation is like scaling the size of the transistor delay is decreasing and device becoming more faster but with the same proportion of interconnect scaling delay is increasing so the performance benefits of smaller transistor are lost due to increase wire RC delay.

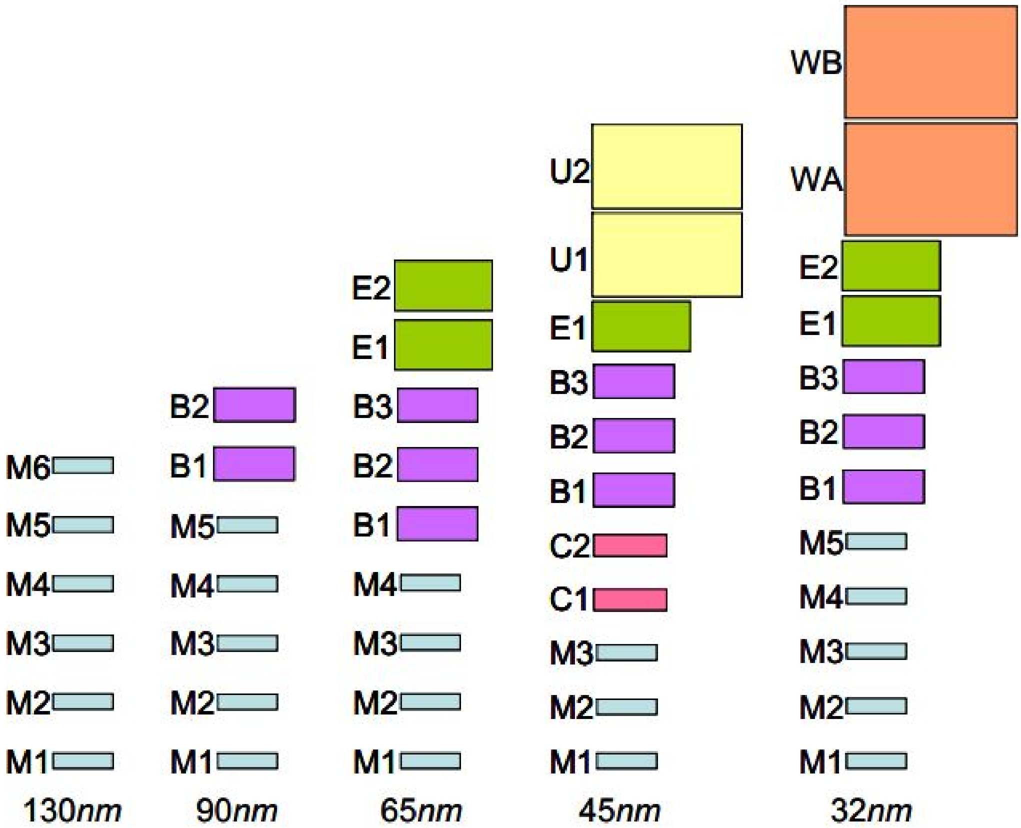

Figure 3.9: Metal layer stacks for the last five technology nodes

Chapter 4

Design for Manufacturability

4.1 Introduction

DFM is the way to improve the competitiveness of a manufacturing by developing the chips which are easier,faster and less expensive to fabricate with maintaining standards of quality,functionality and marketability.Design for manufacturability is the major part for development effort designed to meet and enhance the latest technology advancement and to improve the manufacturing process. Early manufacturing involvement (EMI) is also the same concept to develop the manufacturing process more advance and reliable.[9]

Yield dropout due to,

- Random Defects

  This defect occurs in manufacturing process due to impurities in Silicon or the dust particles present on the wafer during the fabrication process.Because of Random defects metal open or metals shorts occurs in the chip.As the feature size of the chip is decreasing,process technology becoming more complex which causes increase in random defects.

- Systematic Defects

  Systematic defects are occurring due to limitations of process technology in fabrication.Systematic defects are the major contributor in yield loss in ultra deep sub micron technology.Systematic defects are related to process technology due to limitation of lithography process which increased the variation in desired and printed patterns. Another aspects of process related problem is planarity issues make layer density requirements necessary because areas with a low density of a particular layer can cause upper layers to sag, resulting in discontinuous planarity across the chip.

- Parametric Defects Parametric defects are occurring due to improper modeling of interconnects parasitic.It is most critical defects in ultra deep sub micron technology.In this defect chip which is fabricated does not meet the results of the simulation before layout and post layout.It is just because model which is calculating the parasitic extraction of the interconnect having some error.

4.2 DFM rules for device level

Design for Manufacturability is the proactive process which ensures the quality of the chip, reliability, cost effective and time to market.

- Antenna effect guidelines
- Minimum Area of physical layers
- Density Gradient
- Contact Enclosure by Diffusion/Poly silicon
- Metal extension of Via/contact at Line Ends
- Gate Extension on diffusion(End Cap)
- Contact/Via Redundancy
- Metal to Metal spacing
- Via to Via Spacing

4.3 DFM rules for System On Chip Hardware

- Filler cell insertions (consisting of diffusion and poly silicon structure)
- Via optimization
- Wire spreading

- power/ground connected fill
- Litho hotspot
- Dummy Metal fill
- CMP hotspot detection

4.4 Metal fill

Metal fill is one of the solution for the DFM rules.Metal fill is spreaded in the empty region of the layout where no any wires are routed.Every metal layers has metal fill wire in it.Sometimes it may happens that due to dummy fill there is degradation in timing due to coupling capacitance.But it is necessary to add dummy fill to meet DFM rules from the foundry.

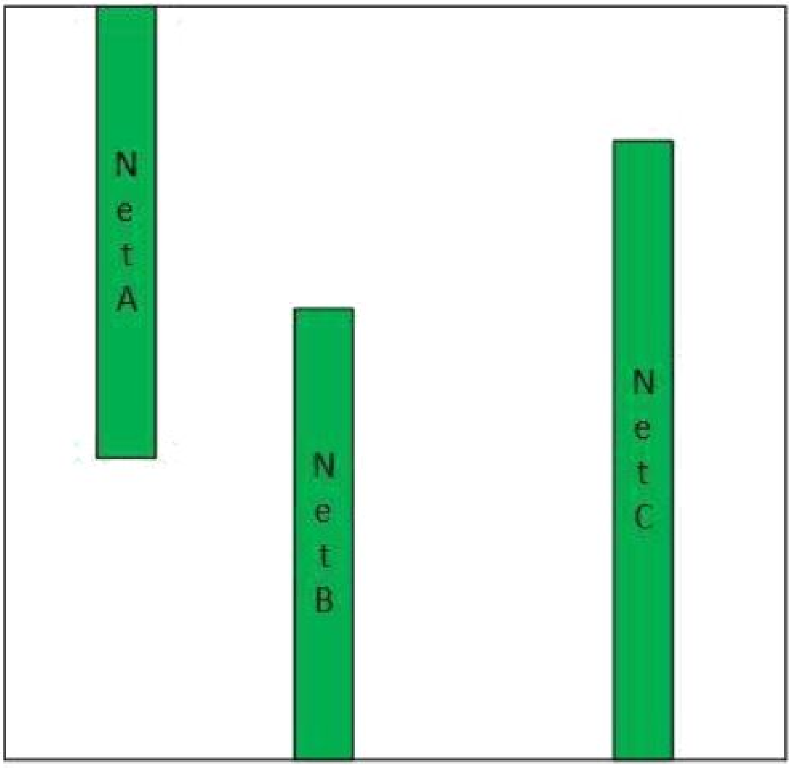

Figure 4.1: Layout without fill

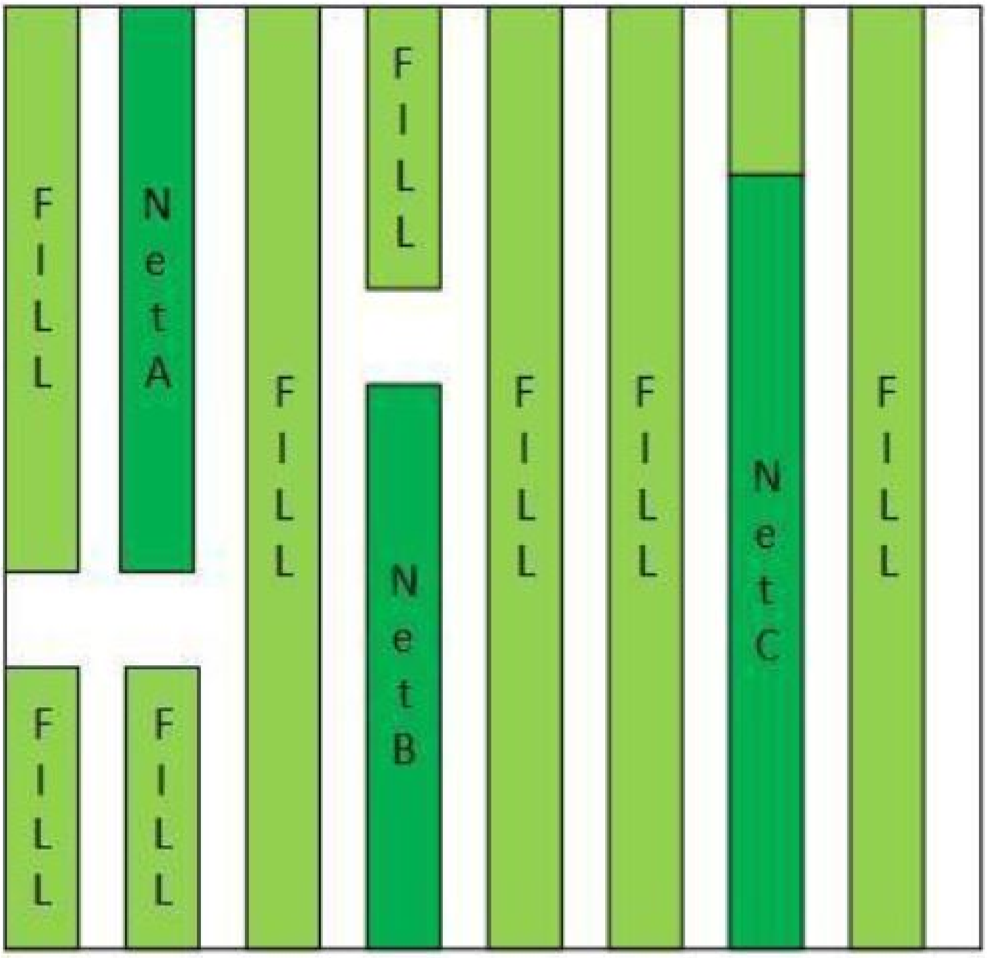

Figure 4.2: Layout with fill

4.5 Problem Statement and Solution

Due to DFM Via density rules,there must be some number of via inserted in the particular area of the layout.For that dummy fill wires are added and vias are inserted to maintain the via density as per the rule.

But sometime it happens that due to very high routing congestion in any specific metal layer for the specific region, it is not possible to meet the via density rule criteria.In that scenario it is needed to upgrade or downgrade the wires from that specific region to get the free region where fill can be added and via can be inserted over the fill.

Downgrade or upgrade of metal layers means wire which is routed in any specific metal layer is upgraded in higher metal layer then which is routed presently or same way it might routed in lower metal layer then it is routed for downgrade.

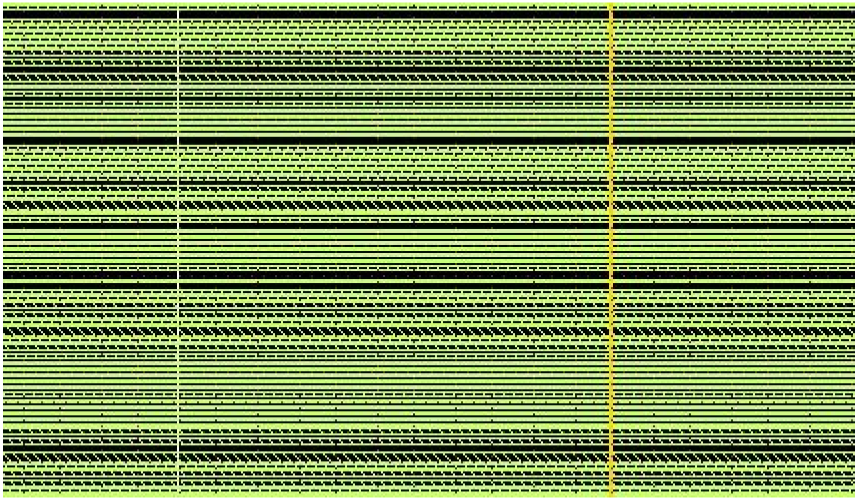

Figure 4.3: Routing Congestion in Metal layer

It is shown in the above Figure.4.3 that in specific metal layer there is lot of congestion where it is not able to insert any single via in that region.In such case to satisfy the via density rule , downgrade or upgrade of metal layer is necessary.

Figure 4.4: After downgrade to lower metal layer

As Shown in the Figure4.4, After downgrading the wire to the lower metal layer we are able to find some region in the that region to add fill wires for the via insertion.

Automation which is developed, It will automatically upgrade or downgrade net to given metal layer finding free tracks in upper or lower metal layer then the metal in which is routed and it is DRC clean also.

Chapter 5

Utility to Route Best Topology

5.1 Introduction

Global router is used for the routing wires with different topologies from pin to pin connection as per the input netlist.This router gives many topologies for the single net to be routed in the layout.But it need to be decided that which topology is best for the routing as per our requirements. Here while routing the net, have given some constraints for the router on which my algorithm will take the decision to select the best topology from the available topologies.[10]

Below are the constraints :

- Metal layer
- RC delay
- Pin to pin length
- Open length
- Short length for the topologies

5.2 Problem Statement

While doing routing on the section level,we need to route some nets manually and for that timing calculations are done for the net.Also we need to route the net in the such a way that less number of shorts occur and it will try to connect till the pin.Some time for routing the clock net we need to find the best topology from global driver to the clock pin the specific section.In that situation also there might possible many topologies for the clock routing and from that we need to find the best topology.

5.3 Flowchart

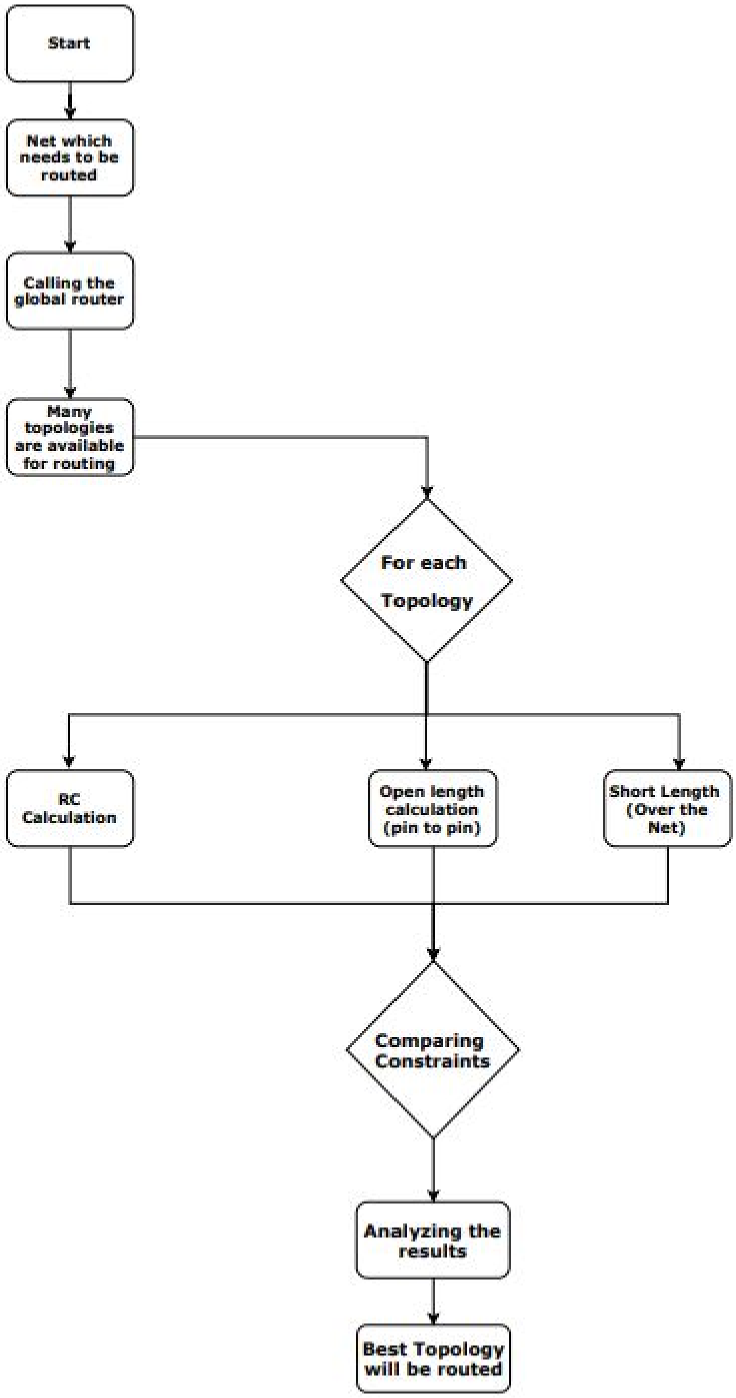

Figure 5.1: Flowchart for the Best topology algorithm

5.4 Algorithm to Route Best Topology

Input:

Set optimization mode and objectives.

input netlist

Get list of the net which need to be routed.

Get arrival and required times from the timeing analysis.

Output:

best topology is selected and routed

Optimization:

foreach net [routing different net topologies]

foreach net [calculating RC delay]

net [calculating Open length]

net [calculating short length]

marking the data,

taking the best and required values from the results

Detail route the change as needed

end

Above algorithm will route the best topology of the net considering the given constraints in Layout.

Chapter 6

Utility to Fix Timing Violation For the Routed Best Topology

6.1 Introduction

Once the best topology is routed for the given net, we need to check timing for that net is meeting or not.If timings are not meeting for the routed topology we need to upgrade-downgrade metal layer or widening the metal layer for the net. Remedies to meet the timings for the topology,

- Widening of the metal layer
- Upgrade the metal layer
- Downgrade the metal layer

Developed automation will try to first wide the metal layer for the given net for the specific metal layer and will check for the timings. If there is high difference in the values of RC delay, in that scenario need to upgrade or downgrade the metal layers to meet the timings.

If RC Delay is very high in that scenario need to route the net in higher metal layers which will decrease the RC delay and improves the timings also.

If RC Delay is very less and signal is reaching very quickly then the required time will be high, In that scenario need to downgrade the metal layers.So that RC delay can be increased.Hold violation can be solved.

6.2 Flowchart

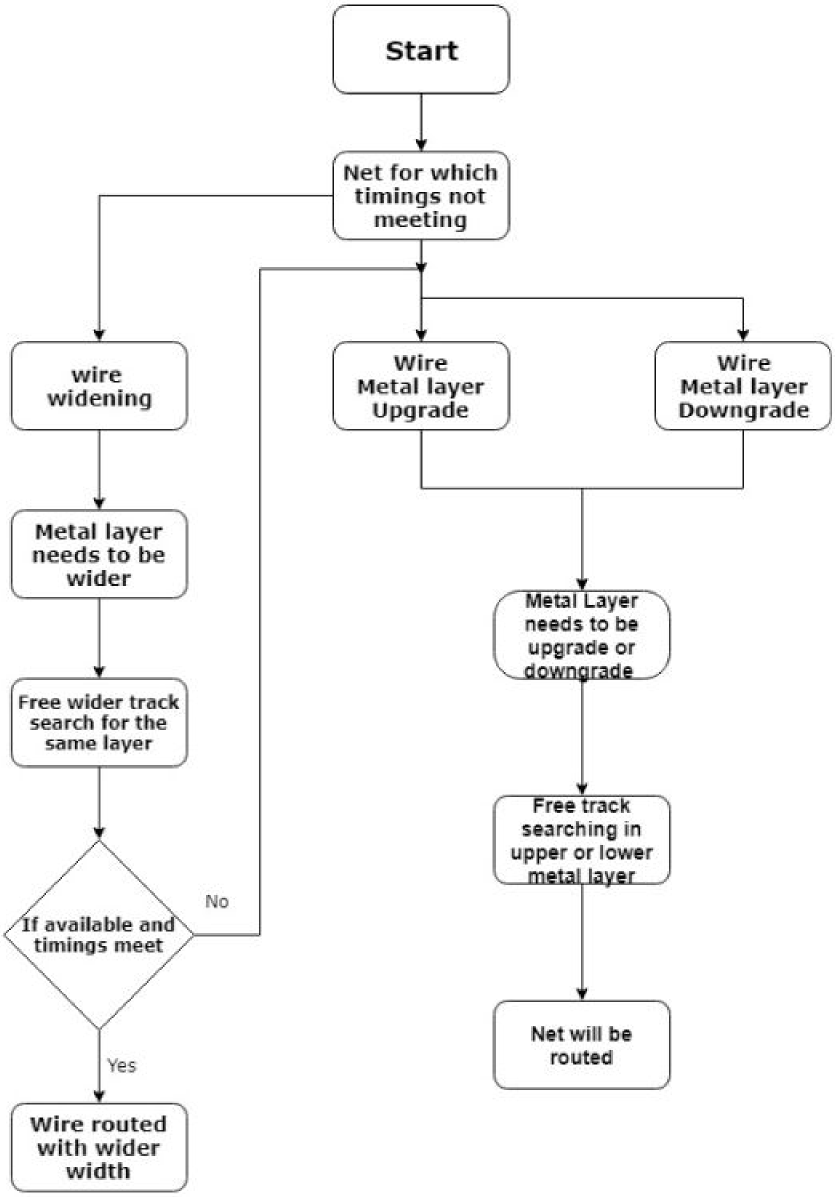

Figure 6.1: Flowchart to Fix Timing Violations in Layout

6.3 Algorithm to Fix the Timing Violation

Input:

Set optimization mode and objectives.

input netlist

Get list of the nets which are having timing violations

Get arrival and required times from the timing analysis.

Output:

Single net is taken from the list

Optimization:

for specific metal layer net [widening of the metal layer of the net]

calculating Slack over the net

If [timings are meeting]

That widened net is routed

Else

Metal layer upgrade - downgrade for the net

timings are calculated

Net will be routed with meeting the timings

End

Above algorithm will route the best topology with meeting timings using different solution of layout.

Chapter 7

Results

Developed utility has routed different 4 topologies for the given single net.It has also calculate the RC delay, Open length from pin to pin routing and Short length over the routed net with other nets.

After the best topology routed it will check that timing slack is meeting or not and if it is not meeting then it will upgrade the metal layer of the net to meet the timing constraints.

7.1 Routing Topologies Available for the Net

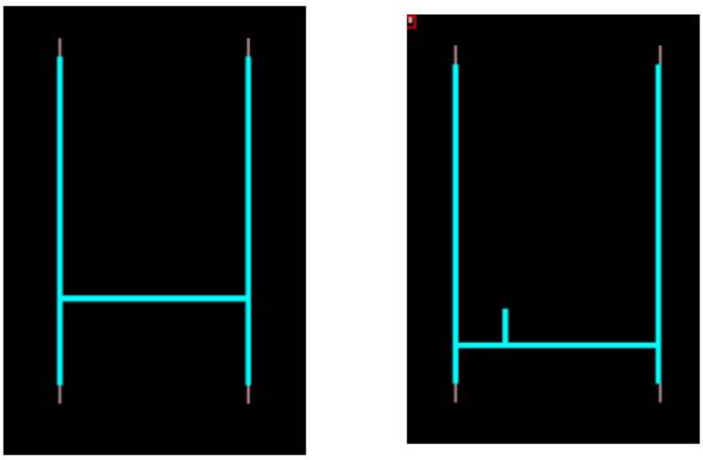

Figure 7.1: Topology - 1 & Topology - 2

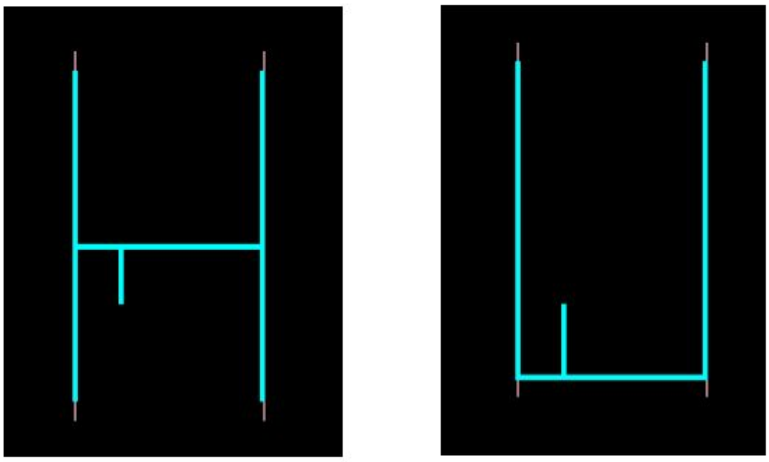

Figure 7.2: Topology - 3 & Topology - 4

7.2 Routed Best Topology Results

Topology	Resistance (μΩ)	Capacitance (pF)	Open Length (μm)	Short Length (μm)	RC Delay (pS)
Topology 1	1157.834	0.402	20.6	19.47	0.000465
Topology 2	1183.88	0.427	20.8	70.57	0.000505
Topology 3	1183.818	0.426	20.9	19.47	0.000503
Topology 4	1148.737	0.436	23.7	30.88	0.0005

Table 7.1: Routed best topology results

7.3 Metal Layer Upgrade Result Comparison

Topology	Resistance (μΩ)	Capacitance(pF)	Open Length (μm)	Short Length (μm)	RC Delay (pS)
Topology 1	947.648	0.346	19.4	15.46	0.000327
Topology 2	1047.847	0.398	23.8	48.26	0.000417
Topology 3	1048.345	0.402	27.9	23.34	0.000421
Topology 4	1023.763	0.405	29.5	15.23	0.000414

Table 7.2: Metal layer upgrade results

7.4 Delay Comparison For Modified Routing Solutions

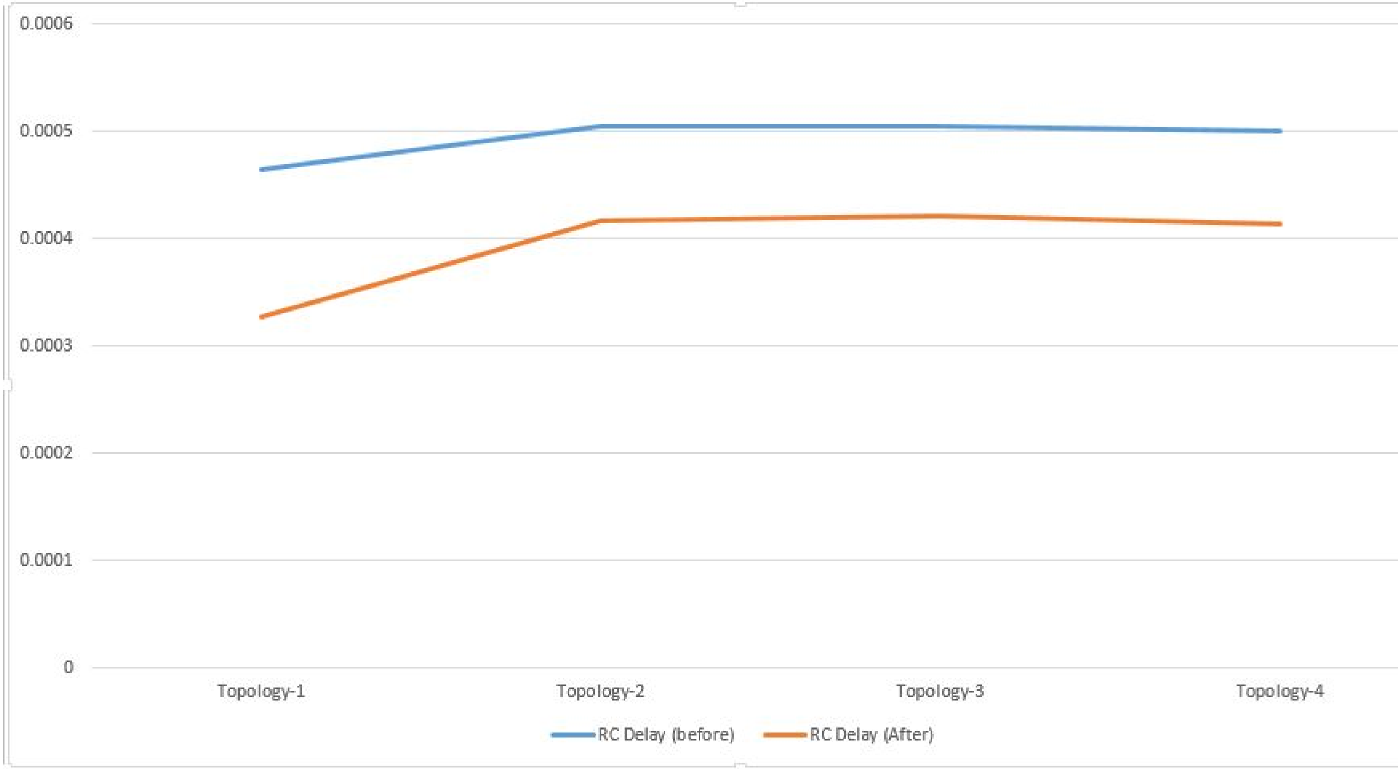

Figure 7.3: Graphical representation for RC Delay comparing both the results

From the Figure.7.3 It is clearly observed that after the use of developed utility RC Delay is decreased for each topology.For the Topology-1 delay is minimum from all the topologies.Topology-1 will be routed with meeting timings in layout.

Chapter 8

Conclusion

In this thesis, Developed the flow which will route different topologies for a single Net.It will also calculate the RC delay,pin to pin open length and short length on each topology.Comparing the results for each topology results , It will route the best topology as per the constraints provided to the router.

Once the best topology is routed, slack is calculated for that net and If positive slack is there then the routed topology will be the best topology meeting timing also.

If the slack is negative for the routed topology,need to meet the timings from Layout.For that developed utility will try to improve the timings using different topology using widening of wire or upgrading-downgrading of metal layers for that wire.This newly routed net will be DRC clean meeting all the timing constraints.

In this way using this utility timing violations are fixed using some layout solutions and which will decrease around 60% manual efforts for fixing timing violation.

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