Design and Analysis of Frequency Synthesizer

Major Project Report

Submitted in fulfillment of the requirements
for the degree of

Master of Technology
in
Electronics & Communication Engineering
(VLSI DESIGN)

By

Parth Ramanuj

(17MECV14)

Electronics & Communication Engineering Department
Institute of Technology
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Ahmedabad-382481

May-2019

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Under the guidance of

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May-2019

Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI DESIGN at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Parth Ramanuj

17MECV14

Disclaimer

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Date: Place: Ahmedabad

Dr. Akash Mecwan
Internal Guide

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Program Coordinator

Dr. D. K. Kothari
Section Head, EC

Dr. Alka Mahajan
Director, IT

Certificate

This is to certify that the Major Project entitled **"Design and Analysis of Frequency Synthesizer "** submitted by **Parth Ramanuj (17MECV14)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in VLSI DESIGN, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination.

SHRI.Arindam MAL
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Statement of Originality

I, **Parth Ramanuj**, Roll.No. **17MECV14**, give undertaking that the Project Report on "**Design and Analysis of Frequency Synthesizer**" submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electronics and communication (VLSI Design)** of Institute of Technology, Nirma University, Ahmedabad, contains no material that has been awarded for any degree or diploma in any university or school in any territory to the best of my knowledge. It is the original work carried out by me and I give assurance that no attempt of plagiarism has been made.It contains no material that is previously published or written, except where reference has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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Dr.Akash Mecwan

Acknowledgements

I would like to express my gratitude and sincere thanks to **Dr. N.M.Devashrayee**, PG Coordinator of M.Tech Vlsi Design and **Dr.Akash Mecwan** for guidelines during the review process.

I take this opportunity to express my profound gratitude and deep regards to **Dr.Akash Mecwan**, guide of my internship project for his exemplary guidance, monitoring and constant encouragement.

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- Parth Ramanuj

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Abstract

The frequency synthesizer is the most versatile application. The Application of frequency synthesizer is clock generation and clock recovery in microprocessor.In thesis this, design and implemented of an individual block of the frequency synthesizer. In order to improve the frequency synthesizer performance, the different technique will be used and all this technique are discussed. In this thesis, frequency synthesizer first block is designed is charge pump. The main of the CP is to improve matching current, leakage current and wide range of the output voltage. The design of CP is proposed and simulated in the cadence virtuoso tool at sbc 180nm CMOS Technology. The design of NMOS cascode CP is achieved wide range output voltage swing at 0.4 to 1.2 V and improves mismatch current using this cascoded charge pump. Voltage controlled oscillator is the most important block in a frequency synthesizer. In this thesis, we design a single-ended ring oscillator with 0.5GHZ to 1.17GHz tunning range has been designing with the total power consumption of the VCO is 6.8mV and the phase noise -110.92dBc/Hz at 1MHz frequency offset. In the thesis, we are also design differential ring oscillator with 1GHZ to 2GHz tuning range, with the power consumption of the VCO is 8.7mW and the phase noise -114.2dBc/Hz at 1MHz frequency offset. In this thesis, we are designing a 6-bit multi-modulus frequency divider and It can work up to 3GHz operating frequency where power supply is 1.8V. The division ratio can be varied from 64 to 127 and it can be achieved using the MMD technique. In multi-modulus frequency divider The main block is 2/3 prescaler and it's designed using TSPC D-FF logic. In the future with an incremental step of one the proposed multi-modulus frequency divider is suitable for sigma-delta fractional-N frequency synthesizer implementation.

Chapter 1

Introduction

1.1 Introduction and Motivation

Nowadays low power consumption and High Speed are extremely important for the electronics system. A frequency synthesizer is the most important block in the modern technology of electronics including Communication system. The general application of the PLL(Phase Lock Loop) is for clock recovery and clock generation in microprocessors, frequency synthesizers, and communication systems. The frequency synthesizer is commonly used to generate clocks signal for high major performance electronics systems. The frequency synthesizer is mostly used for synchronization of the clock in system, noise and skew reduction in communication systems. a frequency synthesizer is a -ve feedback closed-loop system which provides a fixed phase relationship between the reference clock phase and output clock phase. There are mainly five blocks in a PLL, which shown in figure 1. There is five blocks in a frequency synthesizer. Phase Frequency Detector (PFD), Charge Pump(CP), Loop Filter or Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO) and Frequency Divider is the part of the frequency synthesizer. The prime function of the frequency synthesizer or PLL is to generate the same phase signal as the phase of a reference signal and output phase signal. This phase synchronization

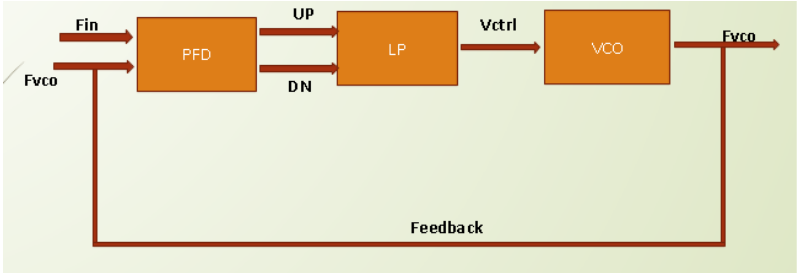

Figure 1.1: Block diagram of frequency synthesizer

is made by many redundancies techniques by comparison of the feedback signal to the reference signal. After comparison, the PLL continues to compare the phase of two signals. If the reference signal and feedback signal gets the same phase and zero phase delay then the system provides constant output due to lock mode.PFD is a main component of the PLL circuits. It compares the phase as well as frequency mismatching between the feedback clock signal and a reference clock signal.

In frequency, a synthesizer oscillator is the most fundamental part of many electronic systems. nowadays integrated circuit is covering towards CMOS, the design of robustness and high-performance CMOS oscillator is more important. The key point of VCO is a required oscillation of frequency, tuning range, phase noise, and power consumption. The oscillation frequency is determined by the application in which the VCO is used such as the microprocessor and mobile phones. The other major key point is phase noise. when low phase noise is another major direction of research. In the digital circuit or microprocessor phase noise of the oscillator will directly effect clock signal, jitters and timing margin they are limit the system performance.

Frequency dividers or prescaler are required for a PLL to reach frequency synthesis capability. This is the block that can reproduce the stability of the lower reference frequency into the output frequency. The prescaler and divider is one of the most evaluative blocks in the frequency synthesizer since it operating at the

highest frequency. frequency dividers or prescaler introduce to any system that has the capability to divide a particular frequency by a particular number. As long as the divider is a connection between the PFD and the VCO, the divider wants to operate at the frequency that the VCO induce. In order to connect the frequency synthesizer, the divider wants to divide the VCO frequency by a particular number that will produce frequency equal to the particular range reference frequency. With that logic, we can conclude that the division ratio N, is literally being multiplied to the reference frequency in order to generate the actual output at the VCO.

1.2 Organization of thesis

Thesis has been divided into 6 separate chapters. The chapters go into nitty-gritty details of all the components comprising the Design and Analysis of frequency synthesizer. Following is a list of the chapters including their brief summaries.

Chapter 1: In this chapter the reader is introduction to frequency synthesizers and their application in wireless communication systems.

Chapter 2: Here,In this chapter the reader will be provided literature survey.

Chapter 3: In this chapter we will discuss The basics of the voltage controlled oscillator, its circuit/layout design techniques, and simulated performance.

Chapter 4: In this chapter we will discussed the understanding of the charge pump circuit.Discussion will be provided on its non idealities and techniques to improvement them. And finally, simulated performance supporting the claims will be discussed.

Chapter 5: In this Chapter we will discussed D-FF based on TSPC and also we

discussed how to design 2/3 prescaler.Here, we are also discussed how to design Multi modulus frequency divider using 2/3 prescaler.

Chapter 6: Finally, the thesis will come to an end in this chapter with some concluding remarks and ideas for future improvements.

1.3 Technology overview

All the circuits presented in this thesis have been developed in a 0.18 m CMOS-RF process supported by SBC18. For almost all transistors level designs and analyses, software packages from Cadence Design Systems have been used. Schematic capture and mask layout drawings were done in the Virtuoso-GXL platform while simulations were performed with Spectre-RF. The frequency synthesizer being such a large circuit, a lot of different methodologies were undertaken in order to meet convergence during simulations. Additionally, due to having access to the simulator in a system with rather limited resources, some performance parameters needed to be loosened. Doing so certainly helped in achieving convergence and generated expected results; however, it also reduced the accuracy of the results by a small fraction.

Chapter 2

Literature survey

Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill Edition, 2002.In which He a describe the physics behind the voltage controlled oscillator and how to generate the periodic signals. He also tell about the charge pump and what is the effect of power supply on charge pump. To reduce this he used the pair of transistor in series.

Analysis and Design of a Low-Power Low-Noise CMOS Phase-Locked Loop by Cheng Zhang B.A.Sc., Simon Fraser University, 2009.In which is describe analysis and modeling of charge pump using diff rent topology.He is also describe the low phase noise voltage control oscillator using differential oscillator[1].

O. Kazanc, "High Frequency Low-Jitter Phase-Locked Loop Design," Yeditepe University, Istanbul, Engineering Project Report, 2008. in this thesis he was describe differential ring VCO technique are reviewed and pros and cons for each type are provided and describe Nmos cascoded charge pump and using different technique reduced mismatch current and leakage current is describe in this thesis[23].

Y. Ji-ren, I. Karlsson, and C. Svensson, A true single-phase-clock dynamic CMOS circuit technique, IEEE J. Solid-State Circuits, vol. 24, no. 2, pp. 62-70,Feb.1989.In this ieee paper he is describe TSPC technique and describe their operation.he is design Flip Flop using TSPC technique and describe the hold and evaluation mode operation[17].

Ram Singh Rana, Dual-Modulus 127/128 FOM Enhanced Prescaler Design in0.35um CMOS Technology, IEEE J. Solid-State Circuits, vol. 40, no. 8, pp.1662-1670, Aug. 2005.In this paper he is describe how to design multi modulus prescaler using TSPC and E-TSPC and describe prons and cons[10].

M.Alioto and G.Palumbo, Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits), New York: Springer, 2005.In this ieee paper he is describe current mode logic technique and how is fast as compared to TSPC logic[14].

Sangho Shin, Kwyro Lee and Sung-Mo Kang, 4.2 mW CMOS Frequency Synthesizer for 2.4GHz Zigbee Application with Fast Settling Time Performance,IEEE MTT-S Int. Microwave Symposium, pp. 411-414, May 2006. Ultra Low Power CMOS Phase-Locked Loop Synthesizers 235.In this paper he is describe differential ring oscillator frequency divider and charge pump.In this paper he is describe how improve phase noise and tunning frequency range and also he is design frequency divider using current mode logic[6].

Huimin Liu"A wide range low power CMOS Radio frequency ring oscillator",2009.In this paper,he is describe current steering Amplifier ring oscillator,current starved ring oscillator.The advantages of CSA ring oscillator it's is working very high frequency.

M. Jung, J. Fuhrmann,"A 10 GHz Low-Power Multi-Modulus Frequency Divider using Extended True Single-Phase Clock (E-TSPC) Logic" 2007.In this paper,The propagation speed and power consumption analysis between TSPC and E-TSPC is performed and based on this analysis, an ultra-low power TSPC 2/3 prescalers are proposed.

Vamshi Krishna Manthena "Ultra Low Power CMOS Phase-Locked Loop Frequency Synthesizers" 2011.In this thesis, he is performed a detailed study on the phase noise and power consumption of the CMOS VCO and designed a low power cross coupled LC-VCO with optimized phase noise and also he is analysis on the charge-pump is carried and introduced a low spur gain boosting charge-pump to reduce the reference spurs.

Neda Nouri "A low swing wide tunning range CMOS Phase lock loop"2001.In thesis thesis ,she is design low phase noise and wide tunning range and describe advantages and disadvantages of ring oscillator and LC oscillator.

Chapter 3

Voltage controlled oscillator

3.1 Integrated oscillator

3.1.1 Oscillation principal of oscillator

A normal oscillator produces a periodic output waveform, generally, they are formed in voltage. There is no apply any input in the oscillator circuit, but still, we identify periodic sustaining output. The diagram model of voltage controlled Oscillator can be described in fig.3.1.

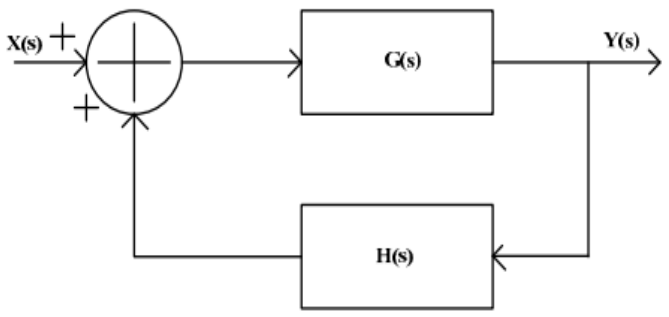

Figure 3.1: Diagram of vco model

The transfer function of VCO model system in fig 3.1. is defined by below.

$$H(s) = \frac{Y(s)}{X(s)} = \frac{G(s)}{1 - G(s)H(s)} \tag{3.1}$$

where G(s) is the transfer function of amplifier and H(s) is the feedback unit. To start the stable and sustain oscillation loop gain must be greater than or equal to 1. For stable oscillation below two conditions or equations are must satisfy.

$$G(s)H(s) = 1 \tag{3.2}$$

$$\angle G(s).H(s) = 2n.\Pi \tag{3.3}$$

This two condition is nothing but "Barkhausan criteria" must be satisfy for stable oscillation.

3.1.2 Types of oscillator

An oscillator is defined as a self-governing circuit and it gives periodic output. For stable oscillation and the constant frequency, at least two states require. There are 3 types of oscillator are LC Oscillator, Ring Oscillator, and Relaxation Oscillator.

For constant frequency ring oscillator require the odd number of stages for the single-ended oscillator or even and the odd number of the stage consists for differential ring oscillator. The relaxation oscillator is a nonlinear electronic oscillator and it produces nonsinusoidal output. LC Oscillator is also called resonant circuit and it's consist inductor and capacitor and both are connected together.

The phase noise analysis and design technique is very good in an LC oscillator as compared to ring Oscillator. But the wide tuning range, low cost, and small chip size make ring oscillator is good as compared to LC Oscillator.

3.2 Ring oscillator

3.2.1 Basic of ring oscillator

Ring Oscillator is made of the odd number of delay stage or gain stage in the feedback loop. In the oscillator output of the last delay, the stage is fed through the input of the first stage of delay. Here, First, we will do a linear analysis of these oscillators using a common source amplifier.

Single stage common source(CS) in feedback is not oscillating,Because it does not fulfill the "Barkhausan criteria". The single stage CS amplifier inverting phase shift and one pole phase shift is 90, So the total phase shift is 270. Then it fails to sustain oscillation. Using a two-stage common source(CS) amplifier gives phase shift but still no sustain oscillation because the gain is less than one. Three stages common source amplifier is enough to sustain oscillation because the gain and phase shift is to fulfill the "Barkhausan criteria".

3.2.2 Single ended ring oscillator

A basic ring oscillator schematic in Figure 3.2 consists of CMOS inverters. To secure oscillation, for the single-ended oscillator is used with an odd number of inverters stage.

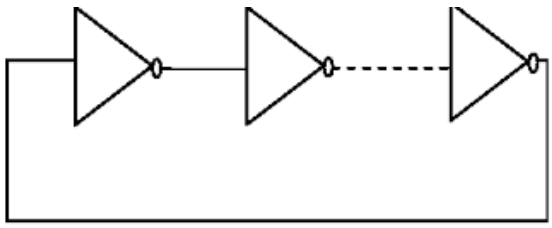

Figure 3.2: Basic design of oscillator

In CMOS inverter current is consuming during transition occurrence while output capacitances are charge and discharge. In inverter with the current sink and

current source, some amount of current is determined at the tail current source or current sinks. A Small amount of current insists when result with a longer transition due to the long duration of charge/discharge output capacitance. The current which flows through the tail current sink or source is control by two bias voltage which is named as Vbn and be voltage. This control voltage controls the current flow consequently the frequency of oscillation.

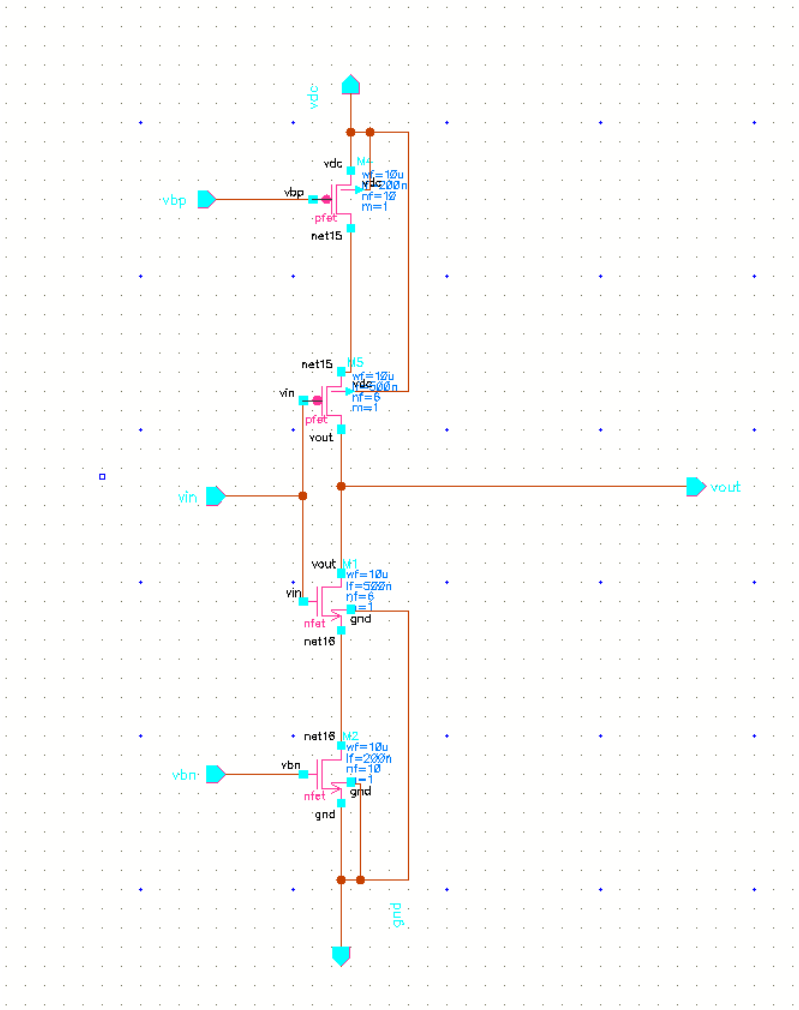

Figure 3.3: Schematic design of inverter

In single-ended Oscillator with tail current sink and current source is shown in Figure 3.3. Ring oscillator circuit required of three current starved inverters is called

as currently starved ring oscillators. The single-ended ring oscillator is highly non-linear and has a very small operating range frequency. when control Vbn is high and Vbp is low then a single-ended oscillator is oscillation.

3.2.3 Differential ring oscillator structure

The Voltage control oscillator in this design based on a differential ring oscillator. The advantages of differential oscillator analyze to a single-ended ring oscillator is the better common mode noise (i.e. power supply and substrate noise) refusal capability. while the differential oscillator is more suitable for recent analog mixed-signal IC on-chip environment, In which the digital circuitry will generate a large amount of power supply and substrate noise.

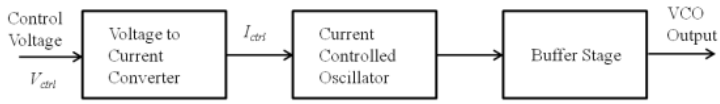

Figure 3.4: Basic block diagram of differential ring oscillator

The block diagram of the differential VCO in this design is shown in Fig.3.4. The control voltage from LP(loop filter) connected into the V to I converter (voltage to current) circuit and create or induced the control current signal and that current is tune in the current controlled oscillator and this control current to generate differential clock signals. In this thesis, For 1.14GHz low power low noise, a 3-stage differential ring oscillator was designed.

3.2.4 V-I converter

The linear voltage to current conversion attribute is going to be fulfilled by using the large aspect ratio transistor, M19, shown in Fig. 3.5, aspect by a very small overdrive voltage (Vov). A first-order relationship between the control voltage (Vctrl) and the

controlled current (Ictrl) has been derived below. The gate to source voltage, Vgs V of the transistor M19in Fig.

$$\text{vgs} = Vth + \sqrt{\frac{2I_ctrl}{K'.\frac{w}{l}}} \tag{3.4}$$

If W/L is hung enough, the above equation can be simplified as:

$$Vctrl - Vth = Ictrl.R \tag{3.5}$$

Thus produce nearly linear voltage to current conversion. Transistor M13 and M14 form a current mirror which gives the control current to each delay stage in the current controlled oscillator.

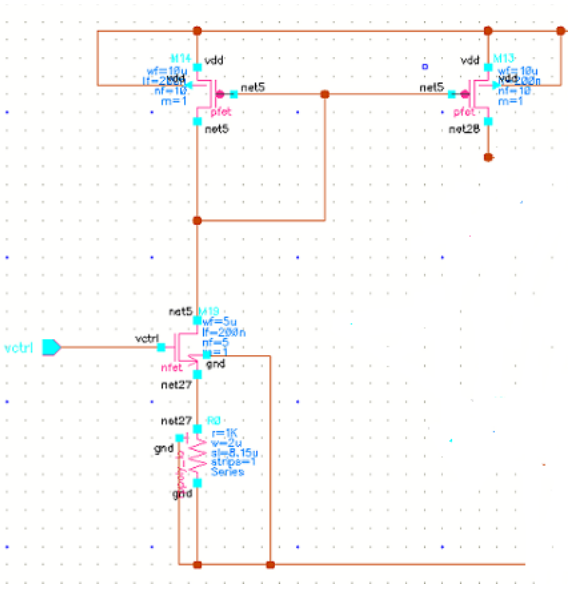

Figure 3.5: Current delay cell

3.2.5 Current controller oscillator

The Current controlled Oscillator is a current controlled current starved Amplifier block shown in Fig.3.6.

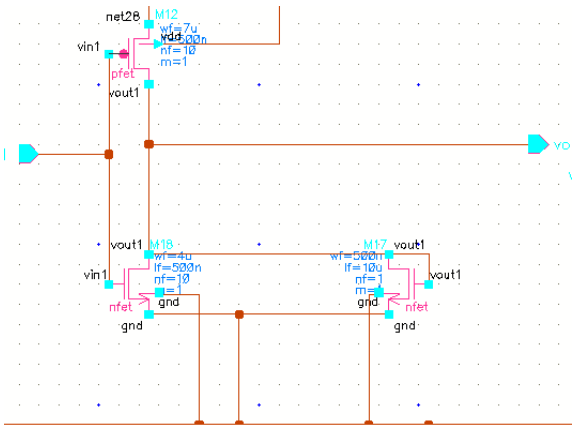

Figure 3.6: Current delay cell

The current steering block requires a current source and a pair of NMOS transistors. M12 is the input device and M17 and M18 is the diode connected load. When Vin is high, M12 is turned on. It sinks the control of current Ictrl and shuts off M17. Under this condition, the resistance of M12 and Ictrl defines the output low voltage VOL. When Vin is low, M12 turns off and Ictrl is steered to M17. Under this condition, the resistance of the diode-connected M17 defines the output high voltage Voh. By varying the control current Ictrl, a current controlled CSA-based ring oscillator is formed with an output voltage swing of.

$$\text{Delta V} = Voh - Vol \tag{3.6}$$

The frequency oscillation and the control current relationship as below:

$$\text{Fosc } \alpha \ \frac{Ictrl}{N.Cl.\Delta V} \tag{3.7}$$

where N is the delay stage in the ring oscillator and CL is the load capacitance. For a fixed range of the Ictrl current, this can be approximated as a quasi-linear relationship. An advantage of the CSA (current starved amplifier) delay stage is

that ground noise coupled from other circuitry within the chip is rejected by the CSA as a common mode noise because both its output and input are referred to the same ground.

3.2.6 Differential ring oscillator circuit design

The 800 MHz 3-stage differential VCO schematic is shown in Fig. 3-30. M10 and R form a linear voltage-to-current converter which provides the control current to the delay cells. M1 to M8 form the differential delay cell. Based on Eqn.3.25 and discussion in Section 3.5.4, transistors M2 and M3 should have a small W/L ratio in order to obtain high voltage swings and thus decrease oscillator noise. In addition, a high control current is preferred for low noise performance, however, increasing the control current also increases the power consumption. Therefore, there is a design tradeoff between noise performance and power consumption. Transistor M8 is added to provide additional bias current for the delay cell. This extra current decreases the VCO gain (i.e. the tuning sensitivity). High tuning sensitivity affects noise performance in the entire PLL system. A small variation in the control voltage will cause a large deviation of the oscillator frequency from its desired value.

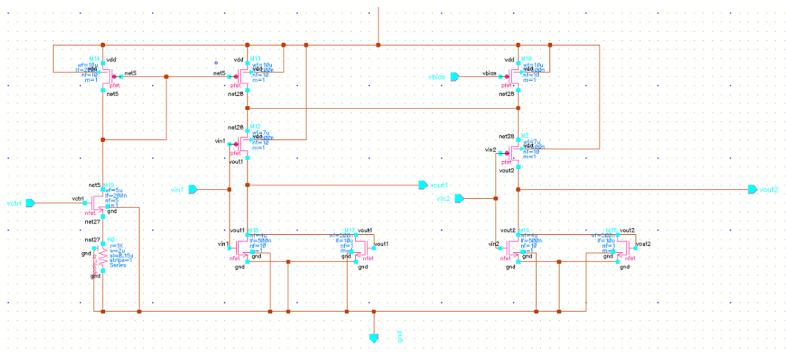

Figure 3.7: Schematic of differential ring oscillator

The waveform of the VCO output is nearly a sinusoidal periodic waveform with

a limited voltage swing.

3.3 Layout design of vco

3.3.1 Layout design of single ended oscillator

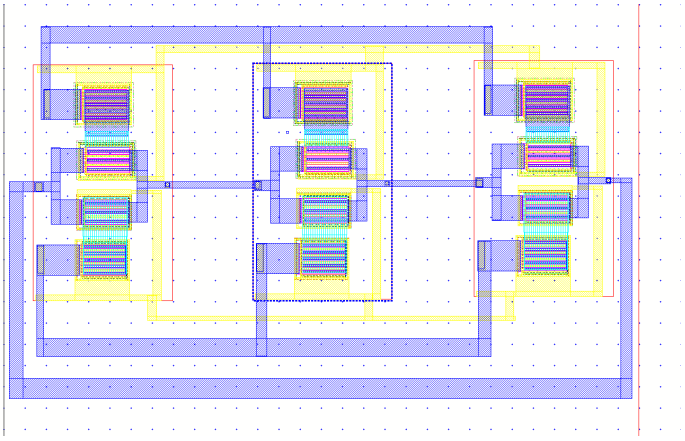

Figure 3.8: Layout design of single ended ring oscillator

3.3.2 Layout design of differential ring oscillator

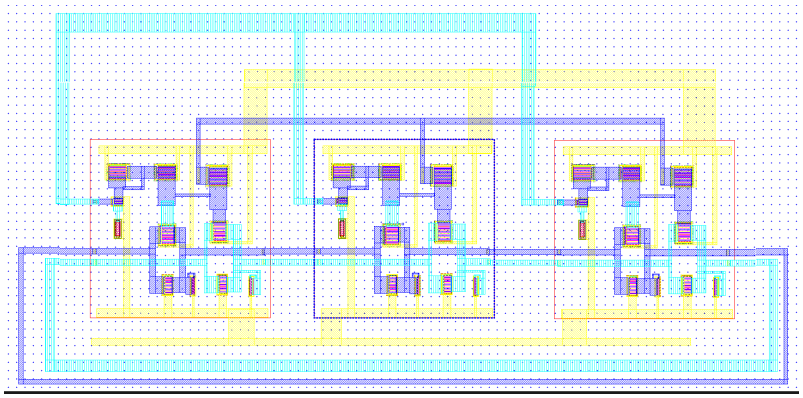

Figure 3.9: Layout design of differential ring oscillator

3.4 Ring oscillator simulation and result

we simulate both the schematic and layout of the ring oscillator in cadence virtuoso ADE specter. when output frequency of the signal is 1.14GHz and control voltage of the single-ended inverter is Vbn is 900mV and Vbp is 100mV.

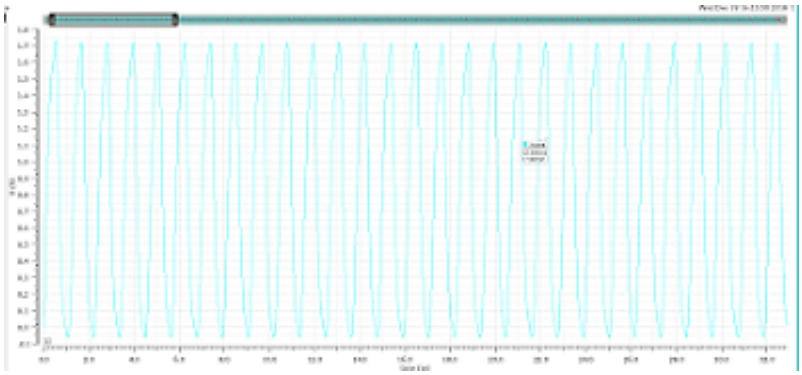

Figure 3.10: Transient analysis of single ended ring oscillator

In Differential ring oscillator we are also checking the tuning characteristics and which are shown in the fig.the output frequency can be changed linearly from 1GHz to 1.9GHz where Vctrl changed from 0.4V to 1.8V.

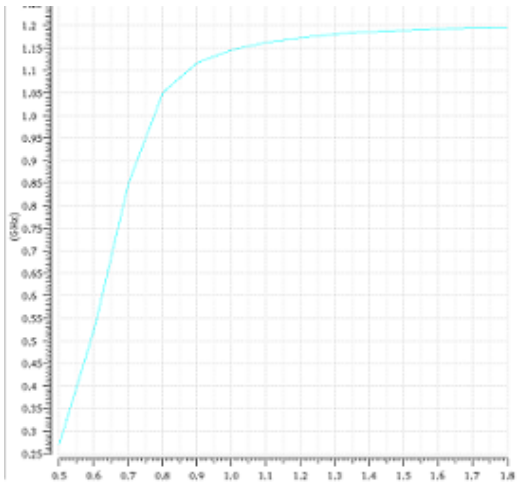

Figure 3.11: Frequency tunning of single ended vco

The other important simulation is phase noise of the VCO operating at 1.17GHz

is simulated using the Spectre ADE simulator and the phase noise measured at offset frequency 1MHz has been found equal to -114.2dBc/Hz.

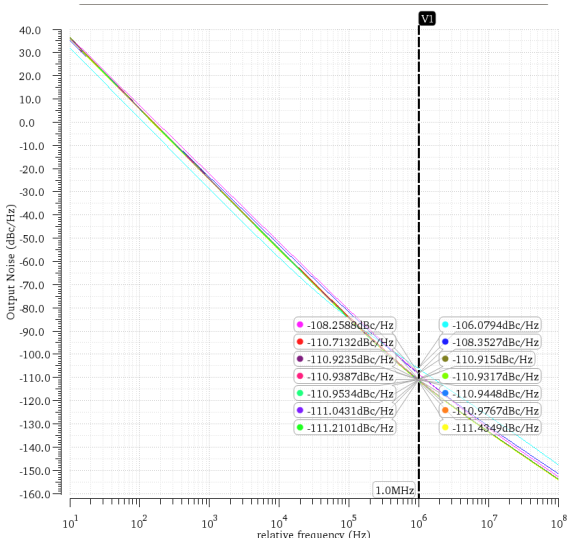

Figure 3.12: Phase Noise of single ended ring oscillator

Here, we simulate both schematic and layout in cadence virtuoso ADE specter,when the output frequency of the signal is 1.14GHz and control voltage of the single-ended inverter is vctrl=900mV .

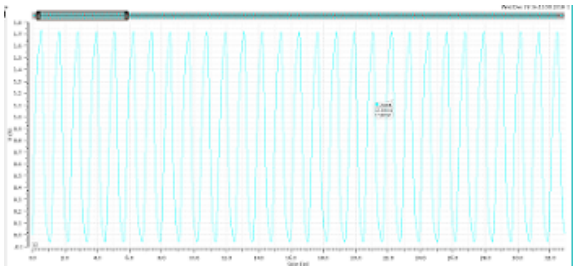

Figure 3.13: Transient analysis of differential ring oscillator

In Differential ring oscillator Most Important simulation is the is tuning characteristics, which is shown in fig.3.13. In VCO we are measured tunning characteristic from 0.5 V to 1.8 V control voltage where output frequency can be changed linearly from 1GHz to 1.9GHZ.

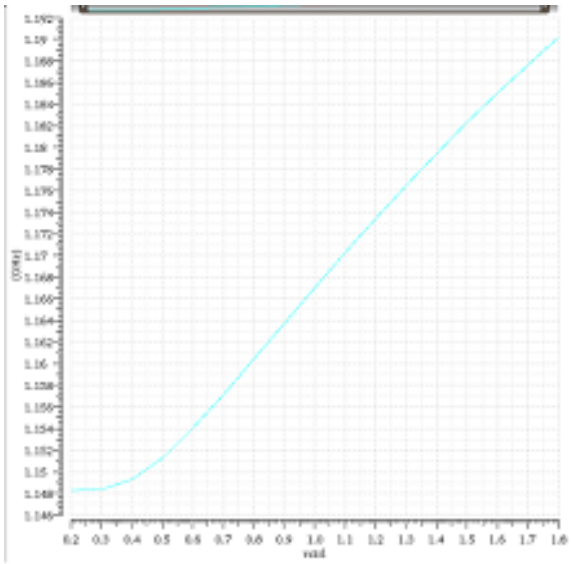

Figure 3.14: Frequency tunning of differential ring oscillator

In Differential ring oscillator we are also checking the phase noise. In this design phase noise, the VCO is -110.92dBc/Hz and we are measured phase noise at 1MHz offset frequency.

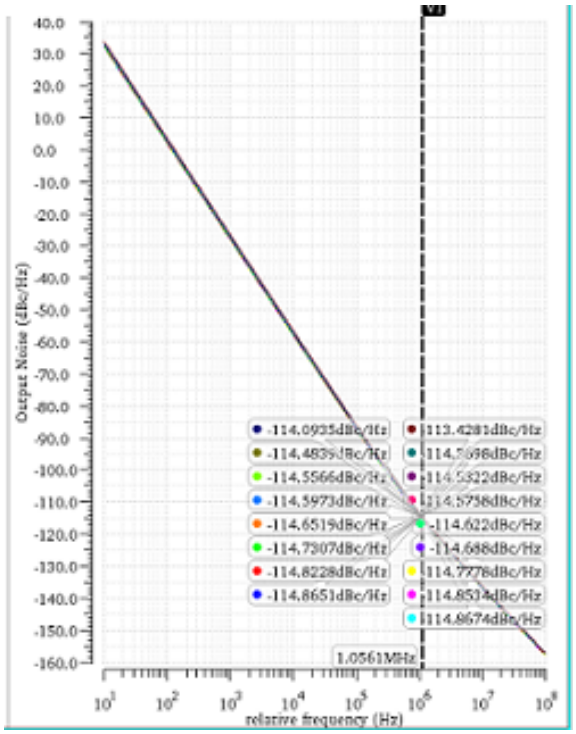

Figure 3.15: Phase Noise of differential ring oscillator

3.5 Summary

The main aim of actual work is to design and analysis of the Voltage controlled oscillator in cadence virtuoso tool. Here, we conclude a wide tuning range and low phase noise ring oscillator was Design in this thesis. Three stage ring oscillator based on single-ended and differential ring oscillator was selected for wide tuning range and low phase noise. The frequency range of the VCO was observed from 0.5GHz to 1.2GHZ.The VCO operating with 1.8V power supply and consumes 6.8mW. Differential circuit provides a linear relationship between the oscillation frequency and the control voltage. This Oscillator is working is very low supply voltage and control voltage.

Chapter 4

charge pump

4.1 Basic design and analysis of cp

The major purpose of the CP Block is to convert voltage-related information by producing Discharging and Charging current that current enters in the LP which that controls the Oscillator. A simple Basic CP circuit with a capacitive Load is shown in Fig.4.1. [6]

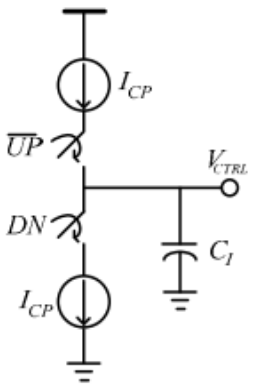

Figure 4.1: Basic design of charge pump

When the up signal is high, the capacitors c1 is a charge and the controls Voltage of input Oscillator are stat the oscillation. When the down signal is low, the

capacitor c1 is discharge and the control voltage of the input of the Oscillator is to Pulldown. The most important parameter is in this Design of CP is the frequency range, CP current.

4.2 Non - ideality of cp

There is no mismatch between the current when the frequency synthesizer block is a lock. But in CP some non-ideality is still there like mismatch current, leakage current at the output of the CP. Here, In this thesis, we are briefly discussed the non-ideality of CP.

4.2.1 Leakage current

In CP major issues is the leakage current. In CP leakage current exist only when both switches are low. Here, how to remove this leakage current with the different techniques we will discuss below.

4.2.2 Mismatch current

In CP another prime problem is the current mismatch and they exist only when both switches is high and also using different technique here discuss how to decrease mismatch current in cp in below discussion.

4.3 Design and analysis of charge pump

NMOS cascaded CP is shown in Fig.4.2.In NMOS cascading CP, we are add additionally Gain boosting stage at the output stage. The reason for the adding Gain stage is we are improve matching current using this technique. In charge pump design in the charge pump up block M22, M23 and M24 is the gain boosting

stage where in charge pump down block M12, M13 and M14 are the gain boosting stage. Here, the operation of the NMOS cascade charge pump is the same as the basis of the charge pump.

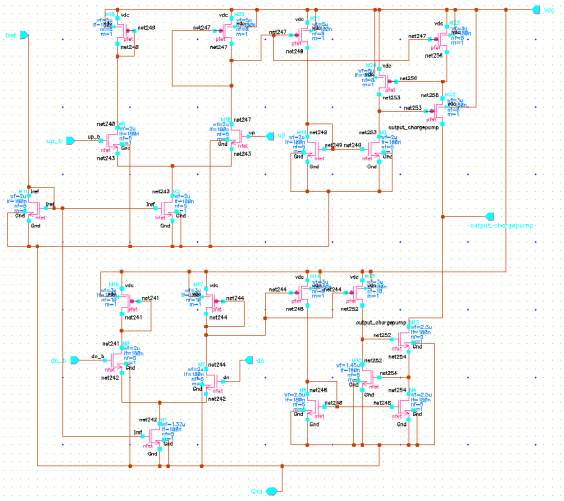

Figure 4.2: Schematic design of charge pump

The schematic of the charge pump used in the design is shown in Fig.4.2. The charge pump circuit consists of two input differential pairs M5- M18 and M0-M7 are controlling switches. There are two current sources switch M2 and M1 for supply for stable current to the differential switches, In charge pump up block M21 and M22 has two outputs to the charge current and in CP down block M4, and M14 has two output which helps to discharge the current

The operation of the NMOS cascade charge pump is the When the up switch is on and down switch off then M7 is off and up switch M10 is on. so charging current will be flow in the M22 and the LP is charging and M7 is off, down switch is off so there are no discharging current flows in M4.

The operation of the NMOS cascade charge pump is the When the up switch is off and down switch on the M7 is on and up switch M10 is off, so discharging

current will be flow in the M4 to the ground and the LP is discharging and M10 is off, up switch is off so there is charging current flows in M22.

In charge pump when both switch M10 and M7 is on then up and down charge pump block is allowing to the current flow into the output node. If both charging and discharging current are the same the current will be stored in a loop filter there no effect on the oscillator control voltage. If mismatch current will occurs in output node so by adjusting the control voltage and remove the mismatch current. The operation of the NMOS cascade charge pump When both the switch up and down is low, M7 and M10 are off and both the charge Pump Up and down the block are switched off. So The charging and discharging currents are equal to zero.

4.4 Layout design of charge pump

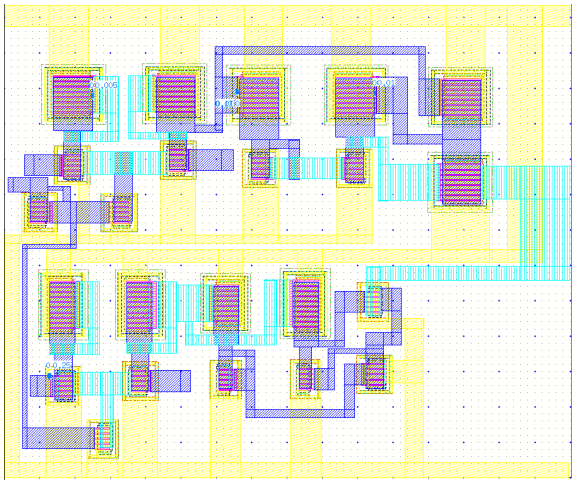

Figure 4.3: Layout design of cp

4.5 Simulation of cp

All the result of the schematic and layout of the CP is obtained in cadence virtuoso ADE specter tool and all the schematic and layout design of CP has been designing using 180nm sbc18 CMOS Technology.where power supply is 1.8V.

In charge pump we are observe matching current when both switch Up and Down is High i.e charging current.

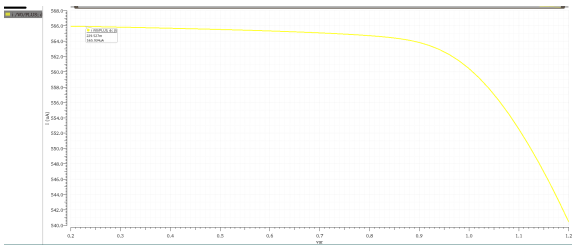

Figure 4.4: Charging up current

In charge pump we are observe when both switch up and down is low i.e discharging current.

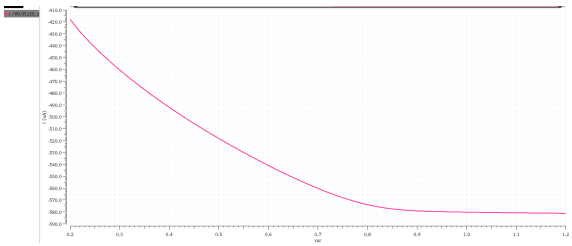

Figure 4.5: Discharging down current

4.6 Summary

The main aim of this actual work is to design and analysis of the charge pump in cadence virtuoso tool. Using the NMOS cascade charge pump we are reduced the non-linearity effect to improve the performance of the charge pump and speed. The design of the charge pump will help to improve the performance of PLL and reduced the PLL reference signal noise and spurs. The output resistance is increased

using current mirror Circuit is provide a large range of output and two component low power high gain operation amplifier improves the matching of charging and discharging current. This charge pump is work at 1.8V and the power dissipation of this charge pump is 8.92mV.

Chapter 5

Programmable Frequency Divider

Frequency dividers or prescaler are required for a PLL to reach frequency synthesis capability. This is the block that can reproduce the stability of the lower reference frequency into the synthesizer higher output frequency. The prescaler and divider are one of the most evaluative blocks in the frequency synthesizer since it operating at the highest frequency. A multi-modulus n/n+1 prescaler such as divide by 32/33 and divide by 64/65 all include of divide by 2/3 block. while the frequency divider can be constructed for a programmable divide ratio, In this chapter we will discuss how the ratio can be made programmable and how this programmable divider to cover all the frequency ranges in the 2GHz. In this chapter, we will discuss How to design a 2/3 divider and How to design a multi-modulus divider using 2/3 prescaler and also we are analysis the result of the simulation and performance of the frequency divider.

5.1 Basic of programmable frequency divider

Frequency dividers or prescaler introduce to any system that has the capability to divide a particular frequency by a particular number. As long as the divider is a connection between the PFD and the VCO, the divider wants to operate at

the frequency that the VCO induce. In order to connect the frequency synthesizer, the divider wants to divide the VCO frequency by a particular number that will produce a frequency equal to the 10 MHz reference frequency. With that logic, we can conclude that the division ratio N, is literally being multiplied to the reference frequency in order to generate the actual output at the VCO. For example, if our communication system needs an oscillator of 1.14GHz, for a 10 MHz reference oscillator, we require to implement a divide ratio N of 114.

Due to we understand the idea of the frequency divider, we also require to understand the idea of its programmable frequency divider. The VCO design for this effort has an output frequency range up to 2GHz So, in order to cover all the mod in both bands using a 10 MHz reference, it can be concluded that the divider division ratio should be range between 111 and 118.

In considering we are implementing an Integer-N frequency synthesizer, we are predicted to have a divide ratio that is an Integer number. The programmable prescaler that has been implemented for this work has two unique part.one of the part of The CML prescaler is make using Current mode logic (CML) and operating at the same high frequency as the VCO output. generally, CMOS logic gate cannot operate at high frequencies, the frequency requires to be scaled down to a suitable range using the prescaler.

The prescaler allows us to generate up to 2GHz mod frequency and decrease the number of programming bits. The programmable dividers or has been created using CMOS logic blocks, which comfortably operates at any frequency less than 1.5 GHz. With the 6-bit program code, the programmable divider can divide the input frequency with divide ratios ranging from 64 to 127. The programmable divider involves of several 2/3 multi-modulus prescaler functions of which are divide the input frequency either by 2 or by 3. while periodically dividing the input frequency with both 2 and 3, we can achieve easily the integer division ratio. using a combination of several 2/3 prescaler blocks we can achieve an integer division ratio.

5.2 Design of tspc based 2/3 divider

5.2.1 Operation of tspc logic circuit

In D-FF we observe two types of operation in TSPC D-FF one is the Hold Mode and second is evaluation Mode is shown in Fig.5.1.

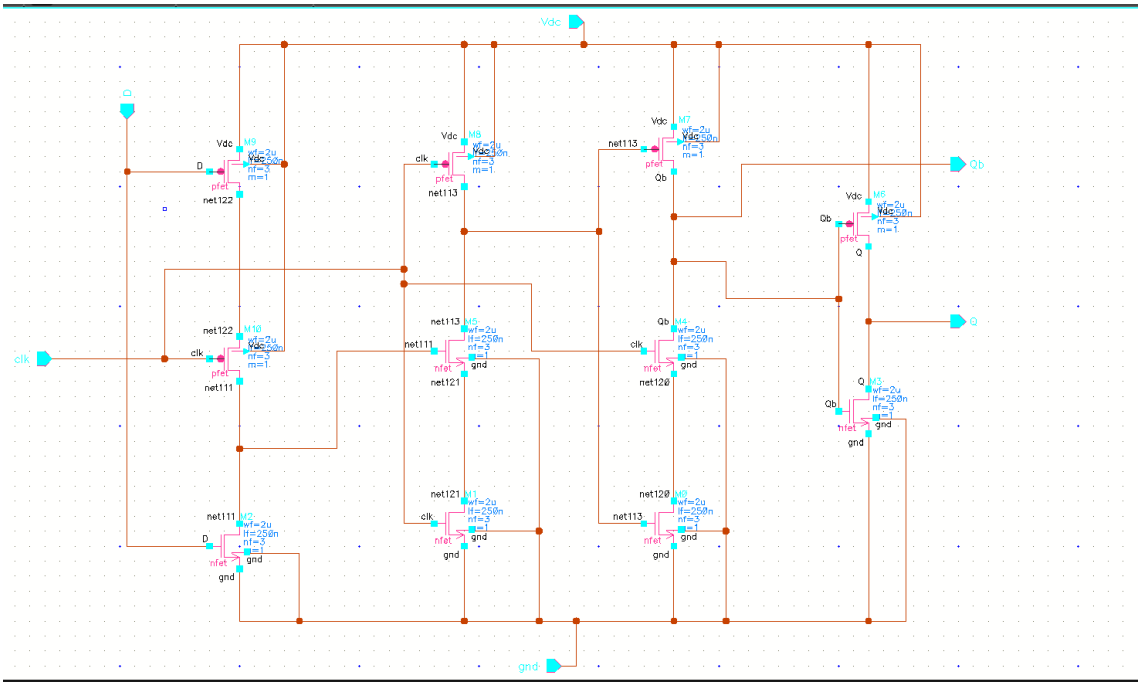

Figure 5.1: D-FF based on tspc

In the hold, mode means in precharge when CLK is Zero and Node S1 is precharge mode to providing on the signal D and Node P1 is precharge by VDC. As transistors M5 and M6 are turned off, output Node Vout becomes floating. In the evaluation mode, when CLK is high and if the Node is precharge by VDC in the Hold mode,

Node P2 is discharge and output node transistor Pull up by the transistor M6. If the Node P1 is precharge to Zero during the hold mode, Node P2 is not discharged, and the output Node transistor is Pull Down by the transistors M6 and M5.

5.3 Design of divide by 2 circuit

A divide by 2 design is implement using TSPC D-FF is shown in fig. This frequency division by 2 is achieved by only when the inverted output terminal is connected directly back to the data input of D terminal.

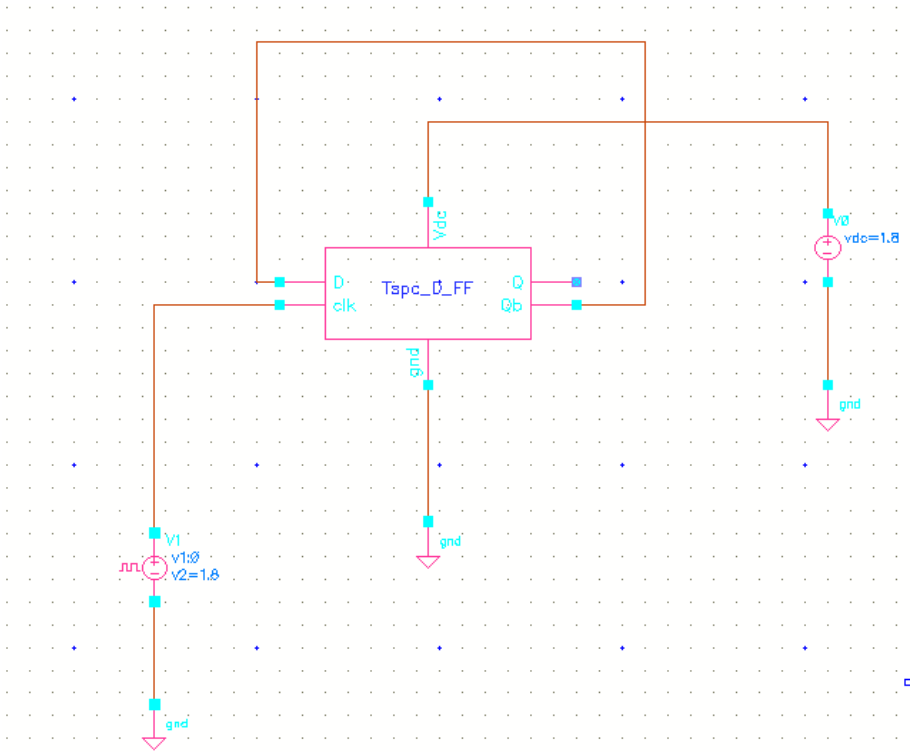

Figure 5.2: Divide by 2 based on tspc D-FF

5.4 Divide by 2/3 and programmable divider circuit

To achieve 64 to 127 division ratio 2/3 prescaler is required. A 2/3 circuit design is shown in fig as below.

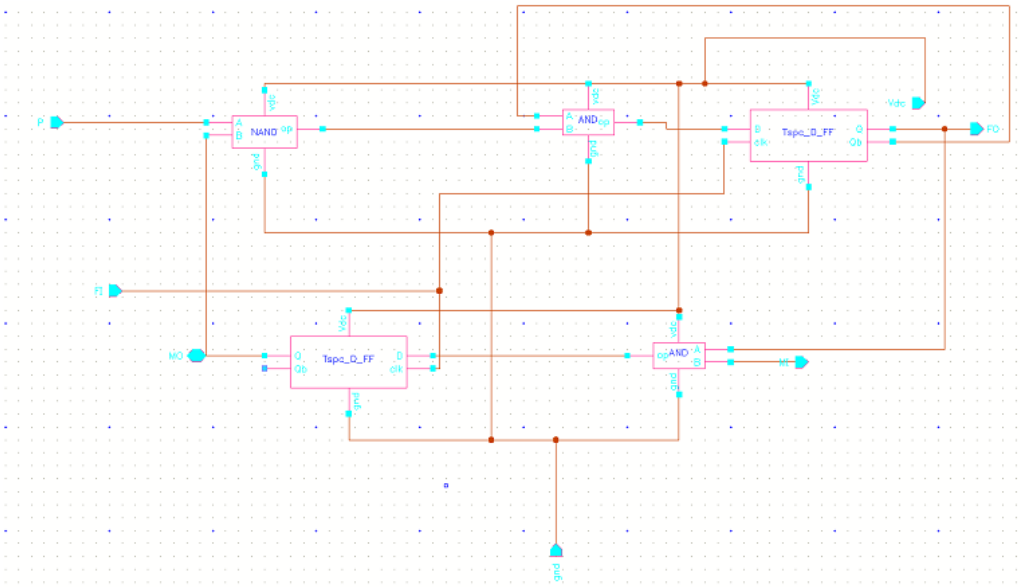

Figure 5.3: Schematic design of 2/3 presacler

A 2/3 divider block or circuit involves two useful blocks,one is the prescaler logic and the second end of cycle logic as shown in Figure 4.It has two input signal: the input MI, the controlling bit P. Two output signals are produced: the output frequency Fout of the stage and an internal feedback signal MO from this stage to the previous stage. The prescaler logic divides the input signal Fin by 2 or 3 which was determined by the end of cycle logic. The function of the circuit is determined by 2 control signal one is MI and second is P. when control signal MI is ”1” and control signal P is ”0” then input frequency is divided by 2. when control signal MI is ”1” and control signal P is also ”1” then input frequency is divided by 3.

5.4.1 Programmable divider circuit design and operation

The full block diagram of the 10MHz to 2GHz divide by 64 to 127 multi-modulus frequency divider is shown in Figure 3.

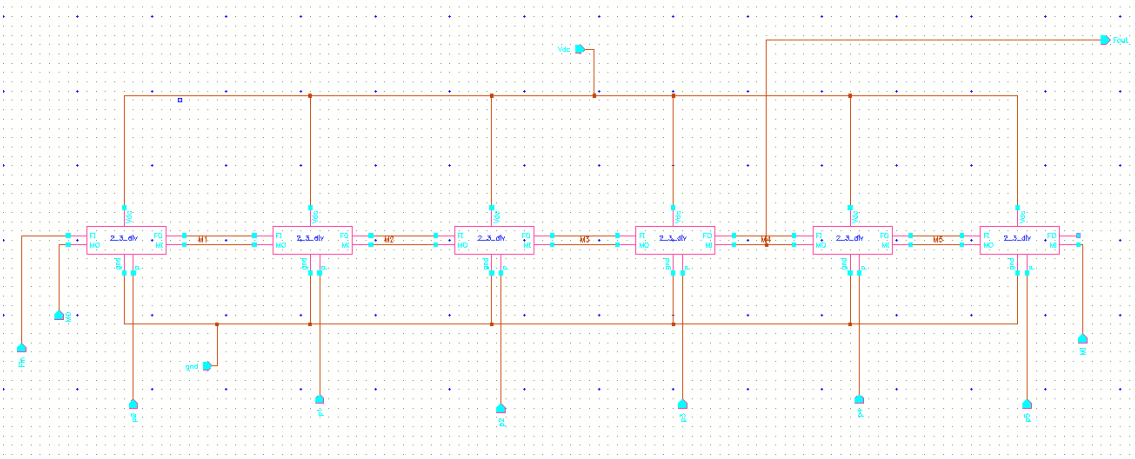

Figure 5.4: MMD divider based on tspc

It consists of six cascaded 2/3 divider block and all six divider block is TSPC based. The multi-modulus frequency divider can be controlled to divide input frequency by any programmable ratio from 64 to 127. It can work at clock frequency up to 3GHz. The Selected bit at the Modulus Controller determines the operation of the multi-modulus frequency divider whether to work in a 5 bit or 6-bit operation. The operations of the frequency divider are based on two programmables division bit P6, P5....P0. Once in a division period, the last block on the chain produced the signal MI which is always high. This signal then propagates up from the last stage to the first stage. For generalizing this idea to a number of 'n' cascade 2/3 division block yield a division range of 2^n to $2^{n+1} - 1$.The division ratio is 6 and it can formulated by below.

$$N = 2^6 + 2^5.P5 + 2^4.P4 + 2^3.P3 + 2^2.P2 + 2^1.P1 + 2^0.P0$$

The output signal period can depicted as:

$$\text{Tout}=\text{N.Tin}$$

Tin is the periods of the input signal and P6, P5....P0 is the binary control voltage of the block.let's one example operation of the circuit is shown in fig. For N= 112 (112=000011). As result first four are operated in a divide by 2 and the last two are operated in a divide by 3 and all they are depending on control bit.

5.5 Layout design of frequency divider

5.5.1 Layout design of TSPC D-FF

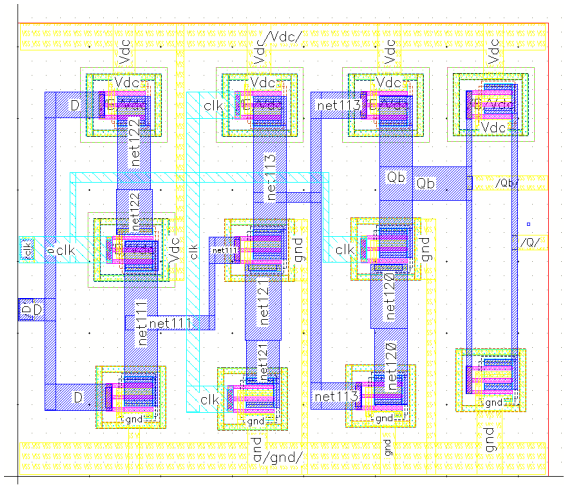

Figure 5.5: Layout design of d-ff

5.5.2 Layout design of 2/3 divider

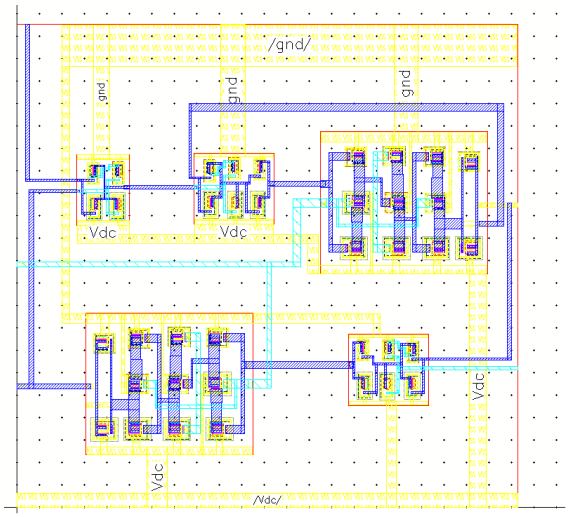

Figure 5.6: Layout design of 2/3 divider

5.5.3 MMD frequency divider layout

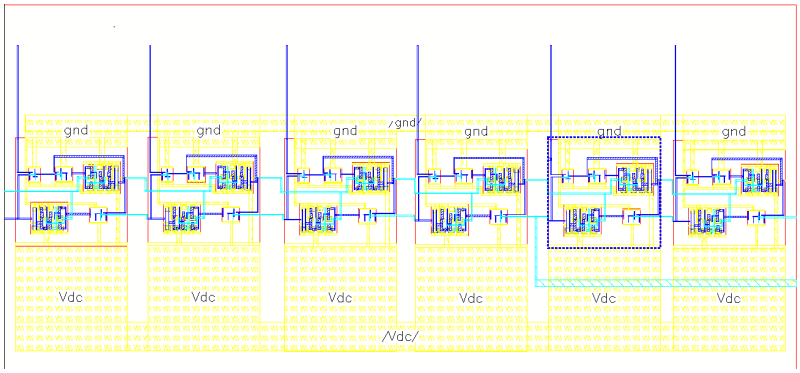

Figure 5.7: Layout design of mmd

5.6 Simulation and Result

In the Transient simulation, we observed a 2/3 prescaler result, where we apply supply voltage 1.8 V in 2/3 circuit.when the frequency of input signal 1.14GHz and

it's work properly up to 3GHz.When signal MI is High and control binary voltage is low then 2 prescaler is work as divide by 2 as shown in fig.

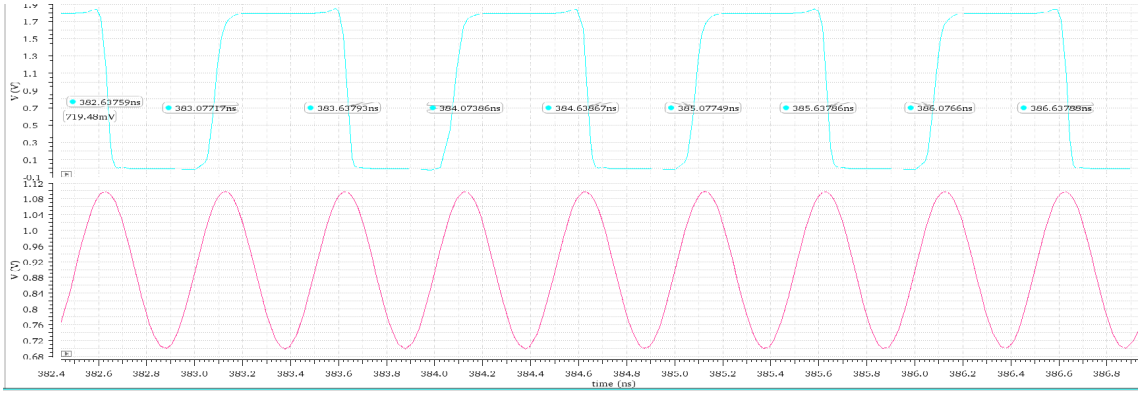

Figure 5.8: Output of divide by 2

Here, When signal MI is High and control binary voltage is High then 2 prescaler is work as divide by 3 as shown in fig.

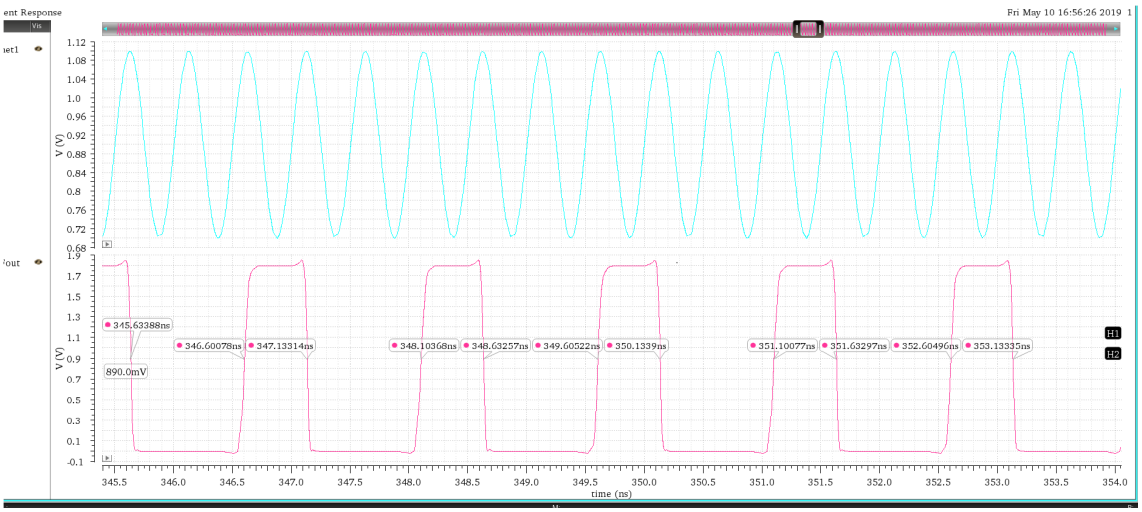

Figure 5.9: Output of divide by 3

The principle of the actual multi-modulus frequency divider is as mentioned above. The divider factor is controlled by the value of P7, P6P0. If P6, P5 are high and others are low, the divider factor of frequency divider is equal to 112 and its result is shown below.

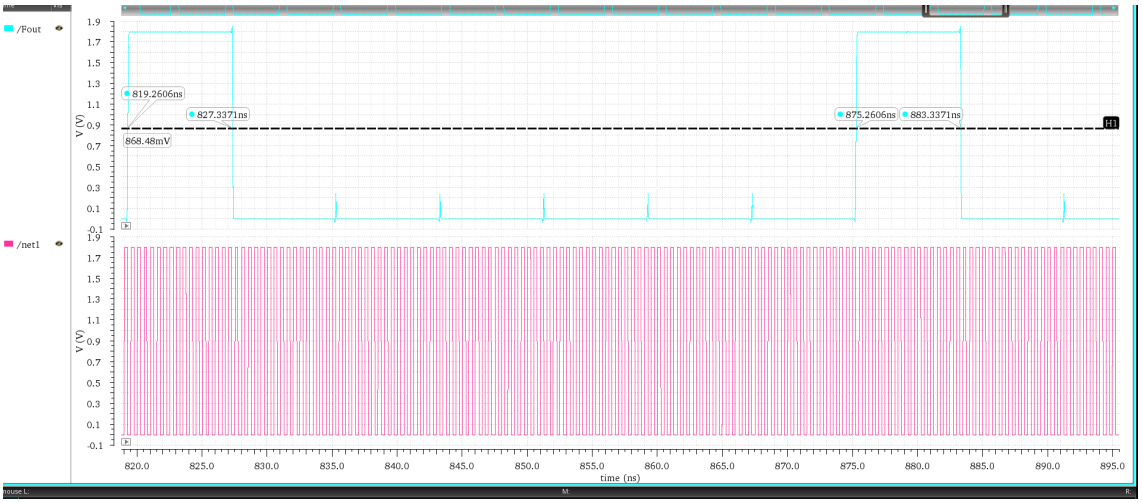

Figure 5.10: Output of divide by 112

Here, we design layout of 2/3 prescaler and multi-modulus frequency divider and we are observed output result and it's the same as above.

5.7 Summary

The Prime aim of actual work is to design and analysis of the multi-modulus frequency divider in the cadence virtuoso tool. In this thesis, we discuss a block diagram for programmable multi-modulus dividers based on an actual TSPC D-FF is presented. The actual divide 2/3 prescaler uses a unique TSPC D-FF logic on 180nm sbc18 CMOS technology with 1.8V supply voltage. It can work up to an operating frequency of 3.5GHz.

Chapter 6

Conclusion and Future scope

In this thesis, we design a wide range and low power RF ring oscillator. A 3-stage ring oscillator based on single-ended and differential CSA block was chosen. The frequency range of both VCO was observed from 0.5GHz to 1.2GHZ. At 1.14GHz operating frequency, the VCO power consumption is 6.8mW and phase noise at 1MHz offset frequency is -114.2dBc/Hz. The main aim is the design and analysis of a charge pump in the Cadence Virtuoso tool. Using the NMOS cascade charge pump we are the performance of charge pump and speed. This charge pump is work at 1.8V and the power dissipation of this charge pump is 8.92mV. In this block, we design a 6-bit multi-modulus frequency divider and It can work up to 3GHz where power supply is 1.8V. The division ratio can be varied from 64 to 127 and it can achieve using the MMD technique. In multi-modulus frequency divider, The main block is 2/3 prescaler and it's designed using TSPC D-FF logic. In the future, with an incremental step of one, The proposed multi-modulus frequency divider is suitable for sigma-delta fractional-N frequency synthesizer implementation

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