Variation Tolerant SRAM Write and Read Assist Technique

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Bhoomika Mali

17MECV18

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

AHMEDABAD-382481

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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Declaration

This is to certify that,

1. The thesis comprises my original work towards the degree of Master of Technology in Electronics and Communication Engineering at Nirma University and Synopsys India Pvt. Ltd. and has not been submitted elsewhere for a degree.

2. Due acknowledgment has been made in the text to all other material used.

- Bhoomika Mali

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Internal Certificate

This is to certify that the Major Project entitled **"Variation Tolerant SRAM Write and Read Assist Technique"**submitted by **Bhoomika Mali (17MECV18)**, towards the partial fulfillment of the requirements for the degree of Masters of Technology in VLSI Design Engineering, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge, havent been submitted to any other university or institution for award of any degree or diploma.

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This is to certify that the Major Project entitled **"Variation Tolerant SRAM Write and Read Assist Technique"** submitted by **Bhoomika Mali (17MECV18)**, towards the partial fulfillment of the requirements for the degree of Masters of Technology in VLSI Design Engineering, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge, havent been submitted to any other university or institution for award of any degree or diploma.

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Abstract

In SRAM design, more challenging task to improve SNM (Static Noise Margin) and WM (Write Margin). In this thesis i used Read and Write Assist technique to improve my WM and SNM in memory. In our memory there is more challenges at lower technology. When we go at low technology at that time some margin voltage will change according to our requirement. So for that we used assist technique to improve this things in memory.

Basically we used assist technique when my read and write operation is fail. In my memory during read operation my read is fail some time because of size and some parameter like voltage etc. For that i have to use read assist technique because my stability is so poor some time because of size problem so i got bad SNM in my memory. To reduce my SNM we changed in design like size change or Vt change and after that i used technique and got better SNM using WL Boosting technique. During write operation, i got bad WM or some time i got write data very late time so i got failure in write operation. For that i used technique which is Negative Bit-line technique. In this i give some dip voltage according to our requirement and got better WM (Write Margin).

Read failure occurs when the cell is not able to preserve a zero and that is possibly because the pass gate becomes too strong as compared to pull down and trip point of the opposite inverter shifts towards 0, because of the weak PMOS and strong NMOS.

Write Failure occurs when the cell is not able to create a regenerative effect and flip the state of the cell and that is possibly because the pass gate becomes weak as compared to the pull up which inhibits the node voltage to go below the switching threshold and flip the state. So, the current through the transistor decreases and the effects of threshold voltage fluctuation cannot be neglected at lower supply voltages. The limitation on the minimum operating supply voltage Vmin is critical and require circuit assist techniques to enhance the functional window of the cell.

Keywords : RA(Read Assit), WA (Write Assist),Floorplan,WM(Write Margin),SNM(Static Noise Margin)

Abbreviations

SoC	System on chip
LVS	Layout Vs Schematics
SRAM	Static Random Access Memory
WA	Write Assist
RA	Read Assist
WM	Write Margin
RM	Read Margin
HD	High Density
HS/HC	High Speed/ High Current
WT	Write Time
PU	Pull Up
PD	Pull Down
PG	Pass Gate
PVT	Process, Voltage, Temperature

Contents

List of Figures

Chapter 1

Introduction

In this project I will do read and write operation for basic 6T- SRAM. In that sometimes our write operation and read operation was fail so for that we used assist technique. In our case why we should write assist?[3]

- We decrease our design like Dimension of our design means Width, Length and according to our requirement we changed in operating voltage according to our technology. According to our technology challenges will increase with different node.

- If we changed in our design like dimension means width or length than we see some changes in intrinsic such as the number and also see the doping of atom location in our channel region of the physical device.

- Because of these changes we faced some threshold voltage mismatch in our design between nearing transistor which reduce the cell Static Noise Margin.

- If we reduce the voltage than we faced problem in read/write stability of the cell. When pass gate is strong as compared to pull down means pass gate to pull down ratio is bad at that time read failure occur and our cell is not able to keep stable data at node point because of weak PMOS and Strong NMOS.

For using write assist technique we changed in our design, like here we changed our power supply voltage at bit line or we VSS raising or WL boosting all that things we

used for better write in our bit cell.

1.1 Motivation

- Tuning of RM/WM setting is Very Important thing for SRAM
- Read and Write operation are main features of SRAM
- For Successful Read and write operation: clock cycle and Access time are the most important things to control
- Read Margin: Memory Clock cycle and Access time
- Write Margin: Cycle time and Write time
- Performance = Tuning of RM + Tuning of WM
- Focus on read and write assist technique. For that focus on that that in which case our write and read operation is good and fail.
- If fail our write operation in any case than what you can do. So at that time you must see on write and read assist technique.
- Write assist technique:
  1) negative bit line
  2) VDD Lowering (Also called VDD Collapse)
- Read assist technique:
  1) Use for getting better SNM
  2) Standard technique for WL lowering used industry wide
- Why our write is fail and read also that all things done in bit cell analysis and resolve this problem by using this read and write assist technique.

1.2 Objective

- Instance vice summary
- Margin vice summary

- Clearly document failed measurements
- Prepare Summary Document
- Understanding of memory architecture and understand operation and take care about technology because if it is change than all terms all operation all method also change.
- Analyzed result
- Run inst-char and inst-eval for characterization
- SNM (Static Noise Margin) and (WM) Write Margin
- Why Assist technique needed
- Circuit Functionality (Write and Read Assist Circuit)
- Note result for that and conclude result

1.3 Overview of the Thesis

Chapter 2 is the Literature Survey. In this will discuss about the Read and Write Assist and Memory Architecture also. In that the most important parameter like ratio of pull up and pull down and also ratio of pull down and pass gate. Taking this two parameter which i mention in above it will decide the margin of read and write in our memory cell (6T-SRAM). For Read and Write Assist technique is described in read and write Assist technique chapter. In that I understand what memory is and discuss architecture with different technology, discuss all point of memory architecture like address decoding, array, data, no of word, no of bit etc. all point I learn and understand.

Chapter 3 will discuss about the Basic SRAM on that I used two different technologies and compare data accordingly. Like read current, write current, SNM (Static Noise Margin), write margin, read margin, compare RM voltage, see different architecture for different technology.

Chapter 4 will discuss about Memory Architecture why we should read and write assist and what is the architecture, size of MOS, Ration of our MOS for read and write

all that things cover.

Chapter 5 will discuss about Compiler Characterization and Evaluation. Here discuss about characterization based on Process, Voltage, Temperature and evaluate that things also. Also discuss some quality assurance who check before compiler release.

Chapter 6 will discuss about The Read and Write Assist Technique of SRAM. In that I understand what is read and write operation in SRAM and I also compare 6-T and 8-T SRAM. Why we should read and write assist? In which case read and write is failure and how? Why we should use technique of write and read?

Chapter 7 will discuss about the Implementation and Results and Conclusion.

Chapter 2

Literature Survey

A Assist Technique we used for improve WM (Write Margin) and Satatic Noise Margin (SNM) in our memory bit-cell. We analysed result at different voltage high to low so we observed that at low voltage we have so many chalanges in margin. For that we used technique for that and we used assist technique also. Here main things which we have to take care about ration of cell and pull up ratio. This two parameter decide our margin of the bit-cells.[1]

2.1 cell beta Ratio

Cell beta Ratio = (W/L of PD) / (W/L of PG)

- The Ratio between pull down of NMOS with width and length to pass gate of NMOS with width and length.
- When we got better value of above ratio than we got better stability during read operation but if got lower value of above ratio than got good read current but also we got failure in SNM. We can not get stable data.

Cell pullup Ratio = (W/L of PG) / (W/L of PU)

- when got better value of above ratio than we got better write margin (WM) during write operation but if got lower value of above ratio than got failure in WM. We can not get proper data at write node.

In variation tolerant SRAM we used assist technique I analysed the operation of basic 6T-SRAM. In that in which case I got failure in write operation and read operation and for that I used read and write assist technique.

In this case I observed our bit cell size, ration of our MOS, then which MOS is in which region that all analysis I did. Then I see different architecture so for that so many things are different like memory architecture. For that I did instance vice summary, I got data for that and I compared all data with reference compiler data and then I looked float generation, latch, decoder method, pre-decoder, x-decoder, read and write all that things I done in memory architecture.

I also see on optimizing Bit Cell Design. For that I see on different compiler like HD (Dense Bit cell) and (HC/HS) High current / high speed.

2.2 Dense Bit cell (HD)

- To support HD memory architectures
- Smaller in area
- Better in leakage
- Read current is comparably less
- Slow speed

2.3 High Current/Speed (HC/HS)

- Bigger in area/size
- Big Drivers
- Big Sense Amplifiers
- High Leakage

2.4 6-T SRAM Bit cell- Device sizing

- For that there is three MOS in bit cell.

- Pass Gate: If made bigger
  - High Read current (better Tcq)

- Better WT/WM
- High Leak
- BL device load increases, so slow Discharge Rate.
- Degraded SNM
- Due to SNM issue, it must be kept weaker than PD.

- Pull Down: If made bigger
  - Area concerns
  - Degraded WM
  - Improved SNM
  - To keep area concern in mind, PD is sized to optimal size, it is still bigger device in BC.

- Pull Up: If made bigger
  - Good SNM
  - Degraded WM
  - Large area
  - Still needed to be kept weaker than PG, to ensure successive write operation.

What is memory:
The Memory is used for stored the data, write the data and read the data. It is use the binary logic that is "1" or "0". In memory there is two types one is Static and another is Dynamic. For that we usually used Static SRAM in our design. In Static they have 6 transistor so there is more challenges comapre to Dynic. In Dynamic there is only pne Capacitor and one transistor.The static is volatile memory. It is like digital design as sequential circuit.

In common, the memory architecture is divided in two part i.e Main array and Periphery. In Main array part,Bit-cells are located in Memory and to write data from bit-cells or to Read data in to bit-cells, the circuits called periphery of memory architecture are designed.[4]

2.5 Basic Memory Architecture

Below,the Basic Memory Architecture is shown in Fig. It is divided into following part.

a] Main Array

b] Control Block

c] Row and column Decoder

d] Column Multiplexer

e] Sense Amplifier

f] IOs Block

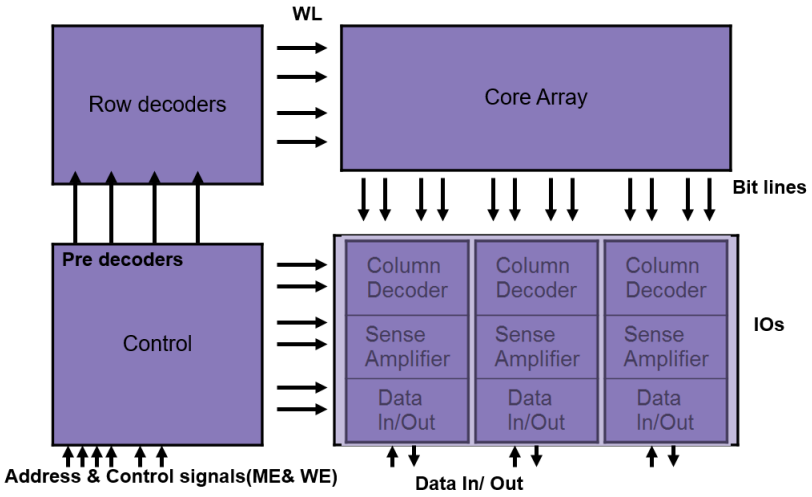


Figure 2.1: Basic Memory Architecture

2.5.1 Main Array

In Main Array memory cell have no of array row and no of array column. There is many block in memory like decoder block, SA block, Main memory array block, Buffer block. It will connected with each other in particular row and column. Each cell is joined with the other cells in the same Word-line in row, and same Bit-line in column.

2.5.2 Control Block

Control block is basically used for generate the signal like data signal, address signal, some internal signal, clock means it will generate mail signal of memory which is input signal. There is so many latches used for hold data till our operation will be finish. In memory the control block also take care about the Hold Time, Set-Up Time , Time-Period etc which is so important part in memory.

2.5.3 Row and Column decoder

Decoding is basically used for select the particular address bit data bit. Suppose we have 4 X 2 memory size in this operate particular top word line at that time decoder decode particular that address bit and data bit and it will activate the particular that word line or bit line.

2.5.4 Multiplexer

It is used select the particular word line and bit-line in memory. In memory there is column multiplexer and row multiplexer is used. when we used column multiplexer than we got half of physical row and we got double physical column. Using Multiplexer we made different architecture like tallest, wide, small etc.

2.5.5 Sense Amplifier

Sense Amplifier is very important circuit in memory. It will use during the operation in 6T-SRAM.In read operation suppose my stored data is "0" & 1 and my word line is off at start state. but when read operation is start my word line is turn on and my one bit-line is discharge when my voltage potential difference generated. In this time my read operation is start and main role of the transistor is pass gate and pull down. for got better read pull down should be strong and we got better read stability here. in my read operation bit-line is fully discharge at that time the sense amplifier sense the voltage difference between two node and it will give result which data is stored in our internal node or in memory.It will useful two detect data quickly in memory.

2.5.6 IOs Block

In IOs block there is column decoder, SA (sense amplifier), Data in/out. Column decoder decode the value in column and select cell which per address. SA is sensing the logic. If our BT¿BB than sense amplifier senses the logic 1 and BT¡BB than sense amplifier senses the logic 0. Here we give data and got output also here.

2.6 Memory Compiler

In System on Chip (SoC) design, i.e. customer required memory with different aspect ratio with different size. Memory compiler provide the features to generate the memory instances with different sizes with different features. In this chapter, how user can inter-

face with memory compiler and different features are described.

The working of memory compiler is shown in Fig. [2] Memory designer design and architects the memory compiler. For different library, there is a compiler is design at technology node. The IC designer gives inputs to the memory compiler to generate memory instance.

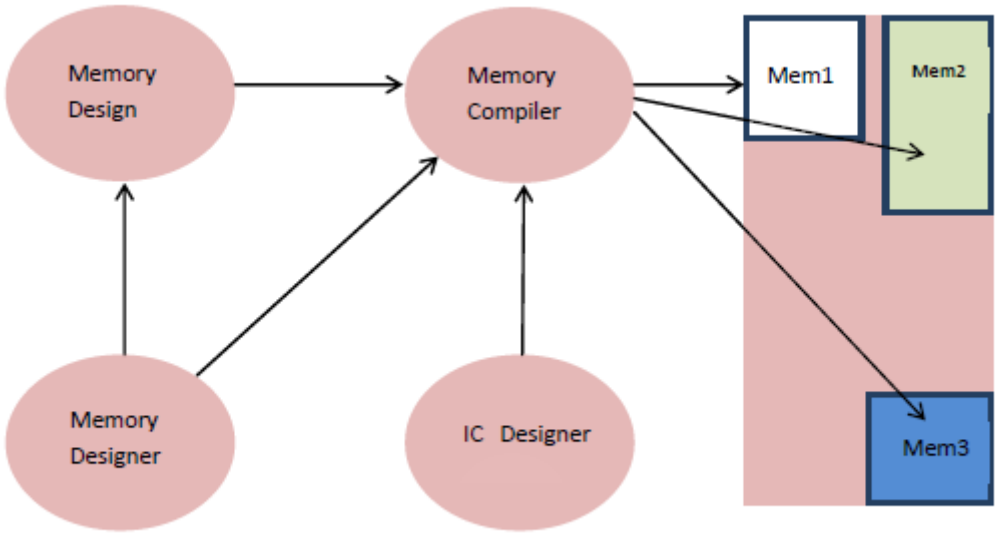


Figure 2.2: Memory Compiler

2.7 Comparison of 6T and 8T-SRAM:

In 6T-SRAM there is basically 6 transistor in memory design and in 8T-SRAM there is basically 8 transistor in memory design. Here we see that in 6T transistor means it will take less area compared to 8T-SRAM.In 8T-SRAM area will be more. We also take care about power. In terms of power there is more power used in 8T-SRAM compared to 6T-SRAM because in 8T-SRAM more transistor so it will take more power to activate each and every transistor. In terms of leakage in 8T-SRAM there is more leakage compared to 6T-SRAM because 8T-SRAM have two more transistor for independently read and write operation.So leakage is more in 8T-SRAM compare to 6T-SRAM. There

is also challenges in SNM and WM.[5]

To resolve that challenges we changed in design like width and length.We changed in design for that i analyzed margin of read and write. In 8T-SRAM there is we got better SNM compared to 6T-SRAM because of two more transistor. I got better WM in 6T-SRAM compared to 8T-SRAM because of less transistor. We also used technique for this debugging margin.

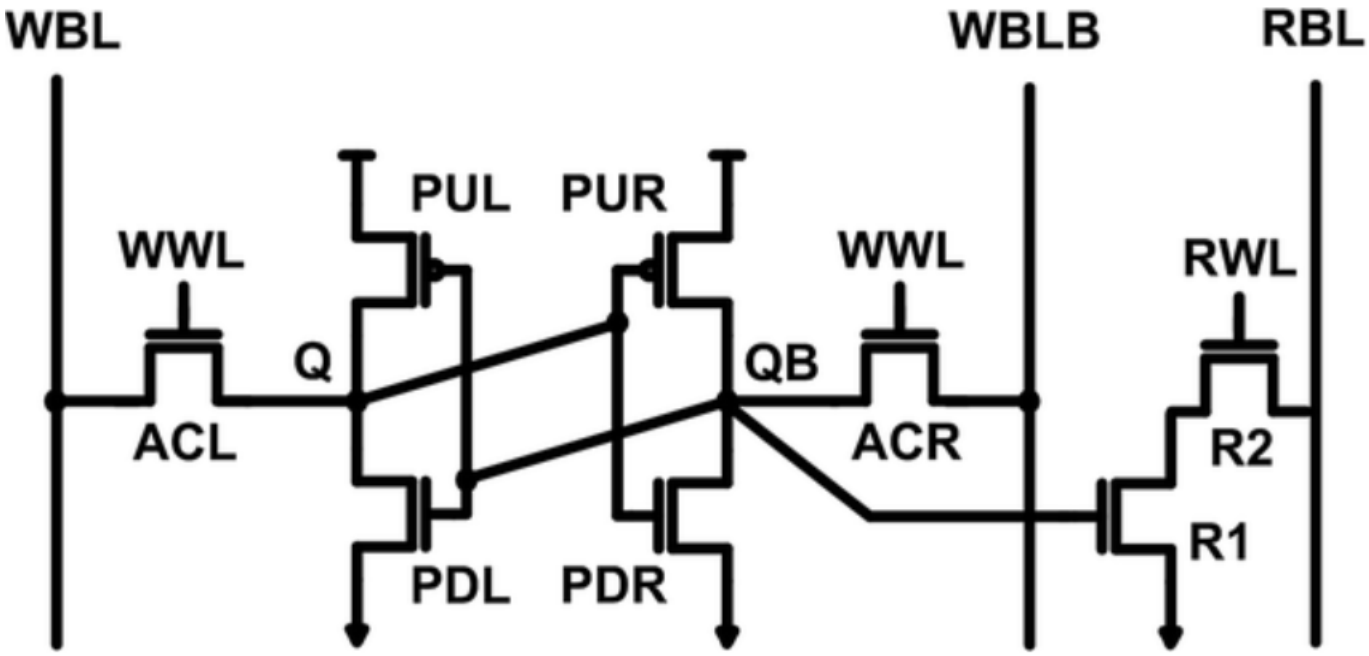


Figure 2.3: 8T-SRAM Cell

For that we used technique Read and Write assist for reducing read and write operation. We apply voltage dip on word line and bit line. To resolve the problem in SNM and WM.

2.8 Read Assist Circuit for WL Lowering:

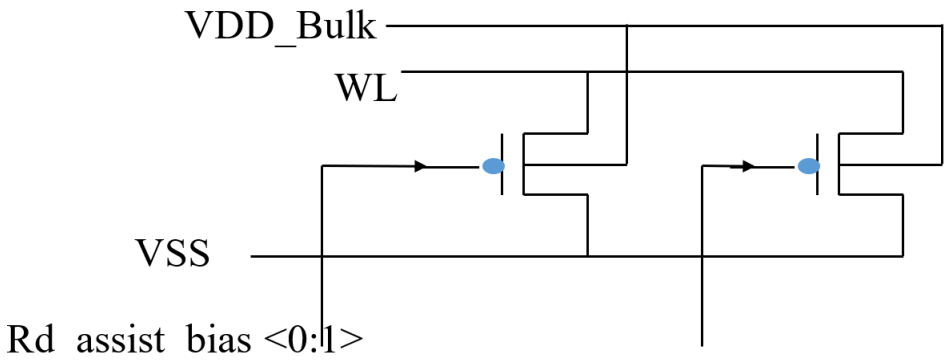


Figure 2.4: Read Assist Circuit

2.9 Architecture of Write Assist:

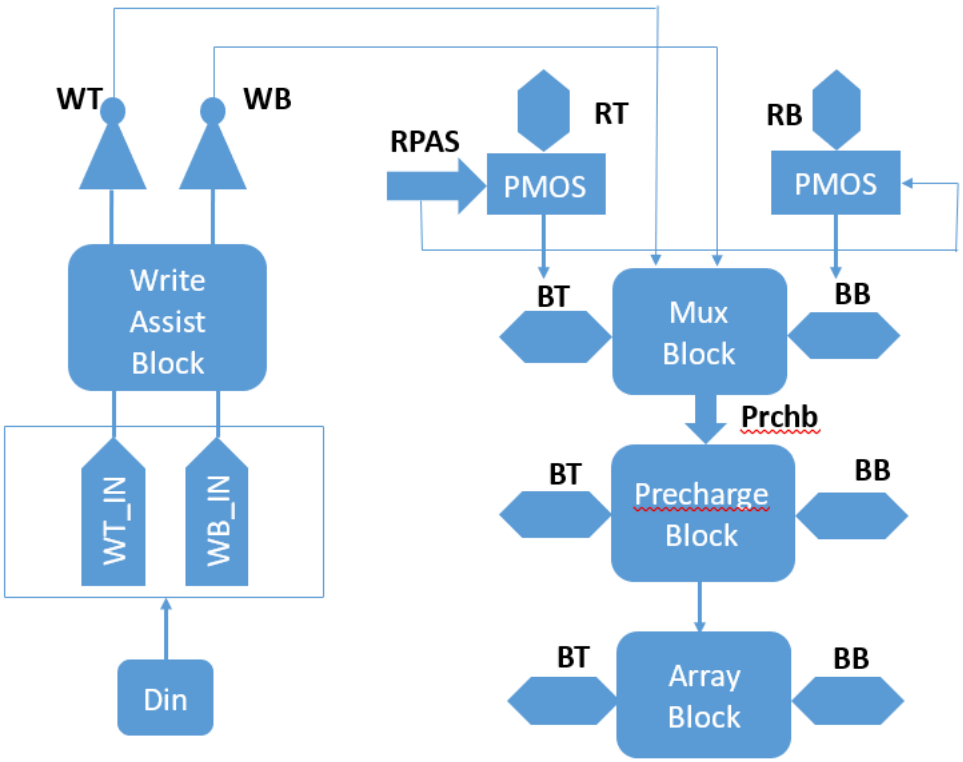


Figure 2.5: Architecture of Write Assist

2.9.1 Write Assist Circuit for Negative Bit line

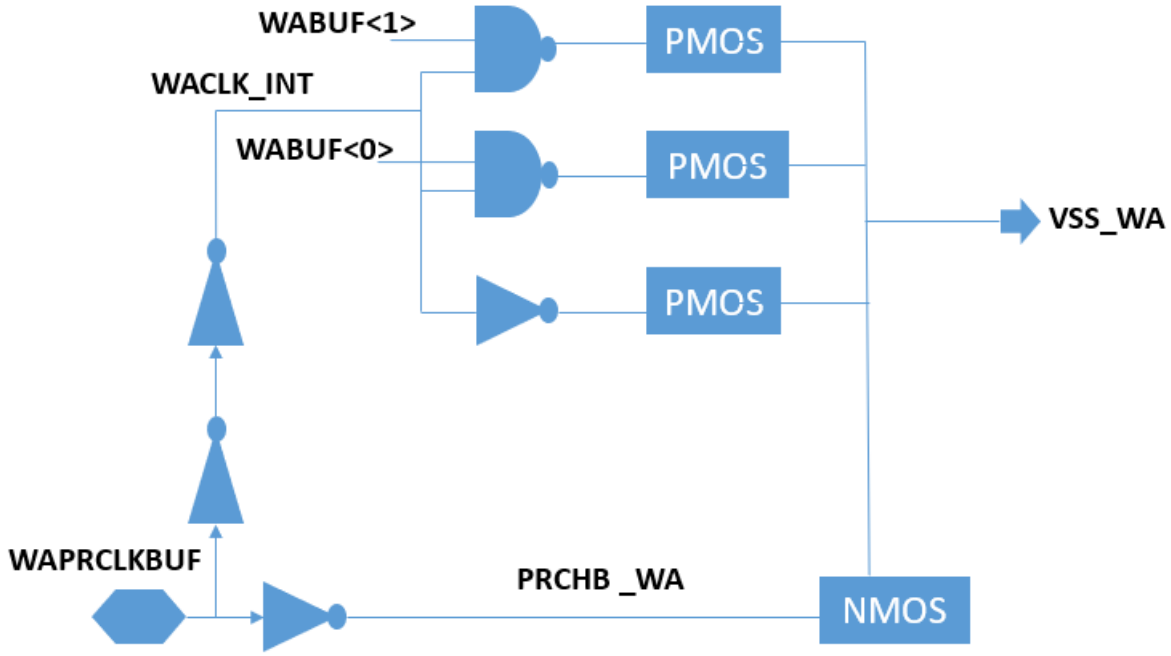


Figure 2.6: Write Assist Circuit

Chapter 3

Basic SRAM

6-T SRAM Bit cell

- Read operation
- Write operation
- Iread
- Ileak
- Write Margin
- Flip time
- Static Noise Margin
- Bit cell device sizing
- Cell ratio

Bit cell of 6T-SRAM:

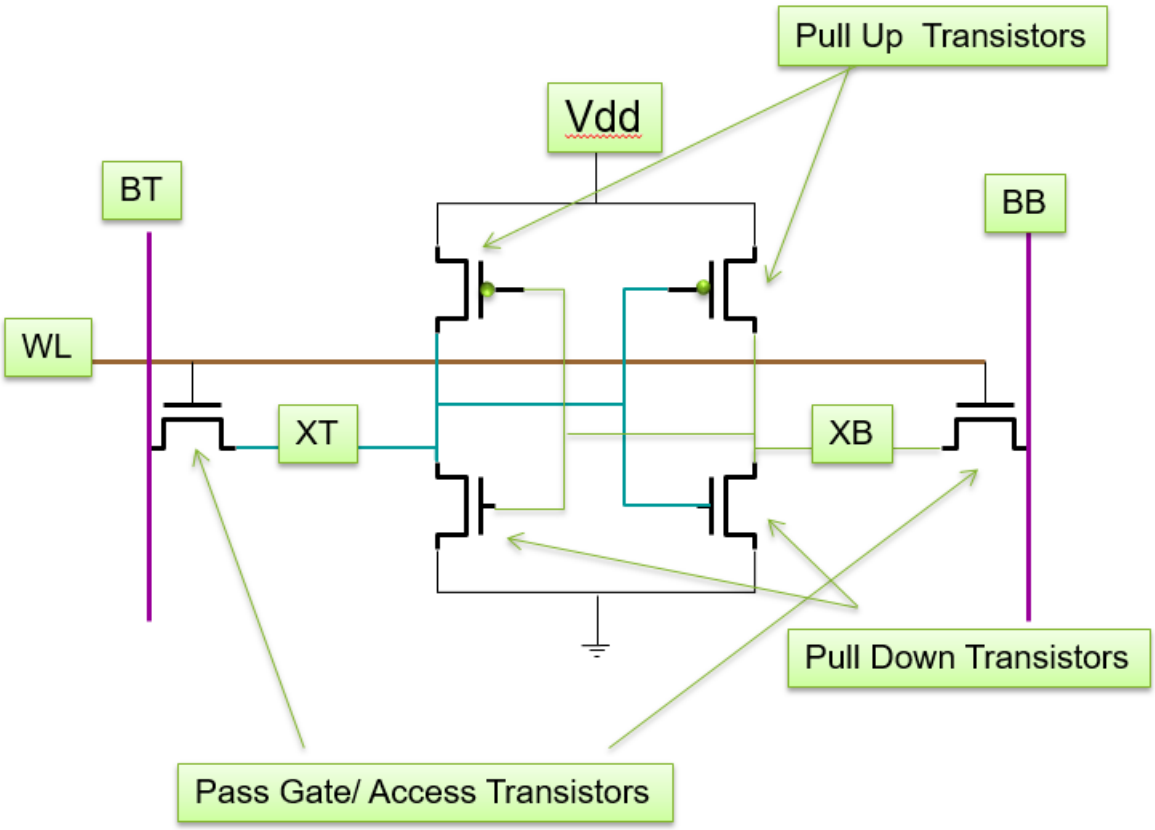


Figure 3.1: Bit cell of 6T-SRAM

3.1 6-T SRAM Bit cell Read Operation

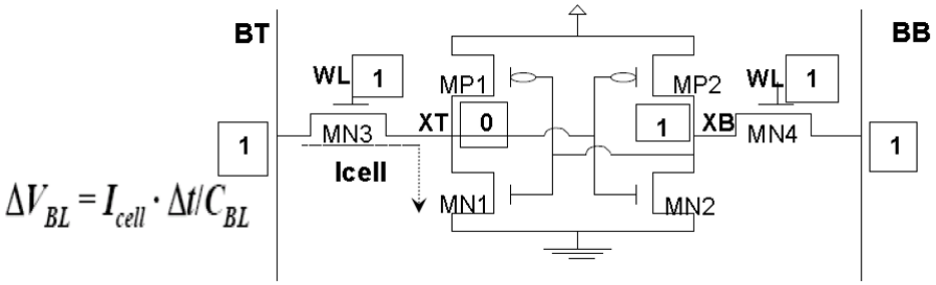


Figure 3.2: Basic 6T- SRAM for Read Operation

- Voltage at node XT should not exceed threshold voltage of MN2
- Pull down stronger than pass gate to meet above criteria.
- Sizing can be decided by equating currents through pass gate MN3 and pull down MN1
- MN1: linear MN3: Saturation

VBL sensed at SA and amplified by SA to be resolved for 0 or 1.

3.2 6-T SRAM Bit cell Write Operation

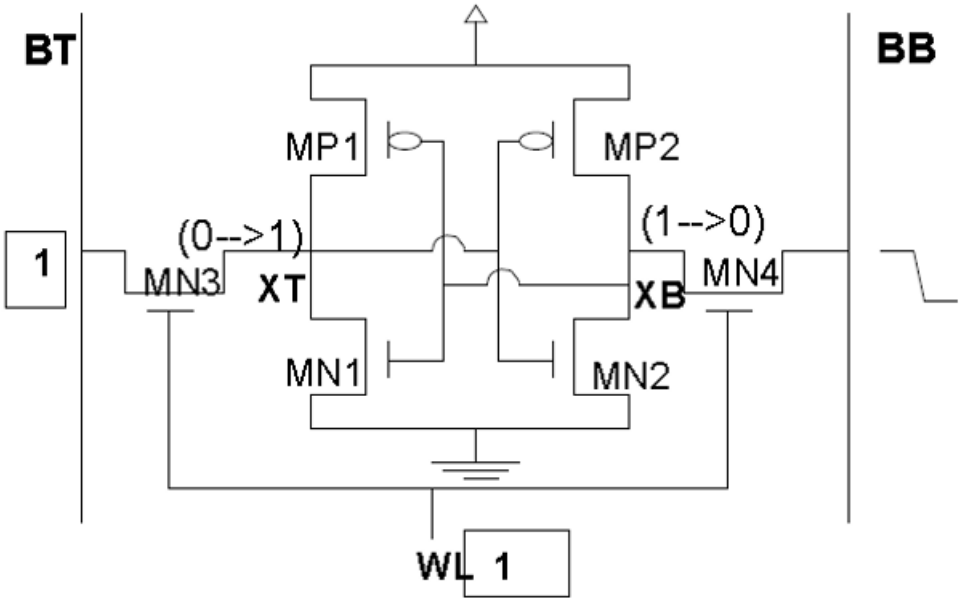


Figure 3.3: Basic 6T- SRAM for Write Operation

- Conductance of pass gate must be larger than pull up so that drain of MN2 is pulled down below switching threshold voltage of inverter.
- Size is determined by pulling drain of MN2 to VT of transistor of MN1 and equating current through pull up MP2 and pass gate MN4.
- MP2: Saturation, MN4: linear

3.3 CLK to WL generation flow:

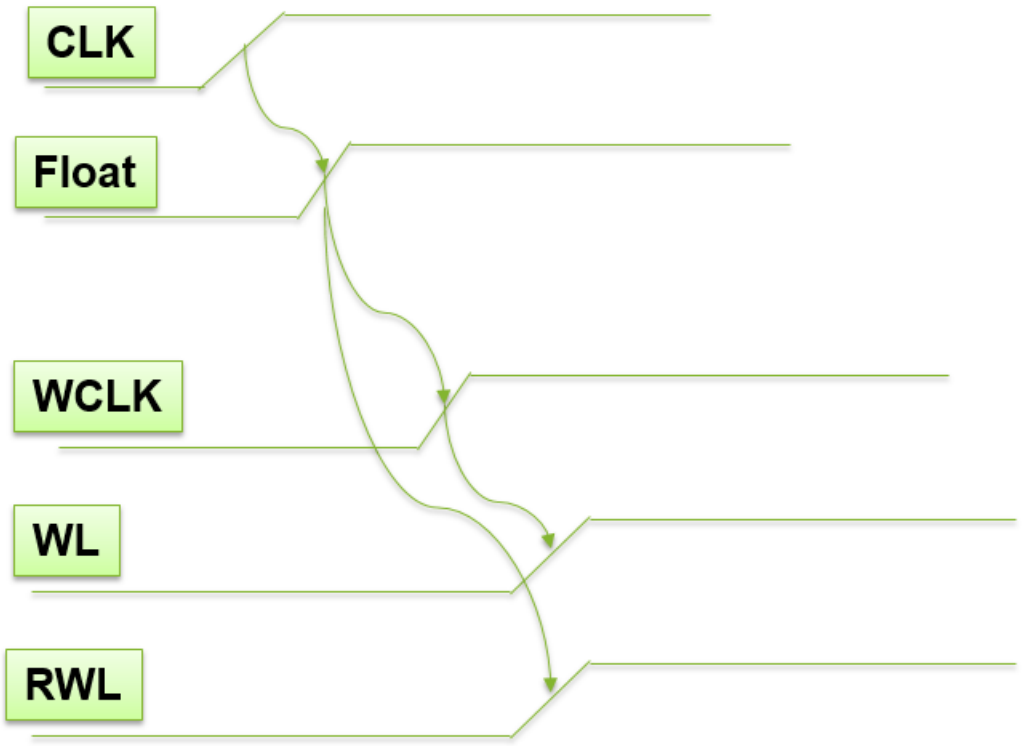


Figure 3.4: CLK to WL Flow

3.4 Read Cycle:

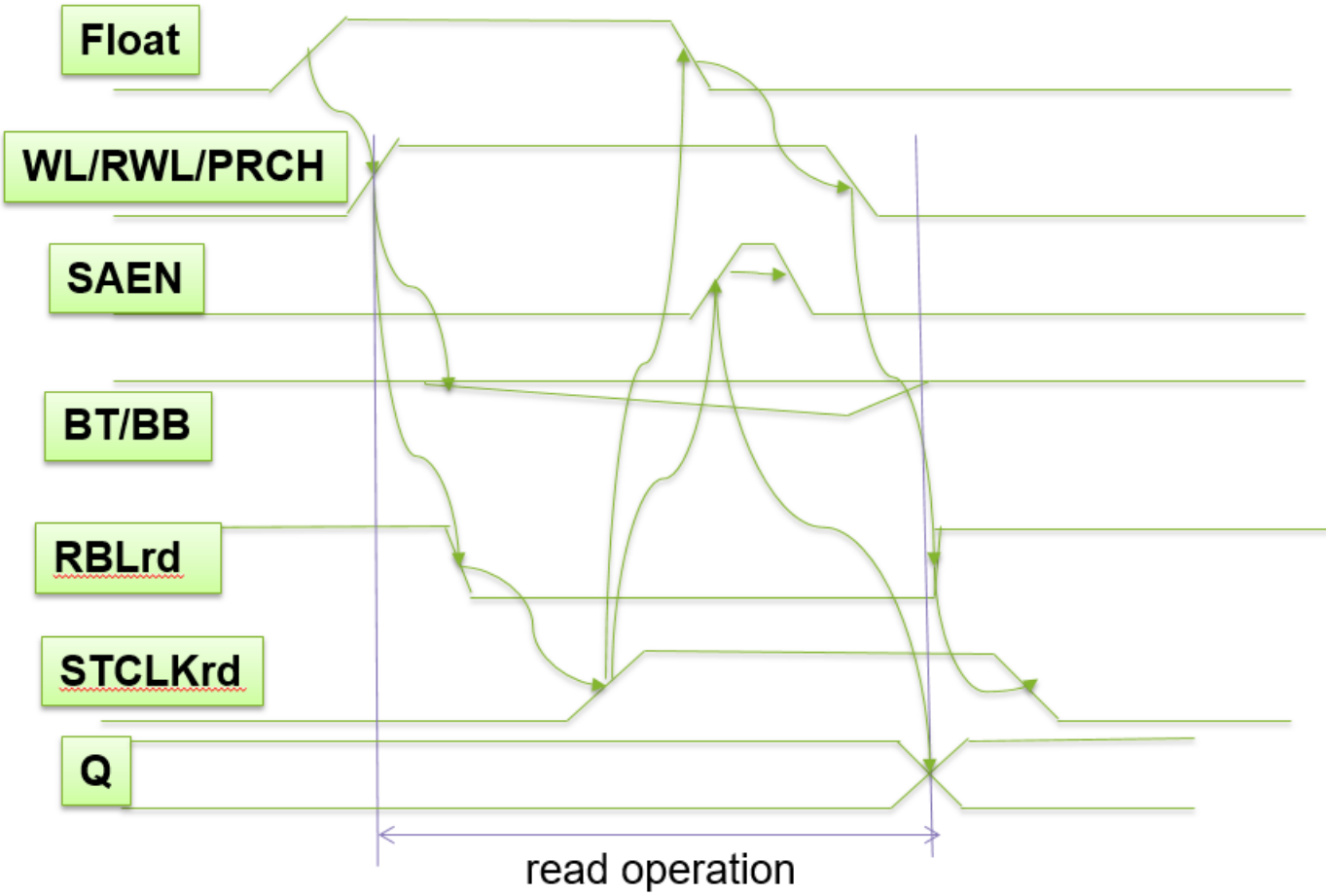


Figure 3.5: Read cycle during Read operation

3.5 Write Cycle:

Figure 3.6: Write cycle during Write Operation

3.6 6T-SRAM Bit cell Read Current (Iread):

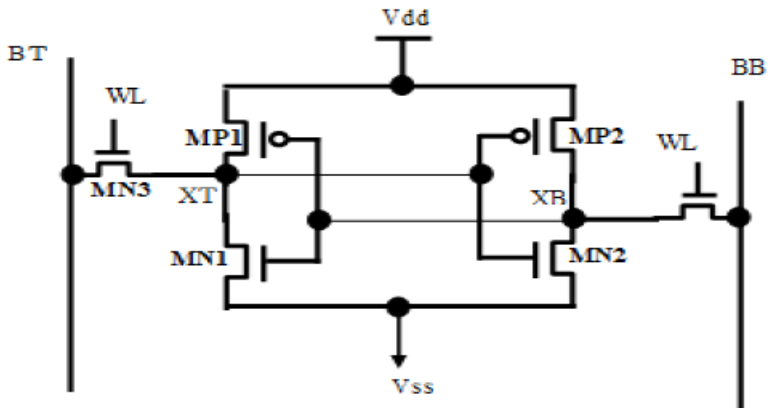


Figure 3.7: 6T-Bitcell Read current setup

- Defines speed of memory read operation.
- Determined PG and PD devices.
- Method (DC characterization)
- XT is initialized to 0.
- XB is initialized to Vdd.
- WL is at Vdd.
- BT is at Vdd.
- BB is at Vdd.
- Iread = current through the pass gate next to node storing 0 (device MN3 in figure)
- Iread Causes Discharge of BT/BB, which is fed to SA through Read mux and thus Bit cells content gets sensed in SA and resolved to toggle output Q.

3.7 6-T SRAM Bit cell Leak Current (Ileak):

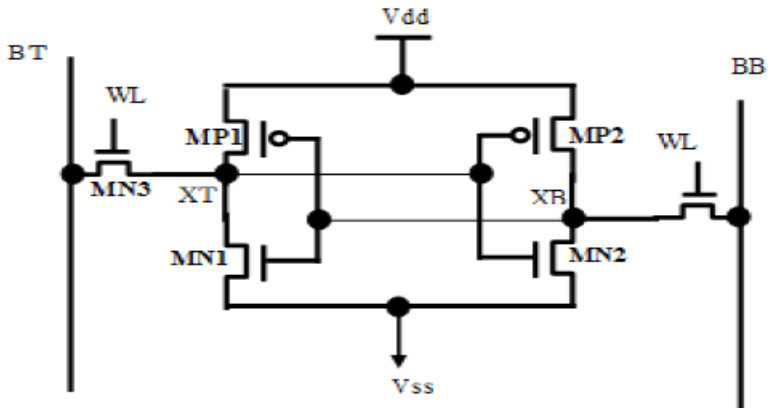


Figure 3.8: 6T-SRAM Leak Current Set-Up

- Ileak is characterized to get maximum number of bit cells that can be supported per column. Since only one-bit cell will be activated during read operation in each column, so rest of the rows 1 bit cells will be in OFF state and deteriorating read operation by giving leak current.

- Ileak is determined by PG device.
- Method (DC characterization)
- XT is initialized to 0.
- XB is initialized to Vdd.
- WL is at 0 (OFF).
- BT is at Vdd.
- BB is at Vdd.
- Ileak= current through the pass gate next to node storing 0 (device MN3 in figure)
- We generally keep Ileak ¡ Iread (max_rpb_support x 10)

3.8 6-T SRAM Bit cell Worst Ileak current:

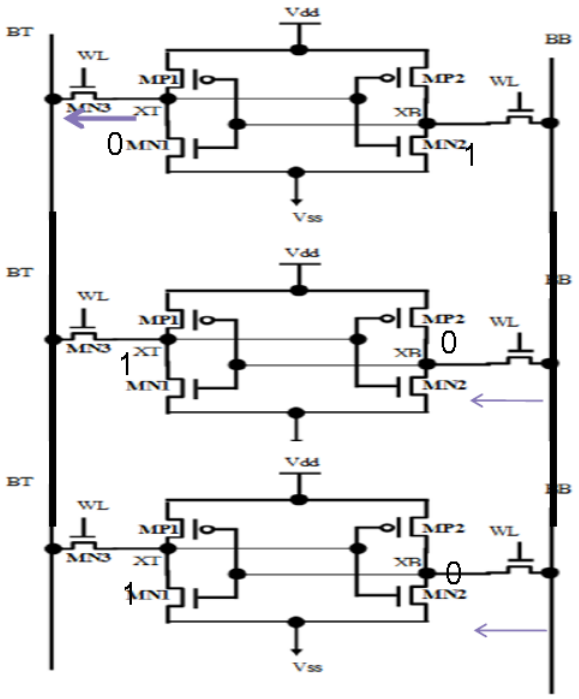


Figure 3.9: 6T-SRAM Worst leak current set-up

In this worst case example, BT is being read and worst leakage current is fed to BB, which will tend to kill Vdiff being fed to SAs internal nodes and thus Read operation will get slowed down.

3.9 6-T SRAM Bit cell Write Margin (WM):

- Write Margin is measured setting WL/BT to Vdd and applying step down stimuli to BB, BCs internal nodes are continuously monitored, and VBB is noted when XT/XB trips.
- WM is Highest level of Bit line to ensure cell flip with WL at Vdd (BL Driven write).
- Or lowest level of WL to ensure cell flip with Bit line at 0.

WM = VBB@XT_XB_trips 5% of Vdd (-5% of Vdd is kept as margin due to IR drop on Vss line)

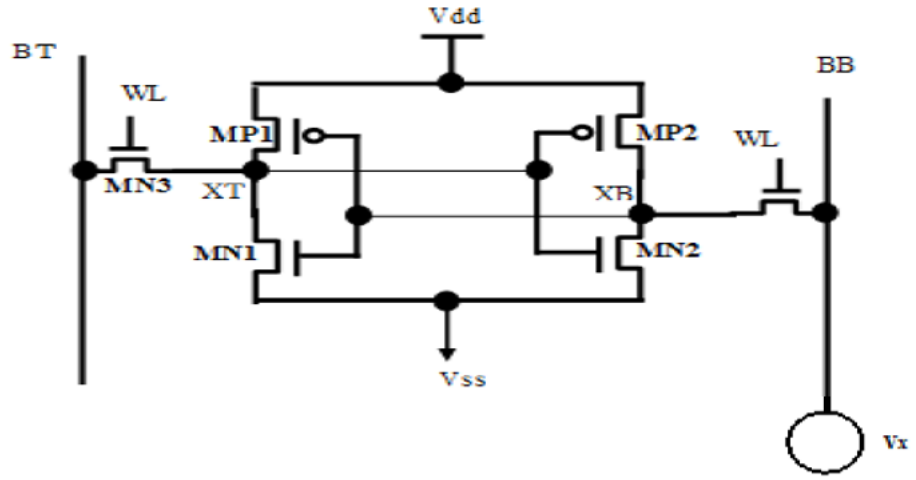


Figure 3.10: 6T-SRAM Write Margin Set-Up

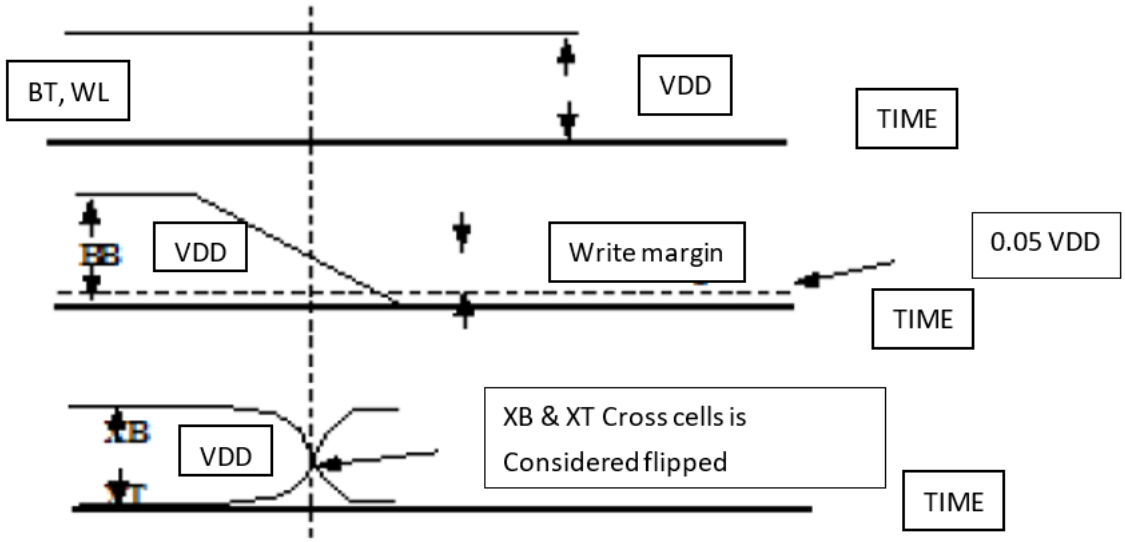


Figure 3.11: Waveform of WM

3.10 6-T SRAM Bit cell Flip Time (BL Driven):

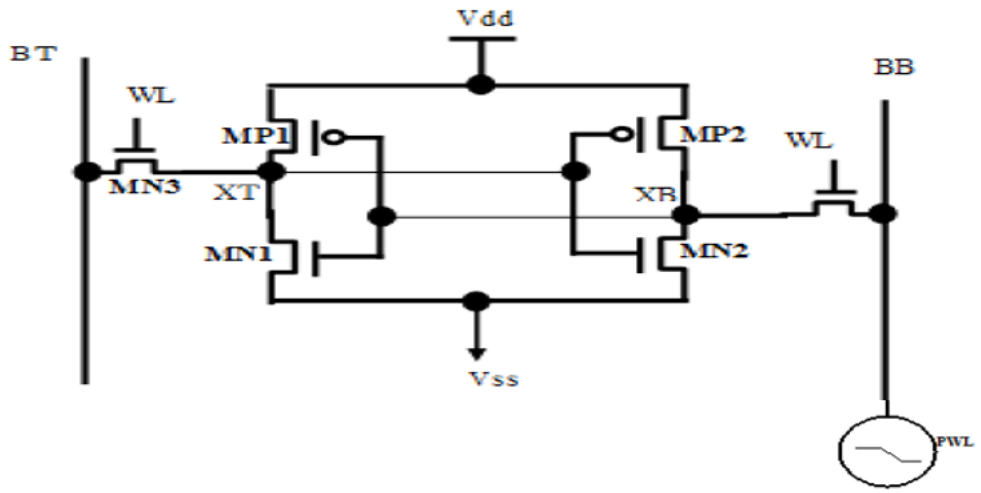


Figure 3.12: Flip Time set-up

- Bit line driven Write Flip time is measured with WL in stable ON state and BT/BB is given the stimuli.
- Method:
  - Xt is initialized to low means 0.

- Xb is initialized to high means Vdd.
- Wl and Bt are at Vdd.
- Bb is transiently varied from high means Vdd to low means 0 using PWL function.
- Flip Time = MAX (T1, T2)

Where:

T1 = BB_fall_50%_to_XT_rise_95%_of_Vdd

T2 = BB_fall_50%_to_XB_fall_5%_of_Vdd

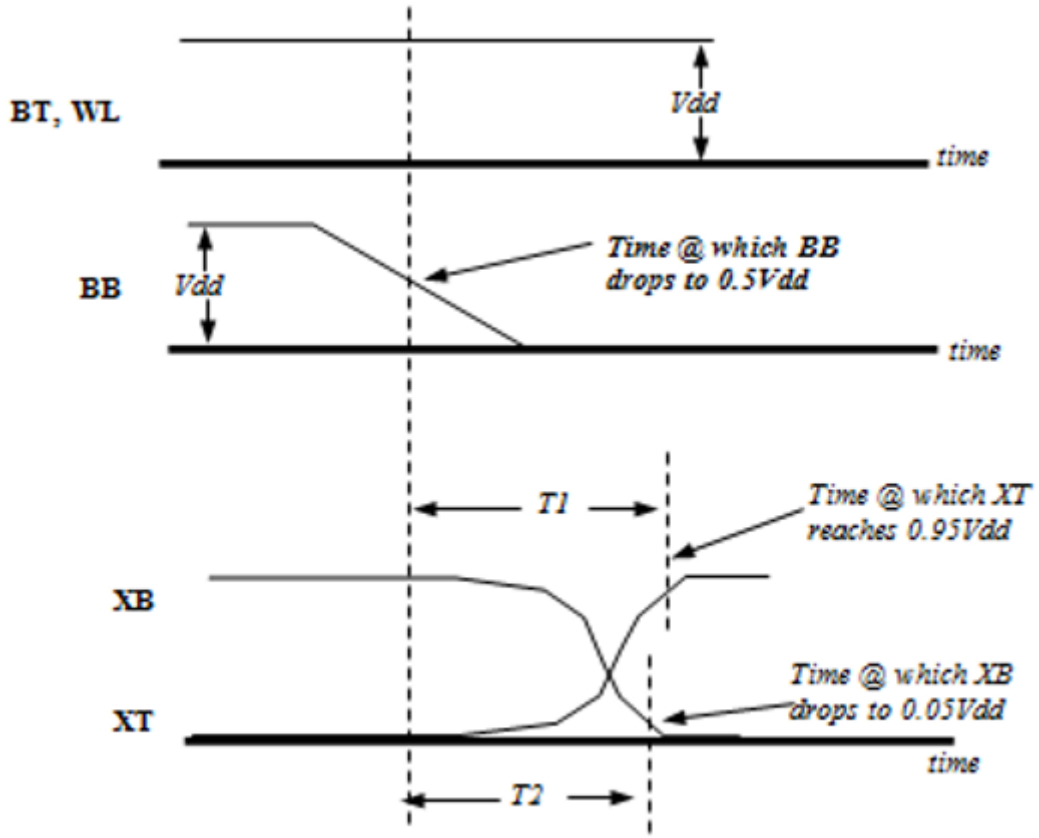


Figure 3.13: Waveform for (BL Driven)

3.11 6-T SRAM Bit cell Flip Time (WL Driven):

- Word line driven Write Flip time is measured with BT/BB in stable state and WL is given the stimuli.

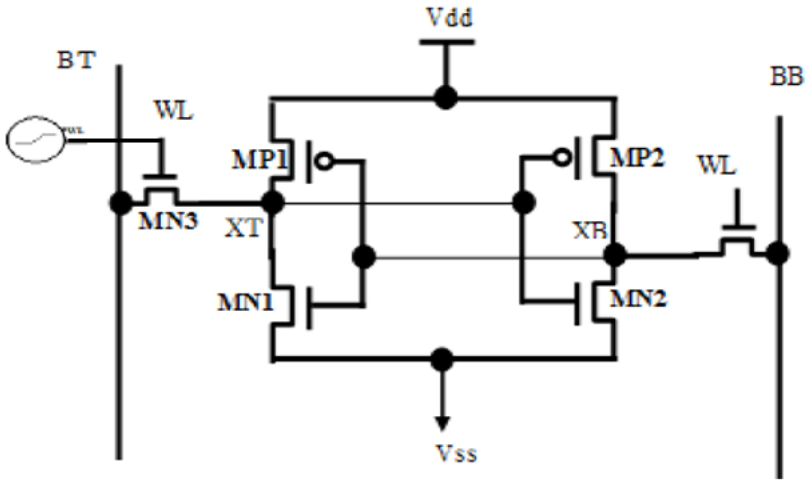


Figure 3.14: 6T-SRAM Flip time setup (WL Driven)

- Method:
  - Xt is initialized to low means 0.
  - Xb is initialized to high means Vdd.
  - Bb is connected to 0.
  - Bt is at Vdd.
  - Wl is transient signal going from 0 to Vdd using PWL function.
  - Flip Time = MAX (T1, T2)

Where:
T1 = WL_rise_50%_to_XT_rise_95%_of_Vdd
T2 = WL_rise_50%_to_XB_fall_5%_of_Vdd

3.12 6-T SRAM Bit cell Static Noise Margin:

- During Read operation a potential divider between PG and PD tend to raise potential of BCs internal node (storing 0), which when mixed with some static noise may flip the contents of the cell leading to SNM failure.
- Method:

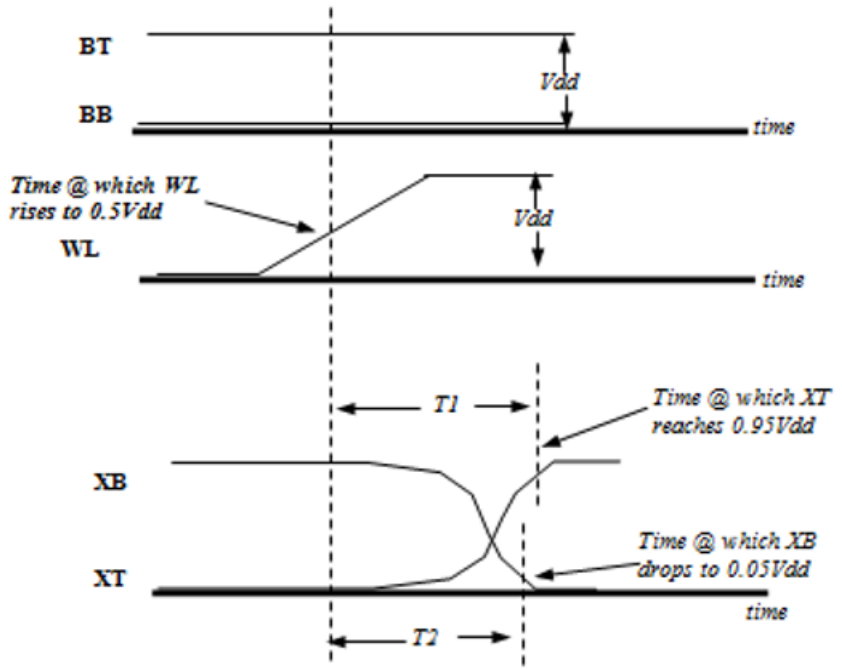


Figure 3.15: Waveform (WL Driven)

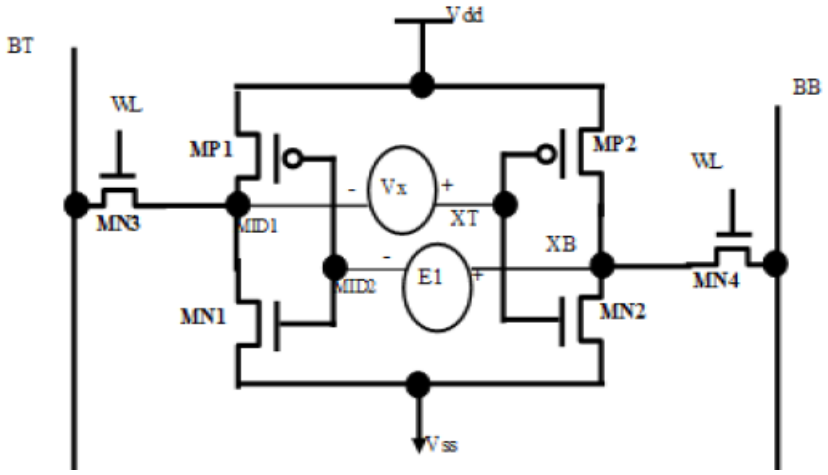


Figure 3.16: 6T-SRAM (SNM Set-Up)

– Wl, Bt, Bb are at high meand Vdd.

– Xb is initialized to Vdd.

– Xt is initialized to 0 and Xb to high means Vdd.

– Slowly increase Vx from 0 and monitor MID1 and Xb to see when cell flips.

SNM = Value of Vx, when cell gets

Chapter 4

Memory Architecture

In this case I observed our bit cell size, ration of our MOS, then which MOS is in which region that all analysis I did. Then I see different architecture so for that so many things are different like memory architecture. For that I did instance vice summary, I got data for that and I compared all data with reference compiler data and then I looked float generation, latch, decoder method, pre-decoder, x-decoder, read and write all that things I done in memory architecture.

4.1 6-T BITCELL:

4.1.1 Array-Structured Architecture:

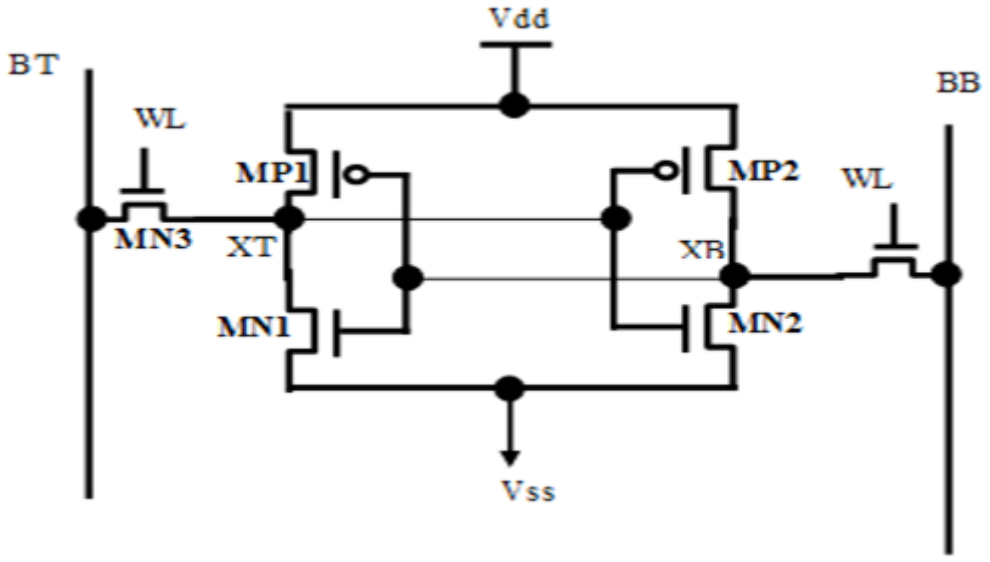


Figure 4.1: Basic 6T-SRAM Array Structure Architecture

4.1.2 Decoding scheme-based Architectures:

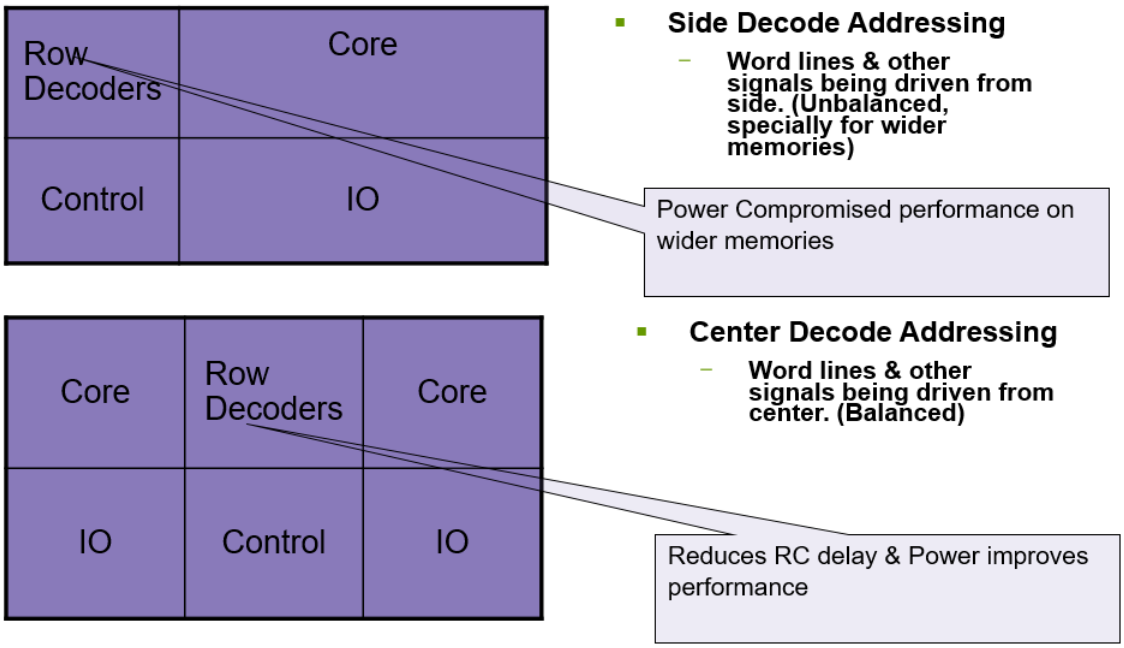


Figure 4.2: Decoding Address in Memory Architecture

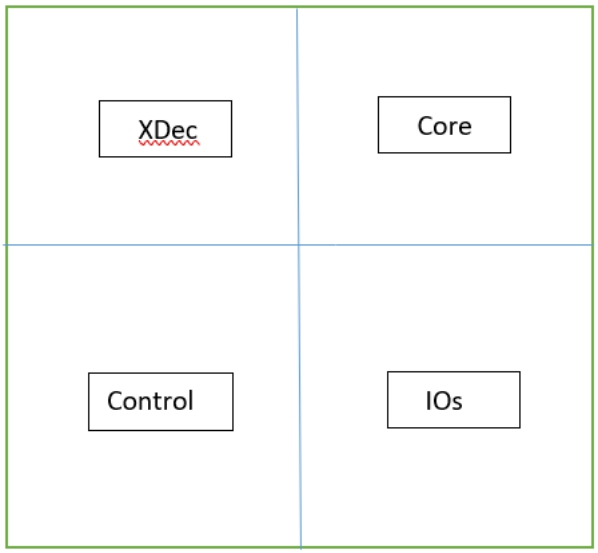


Figure 4.3: Basic Memory Architecture with Word and Bit

Word	1
Bits	1
Memcells	= (word x bits) =1
IOs	Bits=1
Row	Words=1
Column	Bits=1

Figure 4.4: Memory information

Size of memory: Nw x Nb

- Nw= Rows * Mux
- Nb= column/ Mux

Figure 4.5: Memory Size

Words	8
Bits	4
Memcells	= (words x bits) =8 x 4=32
IOs	Bits=4
Raw	Words=8
Column	Bits=4

Figure 4.6: Size of Memory

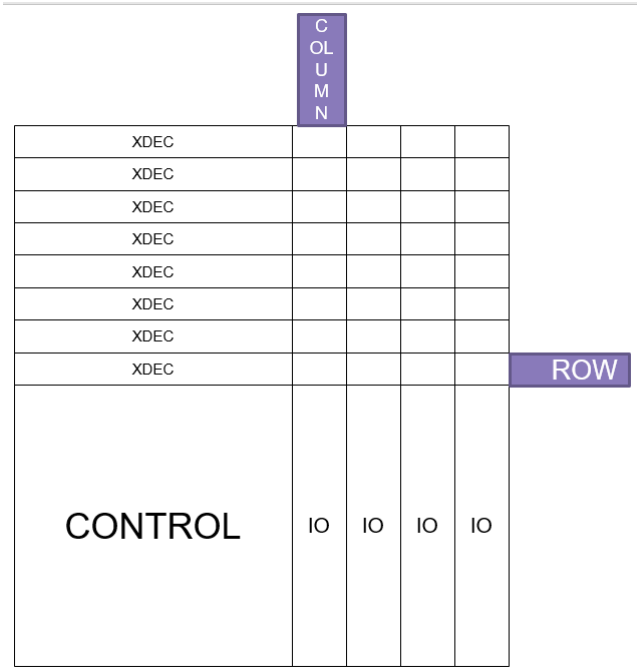


Figure 4.7: Apply Size after Design

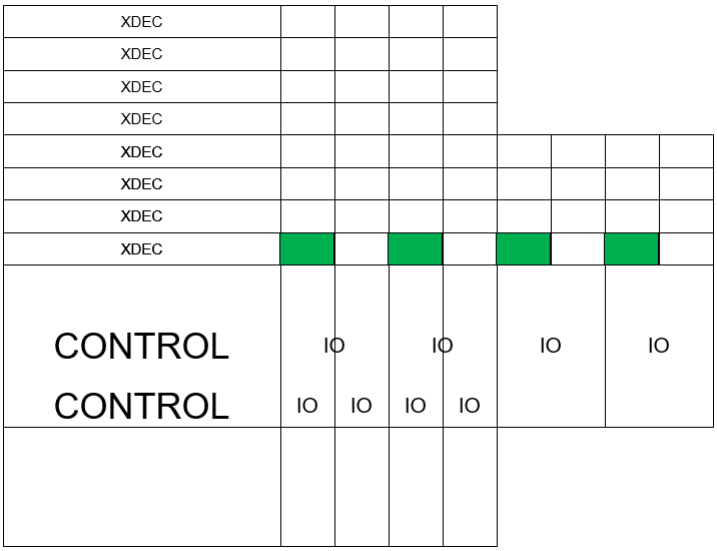


Figure 4.8: Apply CM after Design

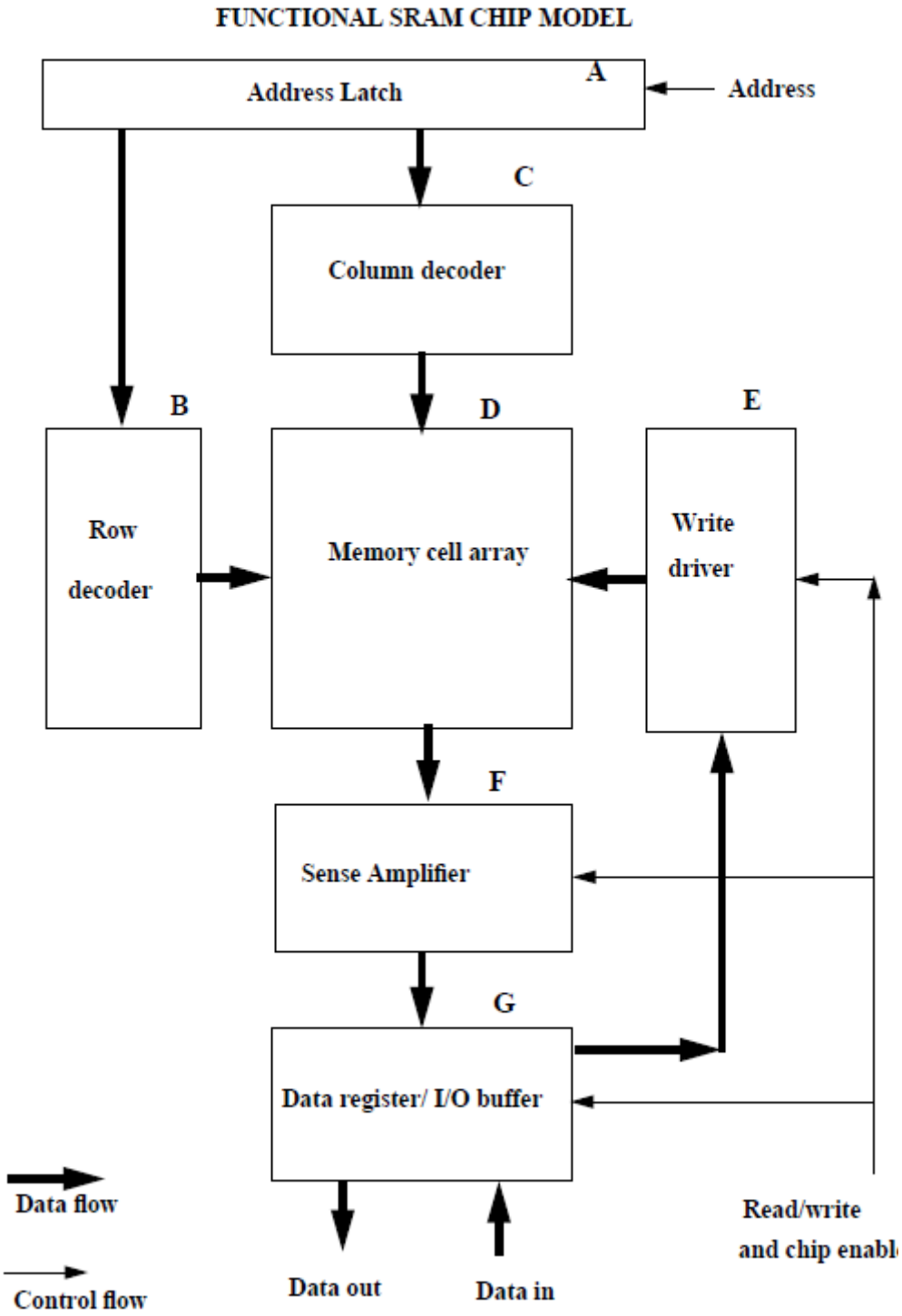


Figure 4.9: Functional Block Diagram of Memory

- Waveform

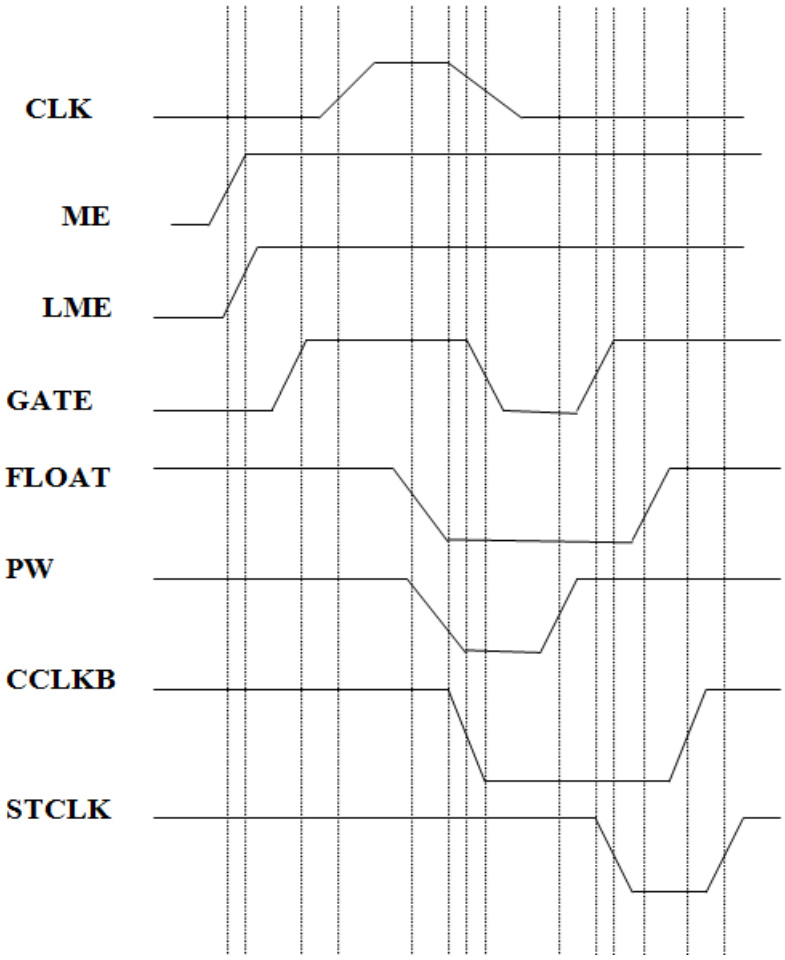


Figure 4.10: Waveform of Memory

4.2 STCLK and SAE generation:

Some reference is needed to generate STCLK / SAE when required bit line differential has developed?

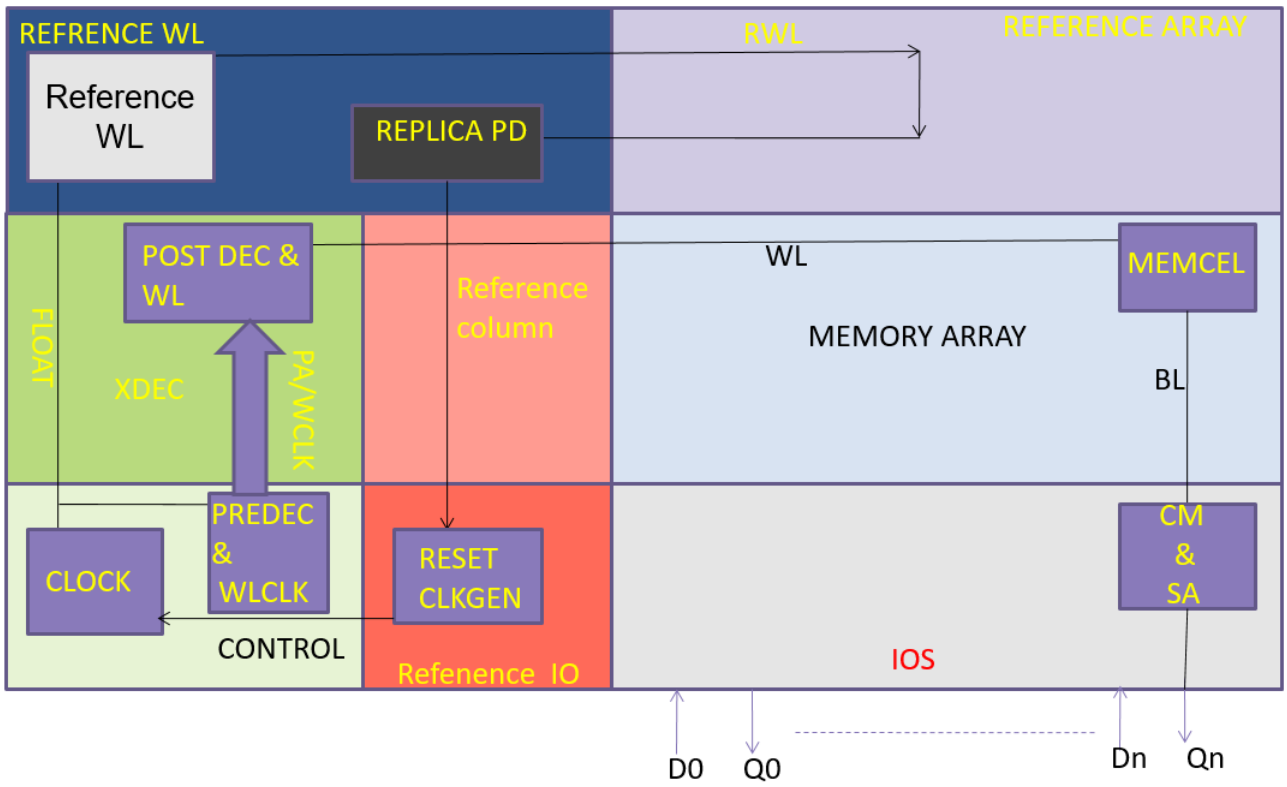


Figure 4.11: Block diagram of STCLK and SAE Generation

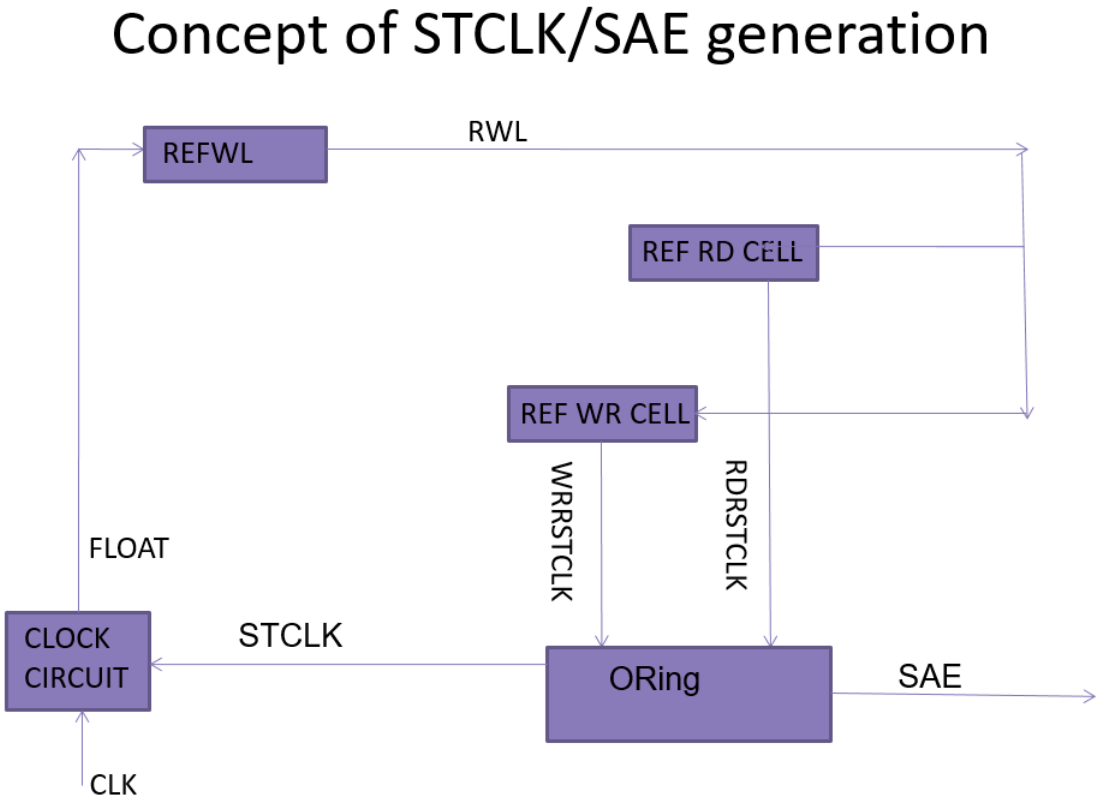


Figure 4.12: Signal Flow of STCLK/SAE

4.3 Read Margins:

The Read Margin (RM) pins let your trade-off between speed and robustness. Use the RM pins to set the time to strobe the sense amplifiers. The bit lines Bt and Bc are precharged before accessing a cell of memoty.

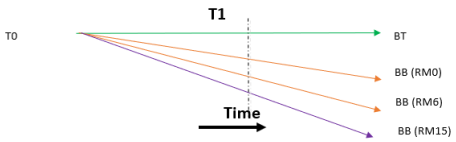
When the cell of memory is accessed, it produces a differential signal between the Bt and Bc that takes time to develop. The differential signal is fed to the sense amplifier.

The more time allowed for signal development, the easier it is for the sense amplifier circuit used to checked the difference or read the data which is stored in internal node. The time allowed for signal development directly impacts access time. So, you can use the RM feature to trade off access time for memory robustness.

Set of 4 pins RM [0:3], helps control self-timing in the memory, by adding the different numbers of pull down on reference bit lines. These could be also custom based on design requirements.

RM	RM3	RM2	RM1	RM0	Pull downs
0	0	0	0	0	1 (or 2, as required default, i.e. fixed)
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	1	1	0	0	12
13	1	1	0	1	13
14	1	1	1	0	14
15	1	1	1	1	15

Figure 4.13: RM Setting for Read Margin



RM	Differential @ T1
0	70 mV
6	150 mV
15	225 mV

Chapter 5

Compiler Characterization and Evaluation

In compiler there is one central data base file which includes all timing and power related information. This file is called as a compiler.cdb file. In these two processes in memory compiler design.

- Characterization
- Evaluation

5.1 Characterization

To describe the actual behaviour of a circuit in Real time. In Real time condition following things affected:

- Process
- Voltage
- Temperature

In this characterization, simulation was done on particular instance and all things which are write above related measurement are done. This all information is dump into compiler.cdb file. This simulation is called as instance characterization. Below figure is for instance characterization.

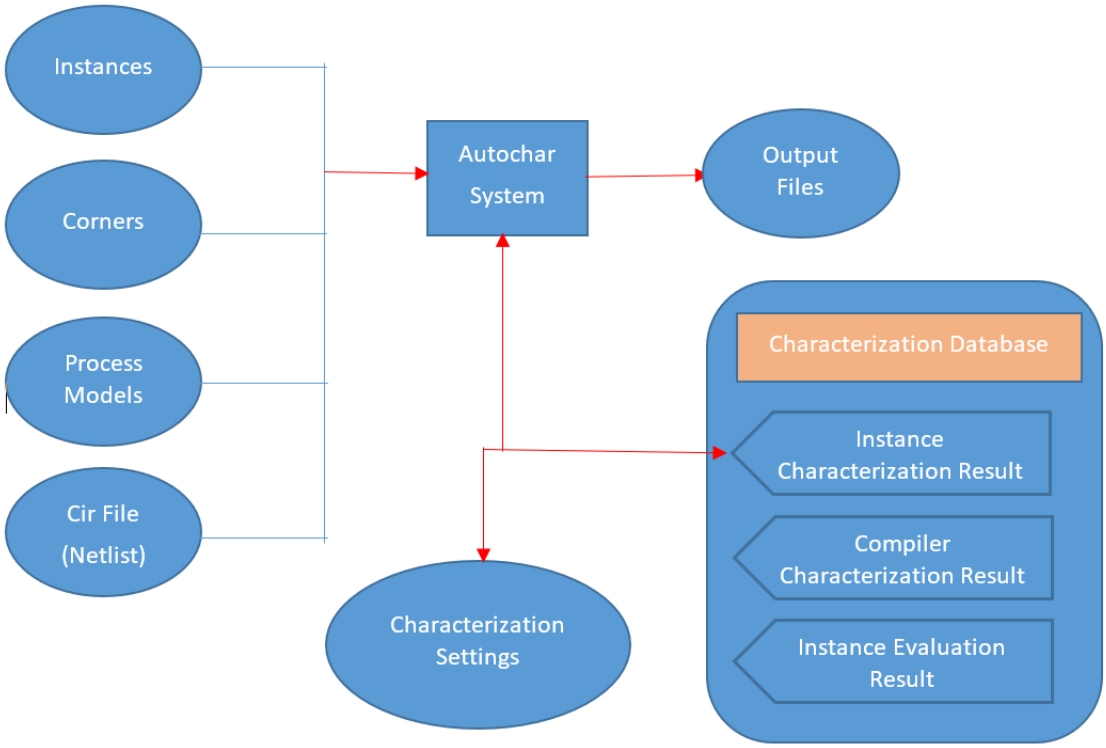


Figure 5.1: Block Dig. of Instance characterization

Before Quality Assurance (QA) analysis compilers whole instances are characterized. So, that type of simulation is called is Compiler Characterization. Below figure explain about Compiler Characterization.

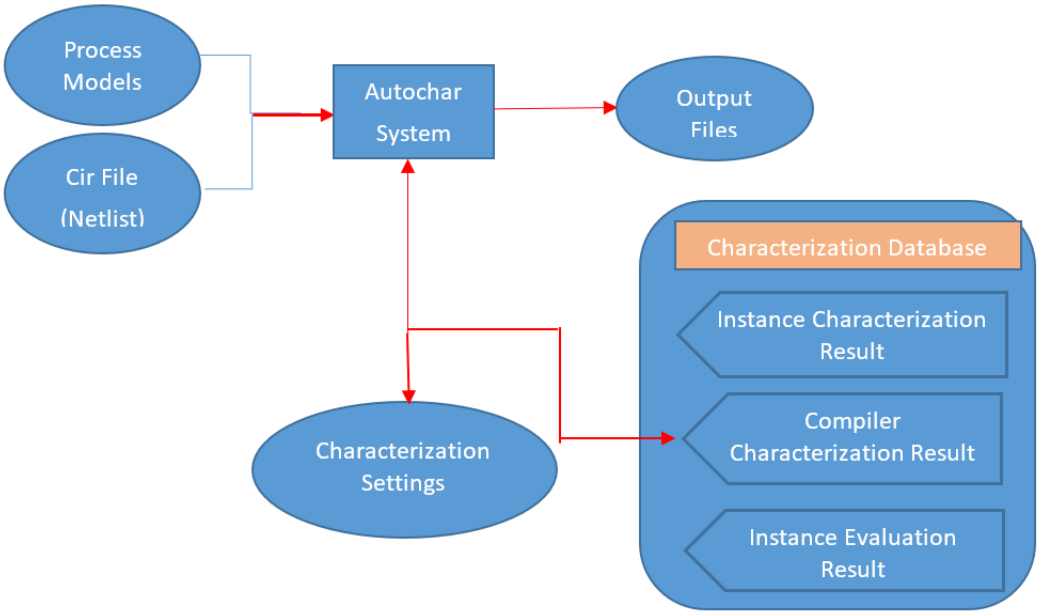


Figure 5.2: Compiler Characterization Flow

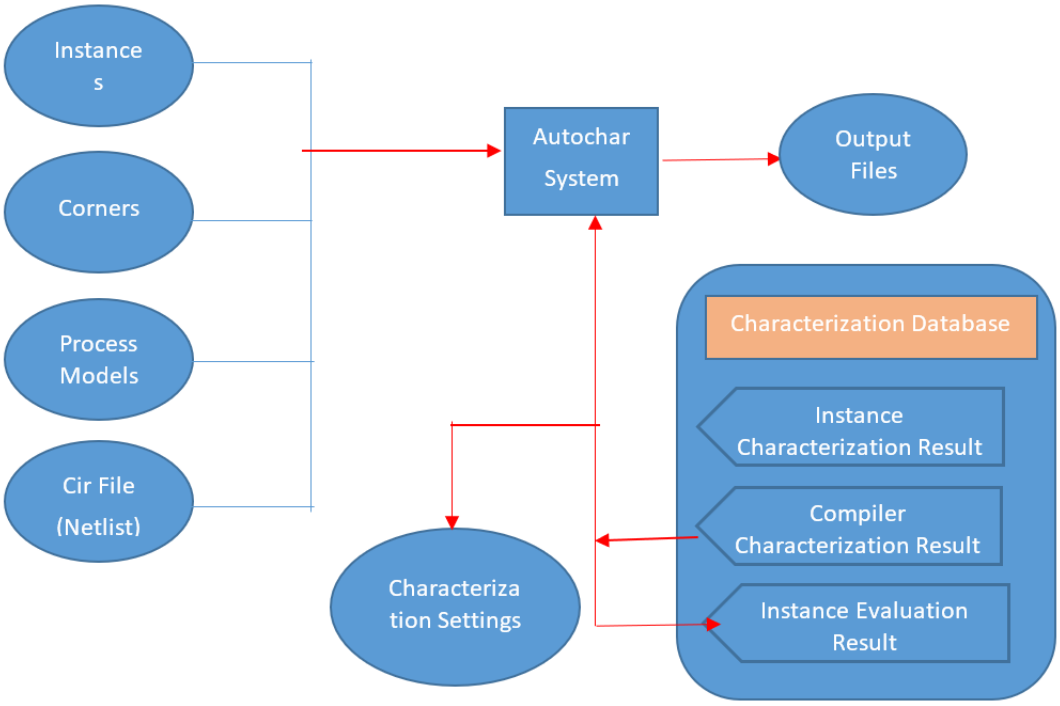


Figure 5.3: Evaluation Flow

5.2 Evaluation

In instance evaluation output is coming from compiler characterization result. That is only compiler characterization information based on evaluation only. Above figure is for instance evaluation flow. In compiler characterization result if particular instance information is not available than it gives result from interpolation by taking of nearby instance characterization results.

5.3 Quality Assurance of Memory Compiler

To check quality of designed compiler for that following QA checks done on compiler before release.

5.3.1 Primetime

It is used for timing analysis. It is Verilog model verification. This command checks the Synopsys library syntax and ensures the timing arcs defined in the Synopsys library exist in the Verilog model.

Synopsys model vs. Verilog model verification. It reads Synopsys library using Prime

Time, produces an SDF file and back annotates the Verilog with the SDF. It also checks the Synopsys library syntax and ensures the timing arcs defined in the Synopsys library exists in the Verilog model.

Run Command: pipe -f Primetime.tcl -v Primetime -r PrimetimeReport >& log &

The PrimeTime plugin tries to accomplish the following tasks: -
1. It checks all the options provided and exits if the option values are not valid.
2. It creates directory structure by looking into user supplied options.
3. It copies/creates the required files into appropriate locations.
4. It creates command/run file and executes it.
5. The plugin creates different run scripts into simulator directories.
6. If enabled, it creates quick result files based on simulations at the location -

/run directory/compout/primetime/lc_report
/run directory/compout/primetime/pt_report
/run directory/compout/ primetime/simulator/_report

7. The plugin collects all the log file generated by different tools and scans them for errors and warnings and generated different report files. These are:

/run directory/compout/primetime/instance name/PVT/simulator/inst_report
/run directory/compout/cover_report

5.3.2 Libscreen

It is to check monotonicity or variation of the liberty the data. This check verifies the slope of the timing arcs. Synopsys model monotonic checks. It performs Synopsys input slope and output load dependency timing checks.

LIBSCR provides checks for:

- Monotonicity Checks

horizontal: Values are ascending or descending within the defined tolerance from left to right. vertical: Values are ascending or descending within the defined tolerance from top to bottom.

- Delta Checks for Slope vs. Load tables
  The slope between consecutive entries in the table is compared against every other slope in the same row. Check that each slope is less than the last slope in the row to within the defined tolerance.

- KTd checks for Slope vs. Load tables
  The slope between consecutive entries in the table is compared against every other slope in the same row. Check that each slope is less than the last slope in the row to within the defined tolerance.

Run Command: pipe -f Libscr.tcl -v Libscr -r LibscrReport >& log &
Check LIBSCR.options file present in run directory to learn more about libscr run.

5.3.3 Timever

It is used for check the Hold-time and Set-Up time in our design and also check the cycle time and all things in timever. Also check the margin and delay also in design.This check adds timing parameters to the Verilog and checks for read/write setup/hold, tcc on the Verilog.

5.3.4 Libcompare

It will compare the datasheet between compiler version which is given in tcl file. It will compare power, timing and area between two compilers and it reports the percentage deviation in the above-mentioned parameters in XLS format.

5.3.5 Espcv

It is formal equivalence check between Verilog model and a structural model created by tool for verify functionality. ESP-CV is check between behaviour vs. functional level design. It will also check the Set-Up time and Hold-Time in design also check Tcc. Also check the verilog file and check delay part in design.

Innologic Verification for functional equivalence of two different design representations Verilog and structural.

Run Command: pipe -f Espcv.tcl -v Espcv -r EspcvReport >& log &

Espcv also provides an option to run any one or more of the following verification flows:

1. func.v vs. behavioral model (default).
2. RTL vs. behavioral model. The plugin automatically picks up _rtl.v if it is present or uses +VIRAGE_FAST_VERILOG if rtl.v is not present.
3. Ikos vs. behavioral model.
4. Verilog fast model vs. behavioral model.

5.3.6 Funcver

Run Verilog functional verification on memory instances. Before running Funcver selects between the Verilog models and VHDL models in TCL file. To run simulation on both Verilog and VHDL models, set the value to both. It expects the existence of std_cells.v file for simulation and exists if it can not locate the file.

Run Command: pipe -f Funcver.tcl -v Funcver -r FuncverReport >& log &

5.3.7 Prescreen

It is to create Layout vs Schematic and Design Rule Check report for corner instances. It is basically checking the layout part error. It helps in generating the Prescreen information (Like Mini QA for BE Mini QA on Functional timing checks and much more) by generation, verification and reporting for Synopsys compiler.

5.3.8 FamilyVerify

It is reports for whole compiler means reports for all the files and corresponding errors. Also check the compiler structure. Compiler family validation tests are intended to assure quality of a compiler before it is released. Normally, you run family validation if you want to Validate that an existing compiler conforms to one or more family definitions Update an existing compiler to force it to conform to one or more family definitions Create a new compiler that is already conforming to one or more family definitions.

FamilyVerify is run to assure quality of a compiler before it is released. It checks the

difference in compiler files, library files, templates and other files with respect to standard repository and report error in case of mismatch. Check for any zero size file or linked files in compiler area.

Run command: pipe -f familyverify.tcl -v familyverify >& log &

5.3.9 IQA (Integrated Quality Assurance)

It is the integrated QA. It will check whole compiler. It checks Library Vs db , Pins transition etc for corner instances. It ensures the quality of instances before the compilers are released. The IQA check also include the capability to ensure that antenna diodes are always present. Transistor recognition is performed so that a given piece of diffusion geometry can be recognized as a source or drain to a gate. If it is not a source drain, it is a diode and is recorded appropriately.

Integration Quality Assurance (IQA) checks ensure the quality of instances before the compilers are released.

Run Command: - pipe -f Iqa.tcl -v Iqa -r IqaReport >& log &

IQA include the following procedures: -

1. checks for GDS parameters: -
- GDS vs CFG files layers consistency
- no duplication in cell name, instances in a cell
- VSIA tagging information is present

2. Checks for LIB vs PLEF/DS/TLF consistency: -
- Cell name area match.
- Pin name, pin direction match.
- Timing numbers are in order.

3. Checks for Plef pins: -
- Pin is on boundary, Pin is on routing grid.
- There is no geometry with negative coordinates.

4. Checks for Synopsys Liberty Files.
5. Checks for instance files for foundry.
6. Checks for MiniArray and CIR parameters.

5.3.10 Vxl

- Verilog Behavioral model verification of the memory instances.
- From pf file it generate func.v and inst.v. func.v is function verilog, and inst.v is behavior verilog. From template it generates stim and compares both verilog models.
- Func.v is actual design simulation while inst.v is behavior model simulation. Inst.v contain all timing values from cpj, so if this check fail we have to check/ update pf file.

Run Command: - pipe -f Vxl.tcl -v Vxl -r VxlReport >& log &

5.4 Summary

This chapter is about instance characterization and instance evaluation of compiler design. How it will be carried out that things cover in this chapter. It will also include various quality checks which are check before and after release compiler and prior to hand over customer to maintain

Chapter 6

Read and Write Assist technique

In SRAM basic two operations are there.[2]

1) Read operation

2) Write operation

1) Basic Read operation in SRAM:

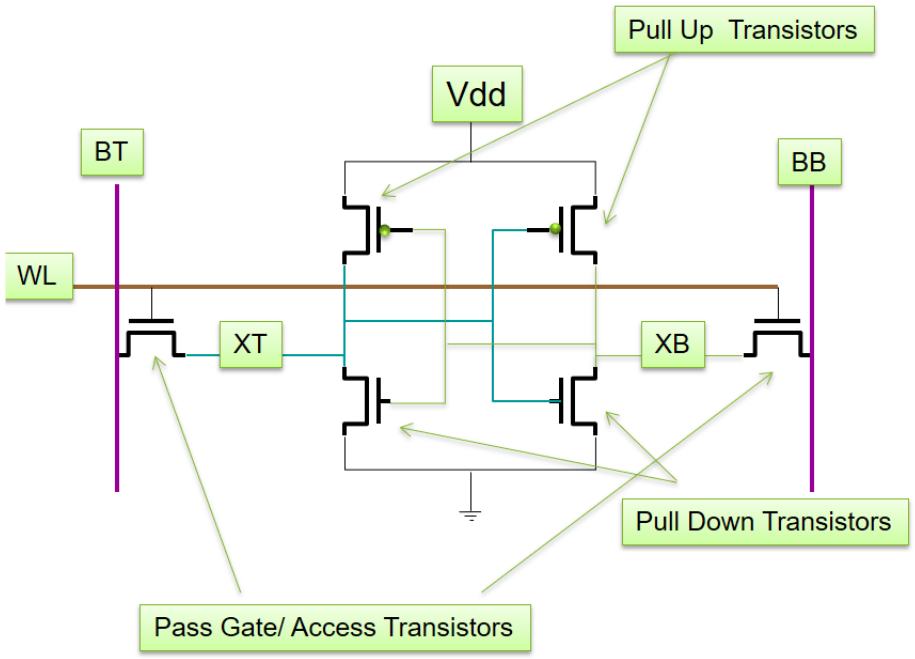


Figure 6.1: SRAM Set-Up

- XT is initialized to 0.

- XB is initialized to 1.
- WL is at VDD.
- BT is at Bit line voltage.
- BB is at Bit line voltage
- BB and BT initially pre-charged.
- BT discharged and sense 0.
- BB remain at VDD.

2) Basic Write operation in SRAM:

- Write operation is accomplished by forcing one-bit line, either BL or BL low while the other bit line remains at about Vdd.
- The cell is designed such that the conductance of N4 is several times larger than P2, so that drain of N3 is pulled below Vs (switching threshold).
- This creates a regenerative effect between the two inverters and changes state of the bit cell.
- Eventually the node Q forces the transistor N1 to turn off and node Q is pulled up by transistor P1 and at the same time N3 turns on and helps N4 in keeping the node low.
- Then the WL can be returned to its original standby level.

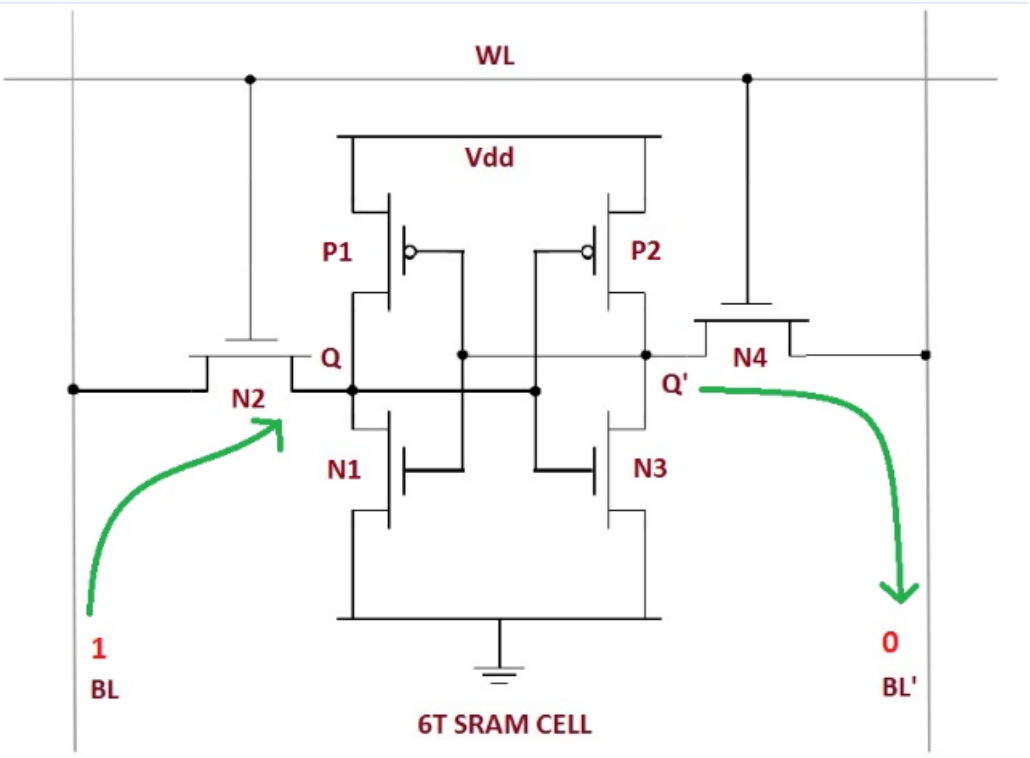


Figure 6.2: 6T-SRAM Write Operation

Basic Write Operation:

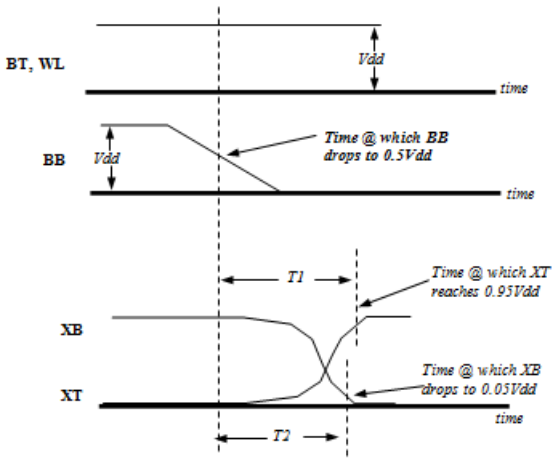
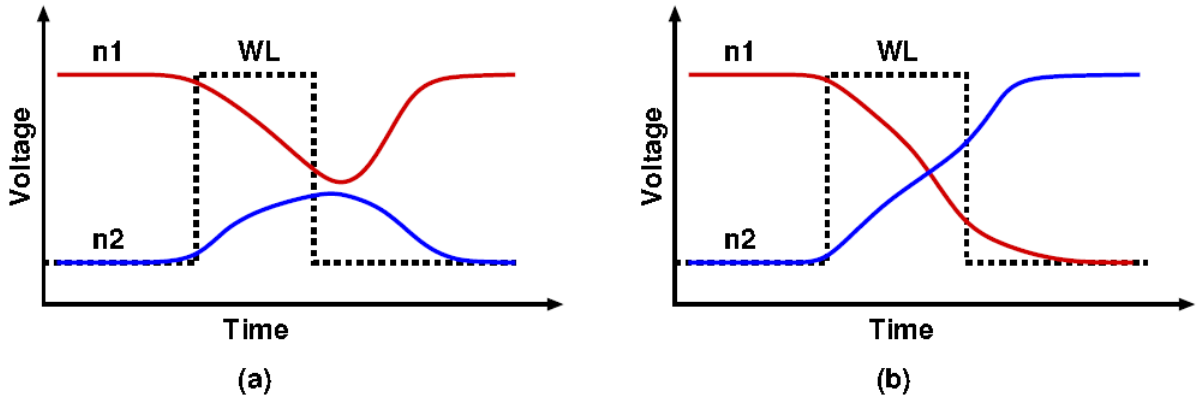


Figure 6.3: Waveform of Write Operation

Need for Write Assist:

- Here we reduced the parameter of our design like width and length and also voltage range using that we got higher challenges in each node.
- If we reduce parameter like width and length and voltage also than it will increase the changes in the doping of atom in channel on physical design.
- These fluctuations lead to threshold voltage mismatch between the neighboring cell transistors which can significantly reduce the cell SNM.
- Reducing the voltage, further degrades the read/write stability of the cell.
- Read failure occurs when the cell is not able to preserve a zero and that is possibly because the pass gate becomes too strong as compared to pull down because of the weak PMOS and strong NMOS.
- Write Failure occurs when the cell is not able to create a regenerative effect and that is possibly because the pass gate becomes weak as compared to the pull up which inhibits the node voltage to go below the switching threshold and flip the state.



- This is equation to check the current in our transistor in design:

$$\text{I } \alpha(VgsVth) Vgs > Vth$$

$$\text{I } \alpha 10(VgsVth)/100mv Vgs < Vth$$

- So, the current in the transistor will reduces and the effects of threshold voltage changes cannot be neglected at lower supply voltages.
- The limitation on the lower voltage Vmin is critical and require assist techniques to enhance the functional window of the cell.

6.1 Technique of Write Assist:

- lowering Vdd
- Raising Vss
- Negative WL Technique
- Negative Bit line

6.1.1 VDD Lowering:

- Write failures reduced by making the PMOS weaker as compared to pass gate (NMOS).
- As we reduce the core array voltage of the write selected columns, the Vgs for the pull up reduces and hence current through the PMOS.

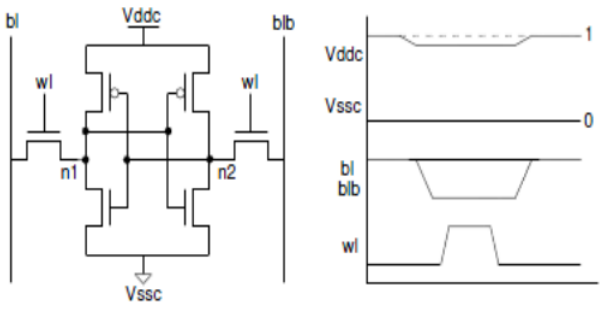


Figure 6.4: WL Lowering Technique

- Techniques used for generating a lower core array voltage:

a) With the use of external power supply that is connect through multiplexer to the particular column.
b) When write operation is start at that time it will generate very less voltage.
c) When this process is occur at that time write column is select and it will be floating.

- In this i simplify the result, the core voltage of the main array is low during the write operation.For that we reduced the Dynamic read noise margin in the bit-cell in the memory design.

Below design give works better compare to normal case but the gain is low, also PMOS is already weak in current case so because of that making weak will not use as a help. This scheme works better than the nominal case but the gain is minuscule, as the PMOS pull up are already weak in current generation bit cells and hence making it further weak does not help much.

a) Vdd Lowering Column Multiplexing:

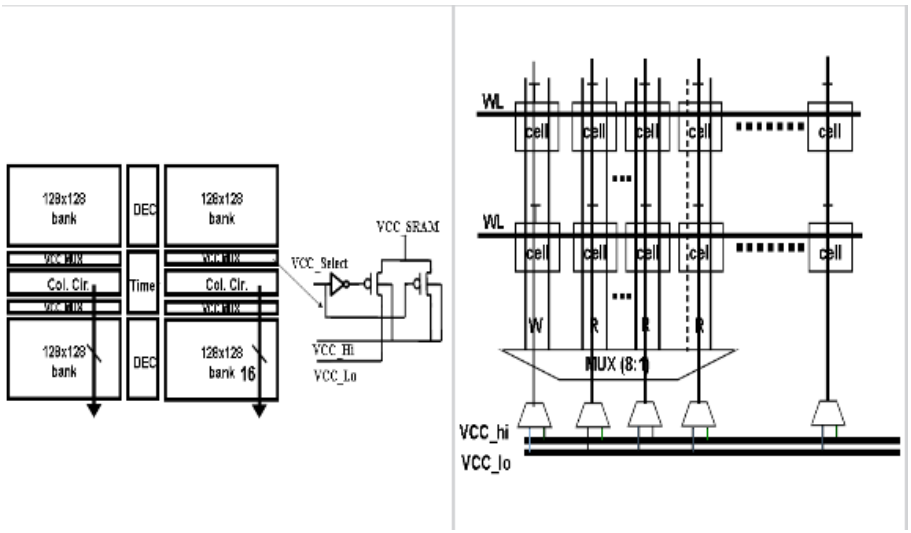


Figure 6.5: Vdd Lowering Column Multiplexing

- In read operation at higher voltage at VCC is connected to to memory, so it will generate the voltage difference between cell and word line and also give better SNM.

- In write operation, at lower voltage it will switched to the memory cells and it will give better negative voltage difference between cell and word line, and also flip the data easily.

- Drawbacks of the scheme:

a) Area overhead.

b) Dynamic Power increases.

c) Settling time for control signals so that supply is stable before the WL is enabled.

b) Vdd lowering Method:

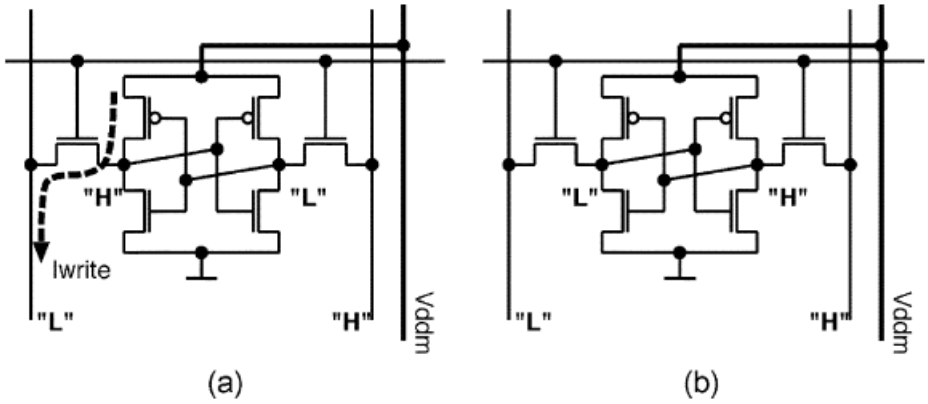


Figure 6.6: Vdd lowering Method

- In one column is connected with another column with Vdd lines seperately.
- Supply voltage Vddm is connected to the Vdd by power supply and it will control by the signal and its turned off when cell is ready to write and it will give change and also floating stat.
- Once data is flipped, the current through pass transistor ceases as both the bit line and the node values are same and hence the Vddm lowering.
- VDD Lowering Limitation

Limitations

Dynamic Modulation of vertically routed VDD

a) Settling time.

b) Use more extra power supplies.

c) Power Hungry.

6.1.2 VSS Raising:

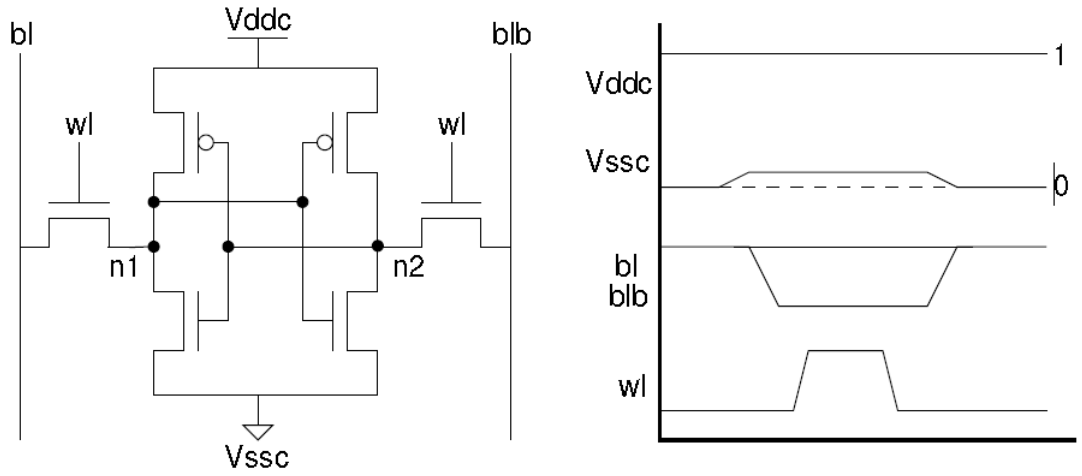


Figure 6.7: VSS Raising Method

- This schematic is used to another way for the write operation.
- In this technique we reduce voltage at ground side and and making gate of the PMOS voltage in place of the node at source side.
- The voltage at ground side is increased when our write operation is start.
- In this method some extra voltage at ground side can be placed and it will individual and it will produce internally also.

Limitations

- Dynamic Modulation of Globally routed VSS

a) Reduced Performance at nominal voltage.
b) Generated some voltage at supply side.
c) Power Hungry.
d) Differentiate MEM cells in the common column.

6.1.3 WL boosting technique:

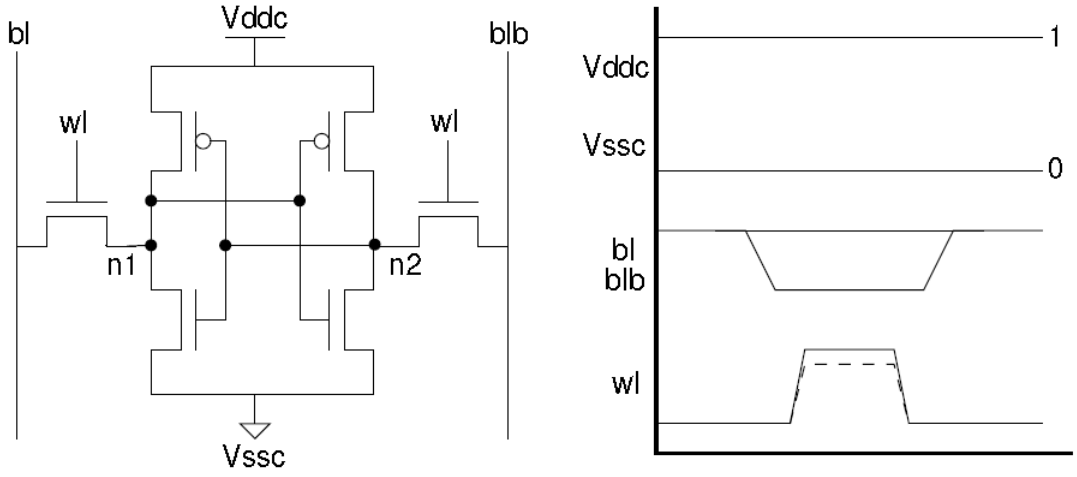


Figure 6.8: WL boosting technique

- In this technique, we boost the WL voltage grater than the gate voltage.
- The voltage increases the Vgs of the PG and because of that the strength of the driver will increases.
- Limitations

Requires extra supply and multiplexing in both row and column periphery.
Incompatible with bit-interleaving.

6.1.4 Negative Bit line WA scheme:

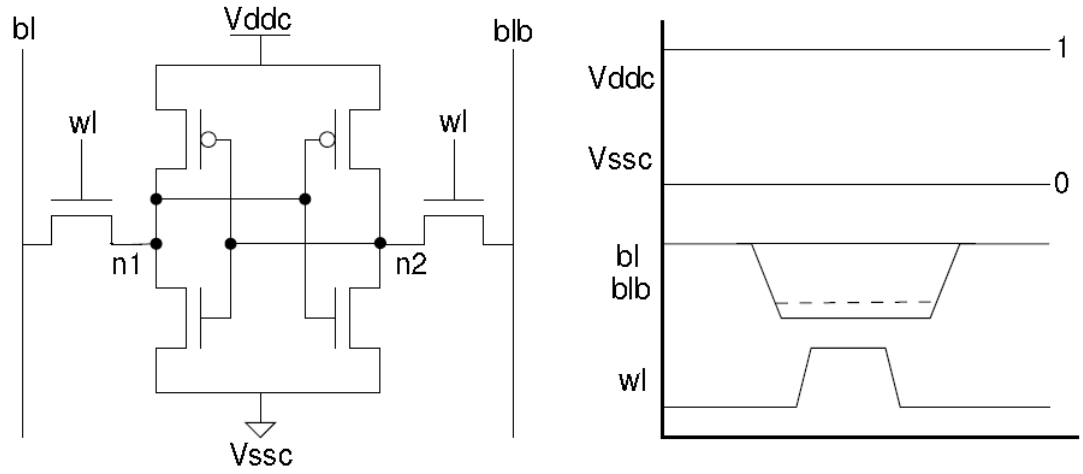


Figure 6.9: Negative Bit line WA scheme

- To increase the Voltage of gate to source for the PG because of that the voltage at Vg have to be high or the voltage at Vs have to be reduced.
- The approach of negative bit line swings the bit line voltage below 0 during the write operation.
- The increase in Vgs causes the PG to become stronger and than data will flip easily.
- Advantage of this technique is that, it will used in column,however the WL for these cells are not asserted and hence their DRNM are not affected.

6.2 Assist Circuits:

- All 16nm compilers support Assist periphery circuits
- Assist Technique for Read (SNM Assist)

- Increase the SNM is allow in the bit cell - Standard technique for WL lowering used industry wide

- Write Assist

- Assist the bit cell to do write operation - Two most used techniques - Negative Bit line - VDD Lowering (Also called VDD Collapse)

6.3 Read Assist Concept:

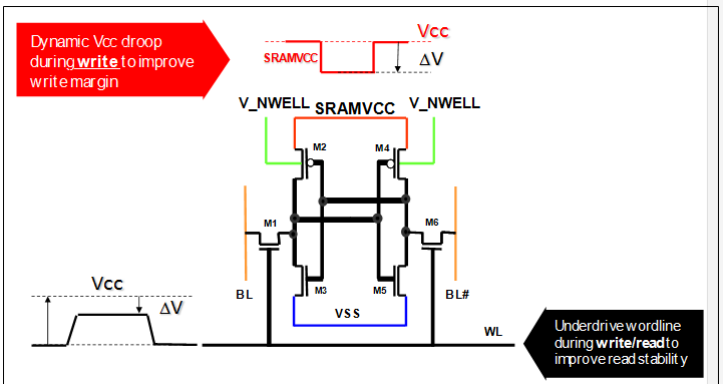


Figure 6.10: Read Assist Set-Up

6.3.1 Read Assist Scheme:

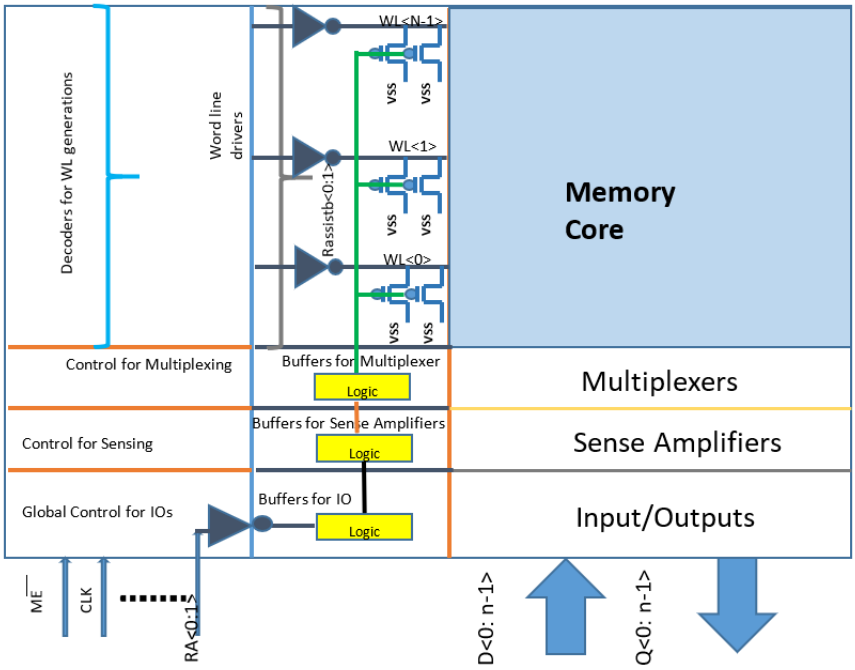


Figure 6.11: Schematic for Read Assist

6.3.2 Read Assist Support:

- Read Assist is a compiler option
- 2 pins are enabled by the flag read assist.
- These 2 pins RA¡1:0¿ are used to control the voltage level on the WL to prevent read disturb.

RA <1:0> setting	WL under drive percent
00	0%
01	5%
10	7.5%
11	10%

Figure 6.12: Internal setting for Read Assist

6.4 Write Assist Scheme (Negative Bit line):

Concept:

- Makes pass transistor

- stronger by increasing its Vgs.

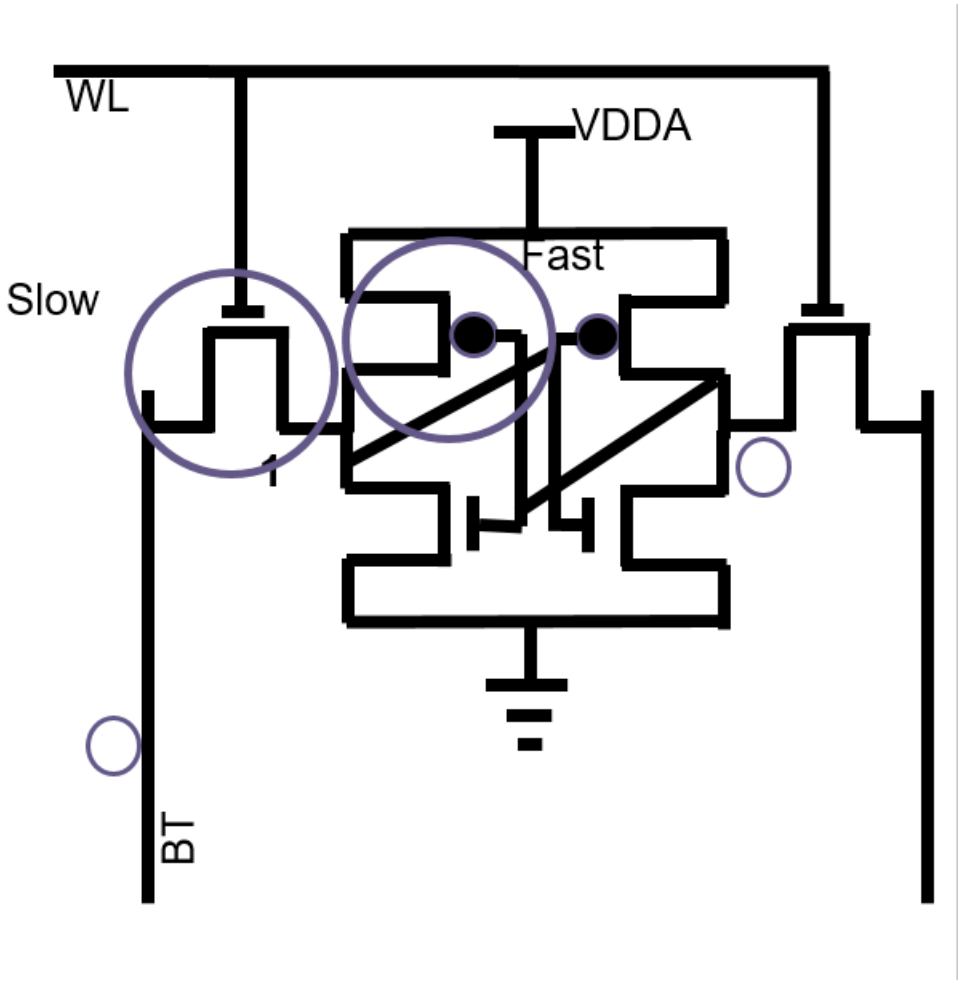
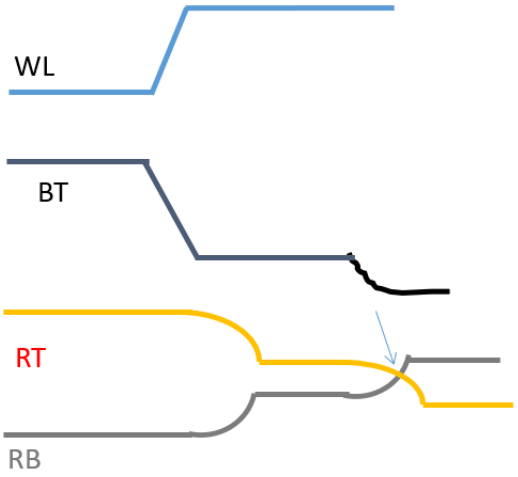


Figure 6.13: Write Assist Scheme (Negative Bit line)



6.4.1 Write Assist Signal Flow:

Margin = (T3 max of (T0, T1, T2)) >= 0.1 *(T3 + max (T0, T1, T2))

Write Assist Support:

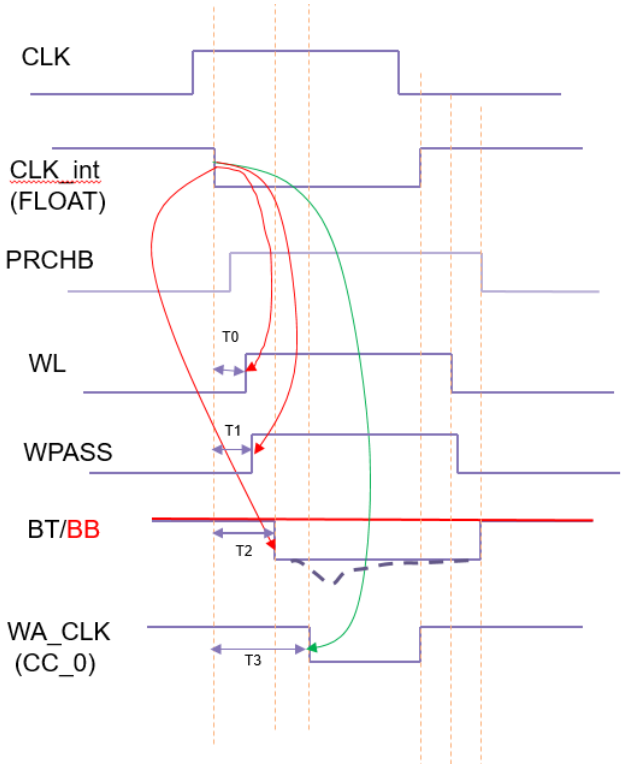


Figure 6.14: Waveform of Write Assist

- Write Assist is a compiler option
- 2 sets of pins are enabled by the flag write assist.
- The memory area increases with addition of Write assist tile. The increase is along the BL direction only.
- The 2 sets of pins are WA <2:0 >and WPULSE<2:0 >.
- WA <2:0 >is used to modulate the level of coupling for the Write Assist technique.
- WA <2 >controls the bypassing of the write assist circuitry. When this pin is set to 1 the bit-line is coupled negatively below vss.
- WA <2:0 >= 100 is the smallest coupling and 111 is the highest coupling.
- WPULSE<2:0 >is used to modulate the internal pulse width of write window.
- WPULSE<2:0 >= 000 is the smallest pulse width setting and WPULSE<2:0 >=111 is the largest pulse width.

- Table below describes the WPULSE and WA settings for the 4 timing modes.

Timing mode	Recommended RA, WA, WPULSE settings
Fast	RA=00, WA=101, WPULSE=000
Default	RA=00, WA=101, WPULSE=000
Slow	RA=01, WA=110, WPULSE=000
Vddmin	RA=01, WA=110, WPULSE=000

Figure 6.15: WPULSE and WA setting for Timing Mode

6.4.2 Write Assist Settings:

WA[2]	WA[1]	WA[0]	Comments
0	X	X	Wrist Assist Disabled
1	0	0	Target capacitance design for (Vddnom – 10%) to achieve 15-20% less coupling compared to WA = 101
1	0	1	Capacitance design for Vddnom – 10%
1	1	0	Capacitance design for Vddnom – 20%
1	1	1	Target capacitance design to achieve 15 – 20% more coupling compared to WA = 110

Figure 6.16: Internal setting for Write Assist

6.5 PPA Impact:

- Read Assist

- Area No Impact
- Power Minimal ¡ 5%
- Performance N/A
- Compiler generates Default/Fast mode with Read Assist off and Slow/Vddmin mode with Read Assist On Option only
- Given Read Assist pins, turning it on and off impacts the internal margin

- Write Assist

- Area 2% to 10% - Power 5% to 8% - Performance 2% to 10% (Cycle Time)

Chapter 7

Implementation and Result:

1) Write operation is done properly for that what is our design:

In our design I take voltage is 0.99 and I analyzed result in FF PVT and I used to write assist = false at that time I got result like this.

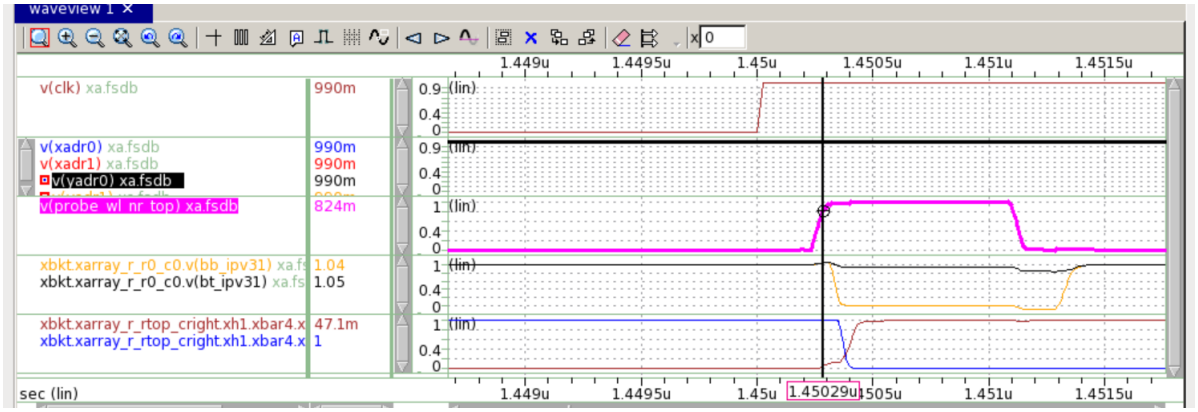


Figure 7.1: Waveform at WA= False and Voltage: 0.99

2) Write operation is not done properly for that what is our design:

In our design I take voltage is 0.63 and I analyzed result in FF PVT and I used to write assist = false at that time I got result like this.

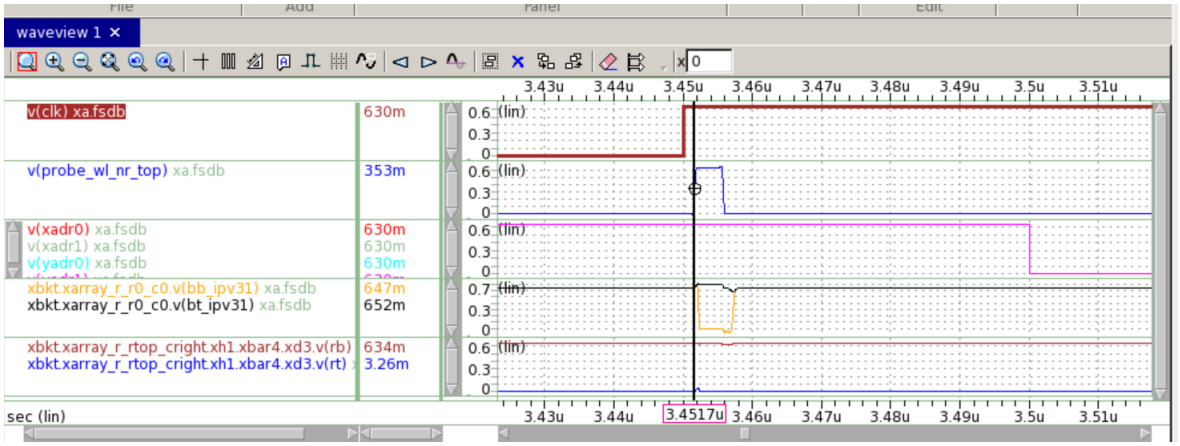


Figure 7.2: Waveform at WA= False and voltage 0.63

3) Write assist is True at that time what is our design:

In our design I take voltage is 0.99 and I analyzed result in FF PVT and I used to write assist = True at that time I got result like this.

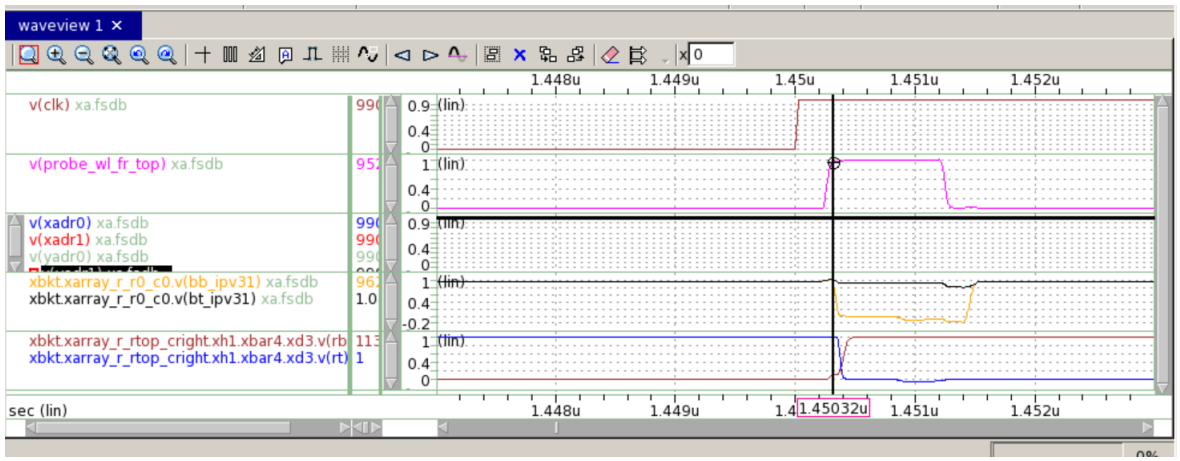


Figure 7.3: Waveform at WA= True and voltage 0.99

4) Write assist is True at that time what is our design:

In our design I take voltage is 0.63 and I analysed result in FF PVT and I used to write assist = True at that time I got result like this.

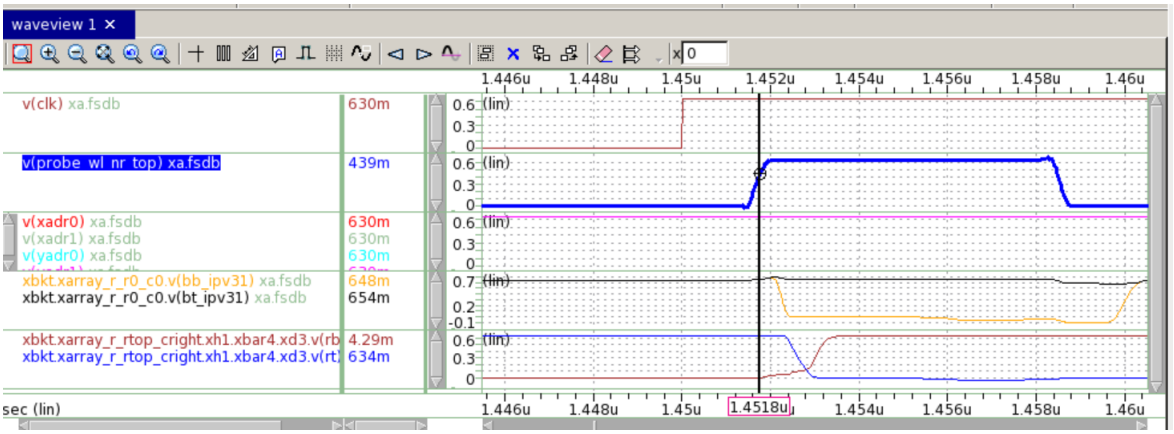


Figure 7.4: Waveform at WA= True and voltage 0.63

5) Results from Bit cell Analysis:

Worst case for SNM= FS_SRAM

STATIC NOISE MARGIN REPORT					
Voltage range for 5%					
Min Vdd	0.72				
Max Vdd	0.72				
Process	Voltage	Temp	Noise Margin	Pass / Fail Criteria	Pass / Fail)
FS_SRAM	0.72	125	0.06748	0.072	FAIL

WL Dip= 5% for normal case

Voltage range for 5%					
Min Vdd	0.72				
Max Vdd	0.72				
Process	Voltage	Temp	Noise Margin	Pass / Fail Criteria	Pass / Fail)
FF_SRAM	0.72	125	1.18E-01	0.072	PASS
FS_SRAM	0.72	125	8.20E-02	0.072	PASS

Mismatch change for Fail Result

STATIC NOISE MARGIN REPORT

Voltage range for 5%

Min Vdd	0.72
Max Vdd	0.72
Sigma Parmeter	5.2

Process	Voltage	Temp	Mean	Sigma	Min	Max	Sigma/Mean	Mean-5.2*Sigma	Pass Criteria	Pass/Fail
FSGlobalCorner_LocalMC_SRAM	0.72	125	0.104	0.01889	0.03116	0.1899	0.1816	0.005772	0.036	FAIL
FSGlobalCorner_LocalMC_SRAM	0.72	-40	0.1259	0.02119	0.03839	0.2192	0.1683	0.015712	0.036	FAIL
FFGlobalCorner_LocalMC_SRAM	0.72	125	0.1136	0.01879	0.03842	0.197	0.1654	0.015892	0.036	FAIL
SSGlobalCorner_LocalMC_SRAM	0.72	125	0.1232	0.01918	0.04563	0.2045	0.1557	0.023464	0.036	FAIL
FFGlobalCorner_LocalMC_SRAM	0.72	-40	0.1365	0.02097	0.05248	0.2333	0.1536	0.027456	0.036	FAIL
SSGlobalCorner_LocalMC_SRAM	0.72	-40	0.1422	0.02175	0.05259	0.2406	0.153	0.0291	0.036	FAIL
SFGlobalCorner_LocalMC_SRAM	0.72	125	0.1334	0.01907	0.05982	0.2118	0.143	0.034236	0.036	FAIL

Mismatch change for Pass Result after WL dip=5 %

Process	Voltage	Temp	Mean	Sigma	Sigma/Mean	Mean-5.2*Sigma	Pass Criteria	Pass/Fail
FFGlobalCorner_LocalMC_SRAM	0.72	125	1.29E-01	1.88E-02	1.46E-01	3.09E-02	0.036	FAIL
FSGlobalCorner_LocalMC_SRAM	0.72	125	1.19E-01	1.89E-02	1.59E-01	1.19E-01	0.036	PASS
SFGlobalCorner_LocalMC_SRAM	0.72	125	1.49E-01	1.91E-02	1.28E-01	4.96E-02	0.036	PASS
SSGlobalCorner_LocalMC_SRAM	0.72	125	1.38E-01	1.92E-02	1.39E-01	1.24E-01	0.036	PASS
FFGlobalCorner_LocalMC_SRAM	0.72	-40	1.50E-01	2.09E-02	1.40E-01	1.35E-01	0.036	PASS
FSGlobalCorner_LocalMC_SRAM	0.72	-40	1.38E-01	2.09E-02	1.51E-01	1.23E-01	0.036	PASS
SFGlobalCorner_LocalMC_SRAM	0.72	-40	1.64E-01	2.10E-02	1.28E-01	1.49E-01	0.036	PASS
SSGlobalCorner_LocalMC_SRAM	0.72	-40	1.53E-01	2.10E-02	1.37E-01	1.38E-01	0.036	PASS

6) DC WM for Normal case - Fail Result:

DC WRITE MARGIN REPORT

Pass/Fail Criteria in % 10

Process	Voltage	Temp	DC Write Margin using 1st model (V)	Pass/Fail Criteria (V)	Pass / Fail
SF_SRAM	0.72	-40	0.02321	0.072	Fail
SF_SRAM	0.81	-40	0.05851	0.081	Fail

-Result when apply WL Dip=5%

Pass/Fail Criteria in % 10

Process	Voltage	Temp	DC Write Margin using 1st model (V)	Pass/Fail Criteria (V)	Pass / Fail
SF_SRAM	0.72	125	2.35E-02	0.072	Fail
SF_SRAM	0.72	-40	2.71E-02	0.072	Fail
SF_SRAM	0.81	125	5.08E-02	0.081	Fail
SF_SRAM	0.81	-40	1.87E-03	0.081	Fail

- DC Write Margin Sim- BL Driven

- SHD Bit cell strategy for Write:
- Write Assist making bit line negative
- Considering only BL driven with Write assist
- Timing mode: Fast, Def, Slow, 95% WL (5% margin to account vdd-drop)
- For Vddmin WL 90% (Read assist applied)
- BL sweep VDD to -200mV, 100M Monte
- Simulating for worst case corner for Write: SF -40C to find negative bit line target:

Negative Bit line Target SHD 1-1-1 (100M)									Neg_bl	Neg_bl Actual	
Process	VDD	VWL	Mode	mean	sigma	mean-6sig	quantile	min	-5%vdd	(128 row)	
SFG,-40	0.72	0.684	Def	9.85E-02	2.69E-02	-6.32E-02	-7.12E-02	-7.12E-02	-0.107	-1.02E-01	
SFG,-40	0.81	0.7695	Fast	1.35E-01	2.70E-02	-2.64E-02	-3.95E-02	-3.95E-02	-0.080	-8.22E-02	wl 95%
SFG,-40	0.675	0.64125	Slow	7.96E-02	2.68E-02	-8.12E-02	-8.70E-02	-8.70E-02	-0.121	-1.30E-01	
SFG,-40	0.63	0.567	Vddmin	1.55E-02	2.67E-02	-1.45E-01	-1.51E-01	-1.51E-01	-0.182	-1.60E-01	wl 90%

Implementation for 8T- SRAM cell:

1) Waveform of 8T-SRAM

Below Simulation results are based on particular technology on different supply voltages. Below simulation done at different mode of operation on SRAM.

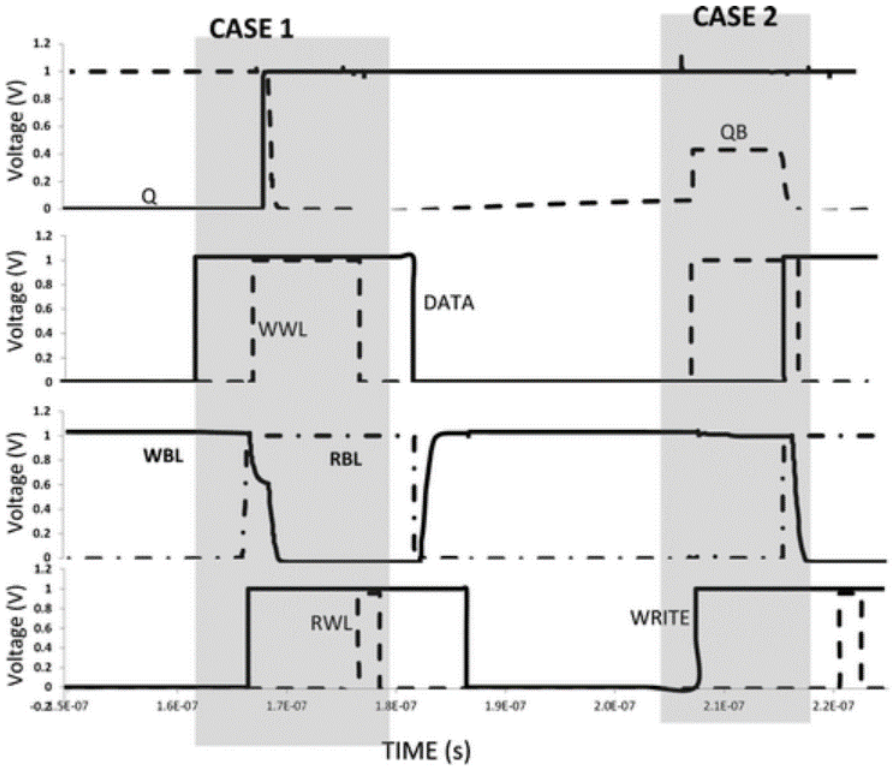


Figure 7.5: Result of 8T-SRAM

Static Noise Margin observed at read part for read stability of the SRAM cell. For SNM we obtained the Butterfly curve & we see the inverter characteristic. while pass gate or access transistor are on and bit-line are precharged at higher voltage VDD. According to our below result, when output (Q) holds logic high according to that invert of output (QB) data also increases even to very large value not affect my original stored data on output (Q). We also simulate the proposed SRAM Bit-cell for output (Q) is at lower voltage as logic 0, word line at write part is logic high, and word line at read part is logic low (i.e CASE 1) & output (Q) is logic high , word line at write part is logic high, word line at read part is logic low (i.e CASE 2).In below figure the shadowed part represent the operation when write word line is activated and at that time my read word line signal is at logic "0". here we take care about below cases.In first case, output (QB) discharge via Pass gate or Access transistor to GND that means write will happen while read word line kept "0". In CASE 2, output node (Q) hold data "1" , at that time voltage at output node (QB) increases to some voltage like 0.4 V, the data is not flip at output node (QB).

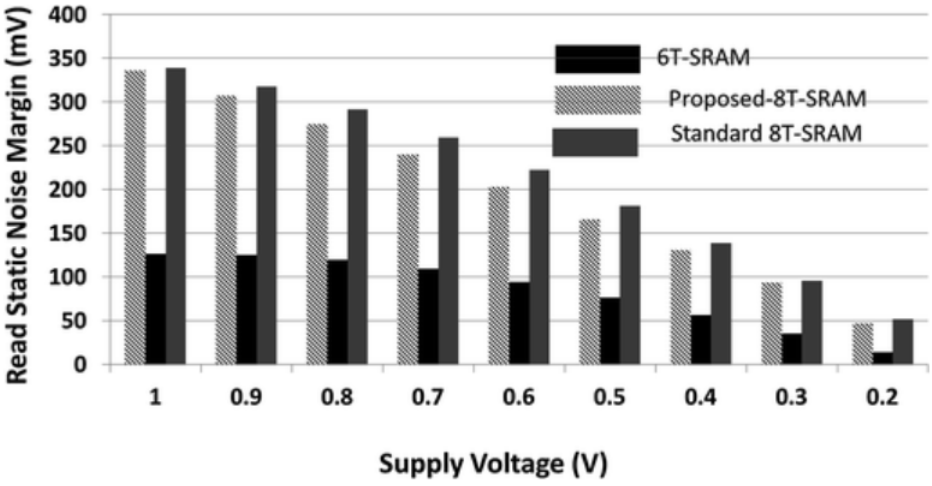


Figure 7.6: RSNM Result for the standard 6T-SRAM, 8T-SRAM and the proposed 8T-SRAM cell

a. 8T-SRAM cell waveform

b. Operation of Read Operation

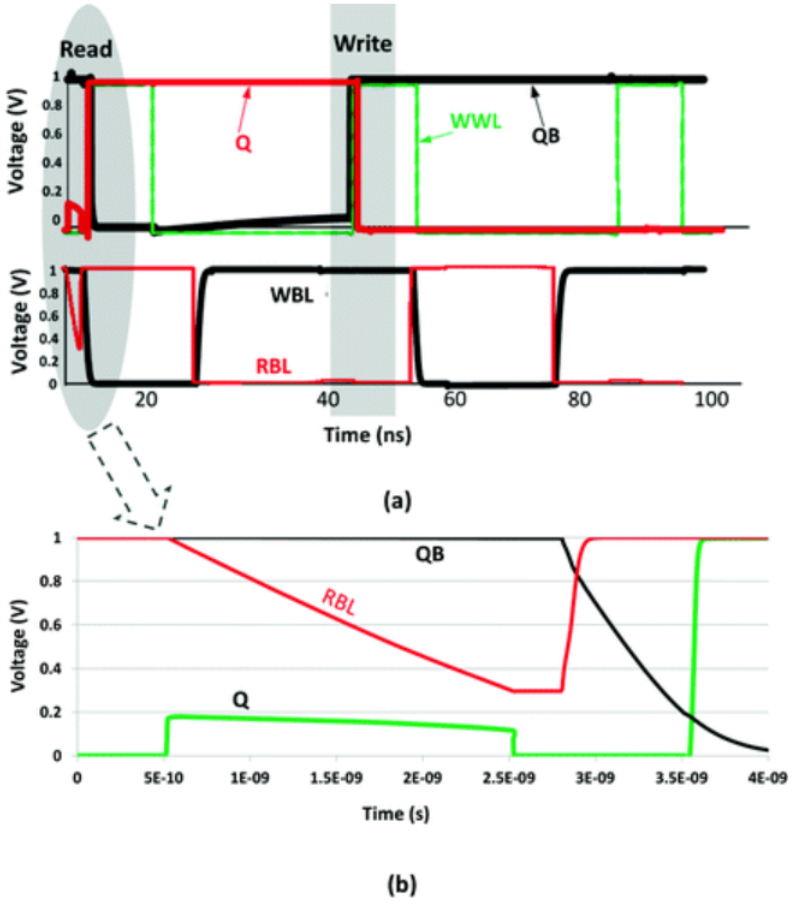


Figure 7.7: (a)8T-SRAM cell Waveform (b)Operation of read operation.

Result Discussion:

- In first result I keep voltage is 0.99 and write assist is false at that time I checked my write operation so here my write operation is properly done.
- In second case I keep voltage 0.63 and write assist is false so at that time I checked write operation so here my write operation is not done properly because my voltage is low so for that reason so now I want to improve my write operation successfully for that I should use write assist circuit.
- In 3rd case I keep voltage is 0.99 and write assist is true at that time I checked my write operation so here my write operation is successful.
- In 4th case I want to check at low voltage my write operation is properly done or not. But here in this case my write operation is done properly because here I used to write assist is true.
- In 5th case I did Bit cell analysis. In this I see SNM (Static Noise Margin). I found worst case for that and I analysed the result. For that I got failure. I did not get expected SNM. So, to achieve good SNM I have to apply wl (world line dip) for improve my SNM. For that I used read assist technique that is Word Line Lowering Technique for improve static noise margin of bit cell.
- In 6th case I checked write margin (WM) for bit cell. For that I found worst case and I analysed result. I got failure in write margin for that I need to use write assist technique. By applying this technique, I got better write margin for bit cell.
- I also analysed result of different voltage with different timing mode for improve write margin. For that I used write assist technique of Negative Bit line Technique.

7.1 Conclusion:

In this thesis, we analyzed that why we used read and write assist technique and what is the need of that. here we observed result on that when my SNM (Static Noise Margin) is not good means i got failure in read during my Read operation so at that time we used read assist technique to improve the SNM.For that we used method word line boosting. In this we gave WL dip according to our requirement and made read assist setting for that and than we got better SNM.

When my write operation was fail or i got bad Write Margin (WM) for that i used this technique. To resolve this problem we used Negative Bit-line technique. In this we applied negative voltage on bit-line according to our requirement than i got better WM using this technique.Here basically we used this technique to got read and write margin of low voltage SRAM cell.i also observed that when i applied read assist technique at that time i got better Read margin. Process variations occurred on read and write assist techniques are observed.

7.2 Future Scope:

- Simulate a given product on different nodes and different schemes.
- More focus on the impact of the schemes on the variations, Process Variability, Margin Sensitivity and Performance (Power, Delay and Cost).

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