Chapter 1.

Introduction

Overview 1.1

Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds. Memories are circuits or systems that store digital information in large quantity. Today, memory circuits come in different forms including SRAM, DRAM, ROM, EPROM, E2PROM, Flash, and FRAM. While each form has a different cell design, the basic structure, organization, and access mechanisms are largely the same.

The preferred organization for most large memories is shown in Figure 1.1.a This organization is a random-access architecture. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called wordlines, while the vertical lines, along which data flow into and out of cells, are called bitlines .

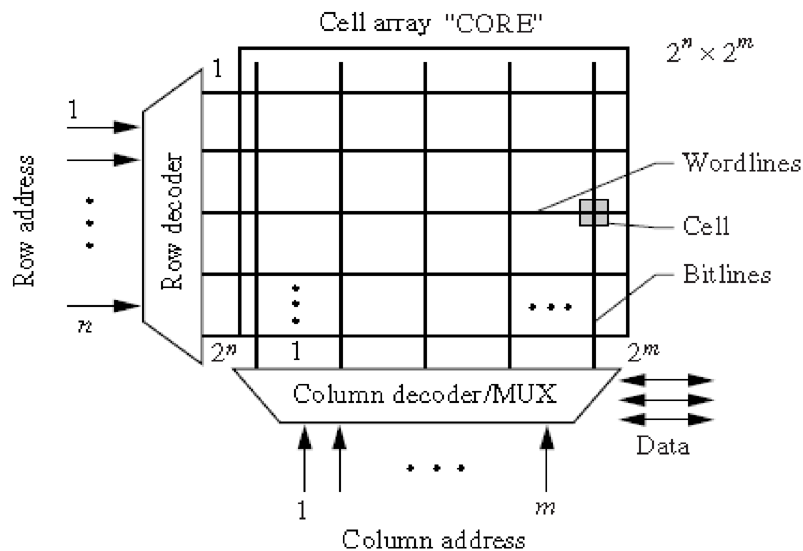

Figure 1.1.a

High-performance large-capacity Static Random Access Memories (SRAMs) are a crucial component in the memory hierarchy of modern systems. SRAM design requires a balancing act between delay, area, and power consumption. The circuit styles for the decoders and the sense amps, transistor sizing of the circuits, interconnect sizing and partitioning of the SRAM array can all be used as a tradeoff for these parameters.

In recent years, power consumption has become a critical design concern for many VLSI systems. In the meanwhile, memory accesses consume a substantial portion of the total power budget for many applications. The system-on-chip (SoC) employs a large number of SRAM as on-chip memory. Thus, reducing the power dissipation in SRAMs can significantly improve the system power-efficiency, performance, reliability, and overall costs.

While CMOS technology has served semiconductor industry marvelously, it faces some major obstacles at sub-90nm process nodes (65nm,45nm and 32nm ect) due to the intrinsic physical limitations of the devices. One of the major barriers that the CMOS devices face at nanometer scale is increasing process parameter variations.To deal with increasing parameter variations, it is important to accurately model the impact of device parameter variations at circuit level and develop process-tolerant design techniques for both logic and memory. This study will examine the impact of process parameter variations on SRAM.

The Memory Compiler automatically instantiates the appropriate memory function based on the options we chose for particular memory configuration. The compiler provides front-end design information, such as datasheets, simulation models and timing models for synthesis. It also allows SoC designers to include specific memory macro instances in their designs by generating place and route views and specifications for memory sizes, configurations, power, speed and temperature ranges. With this information on hand, all of the views required for simulation, synthesis, floor-planning and place and route of an SoC design are generated.

1.2 Objective

The main purpose of this thesis is to propose a new approach to the design of a 6T SRAM memory cell and driver with particular focus on this will further be used in as a primary unit for memory compiler in 65nm technology. After this memory compiler automation flow for generation of various important files such as Netlist file , GDS file , Verilog file etc for different memory instances will be discussed .

1.3 Thesis Organization

Chapter 1- **Introduction**: Presents a brief introduction and overview of general requirements and challenges in the design of low-voltage and process-variation-tolerant SRAM. It also includes some of the terms and acronyms used in the rest of this thesis.

Chapter 2–**6T SRAM Cell Design**: Illustrates the basic structure of the 6T cell, read and write functions, and periphery circuits. Subsequently, both read and write cell stability is investigated. dc and transient analyses of the cell are presented. In addition, a cache architecture utilizing 6T cell is introduced. Its read and write operations and cell stability in different supply voltages are studied. Eventually in the end of the chapter, some of the most recent research works in the design of ultra low-voltage SRAM cell are discussed.

Chapter 3– **Analysis of Failure in Nano-Meter Regime**: Different types of failure such as read failure ,Write Failure ,Access Failure etc. which occurs in nano meter regime will Discussed .

Chapter 4– **PN and Stage Ratio Analysis** :To Drive Bitcell with Different Load we are going to set PN ratio as well as stage ratio of drivers which gives minimum delay.

Chapter 5– **Memory Compiler** : This chapter contains information for memory compilers. These are complete compilers that consist of various generators to satisfy the requirements of the circuit at hand.

Chapter 6 – **Appendix A** **:** Simulation Results

Appendix B **:** Refernces

Chapter 2.

6T SRAM Bitcell Analysis

Memories are said to be static if no periodic clock signals are required to retain stored data indefinitely. The design issues for static memory cells are described in this section.

2.1. Static Memory Operation

The basic static RAM cell is shown in Figure 2.1.a It consists of two cross-coupled inverters and two access transistors . The access transistors are connected to the wordline at their respective gate terminals, and the bitlines at their source/drain terminals. The wordline is used to select the cell while the bitlines are used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side. For reference purposes, assume that node q holds the stored value while node holds its complement. The VTC of cross-coupled inverters is shown in Figure 2.1.b.

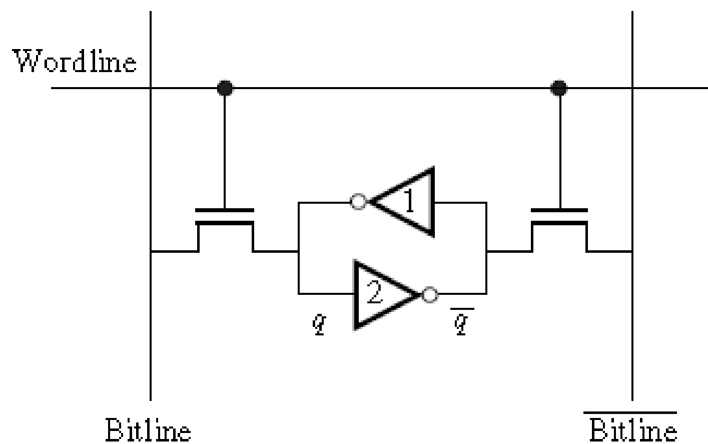

Figure 2.1.a

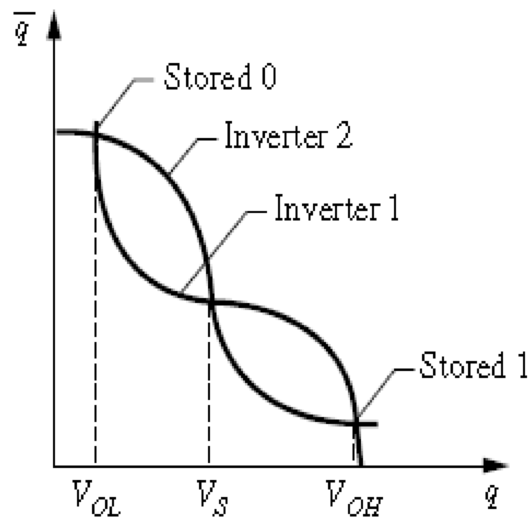

Figure 2.1.b

The VTC conveys the key cell design considerations for read and write operations. In the cross-coupled configuration, the stored values are represented by the two stable states in the VTC. The cell will retain its current state until one of the internal nodes crosses the switching threshold, VS. When this occurs, the cell will flip its internal state. Therefore, during a read operation, we must not disturb its current state, while during the write operation we must force the internal voltage to swing past VS to change the state.

The six transistor (6T) static memory cell in CMOS technology is illustrated schematically in Figure 2.1.c. The cross-coupled inverters,M1,M5 and M2,M6, act as the storage element. Major design effort is directed at minimizing the cell area and power consumption so that millions of cells can be placed on a chip. The steadystate power consumption of the cell is controlled by subthreshold leakage currents, so a larger threshold voltage is often used in memory circuits. To reduce area, the cell layout is highly optimized to eliminate all wasted area.

The design of the cell involves the selection of transistor sizes for all six transistors of Figure 2.1.c to guarantee proper read and write operations. Since the cell is symmetric, only three transistor sizes need to be specified, either M1,M3, and M5 or M2, M4, and M6. The design of the cell involves the selection of transistor sizes for all six transistors of Figure 2.1.c

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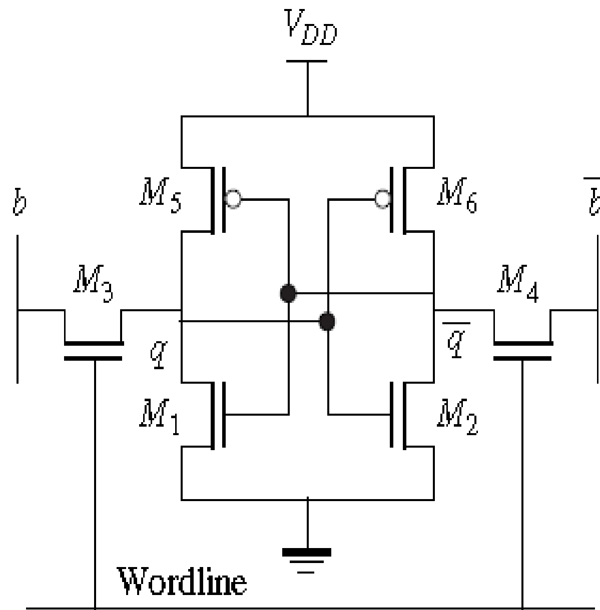


Figure 2.1.c

2.1.1 Read Operation

Assume that we want to read ‘0’. This means a 0 is stored at Q or implicitly a 1 is stored at QB. Furthermore, assume that both bitlines are precharged to 1V before the read operation to be initiated. The read cycle is started by asserting the wordline, enabling two pass transistors. Consequently, the contents stored at Q and QB begin to transfer to the bitlines BL and *BL_B* respectively. Design details of the 6T RAM cell for the read operation using Figure 2.1.1a and Figure 2.1.1b. Therefore, M1 is on and M2 is off. Initially, BL and BL_B are precharged to a high voltage around VDD by a pair of column pull-up transistors (not shown). The row selection line, held low in the standby state, is raised to VDD which turns on access transistors M3 and M4. Current begins to flow through M3 and M1 to ground. The resulting cell current slowly discharges the capacitance Cbit.Meanwhile, on the other side of the cell, the voltage on remains high since there is no path to ground through M2. The difference

between BL and BL_B is fed to a sense amplifier to generate a valid low output, which is then stored in a data buffer. Upon completion of the read cycle, the wordline is returned to zero and the column lines can be precharged back to a high value.

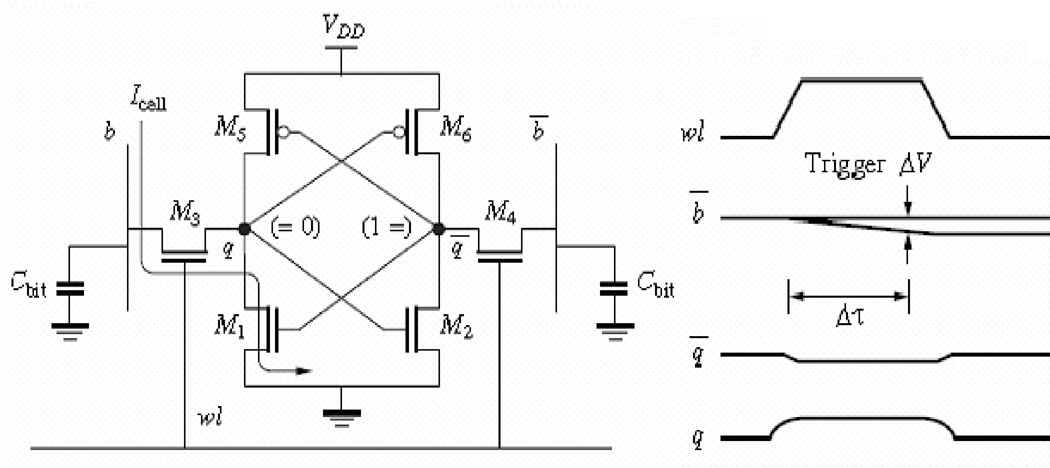


Figure2.1.1a

Figure 2.1.1b

2.1.2 Write Operation

The operation of writing 0 or 1 is accomplished by forcing one bitline, either BL or BL_B, low while the other bitline remains at about *VDD*. In Figure 2.1.2a and Figure 2.1.2b to write 1, BL_B is forced low, and to write 0*,* BL is forced low .The cell must be designed such that the conductance of *M*4 is several times larger than *M*6 so that the drain of *M*2 is pulled below *VS*. This initiates a regenerative effect between the two inverters. Eventually, *M*1 turns off and its drain voltage rises to *VDD* due to the pull-up action of *M*5 and *M*3. At the same time,*M*2 turns on and assists *M*4 in pulling output to its intended low value. When the cell finally flips to the new state, the row line can be returned to its low stand b level.

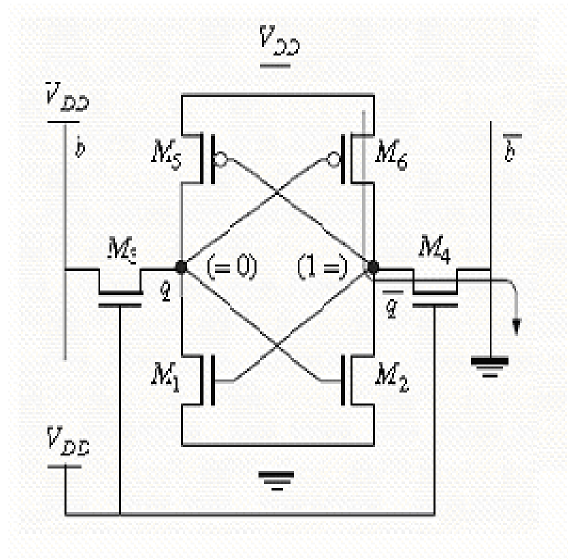


Figure2.1.2a

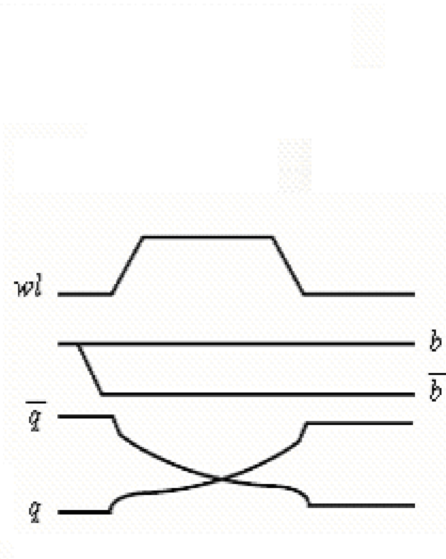


Figure 2.1.2b

2.2 Design of SRAM Bitcell :

(1): When write '0' operation is perform then definitely M3 will in saturation and M1 will in linier region , Saturation current flowing through M3 will going to flow from M1.If width of M3 will more then M1, then current flowing through M1 will more according to which at q point voltage drop will going to increase which will turn on M2 that not required so always width of pass transistor will taken several times lower then width of NMOS transistor of inverter .

(2): Further increment in width of M1 will give improvement in "Read Access Time" but

more width will cause to increase “Write Access Time “.

(3): Design width of NMOS is obtain from pull down path as by tacking Cell NMOS (W/L) to Pass transistor NMOS (W/L) ratio equal to 1.5 .

(4): Design width of PMOS is obtain from pull up path as by tacking Pass transistor NMOS (W/L) to Cell PMOS (W/L) ratio equal to 1.5 .

2.3 Analysis For SRAM Bitcell :

1.Static Noise Margin (SNM)

2.Read current

3.Bitline Leakage

4.Standby power

5.Write Margin

6.Flip time (Write Access Time)

2.3.1. Static Noise Margin (SNM)

“Static Noise Margin is defined as the maximum value of dc disturbances that the cell nodes can tolerate before flipping its state”. Static noise is dc disturbance such as offsets and mismatches due to processing and variations in operating conditions. In this work, only static-noise sources are taken into account. The SRAM cell should be designed such that under all circumstances, there would be some SNM to deal with the dynamic disturbances caused by alpha-particle incidences, crosstalk, supply voltage ripple, and thermal noise.

Two types of static noise margin (SNM) measurement for SRAM Cell will be done. First is Read SNM and second is Hold SNM ,for these analysis setup is given as in Figure 2.3.1a . Two equal dc voltage sources, V_N are placed between inverters indicating the dc noise

sources. These voltages are swept from 0 to $V_{DD}/2$ (i.e. 0.5 V) or more until the cell storage data flips. These flipping voltage is define as SNM for particular Bitcell .

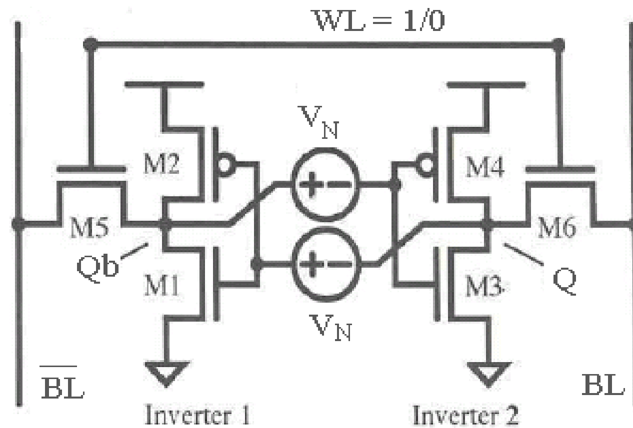


Figure 2.3.1a

Here when bitcell is in hold position means WL ='0' & when bitcell is in read position means WL ='1' and at the same time BL and BL_B are set to Vdd .

2.1.2. Read Current

To read a value from an SRAM cell, both bitlines are precharged high and the wordline is raised turning on the pass transistors. The bitline relative to the cell node that contains 0 begins discharging. The sense amplifier, which is connected to the bitlines, detects which of the bitlines is discharging and hence reads the stored value.For this analysis we have see current of pass transistor that is closer to sense amplifier .

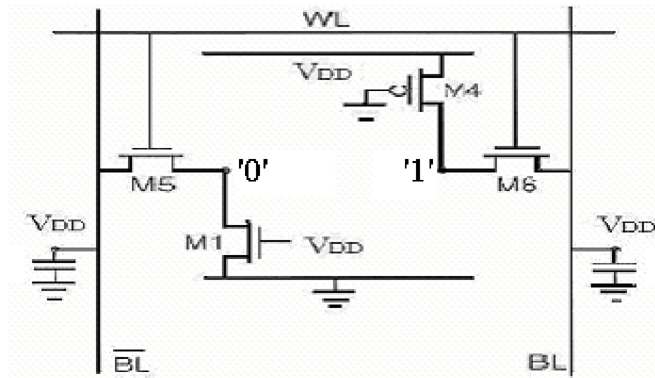


Figure 2.3.2a Simplified cell during read operation. (Read ‘1’)

2.3.3. Bitline Leakage

In this analysis bit & bit_b line are precharge to vdd and at the same time word line is not selected .Then we are going to measure how much leakage current is flowing through bit /bit_b lines to bitcell .

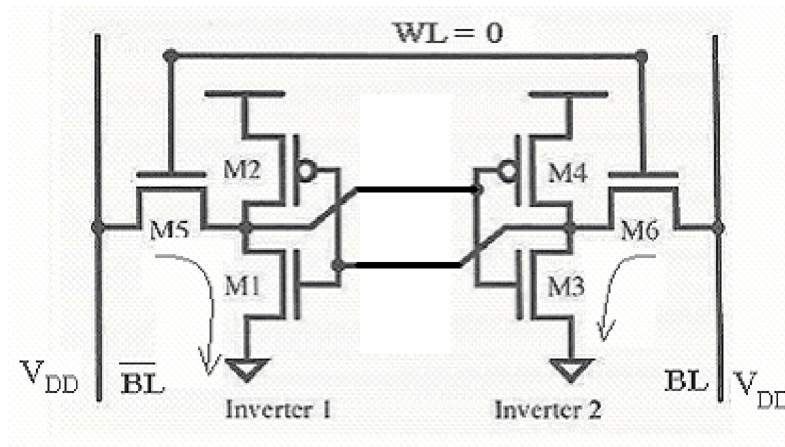


Figure 2.3.3a Cell during Bitline leakage

One important equation always be taken care that Active Cell current will always be greater then Sum of Inactive Cell current (leakage current) which is given by Eq(2.3.3.1)

I_cell > = (No. of Rows -1)*I _leak………………. …………….. Eq(2.3.3.1)

2.3.4. Stand By Power

Stand by Power analysis done when cell is in ideal mode means WL is set '0' (Retention Mode) .When cell is retention mode current flowing through Vdd and Vss are measured .For this same setup as shown in Figure 3.1.3a is made. Here current is multiply by voltage for power calculation. During stand by power calculation different currents flowing in stand by mode is shown in figure 2.3.4a.

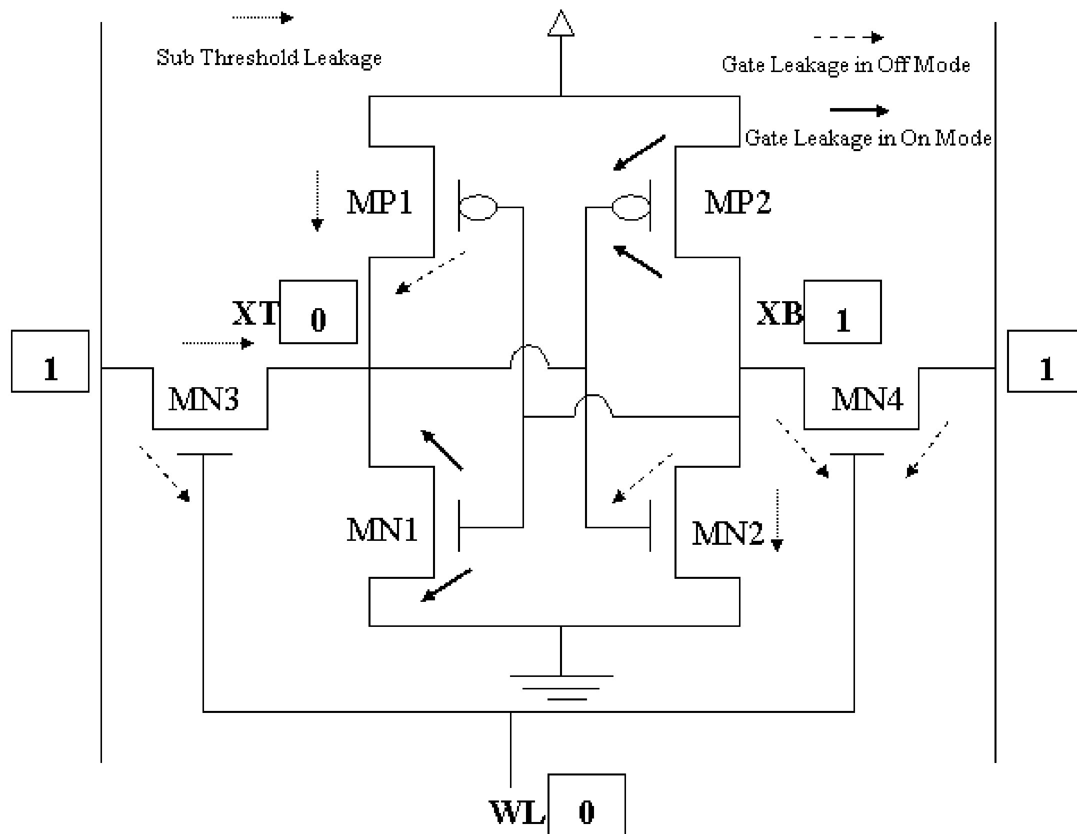


Figure 2.3.4a

2.3.5 Write Margin

Generally for writing a particular value to bit cell we make any of bit line to one or zero value according to word line selection cell is selected from array. Write Margin analysis done by two way first one is bit line driven write margin and second is word line driven write margin .In bit line driven write margin word line is set to a stable value first then bitline signal changes will done as shown in figure 2.3.5a . In word line driven write margin bitline are set to a stable value first then changes in word line will make as shown in figure 2.3.5b.

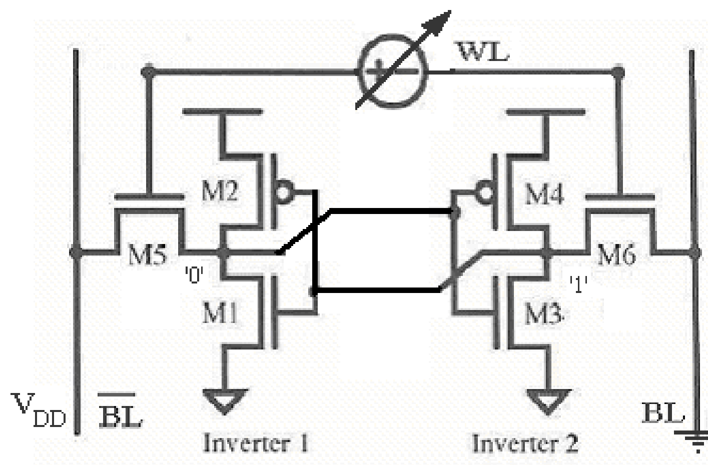


Figure 2.3.5a to write ‘0’ in bitcell word line driven write margin

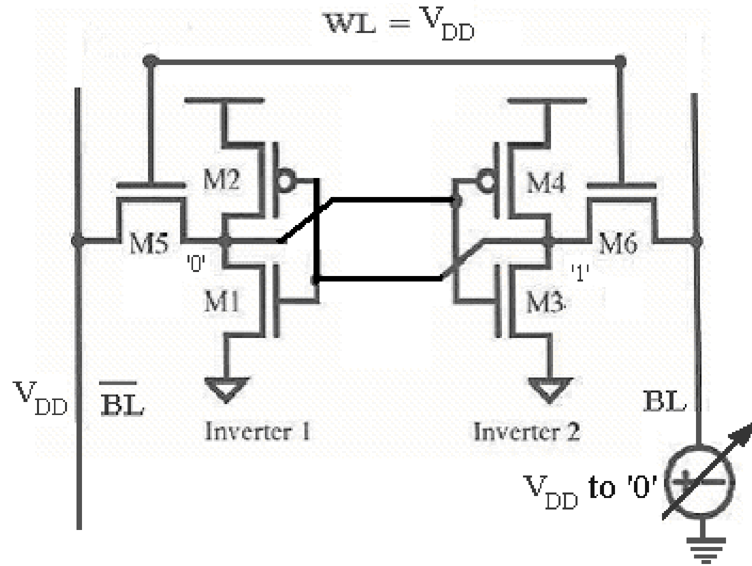


Figure 2.3.5b to write ‘0’ in bitcell bit line driven write margin

2.3.6. Flip Time (Write Access Time)

In this analysis calculation of write access time will be done as previously we know that write margin analysis will done in two way .Similarly Flip Time will also calculate in two way between them larger value is actual Flip Time (write access time) of bitcell .

Chapter 3

Analysis of Failure in Nano-Meter Regime

3.1 Analysis of Failure in Nano-Meter Regime

In nm tech. while scaling down devices technology Ion to Ioff ratio will decreases as leakage current will going to increases .As result exponentially increasing in leakage power as we continuing scaling. There is two major cause of failure in nm technology :

1.Random Dopant Fluctuation.

2.Process Variation.

3.1.1.Random Dopant Fluctuation

As compare micrometer region in neno meter region number of dopant per unit area will be lower (if in micrometer region number dopant per unit area is 1000/10000 or uncountable then in neon region it's just 100/50 or countable). So because of lesser number of dopant particular area possibilities of fluctuations will more .Random dopant fluctuation in nm tech. is shown in figure 3.1.1.a.

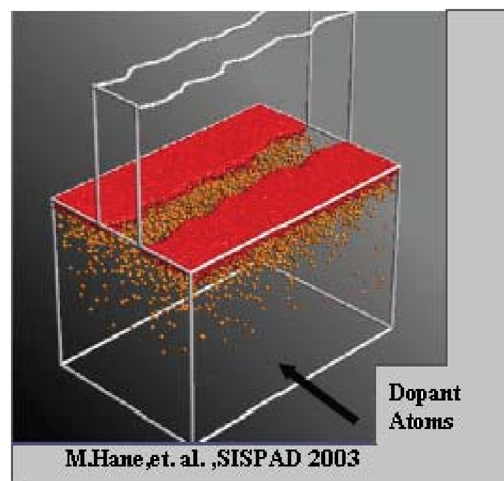


Figure 3.1.1.a

3.1.2.Process Variation

This will seen as inter-die and intra-die variation .Die to die variation will known as inter die variation (example if n number of die's are used in IC then variation in top die vt as compare bottom of die's vt) and within the die variation is known intra-die variation .

3.2 Major Challenge in nm tech

Major challenge in nanometer region are leakage and variability .

3.2.1. Leakage

3.2.2. Variability

As we discussed previously in section 3.1 that in nanometer region leakage is major factor which will be must taken care before and after fabrication. Major part of leakage at transistor level are given as :

1. Sub-Threshold Leakage .
2. Gate Leakage.
3. Reverse Bias Band to Band Tunneling (RB BTBT).

Variability will be further be divided in two part :

1. Length Variability
2. Threshold Voltage Variability (Due to Inter die & Intra die variation).

3.3 Failure Occur in SRAM in NM Tech

Most of failure occur in SRAM in nanometer technology is after fabrication failure . These failures are given as :

1. Read Failure .
2. Write Failure .
3. Access Failure .
4. Hold Failure .

3.3.1 Read Failure

Due to process variation read failure occur in SRAM Cell which will given by figure 3.3.1a. When ever reading operation will perform value stored in Bitcell will disturb during reading or not to be read the exact value stored in Bitcell this kind of failure is known as read failure .

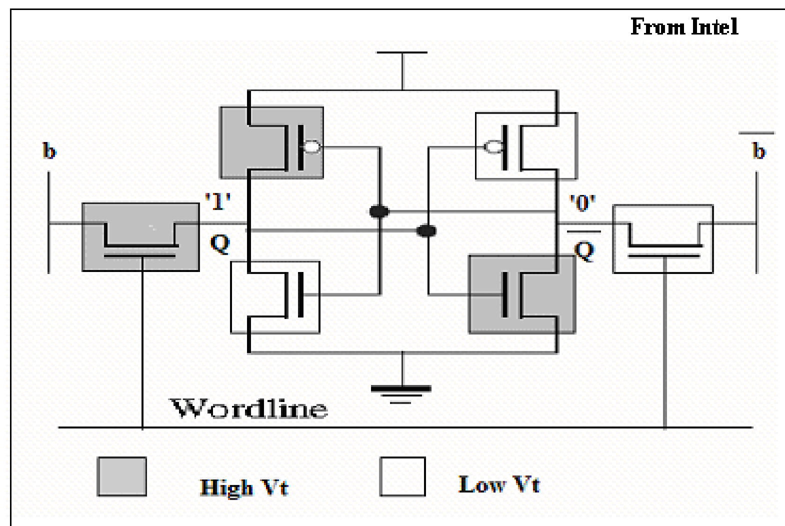


Figure 3.3.1a

Once when we fixed all design constraint then there must not be any type of failure occurred but due to process variation failure will present. Due to this as shown in figure 3.3.1a some of the transistor Vt will increased and some of the transistor Vt will decreased in such condition

as compare ideal case for left sides inverter's Vtn on will reduces and right side inverter's Vtn on will going to increases. These operation will disturb tripping voltage (Vs) of inverters. When designing the transistor sizes for read stability, we must ensure that the stored values are not disturbed during the read cycle. The voltage at node of one storing inverter may drop a little but it should not fall below Vs. To avoid altering the state of the cell when reading, we must control the voltage at node *q* by sizing of inverter transistor and pass transistor appropriately. In theory, the voltage should not exceed Vs, but this design must be carried out with due consideration of process variations and noise. In effect, the read stability requirement establishes the ratio between the two devices.

3.3.2 Write Failure

When we want to store a particular value to bitcell after write cycle value is not stored in cell then this kind of failure is write failure. During write operation we have to change trip point of inverter to change state of bitcell but (as shown in figure 3.3.1a of read operation) due to process variation this tripping point of inverter will change so far voltage applied by us will not sufficient to change the tripping point .

3.3.3 Access Failure

A particular time allotted to perform read write operation but when during these if reading and writing will not be perform these comes under Access Failure. Due to process variation Vt of mos-transistor will effected which will effect access time during reading and writing operation.

3.3.4 Hold Failure

Bit-Cell is generally operated in two mode Read or Write and Retention mode. During retention mode static leakage is measure concert. When bit-cell is not in use then due to leakage a permanent path through vdd to vss will form this will cause a vary serious issue when we inter in to nano-meter regime .Ion to I off ratio will drastically reduces as we inter into nano-meter regime. Higher Ion to I off ratio is define better stability of state of any device.

3.4 Causes of Failure in SRAM

Due parametric fluctuation in SRAM failure will occur. This are given as :

1. During fabrication step within the die if length of access transistor will increases so its vt is also going to increases. Now we can say that we want to make access transistor of given vt but it will be a high vt access transistor . Similarly if length of cell transistor will decreases then also failure may occur .

2. After fabrication strength of transistor may vary in different direction .If strength of transistor will increases then possibility of leakage will also increases .

3.5 Way to Avoid Failure in SRAM

To increases yield percentage we want good working chip as compare bad chip . Without any redundancy and error correction methods yield percentage for memory compiler will vary less (30% or less) after using this techniques yield will be improved up to 70% to 80%. So for improvement of yield we must think after fabrication which type of failure occur most of time .

If we talk in chip level in memory compiler we conclude that for low Vt corner devices will suffer Hold and Read failure and for high Vt corner devices will suffer Access and Write failure most of time .Due to process variation length of devices , strength of transistor or due to any other cause ultimately Vt will going change according to which failure occur . According to Vt variation probabilities of failure in memory compiler is explained in figure 3.5.1a .

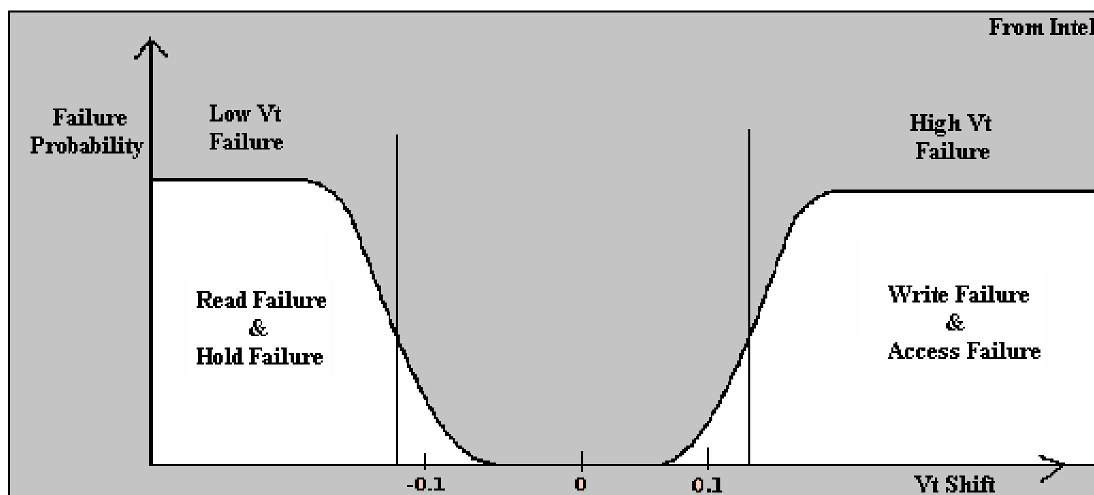


Figure 3.4.1a

So after post silicon process if such kind of failure will occur then by proper compensation it will be avoided. For Write and Access failure we are going for reverse body biasing and For Read and Hold failure we are going for forward body biasing .

CHAPTER 4

P/N Ratio And Stage Ratio Analysis For Driver

4.1 Introduction

Driver is circuit which used to drive data from source point to designation point while doing so data will be in its original form.The CMOS inverter as shown in Fig. 4.1 is basic building block for driver chain . The focus for inverter chain is on the discrepancy between the propagation delay when the output voltage *V*out is switching high-to-low (fall delay time, *τ*PHL) versus switching low-to-high (rise delay time, *τ*PLH). CMOS circuits are generally characterized by the worst case propagation delay. The rise and fall delay times are therefore typically designed to be equal to minimize the worst case delay. The pullup to pull-down ratio *Wp*/*Wn* between the channel width of the PMOS and NMOS transistors at which the rise and fall delay times are equal (*τ*PHL = *τ*PLH) is referred to as the *optimal Wp*/*Wn* ratio (also denoted as *β*opt) in the following sections.

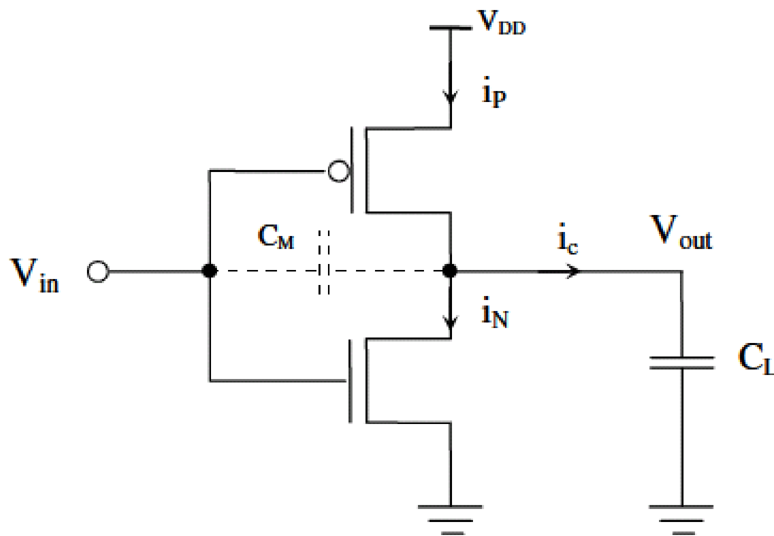


Figure 4.1

This optimal Wp/Wn ratio is typically considered to be independent of design parameters such as the load capacitance CL and input transition time τ. As discussed in this paper, however, due to parasitic impedances and imbalances between the pull-up and pull-down paths, the rise and fall delays differ so that the Wp/Wn ratio should be adjusted to restore the balance.

4.2 Theoretical Background

The switching characteristics of a CMOS inverter are analyzed in this section with a focus on those conditions that produce a difference between the rise and fall delay times. These delay times are described under ideal conditions in Sec. 4.2.1.

4.2.1. Idealized conditions

Under the assumption of a step input voltage, the delay time is the time required for the output voltage to reach half of the supply voltage $V50\%$ (from either zero or VDD). The analysis is based on the classic expression for the current through a capacitor is given by figure (4.2.1).

$$i_c(t) = C \cdot \frac{dV_c(t)}{dt} \quad \text{(4.2.1)}$$

Applying (4.2.1) at the load capacitance of a CMOS inverter, the rise and fall propagation delay times are obtained which will given by equation (4.2.2) and equation (4.2.3).

$$\tau_{\text{PLH}} = \frac{C_L \cdot \Delta V_{LH}}{I_{\text{avg}LH}} = \frac{C_L \cdot V_{50\%}}{I_{\text{avg}LH}}, \quad \text{(4.2.2)}$$

$$\tau_{\text{PHL}} = \frac{C_L \cdot \Delta V_{HL}}{I_{\text{avg}HL}} = \frac{C_L \cdot (V_{DD} - V_{50\%})}{I_{\text{avg}HL}}, \quad \text{(4.2.3)}$$

where $IavgHL$ and $IavgLH$ are the average currents, respectively, to discharge and charge a lumped load capacitance CL.The transient behavior of a CMOS inverter can be described by five regions of operation of the two MOSFET transistors. Assuming idealized conditions, only one MOSFET transistor conducts during each transition while the other transistor is immediately turned off by the step input voltage. Under this simplified condition, delay

expressions for the rising and falling transitions of the output voltage are given by equation (4.2.4) and equation (4.2.5).

$$\tau_{\text{PLH}} = \frac{C_L}{k_p(V_{DD} - |V_{Tp}|)} \left[\frac{2 \cdot |V_{Tp}|}{V_{DD} - |V_{Tp}|} + \ln\left(\frac{4(V_{DD} - |V_{Tp}|)}{V_{DD}} - 1 \right) \right], \quad \text{--- (4.2.4)}$$

$$\tau_{\text{PHL}} = \frac{C_L}{k_n(V_{DD} - V_{Tn})} \left[\frac{2V_{Tn}}{V_{DD} - V_{Tn}} + \ln\left(\frac{4(V_{DD} - V_{Tn})}{V_{DD}} - 1 \right) \right], \quad \text{---- (4.2.5)}$$

4.3 P/N RATIO ANALYSIS

4.3.1 Introduction

Static CMOS gates are a "ratioless" circuit family, meaning that the gates will work correctly for any ratio of PMOS sizes to NMOS sizes. However, the ratios do influence switching threshold and delay, so it is important to optimize the P/N ratio for high speed designs. The aim of this experiment is to determine the best p/n ratio for optimizing the delay. The setup for implementing this experiment is an inverter chain where each stage is driving a same amount of load. The p/n ratio of inverters is varied continuously in a definite step & the plots of different parameters versus p/n are obtained.

Normal symmetric inverters have equal rise and fall resistances. However, this is not optimal for average circuit delay. By using a smaller P/N ratio, the input load can be significantly reduced while only somewhat slowing the rising output. Thus, the average delay of a gate decreases, though the rise and fall times become unbalanced. Consider an inverter driving a fanout of f with an NMOS transistor sized at one unit and a PMOS transistor sized bita times larger, as shown in Figure 4.3.1 a Suppose the gate has equal rise and fall times for bita = k = (i.e. 1.45). Neglect parasitic capacitances because they turn out to not affect the conclusions.

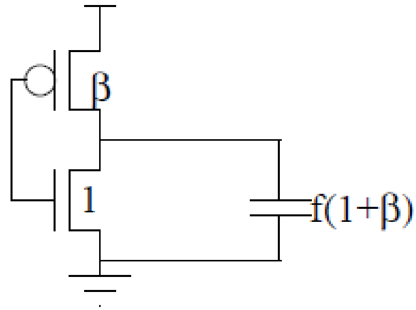


Figure 4.3.1 a

The falling delay is f(1+bita) t. The rising delay is (k/ bita) f(1+ bita) t. Thus, the average delay of the inverter is given as equation 4.3.1 as :

$$\frac{1}{2}f(1+\beta)\left(1+\frac{k}{\beta}\right)\tau \quad \text{-------------------------(4.3.1)}$$

We can solve for the P/N ratio bita that minimizes delay by taking the derivative and setting it to zero which given by equation 4.3.2 as :

$$\frac{dDelay}{d\beta} = 0 = \frac{RC}{2}f\left(1-\frac{k}{\beta^2}\right) = 0 \Rightarrow \beta = \sqrt{k} \quad \text{-----(4.3.2)}$$

Therefore, the optimal P/N ratio to minimize average path delay is the square root of the ratio that gives equal rise/fall resistances.

4.3.2 Analysis steps

We are performing P/N ratio analysis in two steps , which are explained as :

1. In first step tacking a constant width of NMOS devices and the for various value of width of PMOS devise we find various value P/N ratio . Finally P/N ratio which will give optimal delay or P/N ratio with minimum average delay will be selected.

2. In second step when we got a particular value of P/N ratio which will give minimum delay then for this value of P/N ratio we are going to vary width of NMOS from it's minimum value. From this analysis we come to know that in which width of NMOS will give minimum average delay. Each stage is an inverter & driving a same amount of load (5 inverters fan out).For P/N ratio analysis setup is given by figure 4.3.2a.The load is defined by the configuration shown in figure 4.3.2b.

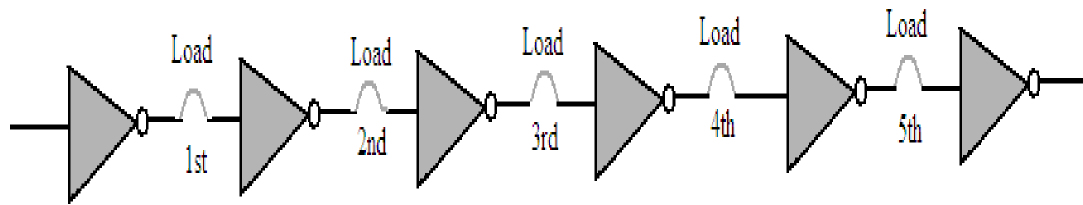


Figure 4.3.2a

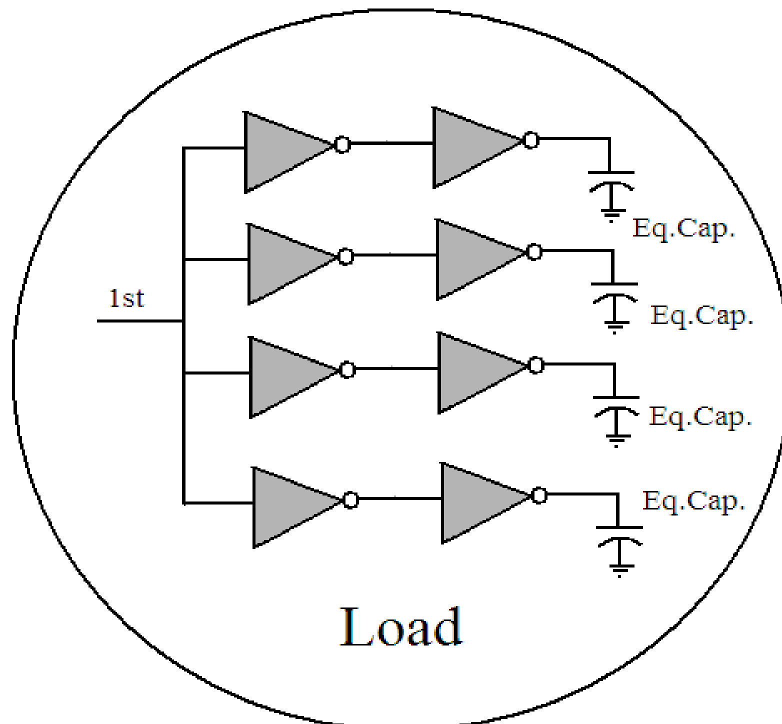


Figure 4.3.2b

4.3.3 MEASUREMENTS DONE

The parameters which are to be measured are

- Rise delay

    Time required in which inverters output will changes from 10%Vmax of initial to 90% Vmax value .

- Fall Delay

    Time required in which invert output will changes from 90% Vmax to 10% Vmax value.

- Average Delay

    Threshold values for calculating delay are 50% value vh, where vh is the max voltage, defined as 1.1V.

- Average current

    The average current is measured as the total amount of current drawn from the supply over the transient pulse time.

4.3.4 SIMULATION CONDITIONS

Apply transient pulse with defined time period at the input. Different process ,voltage and temperatures conditions are typical model corner for Standard Vt , Low Vt and High Vt devices .For different Standard Vt , Low Vt and High Vt devices model parameters are different according to which we are going to simulate this all conditions and corner cases separately .

4.3.5 MEASUREMENT TECHNIQUE:

4.3.5.1 Width of pmos = wp ,Width of nmos = wn

Pn ratio is defined by Wp/Wn.

Keep wn as constant for all the inverters & vary wp.

This way we are changing P/N ratio.

For each value of P/N ratio we are going to measure different delays.

4.3.5.2 Width of pmos = wp ,Width of nmos = wn

Pn ratio is defined by Wp/Wn.

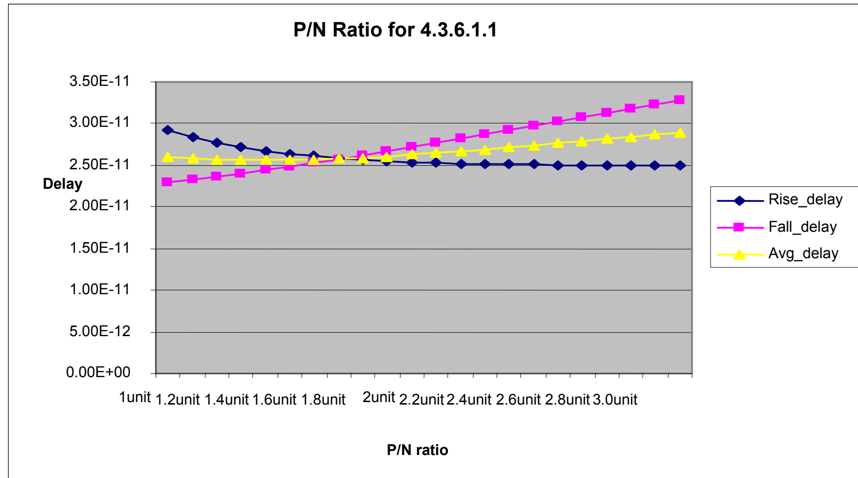
Vary Wn from min value then Wp vary accordingly.

Fix the value of P/N ratio find from step 4.3.5.1

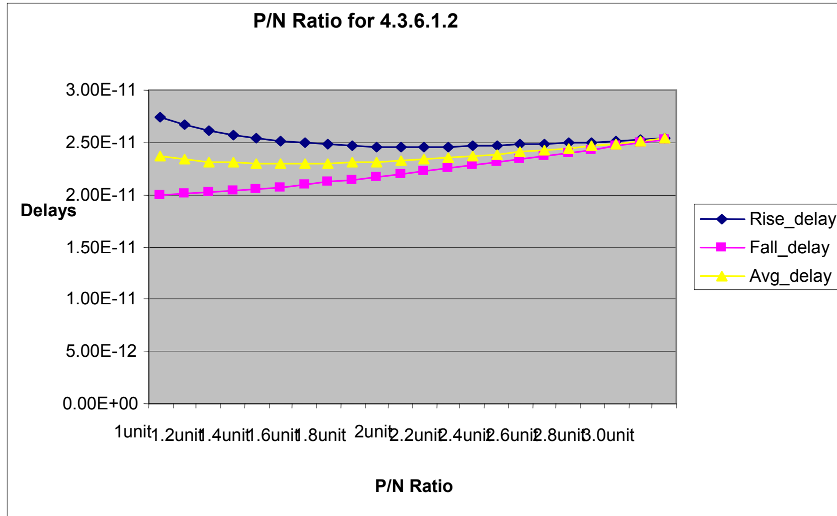
For various value of width of NMOS and PMOS measure all the parameters as mentioned in previous setup.

4.3.6 RESULTS :

4.3.6.1.1 P/N ratio analysis for Best Corner (1.32v, 170c) with fanout-5 and three sigma of svt devices .



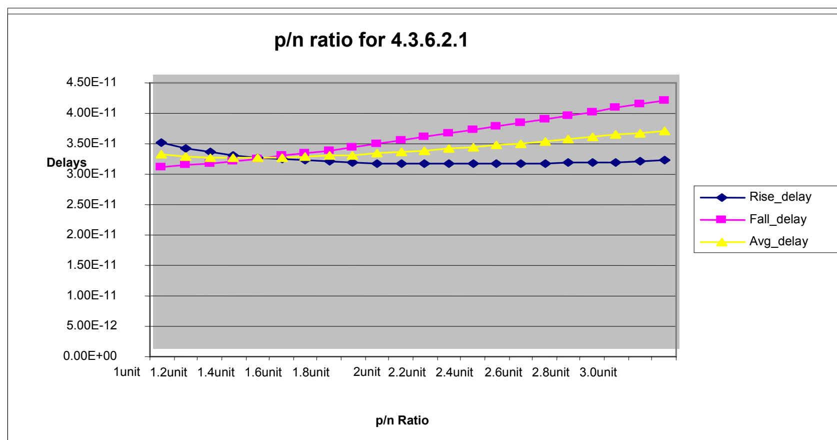
4.3.6.1.2 P/N ratio analysis for Best Corner (1.32v, -40c) with fanout-5 and three sigma of svt devices .



Summary :

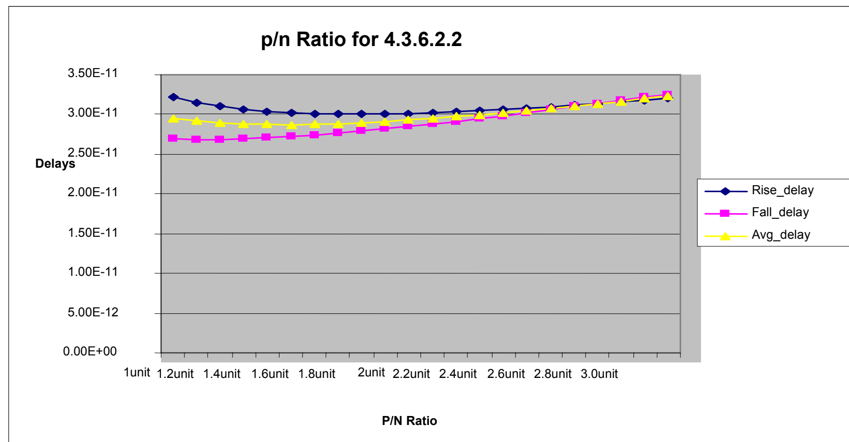
P/N	Rise_Delay	Fall_Delay	Avg_Delay	Process	Voltage	Temp
1.4unit	2.67E-11	2.44E-11	2.56E-11	FF	1.32	170
1.5unit	2.51E-11	2.07E-11	2.29E-11	FF	1.32	-40

4.3.6.2.1 P/N ratio analysis for Typical Corner (1.32v, 170c) with fanout-5 and three sigma of svt devices.



4.3.6.2.2 P/N ratio analysis for Typical Corner (1.32v, -40c) with fanout-5 and three

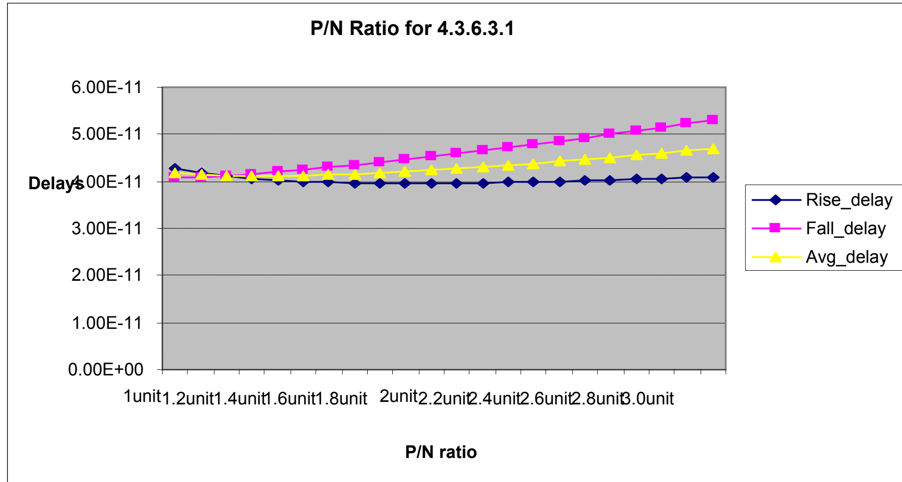
sigma of svt devices.



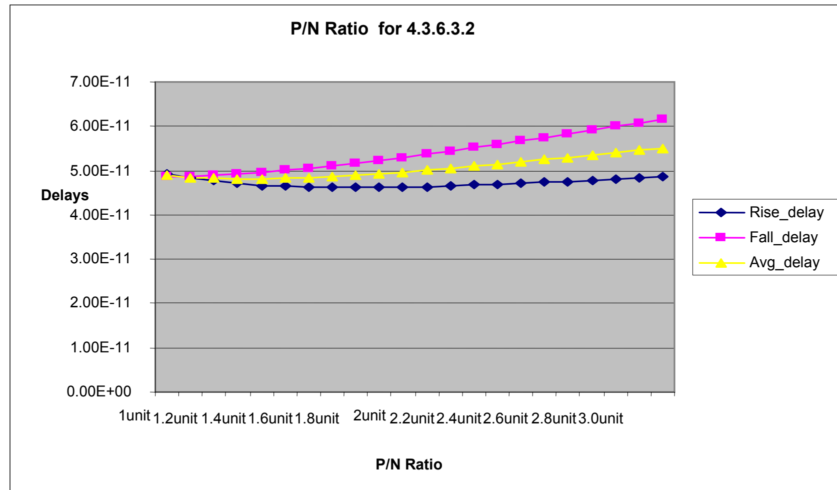
Summary :

P/N	Rise_Delay	Fall_Delay	Avg_Delay	Process	Voltage	Temp
1.4unit	3.27E-11	3.26E-11	3.26E-11	TT	1.32	170
1.5unit	3.02E-11	2.72E-11	2.87E-11	TT	1.32	-40

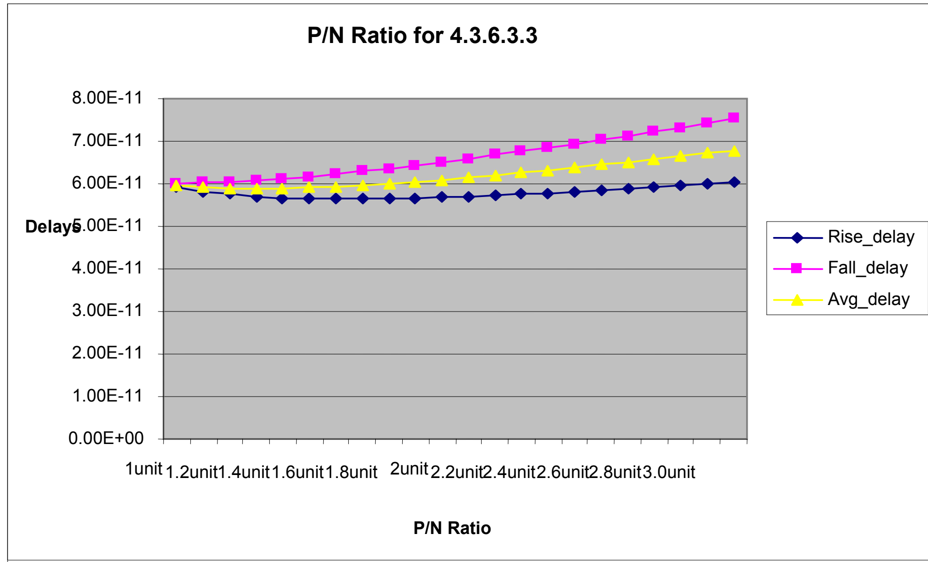
4.3.6.3.1 P/N ratio analysis for Worst Corner (1.32v, 170c) with fanout-5 and three sigma of svt devices.



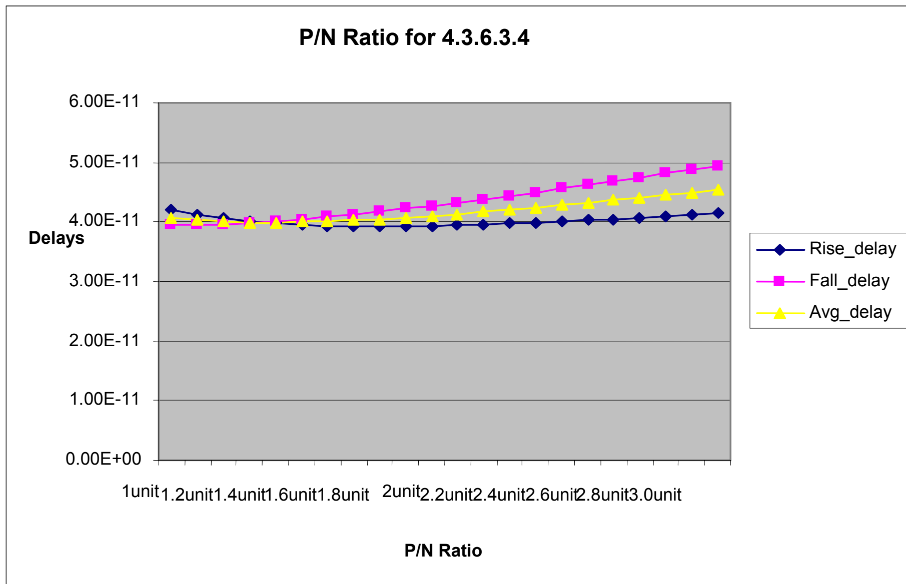
4.3.6.3.2 P/N ratio analysis for Worst Corner (1.2v, 170c) with fanout-5 and three sigma of svt devices.



4.3.6.3.3 P/N ratio analysis for Worst Corner (1.08v, 170c) with fanout-5 and three sigma of svt devices.

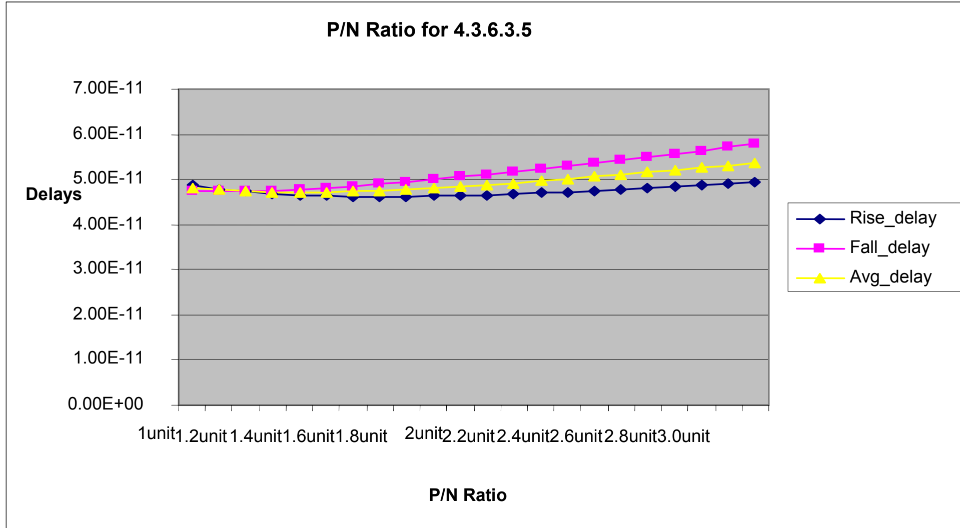


4.3.6.3.4 P/N ratio analysis for Worst Corner (1.32v, 105c) with fanout-5 and three sigma of svt devices.

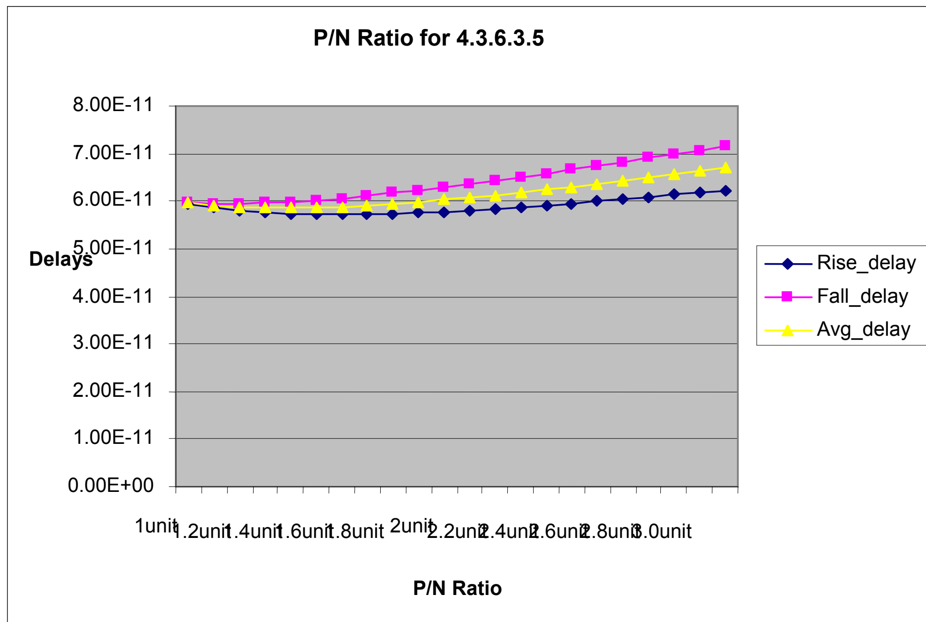


4.3.6.3.5 P/N ratio analysis for Worst Corner (1.2v, 105c) with three sigma analysis

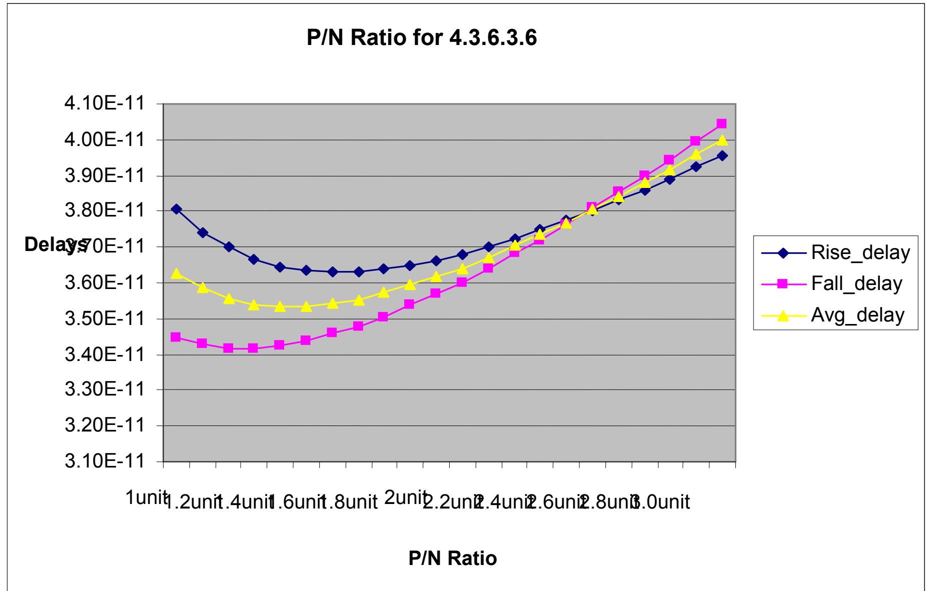
of svt devices.



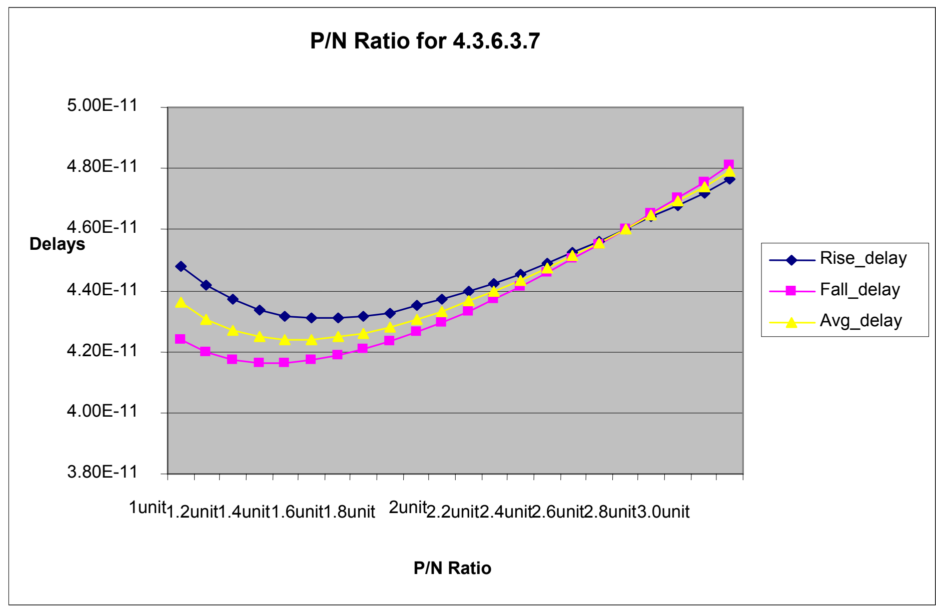
4.3.6.3.5 P/N ratio analysis for Worst Corner (1.08v, 105c) with three sigma fanout-5 and of svt devices.



4.3.6.3.6 P/N ratio analysis for Worst Corner (1.32v, -40c) with three sigma fanout-5 and of svt devices.



4.3.6.3.7 P/N ratio analysis for Worst Corner (1.2v, -40c) with three sigma and fanout-5 of svt devices.



Summary :

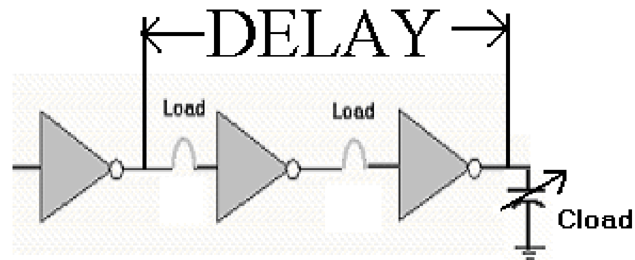
P/N	Rise_Delay	Fall_Delay	Avg_Delay	Process	Voltage	Temp
1.3unit	4.07E-11	4.16E-11	4.11E-11	SS	1.32	170
1.4unit	4.67E-11	4.96E-11	4.81E-11	SS	1.2	170
1.3unit	5.70E-11	6.08E-11	5.89E-11	SS	1.08	170
1.4unit	3.98E-11	4.01E-11	3.99E-11	SS	1.32	105
1.4unit	4.65E-11	4.78E-11	4.72E-11	SS	1.2	105
1.4unit	5.73E-11	5.99E-11	5.86E-11	SS	1.08	105
1.4unit	3.64E-11	3.42E-11	3.53E-11	SS	1.32	-40
1.4unit	4.32E-11	4.16E-11	4.24E-11	SS	1.2	-40
1.5unit	5.47E-11	5.43E-11	5.45E-11	SS	1.08	-40

4.4 STAGE RATIO ANALYSIS

4.4.1 DESCRIPTION :

The aim of this part of project is to determine the sizing ratio between two inverters in a chain to optimize the delay. The simple setup for such experiment is shown below. The o/p stage inverter sizes is varied from ratio one to onwards with different loads & examine the average delay for each stage ratio with different loads.

4.4.2 SETUP :



4.4.3 MEASUREMENTS DONE :

The parameters which are to be measured are

- Rise delay,
- Fall Delay,
- Average Delay

4.4.4 SIMULATION CONDITIONS :

Apply transient pulse with defined time period at the input. The PVT conditions are typical ,worst and best case model corner svt,lvt and hvt devices. Simulations are done at different load conditions which are varying from 50ff to 200 ff.

4.4.5 MEASUREMENT TECHNIQUE:

Width of pmos for inverter = wp , Width of nmos for inverter = wn

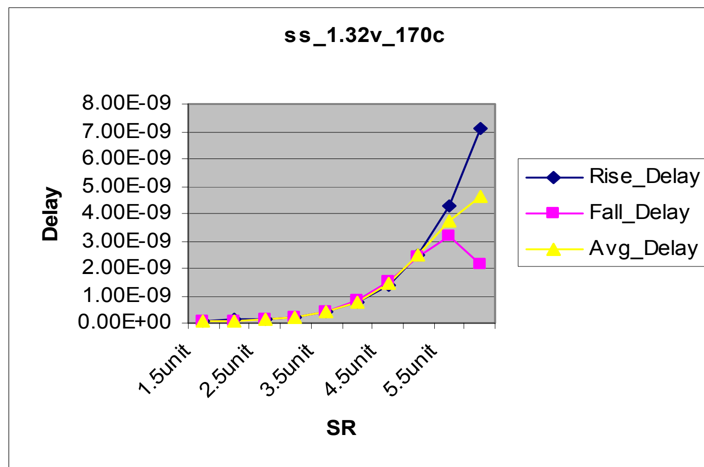
Vary wp & wn both by a fixed ratio. (Known as stage ratio)

This way we are changing Stage ratio.

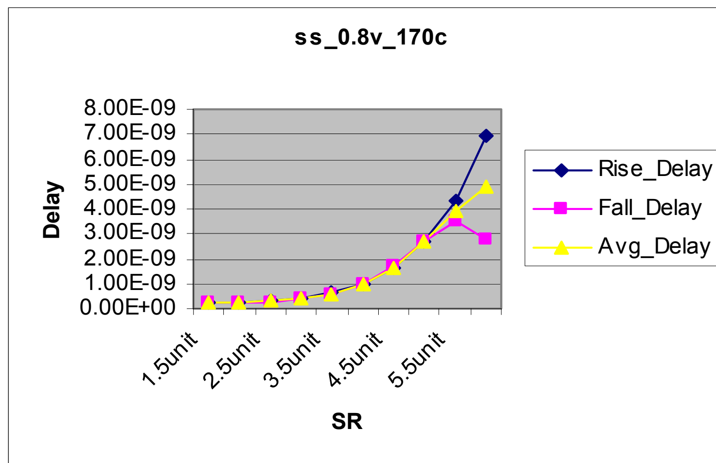
During each stage ratio, measurement is carried out for each parameter at different load conditions. The loads at which simulations carried out are 50ff, 100ff, 150ff, 200ff.

4.4.6 RESULTS:

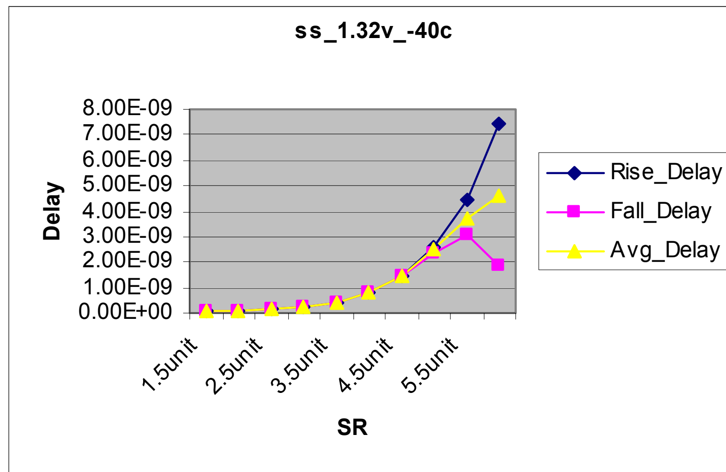
4.4.6.1.Stage ratio analysis for wcs 4 stage of inverter with p/n ratio of 1.5 and load capacitance is 50ff for svt devices voltage supply 1.32v and temperature 170c .



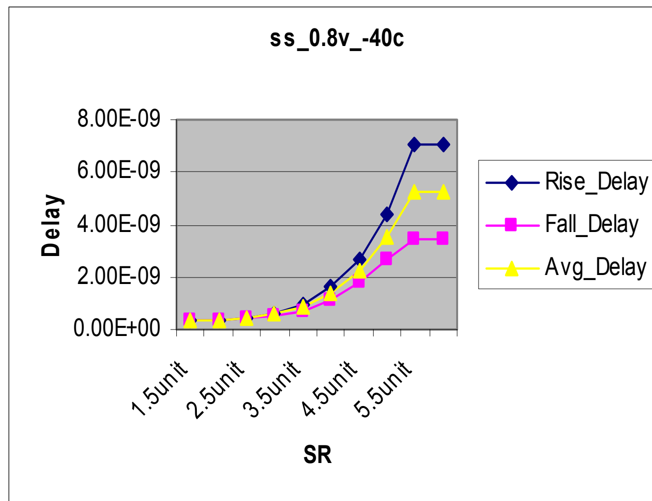
4.4.6.2. Stage ratio analysis for wcs , 4 stage of inverter with p/n ratio of 1.5 and load capacitance is 50ff for svt devices voltage supply 0.8v and temperature 170c.



4.4.6.3. Stage ratio analysis for wcs , 4 stage of inverter with p/n ratio of 1.5 and load capacitance is 50ff for svt devices voltage supply 1.32v and temperature -40c.



4.4.6.4. Stage ratio analysis for wcs , 4 stage of inverter with p/n ratio of 1.5 and load capacitance is 50ff for svt devices voltage supply 0.8v and temperature -40c.



Summary :

I have done stage ratio analysis for worst and best case corner with different load as 50ff,100ff,150ffand 200ff .These all analysis is done for four stage inverter for svt ,lvt and hvt devices .From worst and best case result we conclude that optimized value of inverter stage ratio is laid between 2 and 2.5.

Chapter 5

Memory Compiler

5.1 Introduction

Complete compilers consist of various generators to satisfy the requirements of the circuit at hand. Each of the final building block, the physical layout, will be implemented as a stand-alone, densely packed, pitch-matched array. Using this complex layout generator and adopting state-of-the-art logic and circuit design technique ,Memory cells can realize extreme density and performance. In each layout generator, we added an option which makes the aspect ratio of the physical layout selectable so that the designers can choose the aspect ratio according to the convenience of the chip level layout. Each memory compiler is a set of various, parameterized generators. The generators are:

• Layout Generator : Generates an array of custom, pitch-matched leaf cells.

• Schematic Generator & Netlister : Extracts a netlist which can be used for both LVS check

and functional verification.

• Function & Timing Model Generators : For gate level simulation, dynamic/static timing analysis and synthesis.

• Datasheet Generators : In this portion datasheet for timing and power analysis will prepared .

• Critical Path Generator : There are many special purpose generators such as critical path generator used for both circuit design and AC timing characterization.

For generating these Different view a flow must be needed in which according to configuration of memory (Instances of memory) needed will be generated .

5.2 Memory Compiler Selection

The size of a memory cell is defined by its number of words (WORDS) and number of bits per word (BPW). But, this size is only a logical size. The physical size of a memory is defined by the number of rows (ROWS) and the number of columns (COLS) of its bit cell array. Usually, we can't make the bit cell array with WORDS and BPW because the range of WORDS is much larger than the range of BPW. If we make the bit cell array with WORDS and BPW, most of memory layouts will have too tall and too thin aspect ratio. Therefore, column decoder and y-mux circuit are included in most of memory cells to adjust the aspect ratio.

In memory compilers, the y-mux type selecting option was added to give the customers freedom selecting aspect ratio of the memory layout. Many of the characteristics of a memory cell are depend on its y-mux type. So, when you change the y-mux type from one to the other to change the aspect ratio, you have to know that it will change many major characteristics, such as access time, area and power consumption, of the memory.

According to y-mux type aspect ratio selection will be explained by figure 5.2.a

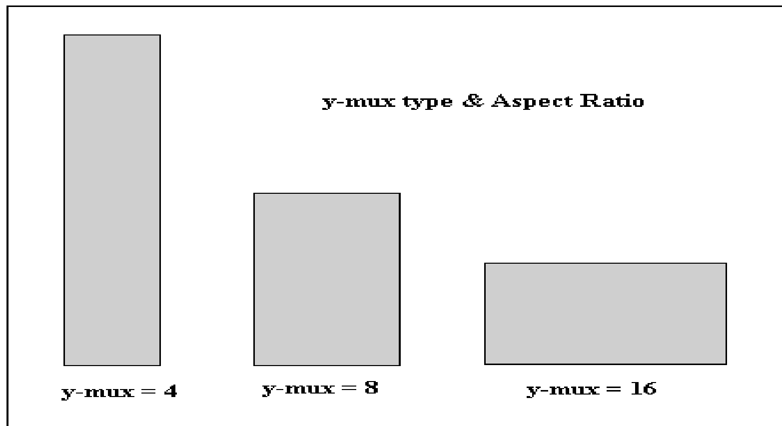


Figure 5.2.a

5.3 Generators and Cell Configuration

Single port synchronous RAM generator's block diagram as shown in figure 5.3.a .

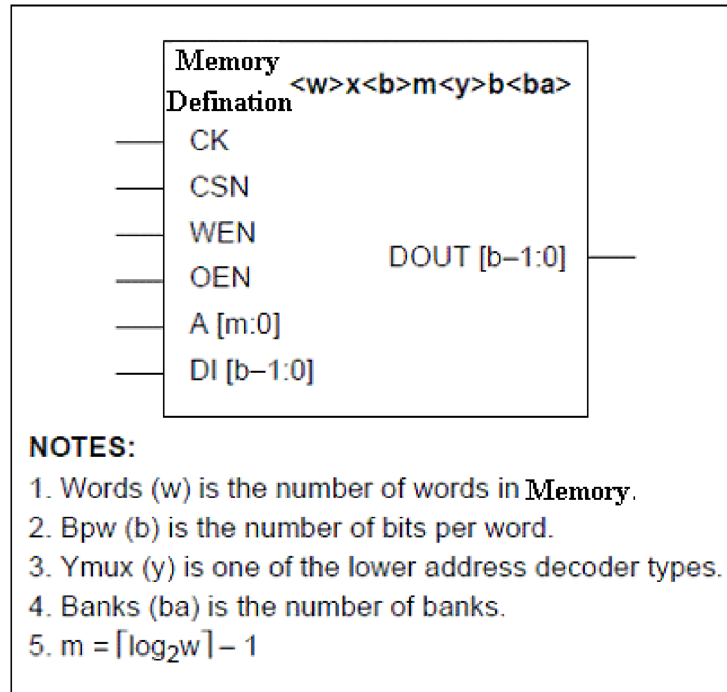


Figure 5.3 a

Memory Gen. generates layout, netlist, symbol and functional & timing model of Memory Gen. The layout of Memory Compiler is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of Memory Compiler, you can give certain values to following four generator parameters:

• Number of words (w)

• Number of bits per word (b)

• Lower address decoder type (y)

• Number of banks (ba).

The valid range of this parameter is specified in table 5.3.1a

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

Table 5.3.1a

Description of pin as given in figure 5.3.a is given as :

1. CK : It is an input pin , “Clock” serves as the input clock to the memory block. When

CK is low, the memory is in a precharge state. Upon the rising edge, an access begins.

2. CSN : "Chip Select Negative" acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur .CSN may not change during CK is high.

3. WEN : "Write Enable Negative" selects the type of memory access. Read is the high state, and write is the low state.

4. OEN : "Output Enable Negative" controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.

5. A[ ] : "Address" selects the location to be accessed. A [ ] may not change during CK is high.

6. D[ ] : When CK rises while WEN is low, the "Data In" word value is written to the the accessed location.

7. DOUT [] : During the read access data world stored will be presented to the Data Out ports. Data out is tri –statable .When CLK is high CSN is low and ONE is low ,only then DOUT drives certain values. Other wise DOUT kept in high -Z state .During write access the value of DOUT will un predictable.

Configuration selection according to no of block or banks used is shown by figure 5.3.b . & figure 5.3.c .

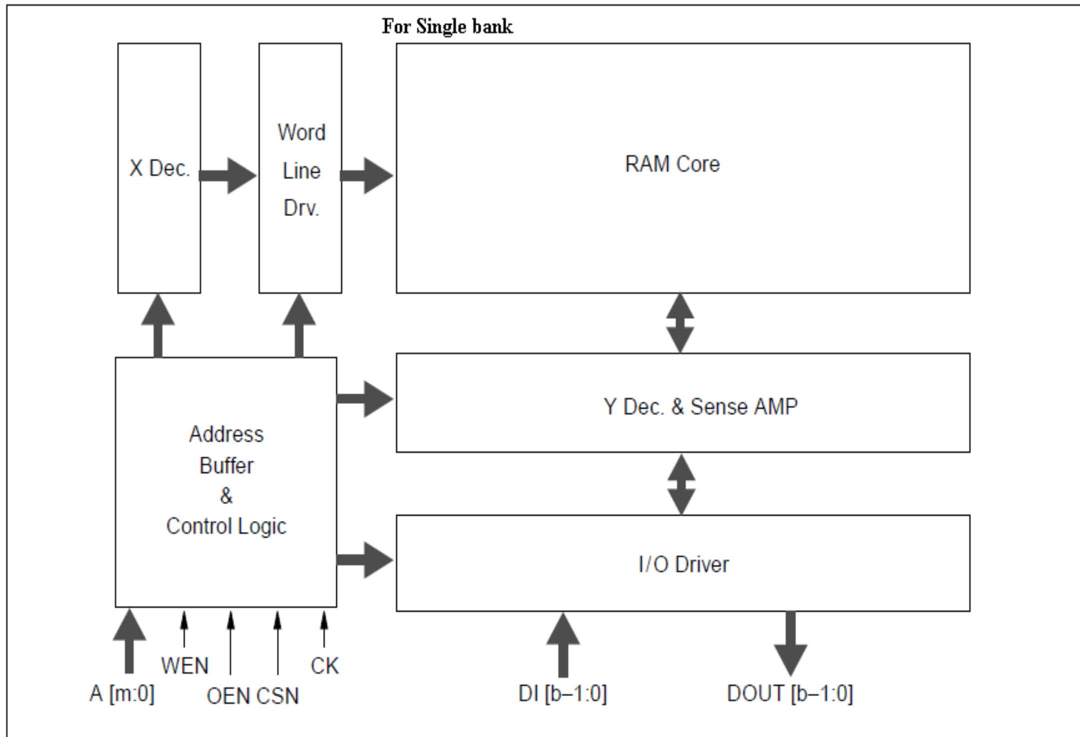


Figure 5.3.b

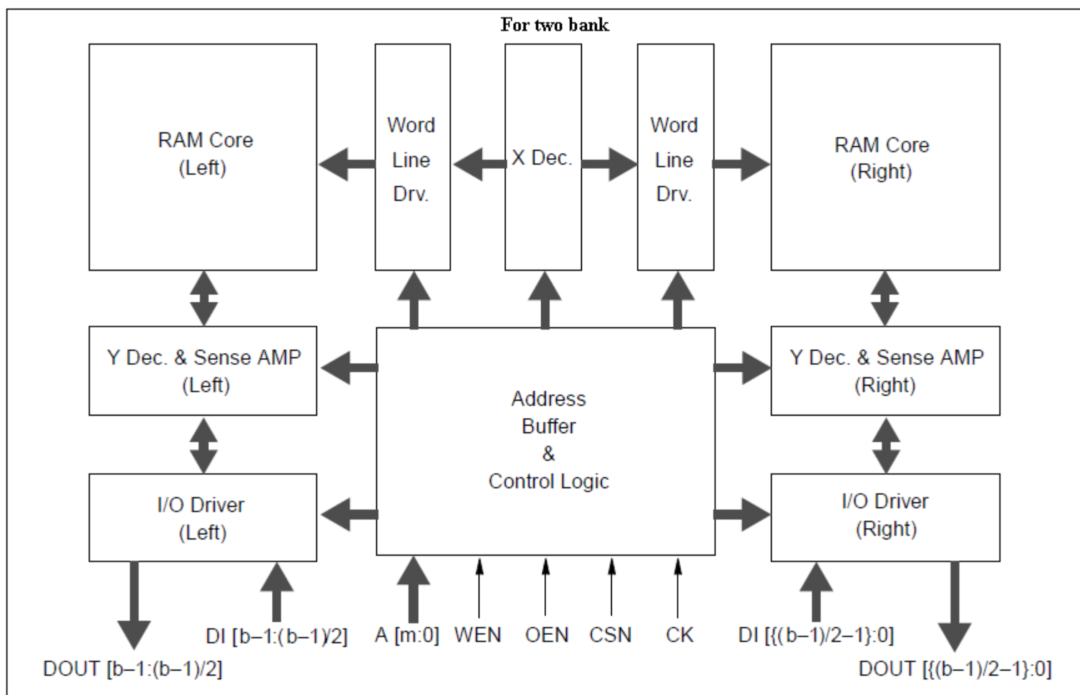


Figure 5.3.c

To enlarge the capacity of Memory, we added one more option to choose number of banks. If we want to use larger Memory than 64K bit Memory , we can select dual bank (ba = 2). We can also select dual bank for smaller one than 64K bit Memory. Dual bank Memory is a little bigger and a little faster than single bank one. One Classical Relation for memory compiler will shown as by equation 5.1 and equation 5.2.

No. of Word Line = Physical Row * Column Mux 5.1

No. of Column = Physical Column * Column Mux 5.2

5.4 Pre layout Simulation Result

Pre layout Simulation with Netlist level Extraction

Access Time analysis of Different instances

2	CMOS65LP	AMS2.10	Pwcs30V100V100T105		
3	c65lp_ram_w04096b016b1c08/16				
4					
5					
6					
7	Acess time pins	CMUX 8	CMUX 16	DIFF	PERCENTAGE_DEVIATION
8	access{"tcq_q0_r"}{2}{6}	7.2471	3.9746	3.2725	45.16
9	access{"tcq_q0_f"}{2}{6}	7.3653	3.9616	3.4037	46.21
10	access{"tcq_q7_r"}{2}{6}	7.2471	3.9746	3.2725	45.16
11	access{"tcq_q7_f"}{2}{6}	7.3653	3.9616	3.4037	46.21
12	access{"tcq_q8_r"}{2}{6}	7.2514	3.9792	3.2722	45.13
13	access{"tcq_q8_f"}{2}{6}	7.3676	3.9664	3.4012	46.16
14	access{"tcq_q15_r"}{2}{6}	7.2514	3.9792	3.2722	45.13
15	access{"tcq_q15_f"}{2}{6}	7.3676	3.9664	3.4012	46.16
16					
17					
18					
19	Note:				
20	Access time comparison result with the change of column mux option				
21					
22	45% timing improvments when we are going from cmux8 to cmux16 .				

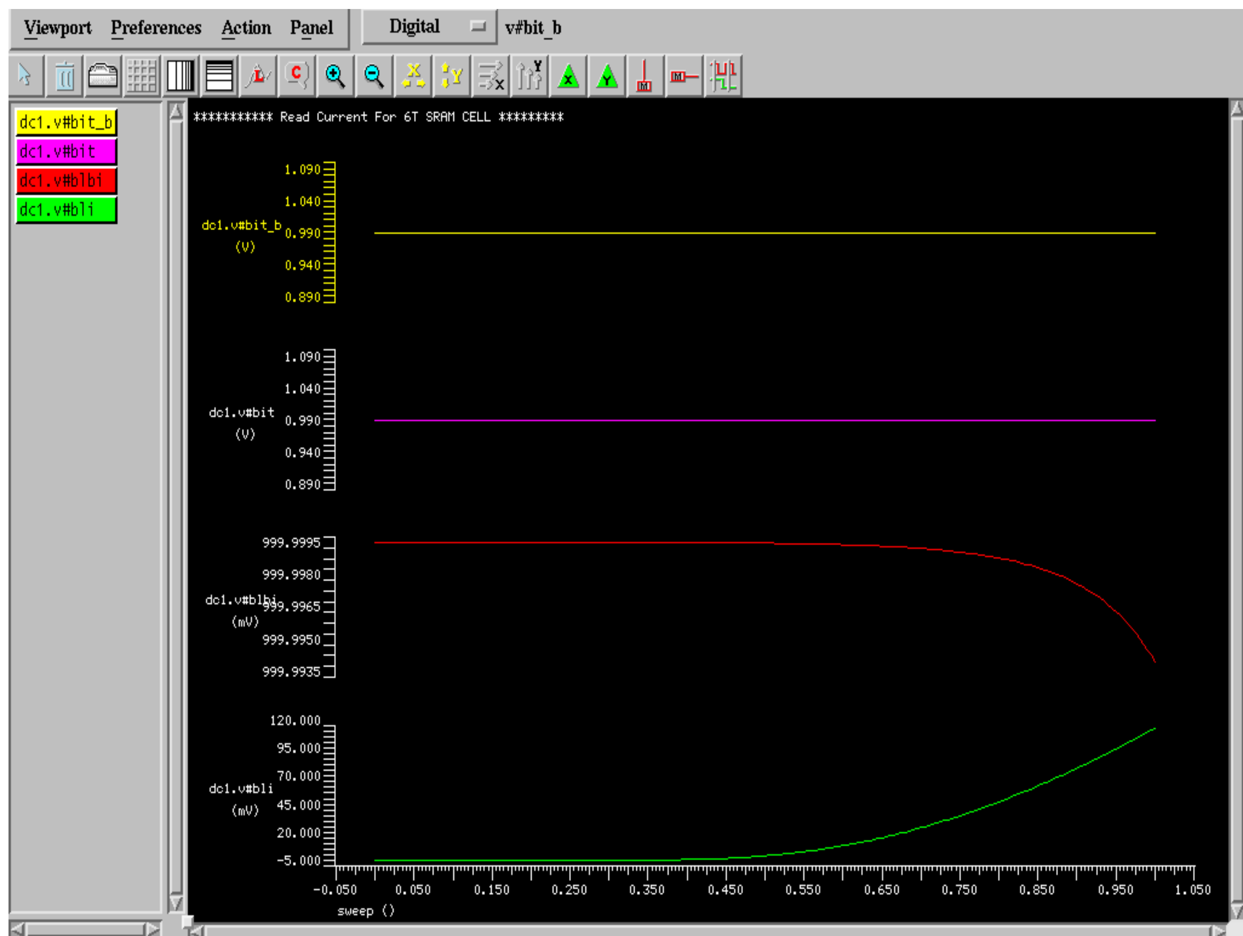
Chapter 6

Appendix A

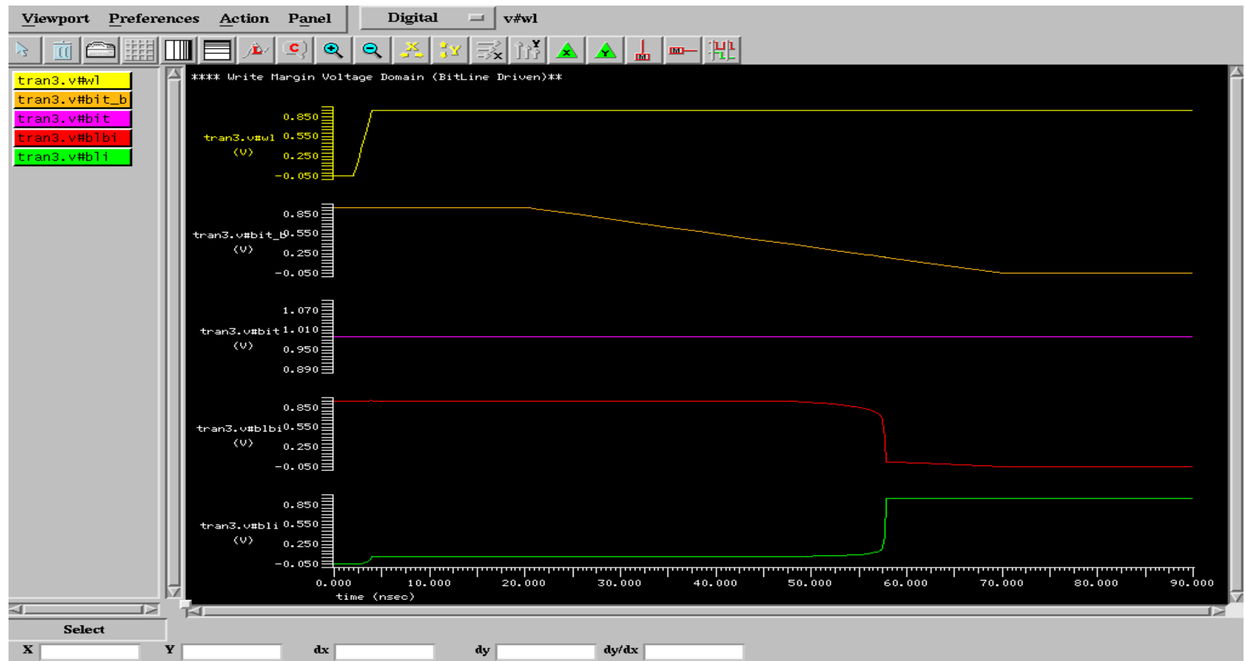
6.1 Simulation Results and Spice Code

6.1.1 SRAM 6T Cell Operation

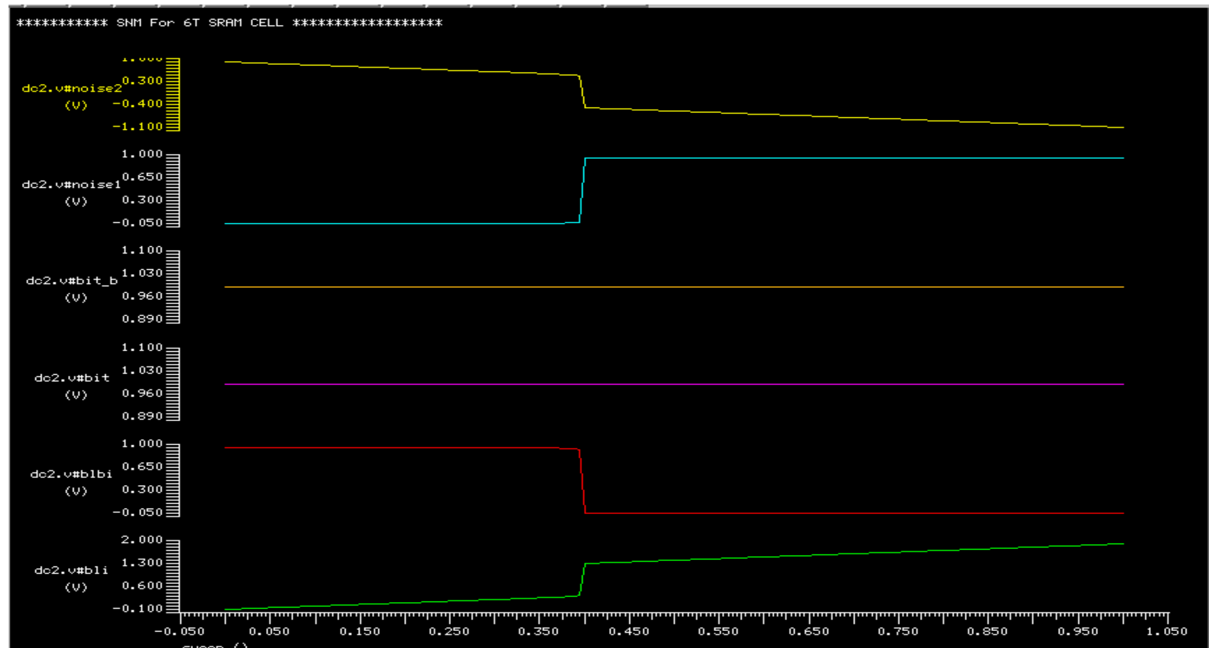
6.1.1a Read Operation



6.1.1b Write Operation



6.1.1c Static Noise Margin



6.2 Driver Design Analysis

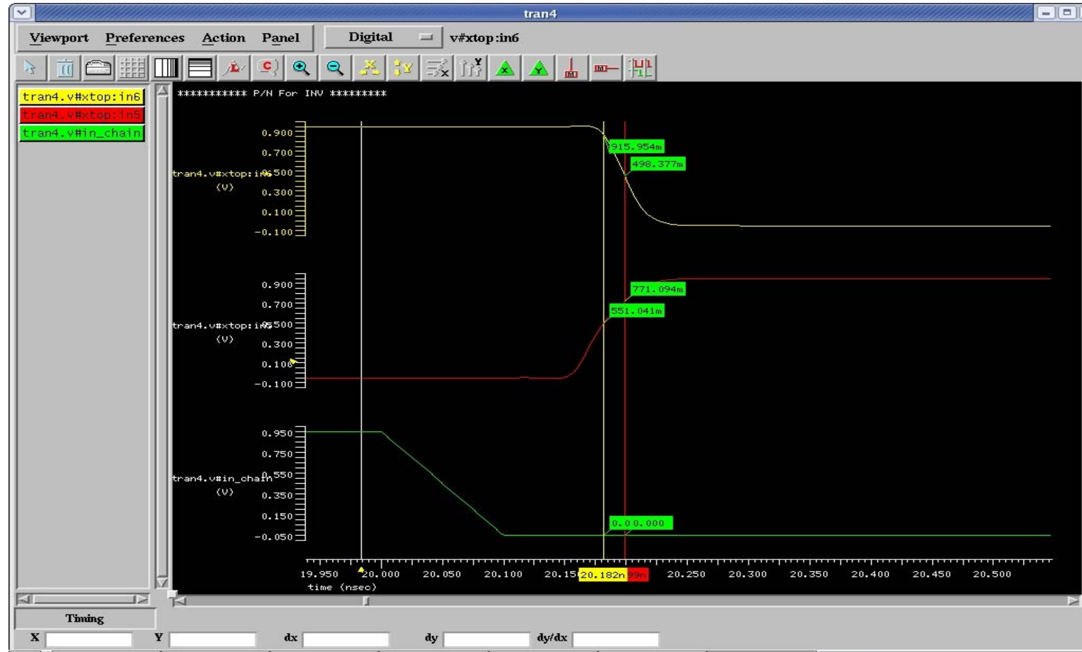
6.2.1.1 P/N ratio Analysis with fixed wn

6.2.1.1a For 1.4 P/N ratio Fall Delay Analysis :

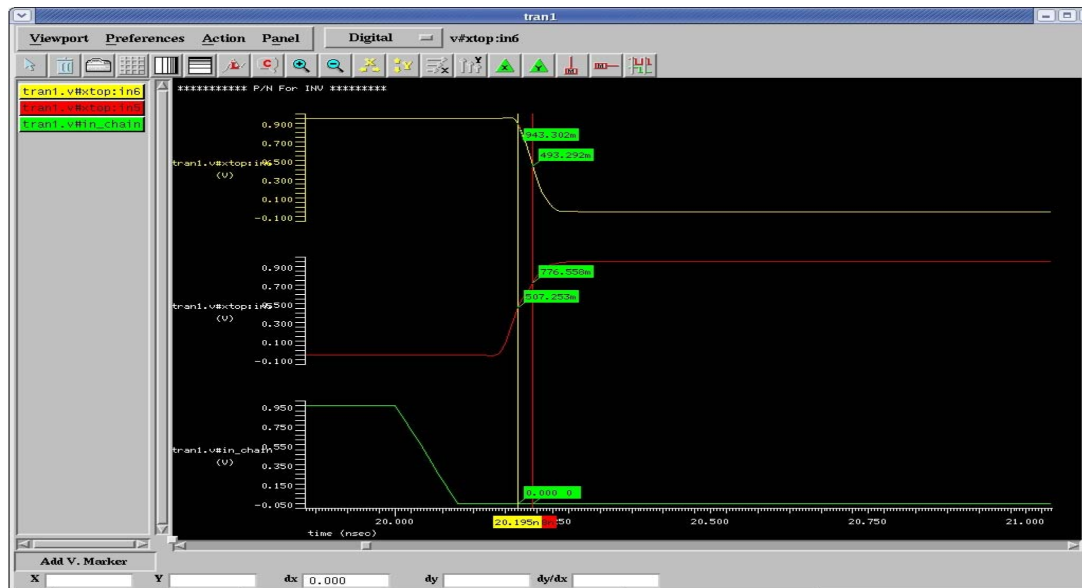
6.2.1.1b For 3 P/N ratio Fall Delay Analysis :

6.2.1.2 P/N ratio Analysis with variable wn

6.2.1.2a For 1.4 P/N ratio with 2 wn Fall Delay Analysis :



6.2.1.2b For 1.4 P/N ratio with 0.25 wn Fall Delay Analysis :



6.3 Spice Code For Various Analysis of SRAM Cell

6.3.1 For Read current Analysis

```
*********** OPTIONS *******************************
.options temp=25
.options dcmethod=newton
*.options scale=1e-06
*.options reltol=0.001

*********** INCLUDES ******************************
.include ../setup_mica/models.lib
.include ../setup_mica/orig_bitcell.cir
.include ../setup_mica/voltages.txt

*********** PARAMS   ******************************
.par data  0
.par gnd   0
.par param_mismatch 0

*********** INITIALIZE ****************************
.nodeset v(bli)=(vddv*data)
.nodeset v(blbi)=(vddv-data*vddv)
.nodeset v(bit)=(vddv)
.nodeset v(bit_b)=(vddv)

*********** SOURCES *******************************
.ground  0
.global  vdd vss gnd
```

```
vvdd vdd 0 dc vddv
vvss vss 0 dc 0
vwl wl 0 dc 0
vbit bit 0 dc vddv
vbit_b bit_b 0 dc vddv
.dc vwl 0 vddv 0.005

*********** MEASURES ******************************
.meas dc access_current max abs(m:xPG:1#id)
.meas dc source_current max abs(m:xPG:1#is)
.meas dc gate_current   max abs(m:xPG:1#ig)
.meas dc bulk_current   max abs(m:xPG:1#ib)

*********** CONTROL STATEMENTS ********************
*.control
*delete all
*destroy all
*set noaskdelete
*save all
***foreach vddv  1.3 1.1 1.0 0.9
*foreach vddv  1.0
*dc vwl 0 vddv 0.005
*plot viewport "VWL" linplot v#wl xlimit 0 1.4
*plot viewport "vbli" linplot v#bli xlimit 0 1.4
*plot viewport "Read Current of 6T SRAM CELL" linplot abs(m:xPG:1#id) xlimit 0 1.4
*end foreach
*.endc
```

6.3.2 For Power Analysis

```
*********** SOURCES ******************************
.ground  0
.global  vdd vss gnd
vvdd vdd 0 dc vddv
vvss vss 0 dc 0
vbit bit 0 dc vddv
vbit_b bit_b 0 dc vddv
vwl wl 0 pwl(0n 0 15n 0)

*********** MEASURES ******************************
.meas tran drain_PG    avg abs(m:xPG:1#id)
.meas tran drain_PU_M7 avg abs(m:xM7:1#id)
.meas tran drain_PU    avg abs(m:xPU:1#id)

.meas tran ipower avg abs(vvdd#i)
.meas tran ivss avg abs(vvss#i)
.tran 0.01n 15n
```

6.3.3 For SNM Analysis

```
*********** SOURCES ******************************
.ground  0
.global  vdd vss gnd
```

```
vvdd vdd 0 dc vddv
vvss vss 0 dc 0
vwl wl 0 dc vssv
vbit bit 0 dc vddv
vbit_b bit_b 0 dc vddv
vnoise bli noise1
e1 blbi noise2 bli noise1 1
.dc vnoise 0 vddv 0.005
*********** MEASURES ******************************
.meas dc noise1flip trig at=0ns targ v(noise1) val=vdd50 rise=1
.meas dc blbiflip   trig at=0ns targ v(blbi)   val=vdd50 fall=1
.meas dc crossing_point when v(blbi)=v(noise1) count=1
*.meas dc input2  =min(noise1flip,blbiflip)
```

6.3.4 For Leakage Power Analysis

```
*********** SOURCES ******************************
.ground  0
.global  vdd vss gnd
vvdd vdd 0 dc vddv
vvss vss 0 dc 0
vbit bit 0 dc vddv
vbit_b bit_b 0 dc vddv
*vwl wl 0 pwl(0n 0 15n vddv)
vwl wl 0 pwl(0n 0 15n 0)
*********** MEASURES ******************************
.meas tran drain_PG    avg abs(m:xPG:1#id)
.meas tran drain_PU_M7 avg abs(m:xM7:1#id)
```

```
.meas tran drain_PU    avg abs(m:xPU:1#id)
.tran 0.01n 15n
```

6.3.5 For Write Margin Analysis

```
*********** INITIALIZE ***************************
.nodeset v(bli)=(vddv*data)
.nodeset v(blbi)=(vddv-data*vddv)
.nodeset v(bit)=(vddv)
.nodeset v(bit_b)=(vddv)
*********** SOURCES *****************************
.ground  0
.global  vdd vss gnd
vvdd vdd 0 dc vddv
vvss vss 0 dc 0
vbit   bit   0 pwl(0n vddv 14n vddv 14.5n 0 25n 0)
vbit_b bit_b 0 pwl(0n vddv 4n vddv 4.5n 0 11n 0 11.5n vddv 25n vddv)
vwl    wl    0 pwl(0n 0 1n 0 1.5n vddv 8n vddv 8.5n 0 17n 0 17.5n vddv 25n vddv)
*********** MEASURES *****************************
.meas tran bli_rise_bl  trig v(bit_b) val=vdd50 fall=1
+                    targ v(bli)   val=vdd95 rise=1
.meas tran blbi_rise_bl trig v(bit_b) val=vdd50 fall=1
+                    targ v(blbi)  val=vdd05 fall=1
.meas tran bli_rise_wl  trig v(wl)    val=vdd50 rise=2
+                    targ v(bli)   val=vdd05 fall=1
.meas tran blbi_rise_wl trig v(wl)    val=vdd50 rise=2
+                    targ v(blbi)  val=vdd95 rise=1
```

Chapter 7

Appendix B

6.4 References

[1] A. wang, A. Chandrakasan, and S. Kosonocky, "Optimal Supply and Threshold Scaling for sub-Threshold CMOS circuits." Proc. IEEE Comp. Society Annual Int. Symp. VLSI pp. 5-9. Apr., 2002

[2] Digital Integrated Circuits by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic

[3] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "SRAM Design on 65-nm CMOS Technology With Dynamic Sleep Transistor for Leakage Reduction"

[4] Ingvar Carlson, "Design and Evaluation of High Density 5T SRAM Cache for Advanced Microprocessors" Linkoping University, Reg nr: LiTH-ISY-EX- 3481-2004

[5] Tae-Hyoung Kim, Jason Liu, John Keane, Chris H. Kim, "A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme", ISSCC 2007

[6] Benton H. Calhoun, Yu Cao, Xin Li, Ken Mai, Lawrence T. Pileggi, Rob A. Rutenbar, and Kenneth L. Shepard "Digital Circuit Design Challenges and Opportunities in the Era of Nanoscale CMOS" Vol. 0018-9219 _2007 IEEE 96, No. 2, February 2008.

[7] Digital Integrated Circuits , Jan M. Rabaey.

[8] Leakage Tolerance in Neno meter Regime, Koishik Ray.

[9] High Speed CMOS VLSI Design, Logical Effort & Sizing , David Harris.