Ch.1 Fundamentals of I/O cells

A chip can be divided into two main part likes Core and I/O.**Core** is nothing but the main circuit which perform the logic for which chip is designed. A core may be a memory, PLL (phase locked loop) or anything. Normally core circuitry operates at a typical Vdd level of 1.2V-0.8v. Any core circuit has some characteristics defined for all the incoming signals. If any of the incoming signal is not suitable for core (as the signal is coming from off-chip environment to the core, it may contain abrupt voltage levels, noise etc.), it may lead to failure of core and also it can damage the core circuit. Here comes the need and importance of the I/O. **I/O's** are placed on the periphery of the chip. These are the cells that allow the interface between the logic inside the chip and the external system. Any I/P signal which comes from off-chip environment (external voltages are at a typical voltage Vdde level of 2.5V, 3.3V or 5V) into the chip, must be checked by I/O for any discrepancy in its behavior other than defined by the core for that particular signal.

1.1 Importance of IO:

Today, the I/O structures require the most amount of circuit design expertise along with detailed process knowledge. It is the I/O element which finally interfaces the core signal to the off-chip environment. Thus however efficient the core design may be, these are the IO's which determine the efficiency of the chip. It is very much important to ensure that designed I/O is functional and works well within the specifications. It is must to analyze the designed I/O under the worst, typical and best practical conditions for different parameters such as functionality, output drive, slew rate, delays, maximum frequency of operation etc.

Following are the Benefits of IO'S:

- **Uniform Power Distribution:**

Typically I/Os are placed at the periphery of the core logic i.e. on the sides of the core logic, except on the corners of the cell .They are placed parallel to one another and vertical to the enclosure containing the core .Also corner cells are used. This helps in maintaining the

power ring continuity throughout the cell, which is very important for uniform distribution of the power to all the I/Os inside the chip.

- **ESD Protection** :

An I/P buffer couples the external off chip signal to the core elements of the chip. Since the external signal can have voltage ranges much beyond the normal CMOS operating voltages, an I/P ESD protection is required for these buffers. Non Destructive break down of diodes is utilized to clamp the voltages between VDD and VSS. The resistor tends to decrease the current reaching gate. But this block introduces RC delay; hence the design has to be optimized, if used in high speed circuits.

- **Hysteresis :**

Hysteresis is often required in input buffers to decouple the noisy external signal from the core circuitry of the chip. For a noisy external signal we desire that the buffer does not switch its state due to noise. We should have a margin for the noise considerations. The basic principle employed for such circuit is the different switching thresholds for input signals from low to high and high to low transitions, i.e. when we apply low voltage to the I/P and ramp it up to the high level the threshold point comes say at a point VIN=Vihhyst. Similarly when we apply a high voltage at I/P and decrease it, the threshold point comes at point VIN=Vilhyst, where Vihlhyst > Vilhyst.

1.2 IO Layout Frames :

- **Core limited Devices**: In core limited devices the dimension is decided by the core dimension. The I/O ring will increase the final size. So, it is necessary to shrink the I/O height as much as possible, thus increasing the I/O width.
- **Pad Limited Devices:** In pad limited device the size is determined by the pad number. The I/O ring contains the as much I/Os as possible. So it is necessary to shrink I/O s width as much as possible, thus increasing the I/O s height.

1.3 Contents Of Standard IO Library :[5]

A Standard I/O library consists of the following components:

- Input Buffers
- Output Buffers
- Bidirectional Buffers
- Compensation cell

- Supply cells
- Fillers
- Corner cells

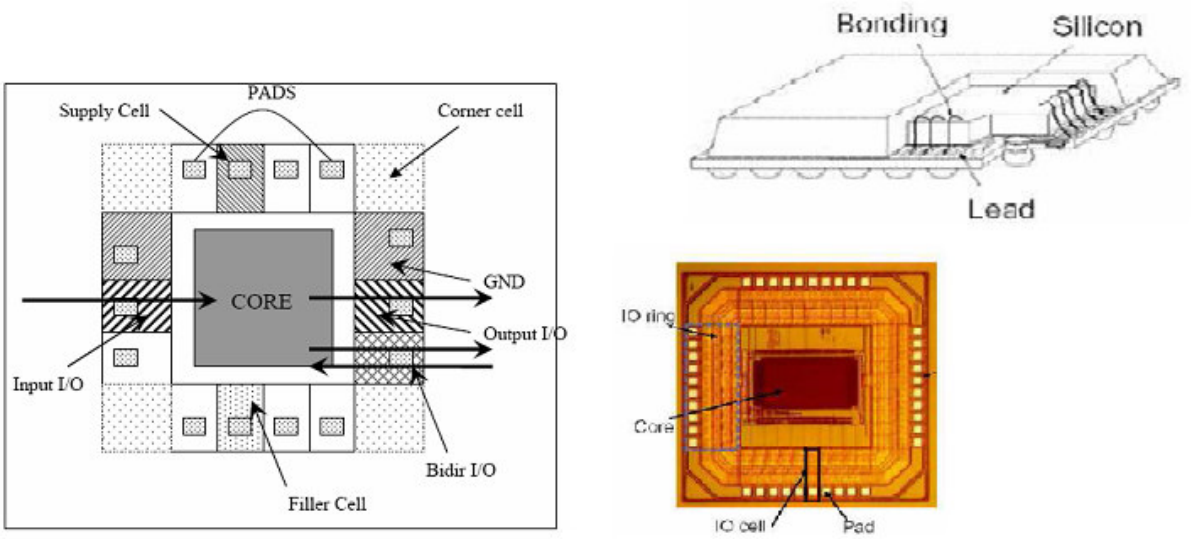

Fig :1.1 Schematic of Chip

1.3.1 Input Buffers:

An I/P buffer couples the external off chip signal to the core elements of the chip. Since the external signal can have voltage ranges much beyond the normal CMOS operating voltages, an input ESD (electrostatic discharge) protection is required for the buffers. After passing through the ESD block, the signal is applied to the I/P buffer. ESD protection is very important to save the chip from unwanted voltages which get developed at the pin due to some sources coming in contact with the pin. The large accumulated charges can destroy the transistor, so a mechanism is needed which can effectively and quickly discharge the unwanted accumulated charge. A typical I/P buffer may be divided into three main stages as represented by the block diagram as shown:

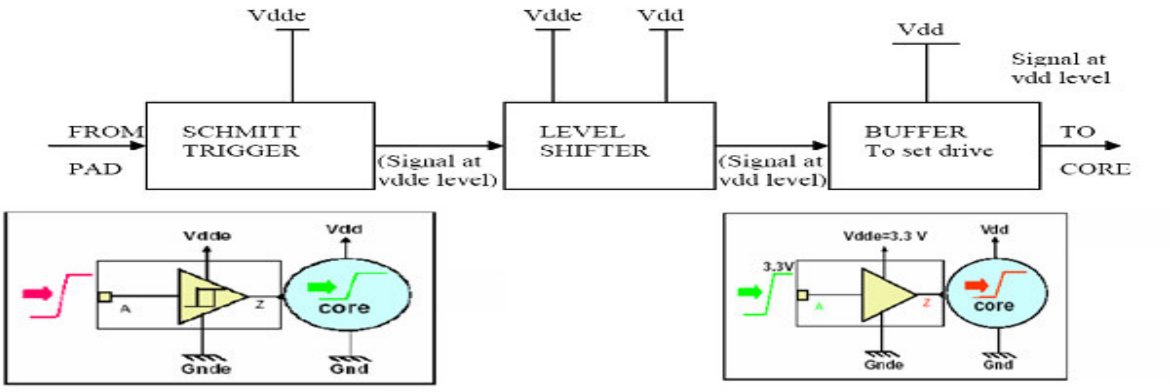

Fig 1.2 Block Diagram of Input Buffer

- **Schmitt Trigger:**

Hysteresis is often required in I/P buffers to decouple the noise external signal from the core circuitry of the chip. Schmitt trigger is used to provide hysteresis. The basic principle employed for such circuit is the different switching thresholds for input signals going from 'LOW' to 'HIGH' and 'HIGH' to 'LOW'.

- **Level Shifter :**

Since core circuit works at a voltage level vdd (typical 1.2V), whereas external signal comes at a voltage level of vdde (2.5V or 3.3V). Hence, the voltage of the signal needs to be shifted down so as to apply it to core.

- **Buffer :**

A weak signal source (one that is not capable of sourcing or sinking very much current to a load) may be boosted by means of two inverters like the pair shown in the previous illustration.

1.3.2 Output Buffers:

These buffers are used to drive large capacitive loads which arise from long interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads. The drive capability of such a buffer should be such as to achieve the requisite rise and fall times into a given capacitive load .Normally the drive capability of I/O buffers is as high as 8 mA. A typical output buffer may be represented by the following block diagram:

Fig 1.3 Block Diagram of Output Buffer

To achieve the specified functionality of the output buffer, different types of output stages are used at the output section :

- **Test pin Block :**

This block is used at the output section of the chip and is connected between the core and Predrivers (slew rate control block). It consists of multiplexer, to select the test mode or basic operating mode, series of inverters to generate two signals NIN and PIN at the output for slew rate control .The signal at NIN rises faster than PIN while signal at PIN falls faster than NIN

- **Predrivers :**

A fast transition of the signal at the output pad tends to introduce frequencies in UHF range into the off chip load being fed .Most of the time it is undesirable and thus appears as noise .The source of this noise is the inductive voltage which is due to the inductance of the introduced by the package pins .To reduce this noise , we generally control the switching which reduces the rate of change of current at the output .Slew rate control circuits thus artificially limit the rate of current switching thereby limiting the UHF interference .One way to achieve this is by breaking the output driving transistors into a series of parallel transistors and switch the stages sequentially one after the other with some delay .The slew rate control circuit consists of a series of nand and nor gates which are driven by PIN and NIN signals respectively .As there is sequential delay in both nand and nor chain, thus they drive the series of output transistors sequentially. This results in total controllability over the rate of change of output current and hence slew rate can be controlled. Sometimes slew rate gets effected due to change in PVT and even the slew rate controller cannot do anything as they are hard coded while fabrication .So to compensate for the change in slew rate in changing PVT conditions, codes are fed through a compensation block which generates the code according to the conditions. Compensation block has only an enable pin and the output pins. This block senses the change and generates a common code for all the slew rate controlling devices.

- **Output Drivers :**

An output buffer must have sufficient drive capability to achieve adequate rise and fall times into a given capacitive load .To achieve the specified functionality of the output buffer, different types of output stages are used at the output section.

☞ **Push Pull Stage** :A push pull stage consists of p and n transistors at the output pad for sourcing and sinking respectively, where each of transistors is controlled through a different chain of tapered inverters fed after buffering .This has two advantages:

· No direct gate contacts of the two output driver transistors.

· Static and short circuit power dissipation can be avoided by bifurcating the inverter chain in a way such that while sourcing current at the output pad, NMOS driver is made off before PMOS is on and vice versa.

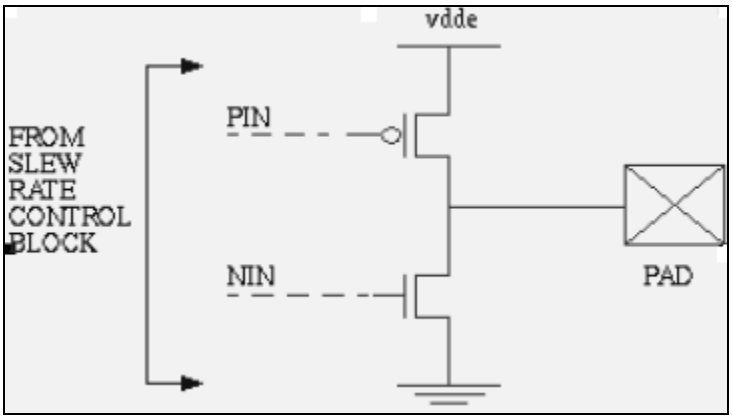

Fig 1.4 Push Pull stage

☞ **Open Drain Output Stage :** This has an advantage over the push pull, and that is, it has just one driver stage. Such configuration avoids gate source-drain capacitance, thus making it faster than push pull. But this configuration can either sink or source current at a time, which limits its usage .

☞ **Push Up/down Stage :** Often the tristated output is put to a particular logic level instead of letting the bus float .Either logic low or high can be made at the output using the pull up or pull down transistors Normally the NMOS transistor is used for pull down and PMOS transistor for pull up .

1.3.2 Bidirectional Buffers:

It has both input and output buffers and an ESD protection. It can be used in both ways i.e. signals from outside world can interact with the chip and vice versa so the name bidirectional. A typical bidirectional buffer can be represented by the following block diagram:

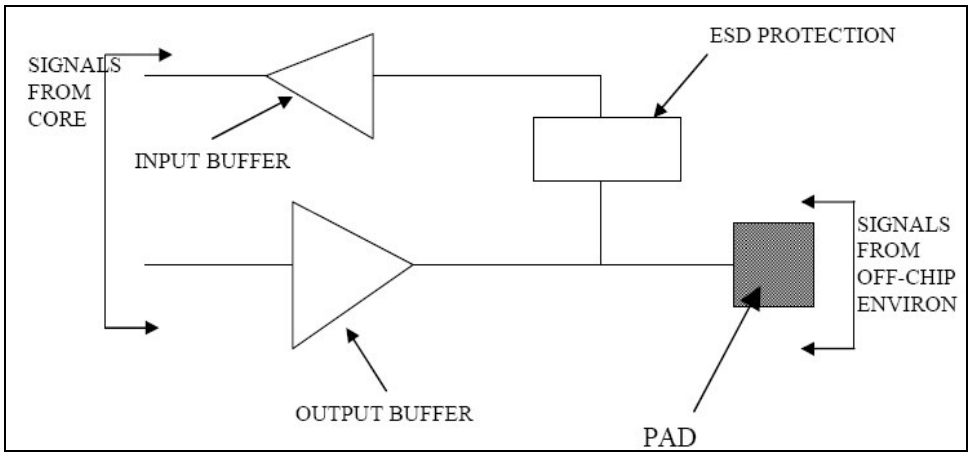

Fig 1.5 Block Diagram of Bider

1.3.3 Compensation cell :

These are cells used in the I/O periphery for the slew rate control. A fast transition of the signal at the output pad tends to introduce frequencies in UHF range into the off chip load being fed. Sometimes this becomes undesirable in applications such as if the signal is fed to a Television chip, cellular phones, radios etc. The signals in the UHF range then appear as noise. Thus many a time s controlled switching of current signal at the output pad is required, achieved by slew rate control circuits. A controlled switching also results in reduced dI/dt power supply noise. The source of this noise is the inductive voltage drop V =L (dI/dt) at the power rails where inductance is introduced by the package pins. Slew rate is typically expressed in units of V/us. Slew rate control circuits thus artificially limit the rate of current switching thereby limiting the UHF interference. Compensation block has only an enable pin and the output pins.

1.3.4 Supply Cells:

These pads are basically a sandwich of various metal layers used in the design. The pads consist of pins and metal connection on all sides to provide the power connection to both the

Core (Internal Library elements) and the I/O elements. Multiple power pads are often used in the same library to reduce the noise. The internal elements of the I/O circuit being connected to one power pad while the external elements, the circuit part which will have interface with the off chip elements being connected to a different power pad. All the power pads are finally shorted by a metal layer at the bonding pad. The noisier power pads (the one connected to the output transistors) are separated from the substrate to prevent the noise coupling through the substrate. The power and ground bus widths may be calculated using the worst case power dissipation estimate of a die with the particular packaging style ,supplying a stable and good power supply and electro migration considerations.

1.3.5 Filler and Corner cells :

In a packaged chip , all the I/Os are abutted to one another .But if there is free spaces between I/Os , filler cells must be used to fill up these empty areas. There are filler cells with different width which can be used to fill up the of different sizes. It is advised to start the filler cell placement by the widest cell possible and then continue with decreasing sizes until the gaps are completely filled. Filler cells only contain the geometrical information of the metal rings at each level of metal. As the I/Os are not placed at the corner edges of the cell and inspite of having filled the gaps between I/Os , complete continuity of metal rings is not achieved unless and until the corner edges are filled by corner cells.

1.3.6 Fillercut cells :

There may be two voltage level supplies in the periphery of the IO ring. These cells are used to isolate voltage level to another.

1.4 Nomenclature of Buffers

A standardized naming convention is adopted for all the types of buffer, so that even at just looking at the name of a buffer, viewer can have sufficient information about the buffer.

Ch: 2 Characterization Flow

In real time operation there is always possibility of variation in input voltage frequency or temperature. So to withstand this variation we must have device capable enough. For this after design we apply various test on design to check its tolerance.

2.1 Characterization:

It is the procedure which involves the timing and constraint analysis of cells in a library to perfect the design over process, temperature and voltage. Timing and characterization involves calculation of delay, output slope, setup and hold constraints and leakage power for a cell at different processes, temperature, voltages, input slope and capacitive loads. By characterization we measure propagation delay, rise time, delay and slope degradation with frequency, leakage power, internal energy and timing constraints (setup, hold, pulse width) For this we use Eldo simulator which simulates each circuit at the given PVTSC.

2.1.1 FE (Front End) Process Flow :

The process in the Front End flow is divided into two groups that perform separate tasks One of the groups is responsible for the timing, power and leakage characterizations and other group handle HDL modeling. The HDL part involves the generation of different models which represents the design in gate level that can be well understood by different simulators.

characterization results in the generation of **.libs**. Libext flow is followed for the generation of synopsys files. Two separate files are created, one of these contains the name of the cells and the other contains the conditions for which the timing and power data has to be taken. Now these files are merged to make complete .ext (executable) files for each cell. These files are used by u2stf tool and STF (Synopsys Technology File) are generated.

2.2 Characterization flow:

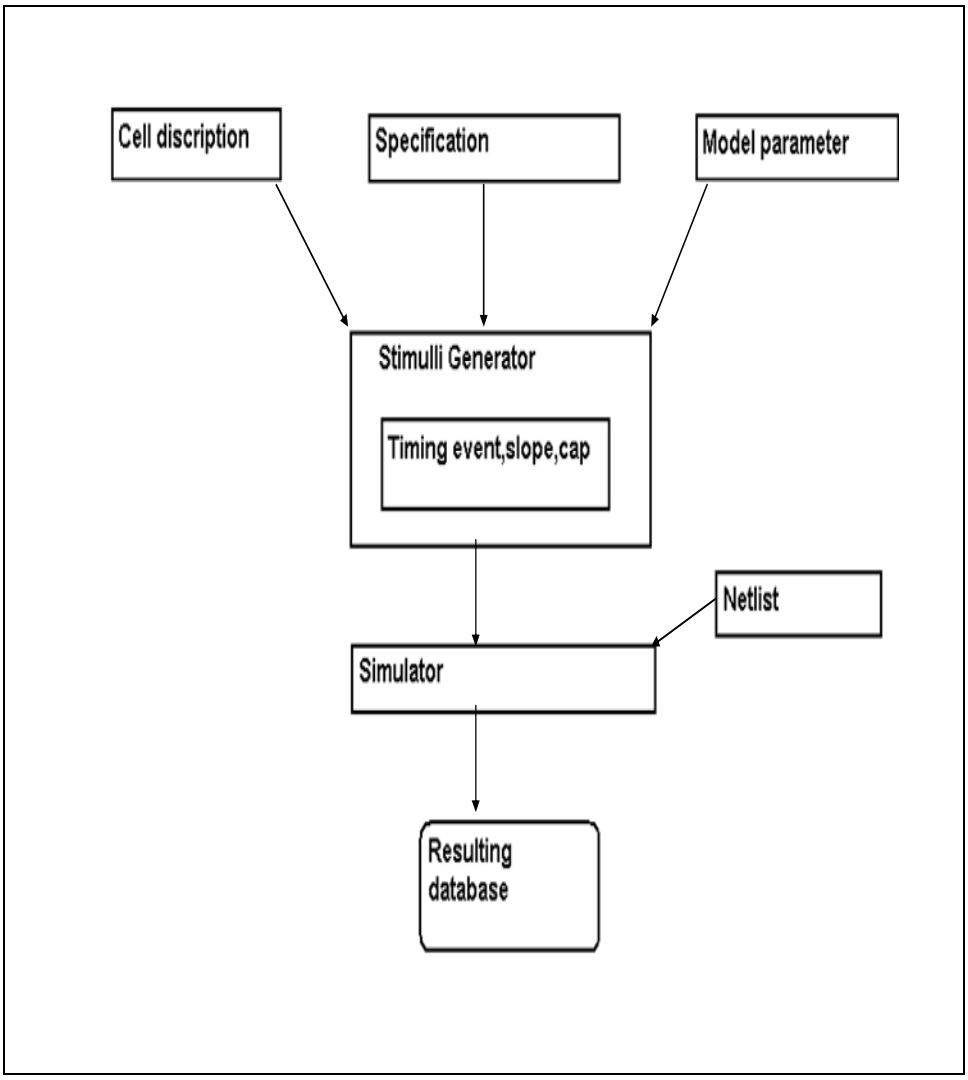

Fig 2.1 Characterization Flow

2.2.1 Cell Description

All parameter which describe the cell as given below are depicted in File. This will be input to stimuli generator.

- the name of the cell,
- the list of inputs,

- list of outputs,
- a short phrase describing the cell,
- netlist.

2.2.2 Specifications

The library specification is now in a simple ASCII format. The file is spec.list, at the root directory.

The library specification file will contain the following information:

- global definition (name, version temperature)
- default units (usually nS, pF, V)
- supplies definition
- pattern description (which values to apply on input pins)
- threshold definition (slope, cload and time)
- capacitance and slope range definition
- PVT definition

Some examples of Keyword used in spec.list are as below:

```
##-----------------------------------
## GLOBAL DEFINITION
##-----------------------------------
        NAME
        TEMP_MIN
        TEMP_MAX

---------------------------------
## UNIT
##-----------------------------------
        TIME_UNIT
        LOAD_UNIT
        VOLTAGE_UNIT
        POWER_UNIT
        ENERGY_UNIT
```

2.2.3 Net list

Netlist reflects the physical organization of the cell. It is a set of assignments. Each assignment line computes the value of an output or an internal signal from the values of the inputs. The internal signals need not be declared before being used.

2.2.4 Stimuli Generator & output

The Specification discuss above gives a complete functional model of a cell. From this, search algorithms generates test patterns which can be used to test cell models and for timing characterization. There are three kinds of test patterns:

- functional
- propagation delay
- timing constraint

For combinational cells, a functional test simply covers all 2n input combinations. A propagation delay test covers all single input changes that result in an output change. Combinational cells have no timing constraints.

For sequential cells, a functional test covers all single input changes for all combinations of input and state variables. A timing test is much shorter, covering only those single input changes for combinations of input and state variables that result in an output change. Timing constraint sequences include setup, hold, pulse width, and other constraints.

The timing information produced by characterization is stored as tables of raw data in an ASCII table format called RDB. In a second step this database can be read to produce all Unidata views having characterization information . finally all output information related to characterization is merged in file called ".libs".

2.3 I2C BUS :[10]

2.3.1 Basic concept

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes:

- Some intelligent control, usually a single-chip microcontroller
- General-purpose circuits like LCD drivers, remote I/O ports, RAM, EEPROM, or data converters

- Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling.

To exploit these similarities to the benefit of both systems designers and equipment manufacturers, as well as to maximize hardware efficiency and circuit simplicity, Philips developed a simple bi-directional 2-wire bus for efficient inter-IC control. This bus is called the **Inter IC or I2C-bus**. At present, Philips IC range includes more than 150 CMOS and bipolar I2C-bus compatible types for performing functions in all three of the previously mentioned categories. All I2C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I2C-bus.

Here are some of the features of the I2C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It s a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode .

For 8-bit oriented digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized

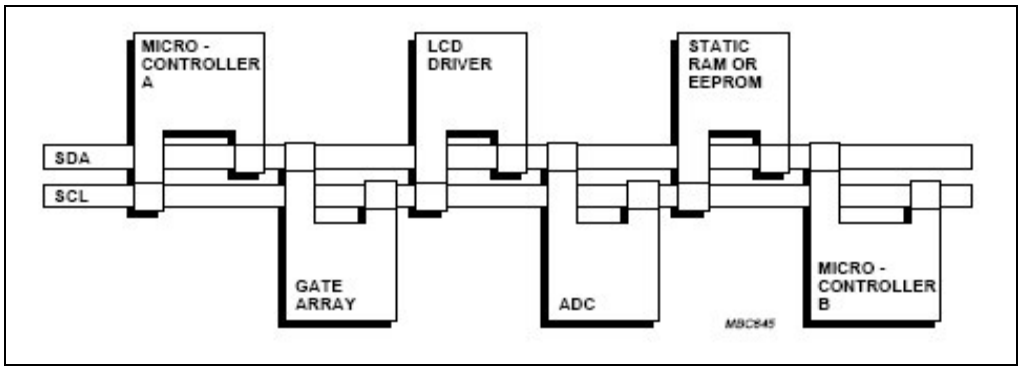

Fig 2.2 : System embedded using I2C bus

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses do not have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system. Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I2C-bus.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor (see Fig 2.3). When the bus is free, both lines are HIGH. The

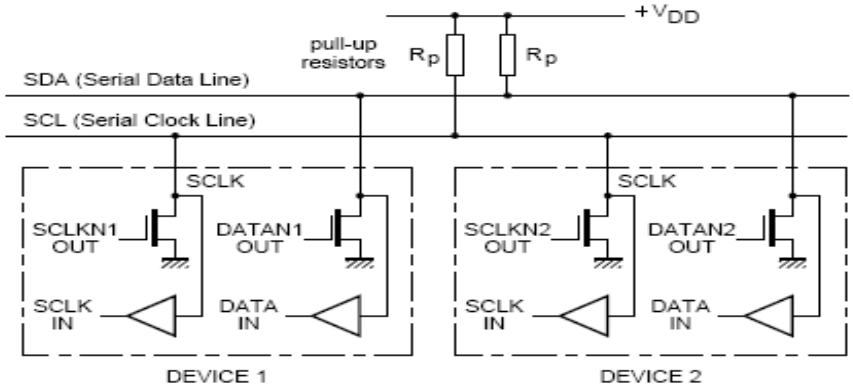

Fig 2.3 : Connection of standard and Fast mode device

output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF

2.3.2 Fast Mode:

With the Fast-mode I2C-bus specification, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines quoted in the Standard-mode I2C-bus specification are unchanged. New devices with an I2C-bus interface must meet at least the minimum requirements of the Fast- or Hs-mode specification .

The Fast-mode I2C-bus specification has the following additional features compared with the Standard-mode:

- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate.
- The inputs of Fast-mode devices incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs.
- If the power supply to a Fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines.

The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I2C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit

2.3.3 Application:

- Inter chip communication

Ch. 3 Design and Simulation

In Previous chapters, need of I/O cell has been described. Characterization of cell is carried out on design at different PVTSC. This chapter includes design specification, block diagram of Buffer and simulation results. Characterization of design has been followed in next chapter.

3.1 ARCHITECTURE OF BUFFER

I2C compatible Library contains many cell as prescribed in previous discussion. This section contains design of Input and Output buffer. Schematic of these buffer are depicted in follow figure.

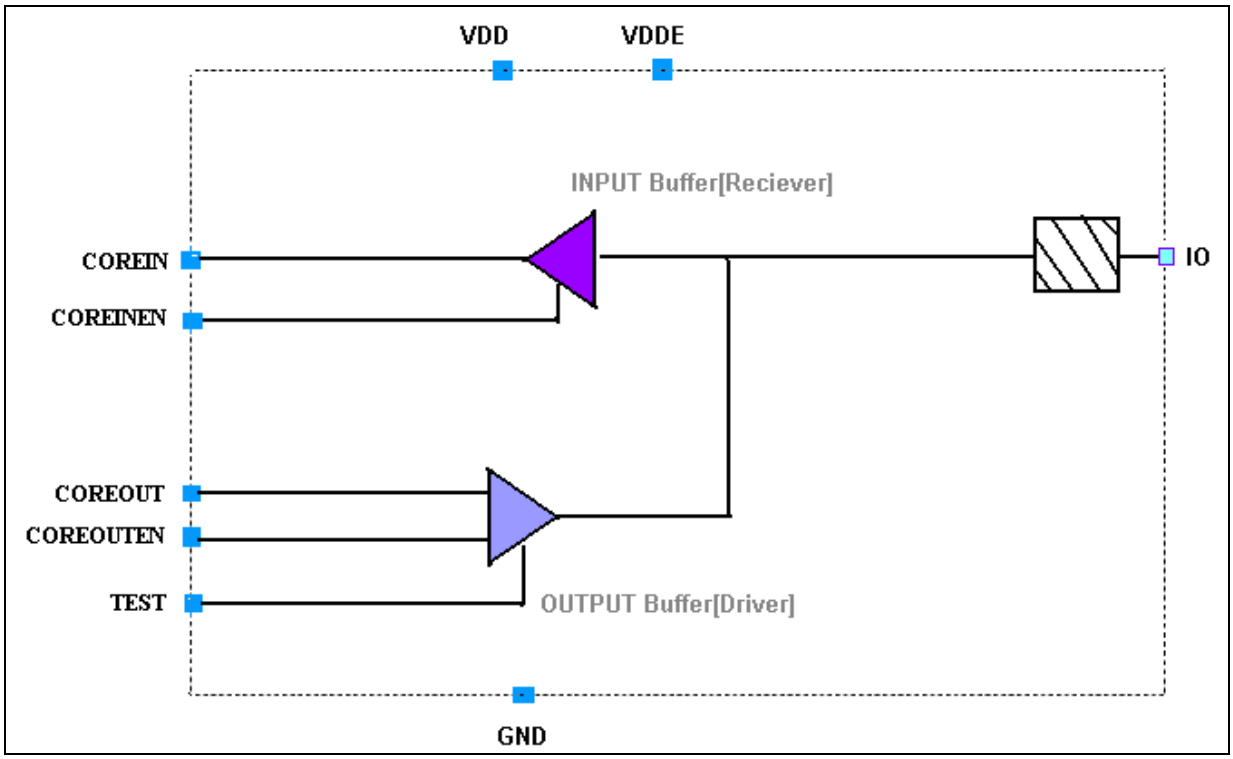

Fig 3.1 : Buffer schematic

3.2 Interface Description:[10]

Pin	Type	Voltage Level(V)	Description
COREIN	Output	1.2	Receiver output to core logic
COREINEN	Input	1.2	Input Enable
COREOUT	Input	1.2	Driver input from core logic
COREOUTEN	Input	1.2	Output Enable
TEST	Input	1.2	TEST = 0 ; Test Mode TEST = 1 ; Normal Mode
IO	Input-output	1.8	PAD
VDDE	Input	1.8	External Power supply
VDD	Input	1.2	Internal Power Supply
GNDE	Input	0	External Ground Supply
GND	Input	0	Internal Ground Supply

3.1 Interface Description

3.2.1 Logic Behavior:

Input Buffer Functional Table

IO	COREINEN	COREOUTEN	COREIN	Mode
X	L	H	X	Input disable
H	H	L	H	Input Enable

Output Buffer Functional Table

IO	COREINEN	COREOUTEN	COREOUT	TEST	Mode
X*	H	L	X	X	Output disable
X	L	H	X	L	Test Mode
H	L	H	H	H	Normal Mode
H	L	L	X	H	Pull up to VDDE

3.2 Logic Behavior:

* X suggests don't care condition

3.3 Electrical Specification:

3.3.1 Operating Condition:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Core Supply	1V2	1.05	1.2	1.35	V
VDDE	Pad supply	1V8	1.65	1.8	1.95	V
V_{hyst}	Hysteresis Voltage	VDDE < 2v	0.10VDDE	-	-	V
Temp	Operating Temperature	-	-40	25	130	^{0}C

3.3 Operating Condition

3.3.2 Transient Characteristics :

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Receiver Characteristics						
Cz	Input capacitance on COREIN pin		0.1	0.3	0.5	pF
Fmax	Input Frequency		-	-	1	MHz
Driver Characteristics						
Cb	Output capacitance		10	20	30	pF
Fmax	Output Frequency	-			400	KHz

3.4 Transient Characteristics

3.3.3 Dynamic Characteristics:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Receiver Characteristics						
t_{PLH}	Propagation Delay [Low to High]	1v8	1.3	-	5.0	ns
t_{PHL}	Propagation Delay [High to Low]	1v8	1.4	-	5.5	ns

t_r	Rise time	1v8	0.48	-	3.4	ns
t_f	Fall time	1v8	0.44	-	3.6	ns
Driver Characteristics						
t_{PLH}	Propagation Delay [Low to High]	1v8	0.5 Cb	-	100	ns
t_{PHL}	Propagation Delay [High to Low]	1v8	0.5 Cb		100	ns
t_r	Rise time	1v8	5 + 0.1Cb	-	150	ns
t_f	Fall time	1v8	5 + 0.1Cb		150	ns

3.5 Dynamic Characteristics

3.4 Design of Input Buffer and simulation

Input buffer contain various component like Schmitt Trigger, Level shifter, Multiplexer etc. The architecture of input buffer given here contains Schmitt trigger , Level Shifter followed by Buffer. This can be described as Receiver section

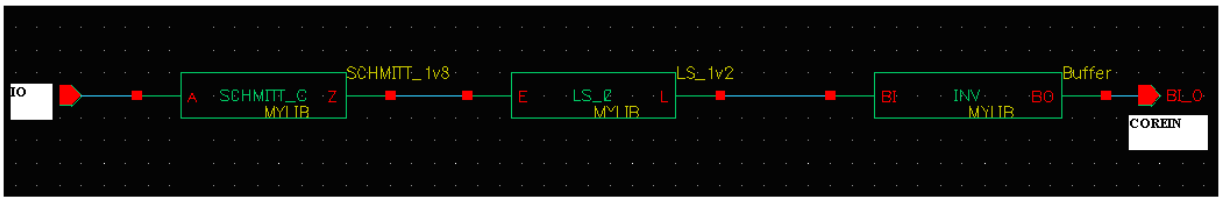

Fig 3.2 : Schematic of Input Buffer

3.4.1 Schmitt Trigger :

3.4.1.1 Basic theory [5,4]

Purpose :

o Hysteresis characteristics for the noise immunity

o Fast switching

Hysteresis is often required in input buffers to decouple the noisy external signal from the core circuitry of the chip. For a noisy external signal we desire that the buffer doesn't switch it's state due to noise . We should have a margin for the noise considerations as shown in the figure. As long as the signal doesn't go below Vilhyst the o/p doesn't change. So you have a margin of Vihhyst - Vilhyst . Normally , without Hysteresis it will start changing as soon as the voltage goes below Vihhyst (in this case).

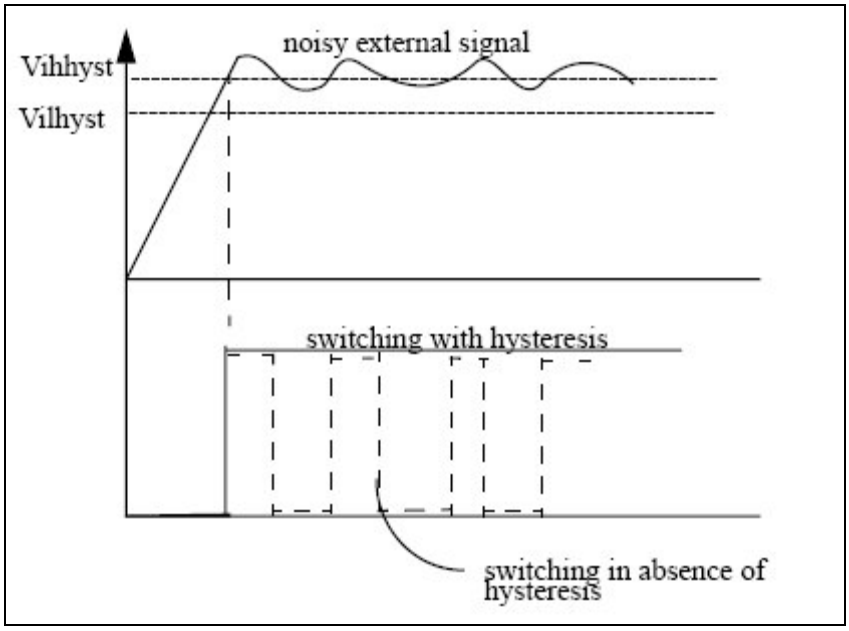

Fig 3.3 : Noise decoupling with hysteresis

The basic principle employed for such circuit is the different switching thresholds for input signals from low to high and high to low transitions ie, when we apply low voltage to the i/p and ramp it up to the high level the threshold point comes say at a point Vin = Vilhhyst. Similarly when we apply a high voltage at the i/p and decrease it the threshold point comes at point Vin = Vihlhyst .We need these points to be different such that Vilhhyst Vihlhyst as shown in the figure below.

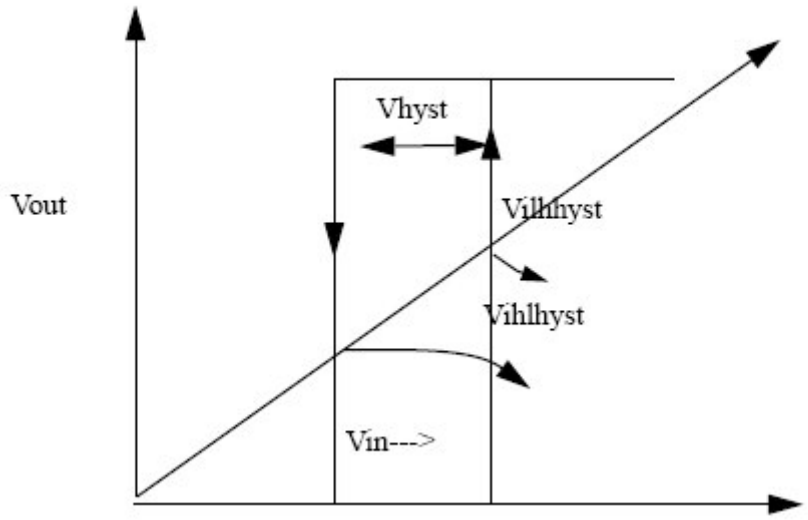

Fig 3.4 : Hysteresis Characteristics

There are different ways to achieve different threshold points. Some of them are discussed below.

A] Back to Back Inverter :

Fig show the circuit for the same design .

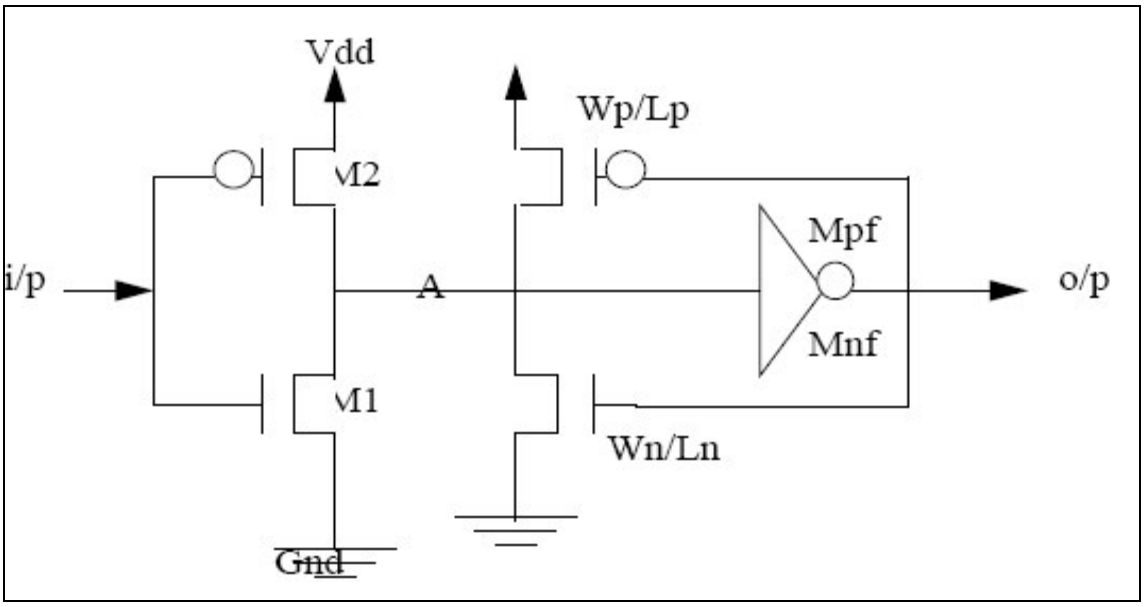

Fig 3.5 : Back to back inverter approach for Hysteresis

Functioning :

- As the input increases from 0v to Vdd

Initially M2,Mp Mnf are ON ,M1,Mn,Mpf are off

At Vin = Vtn M1 turns ON

The voltage at A starts Dropping

At VA = Vdd-Vtp , Mpf turns ON

The voltage at A drops further, output starts increasing

At Vout = Vtn Mn turns ON

This forms a positive feedback loop and quickly changes the o/p state to high

- As the input decreases from Vdd to 0V

  Initially M1,Mn,Mpf are ON . M2,Mp.Mnf are OFF

  At Vin = Vdd-Vtp M2 turns ON

  The voltage at A starts increasing

  At VA = Vtn Mnf turns ON

  The voltage at A builds further, Vout starts decreasing.

  At Vout = Vdd – Vtp Mp turns ON

  This forms a positive feedback loop and quickly changes the o/p state to low.

So the approximate Vilhyst and Vihhyst are at point when output is at Vdd-Vtp and Vtn respectively which will be different due to threshold of NMOS and PMOS

Advantages / disadvantages :

This circuit doesn't have sharp initial dc transition.

It is area effective and simple

B] Standard Hysteresis Circuit :

Fig 3.6 shows a very commonly used Hysteresis circuit. Here again the different threshold voltages of the n-channel and p-channel transistors is used to advantage.

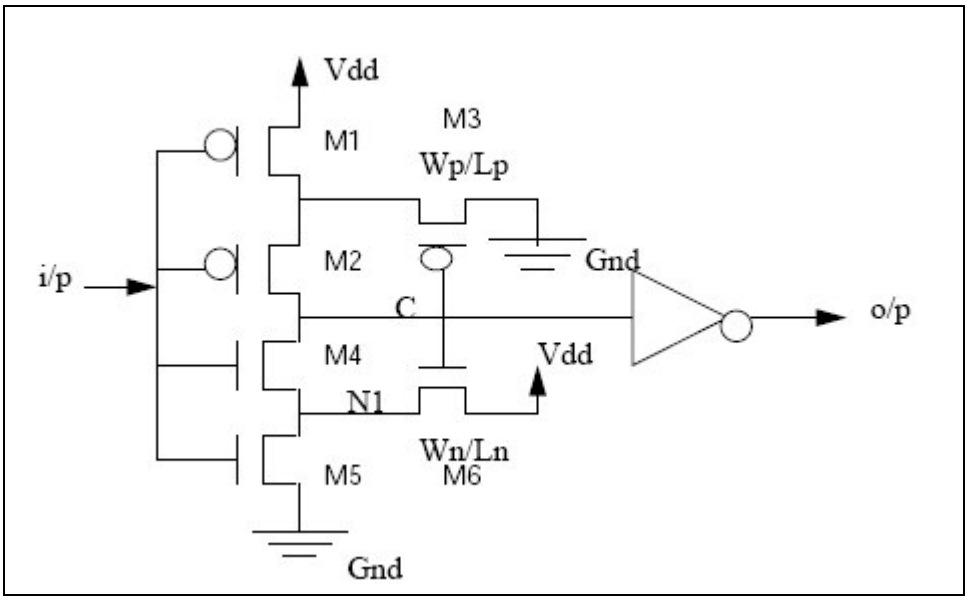

Fig 3.6 : Standard Schmitt Circuit

Functioning

- For the dc voltage sweep from low to high at the input

  Though M5 turns ON after Vin > Vtn5 , M4 does not turn ON as Vt4 (threshold voltage of M4) is shifted due to body affect. Hence output voltage remains at high level .The source of M4 is initially at a voltage of VDD -Vt6 (body affected).

  As Vin> Vtn5,the voltage at node N1 begins to fall. Here M6 and M5 form an inverter pair, having a feedback effect with M6 acting as a resistive load.

  As soon as VGS4 > Vt4 (body affected) ,M4 gets ON and output node is immediately pulled to the ground.

  Also the drive strength of NMOS M4 and M5 is more compared to the PMOS M2 and M1.This explains the sharp transition characteristics of the circuit .The value of Vihhyst depends primarily on W/L of M6 and M5 for a given technology (Vtn fixed).

  Keeping M6 fixed ,greater is the W/L of M5 ,faster is the rate at which the node N1 is pulled down

- For the dc voltage sweep from high to low at the input

  Same Explanation ensues for Signal goes from high to low.

  Feedback transistor M1 and M2 forming the inverter pair with M3 as a resistive load.

  Here the switching threshold Vilhyst depends primarily on W/L of M1.

In the transient analysis b-b circuit fares better in terms of delay and rise times at lower loads . At higher loads (~10pf) standard circuit fares better.

3.4.1.2 Design and simulation of Standard Hysteresis Circuit :[7]

- Using the Inverter Ratio of 2-2.5 we first carry out W/L ratio of M1 , M2 , M4 and M5 for Switching point (in this case Vth = 0.9 i.e.VDD/2)
- M3 and M6 plays important role to acquire threshold point
- When M5 ,M4 and M6 turns ON then output state goes to low.
- For low to high ,we have $V_M = 1.0v$ and for high to low $V_M = 0.8v$
- So we can establish relation as below

$$\beta_5/2 \{[V_{GS} - V_{thn}]\}^2 = \beta_6/2 \{[V_{GS} - V_{thn}]\}^2$$

$$\Rightarrow \quad \beta_5 \{[V_M - V_{thn}]\}^2 = \beta_6 \{[V_{DD} - (V_M - V_{thn}) - V_{thn}]\}^2$$

$$\Rightarrow \quad \beta_5 \{[V_M - V_{thn}]\}^2 = \beta_6 \{[V_{DD} - V_M]\}^2$$

In this case $V_M = 1.0$, $V_{thn} = 0.64$, $V_{DD} = 1.8$ v

We have

$$\boxed{\beta_6 / \beta_5 = 0.2}$$

- Similarly for high to low threshold we have

$$\Rightarrow \quad \beta_1 \{ [V_{DD} - V_M - |V_{thp}|]\}^2 = \beta_6 \{[0 - V_M]\}^2$$

In this case $V_M = 0.8$, $V_{thp} = -0.45$, $V_{DD} = 1.8$ v

Simulation result :

After design is over we have to check this design over various PVTSC condition . Below is some of the results for Schmitt trigger. Each case given below denote output for given design .

Case – I: Vin < Vlhhyst

when input voltage is less then upper threshold voltage at that time output can not reach up to Vdd level . Input are as below:

Process	:	Normal
Voltage	:	0.9v
Temp	:	27 ^{o}C
Slope	:	0.01
Cap	:	0.2pf

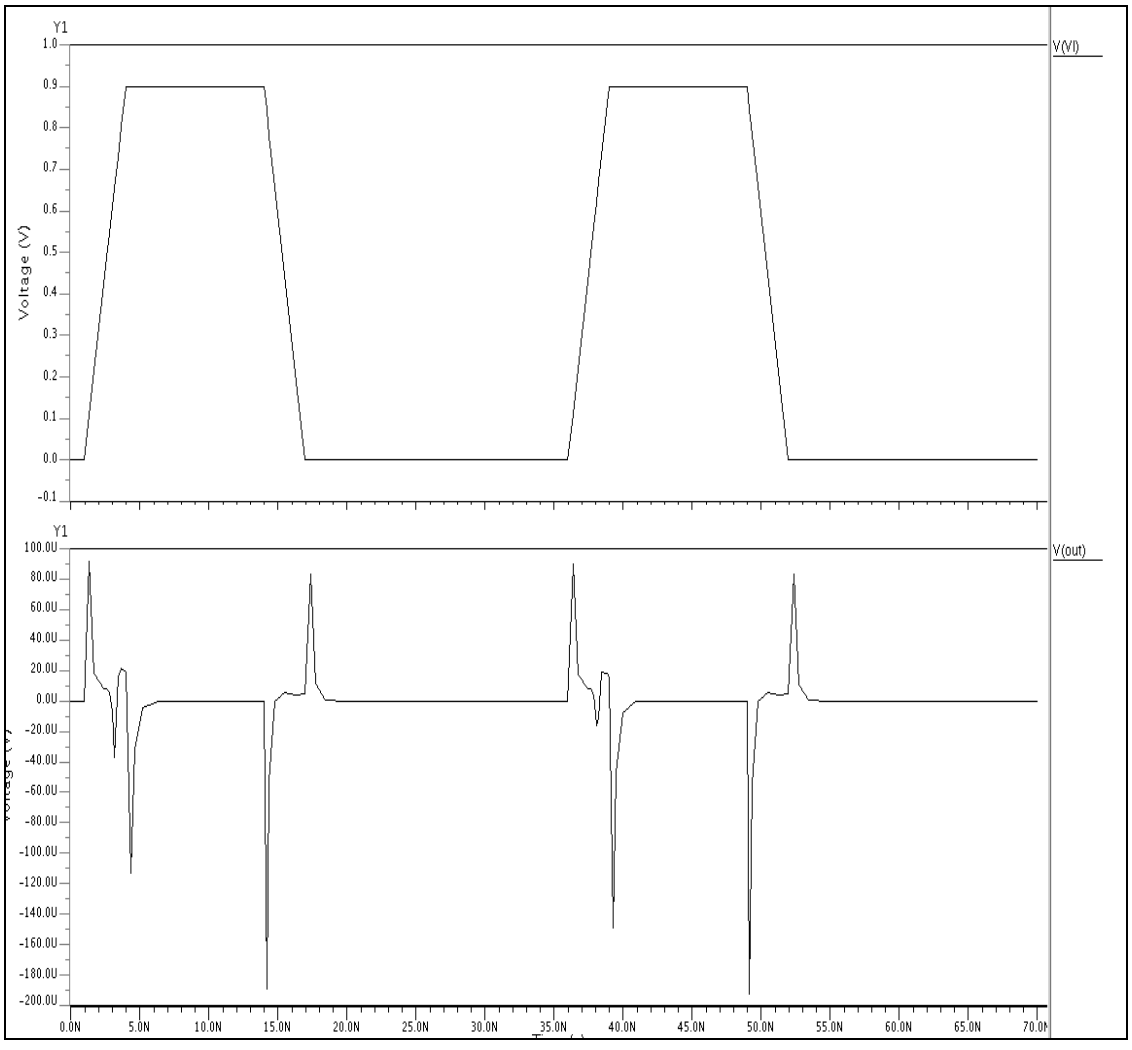

Fig 3.7 : Input level below Vlhhyst

Case – II: Vin ≥ Vlhhyst

when input voltage is more then upper threshold voltage at that time output reach up to Vdd level. Fig given below show output for same case, where input voltage is 1.005v which is sufficient enough to switch devices. In following case Input reach upto upper threshold value, while falling edge goes below lower threshold voltage. On account of this condition output follow the input data.

Process : Normal

Voltage : 0 - 1.005v

Temp : 27 ^{o}C

Slope : 0.01

Cap : 0.2pf

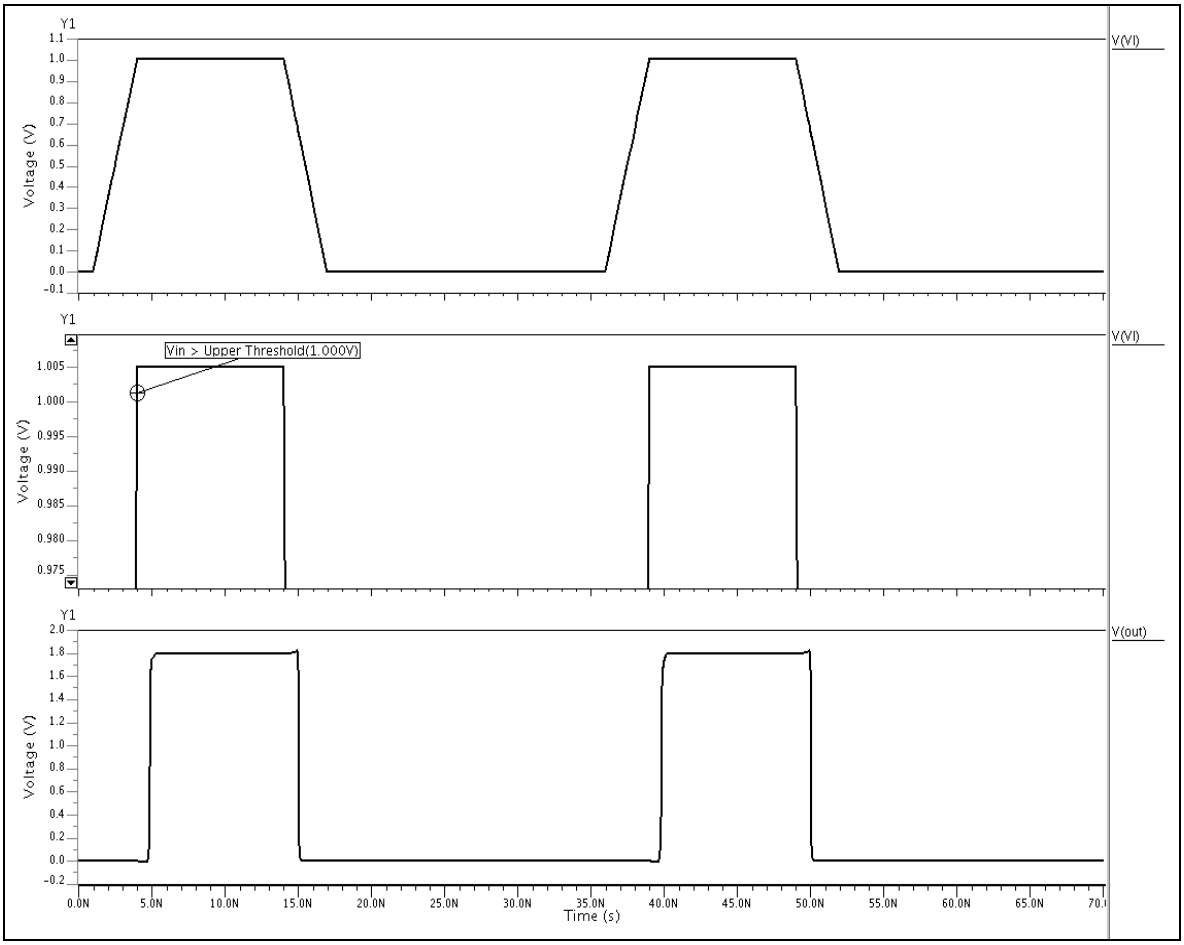

Fig 3.8 : Input voltage at Vlhhyst

Case – III : Vin ≥ Vhlhyst

In case of falling edge , when input voltage is more then lower threshold voltage , output will not switch to lower level. Fig given below show output for same case, where input voltage is 0.810v which is more than Vhlhyst. Here once output switch to high level , no any switching will take place.

Process : Normal

Voltage : 0.810 – 1.8 v

Temp : 27 ^{o}C

Slope : 0.01

Cap : 0.2pf

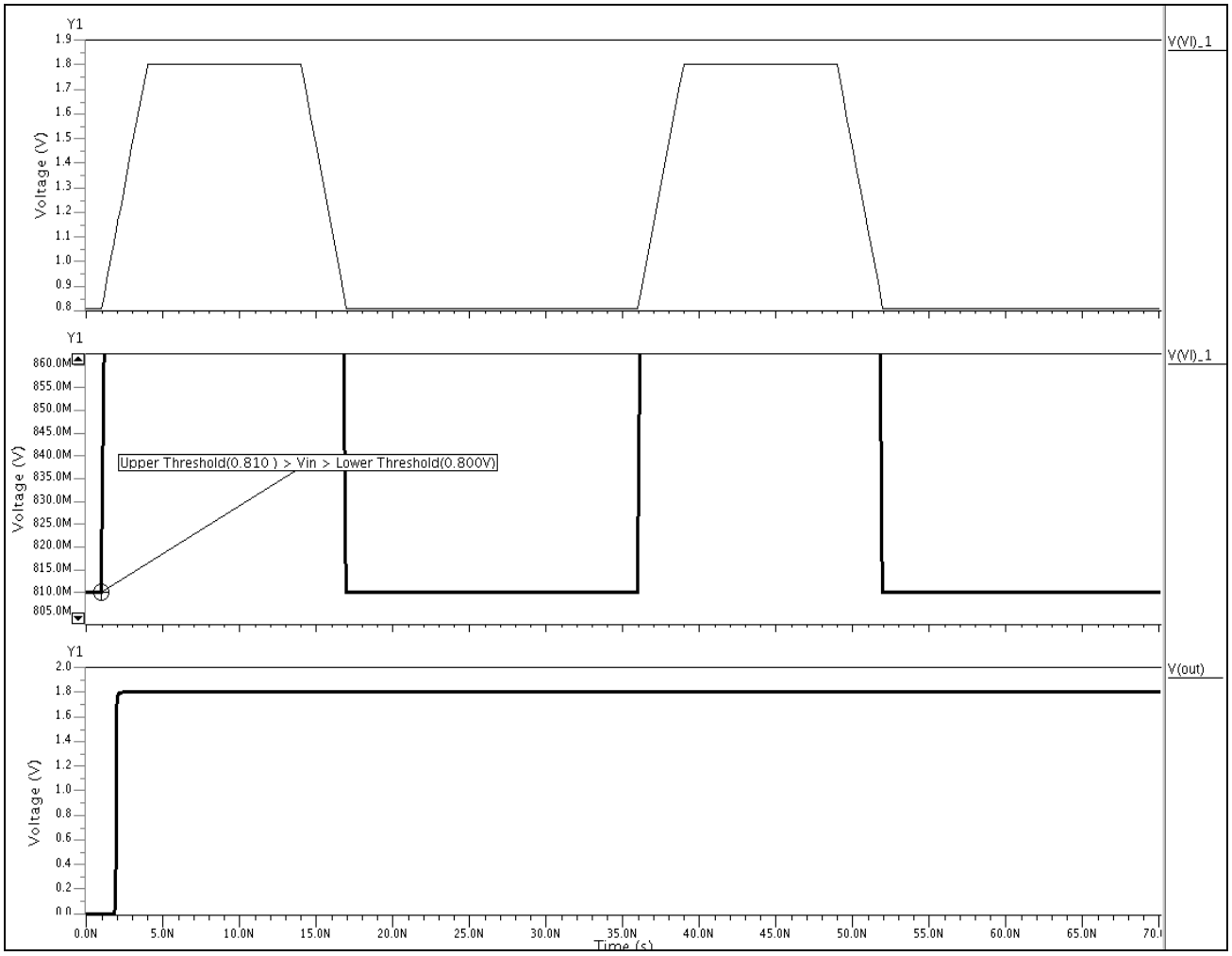

Fig 3.9 : Input is more than Vhlhyst

Case – IV : Vin ≤ Vhlhyst

In case of falling edge , when input voltage fall below lower threshold voltage , output will switch according to input. Fig given below show output for same case, where input voltage is 0.800v. output follow input as both threshold voltage has been applied here.

Process : Normal

Voltage : 0.8 – 1.8 v

Temp : 27 ^{o}C

Slope : 0.01

Cap : 0.2pf

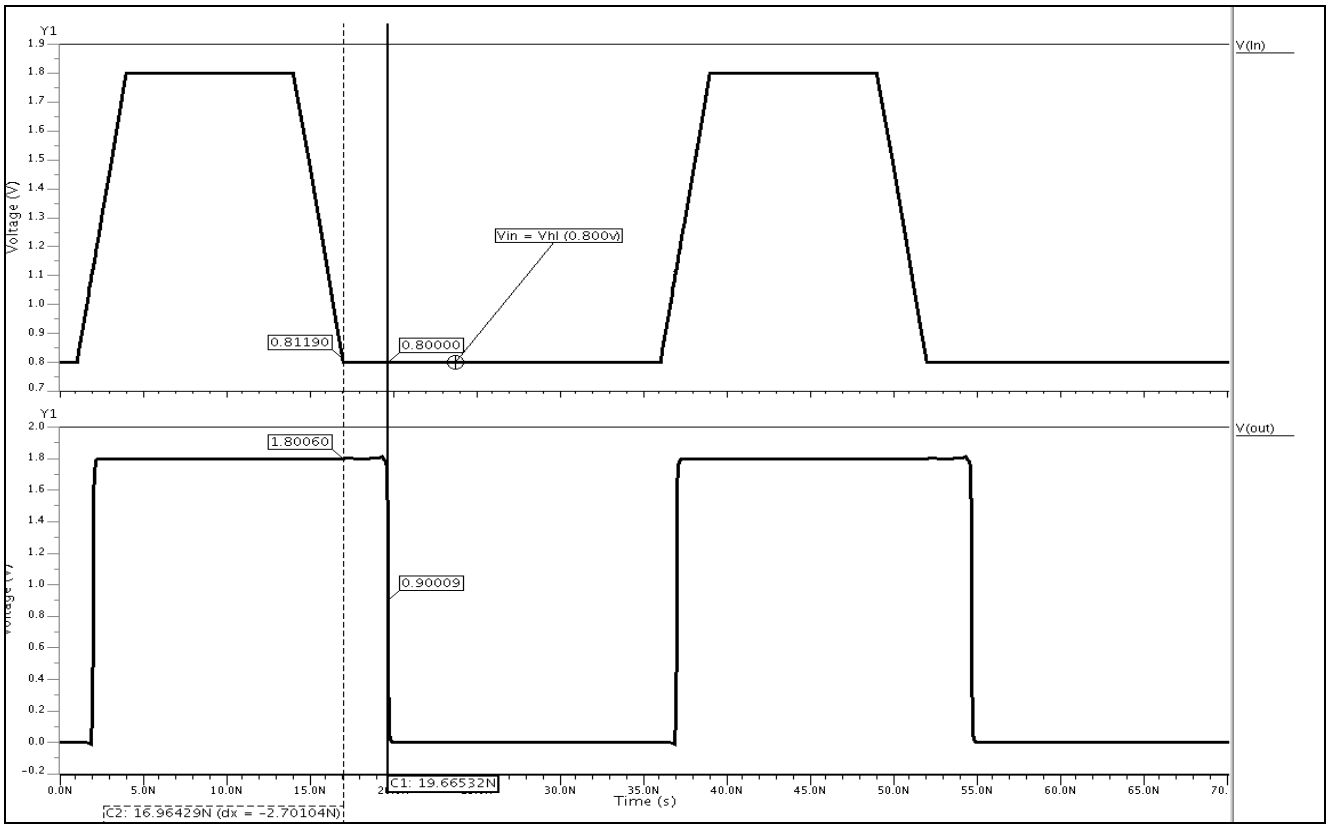

Fig 3.10 : Input at Vhlhyst

3.4.2 Level Shifter :

With the usage of Schmitt trigger we can avoid false triggering of device in noisy environment. After that signal will pass to the CORE circuitry from Pad. Here we need to convert input signal to lower voltage signal comparable to CORE.

3.4.2.1 Basic [5,6]

The dc level converter needs some design consideration in the sense that it has to prevent the static power dissipation. A simple inverter used as level converter will result in unnecessary static current since both p and n MOS will be ON.A low level voltage converter which is the widely used circuit today ,has been shown in figure 3.11 allowing high level off chip signal voltage to interface with low level 1.2V CMOS voltages without consuming any static current. The regenerative action of the latch allows the active NMOS device to turn on the opposite PMOS device which charges it's drain all the way unto 1.2V.

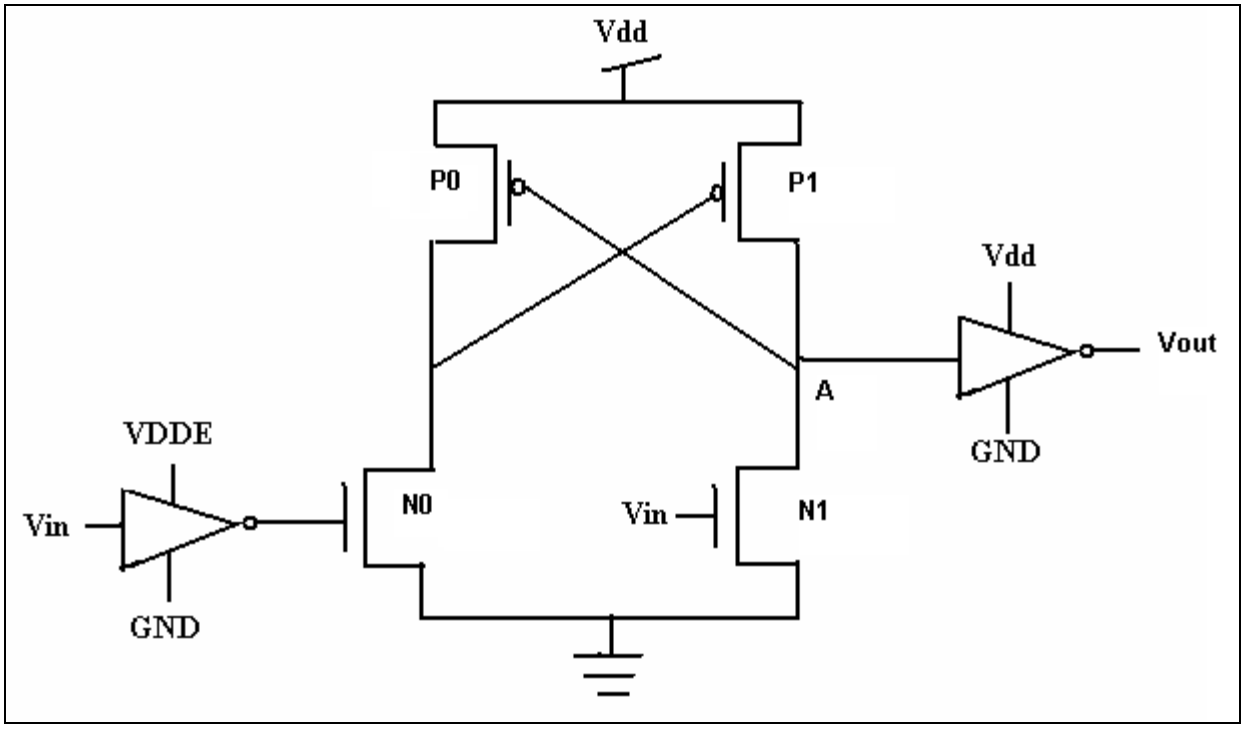

Fig 3.11 : Level shifter [1.8v – 1.2v]

Functioning:

- As input is at Low level

  N0 is ON and N1 is OFF.

At this time P1 will be ON as Source of N0 is at ground level.

Node "A" is at Vdd level, while Vout is at Low level

- As input is at HIGH level

N0 is OFF and N1 is ON

As N1 is ON, it will pull down Node A to ground level

At this moment Vout will be pulled out to Vdd level

3.4.2.2 Design and Simulation results [5,6]

- Using the DC characteristic , we first determine switching point of circuit.
- When input is Low N1 is in cut-off Mode. Input of P1 and N1 are both on Low level simultaneously.

$\beta n/2 [Vgs - V_{tn}]^2 = \beta p/2 [Vgs - V_{tn} - Vdd - |V_{tp}|]^2$

$\Rightarrow \quad \beta n [Vgs - V_{tn}]^2 = \beta p [Vgs - V_{tn} - Vdd - |V_{tp}|]^2$

$\Rightarrow \quad (\beta n / \beta p) = [(3.08)*(0.3)/ (2.52)*(0.07)]$

$$\boxed{(Wn /Wp) = 5.11}$$

Simulation Result :

Fig show DC characteristics and distorted output in case when input is above Vth.

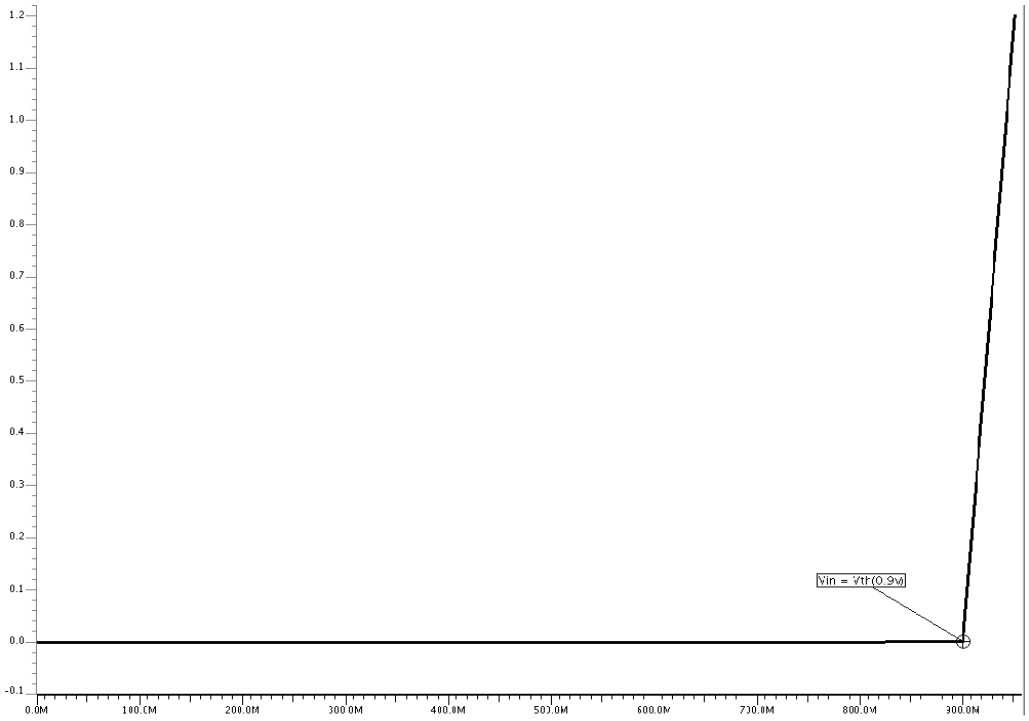

Fig 3.12 : DC characteristics for Level Shifter

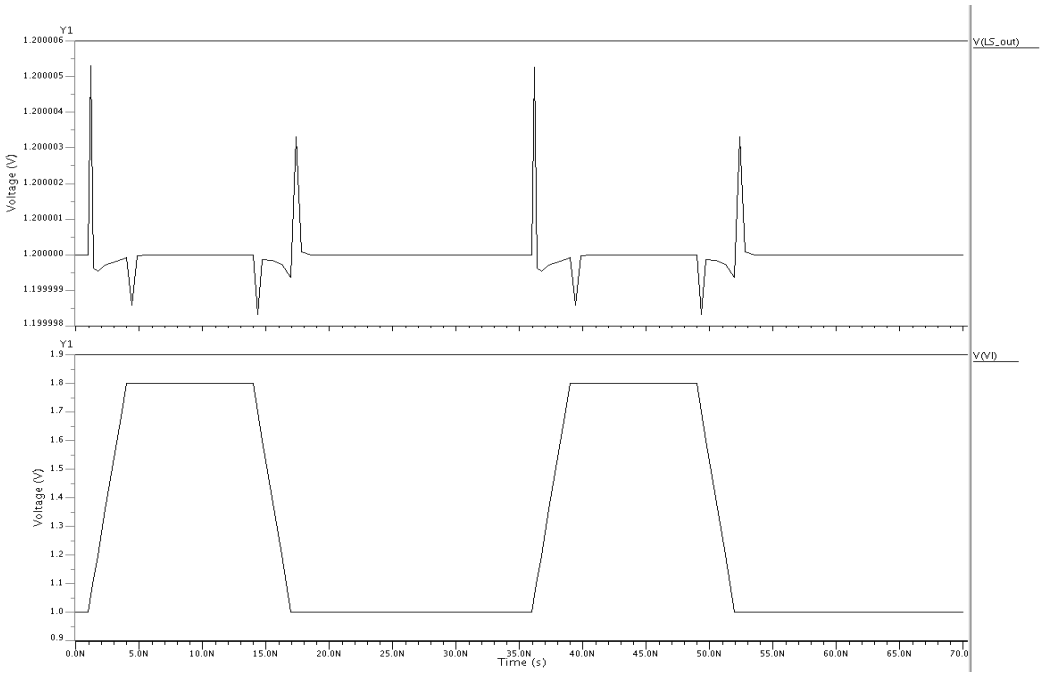

Fig 3.13 : Output swing distorted due to Low input voltage

Fig show various output for Transient Analysis of level Shifter for Different (W/L) ratio.

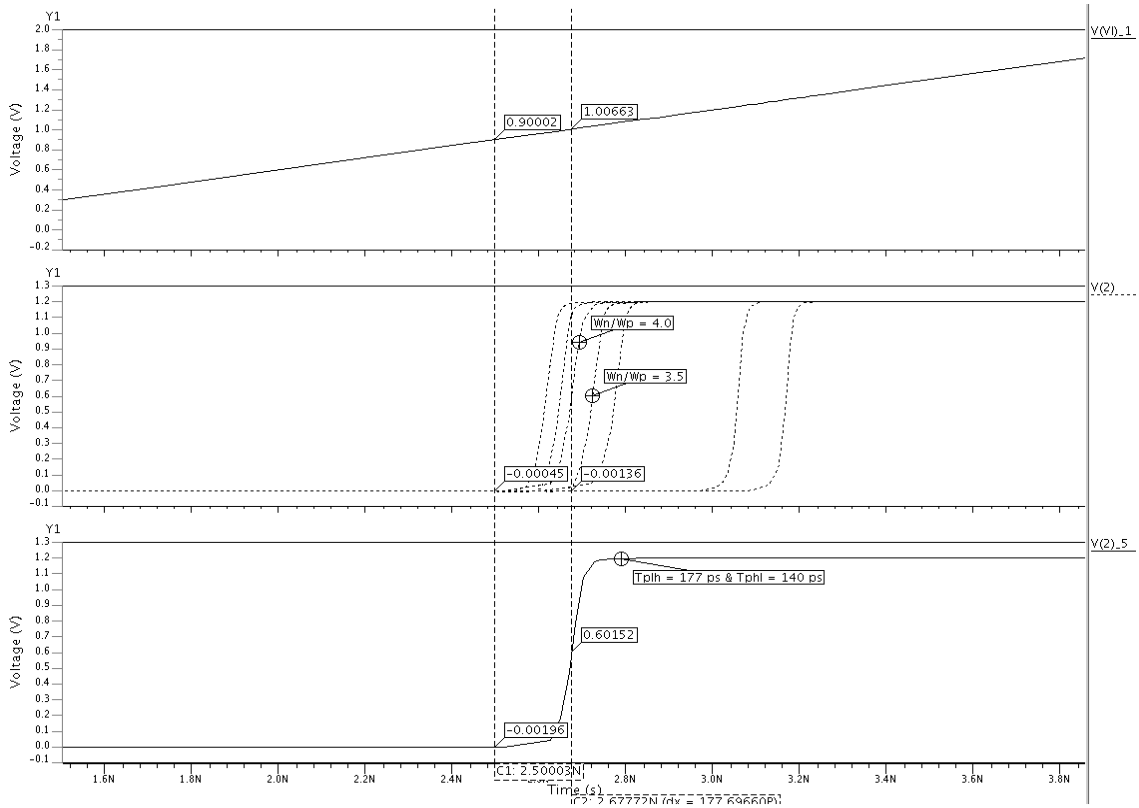

Fig 3.14 : Transient Analysis of Level Shifter at Various W/L

Fig 3.15 show output of Level Shifter . From the output we can analyze that output voltage has been reach to Vdd level ,which is compatible to core supply.

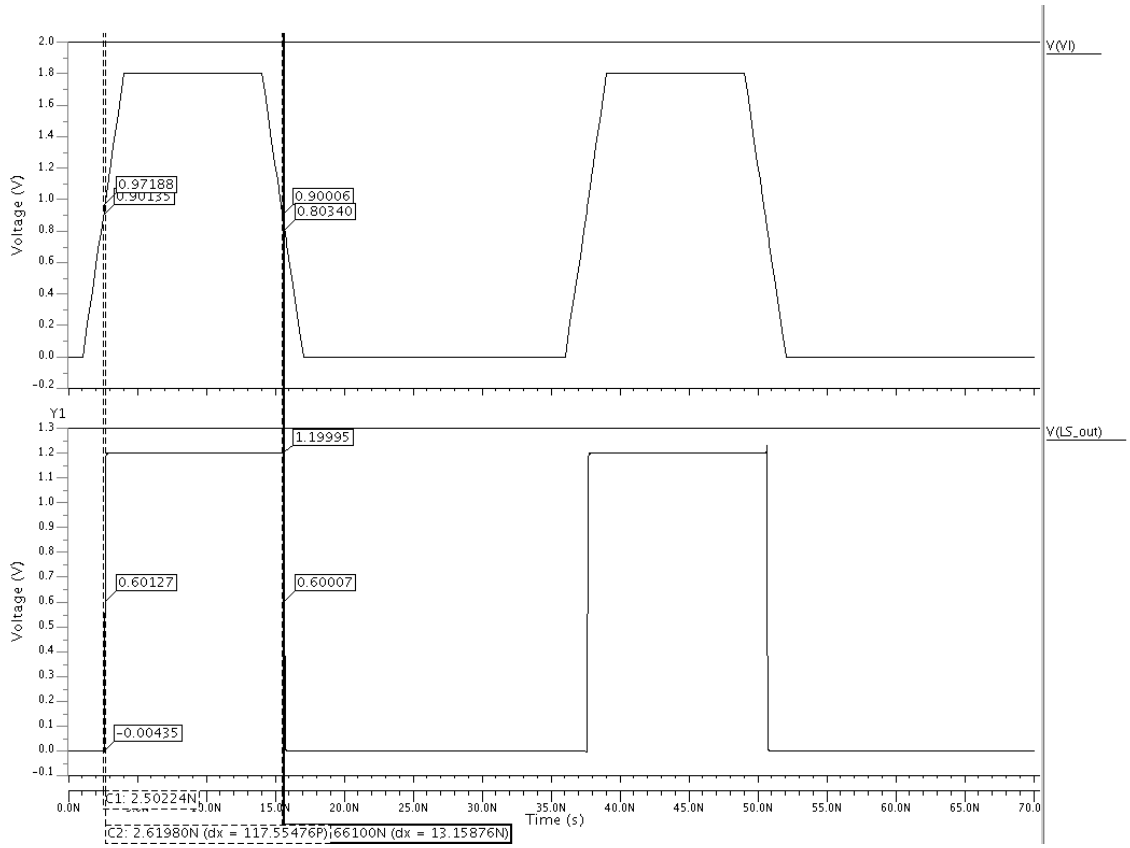

Fig 3.15 : Level Shifter Output

3.4.3 Simulation results of Input Buffer

Fig show output of Input buffer . This buffer contains various Logic Block described above .Each block's output has been shown in fig below.

Process	:	Normal
Voltage	:	0.0 – 1.8 v
Temp	:	27 ^{o}C
Slope	:	0.01
Cap	:	0.5pf

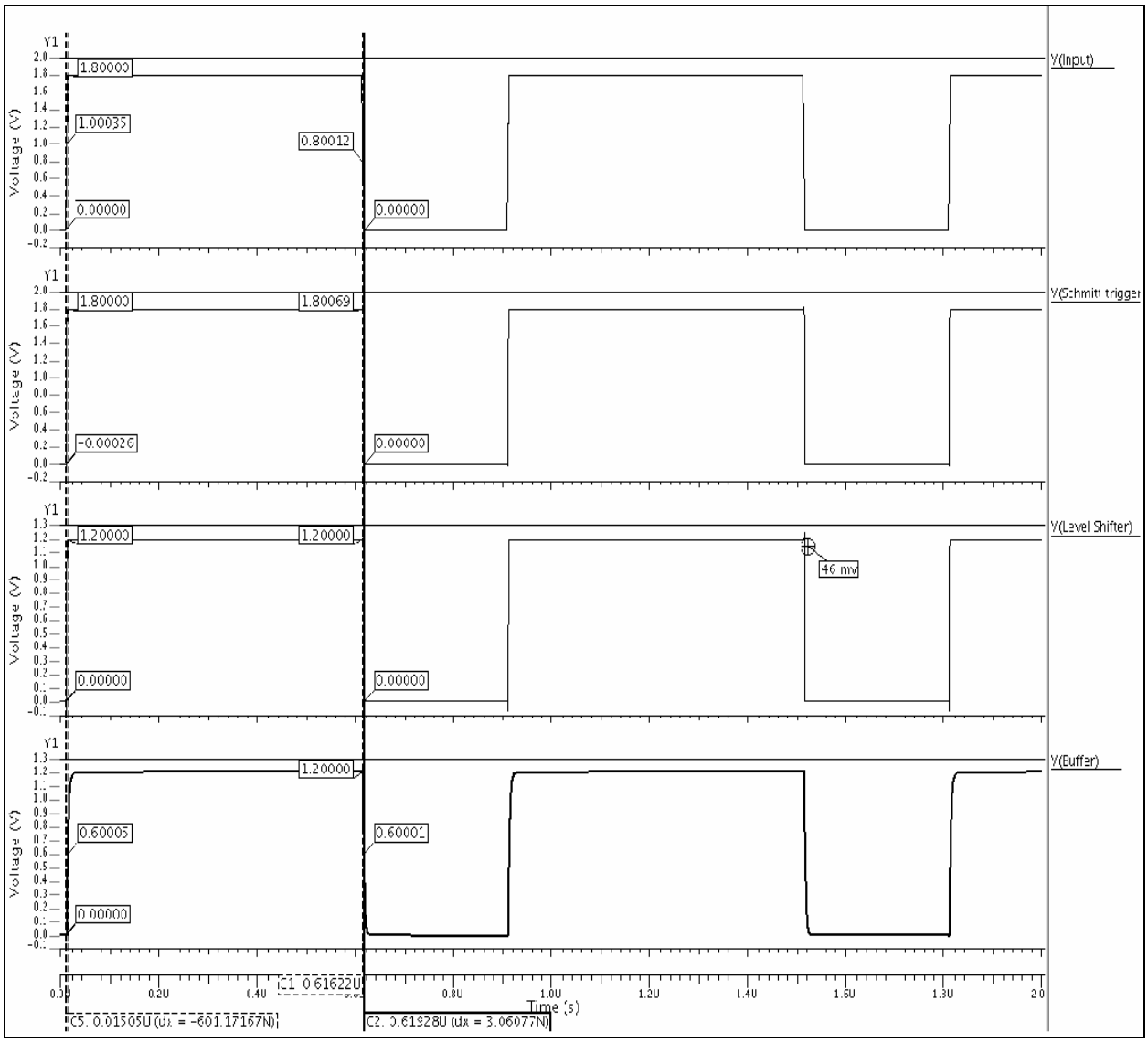

Fig 3.16 : Output of input buffer

Some results of Simulation given below shows output of Buffer at various capacitive load (Fig 3.17)and at different temperature vary from -40 ^{0}C to 125 ^{0}C(fig. 3.18) .

Following Result as shown in fig is obtained under following input condition.

Process : Normal

Voltage : 0.0 – 1.8 v

Temp : 27 ^{o}C

Slope : 0.02

Cap : 0.1pf – 0.9pf

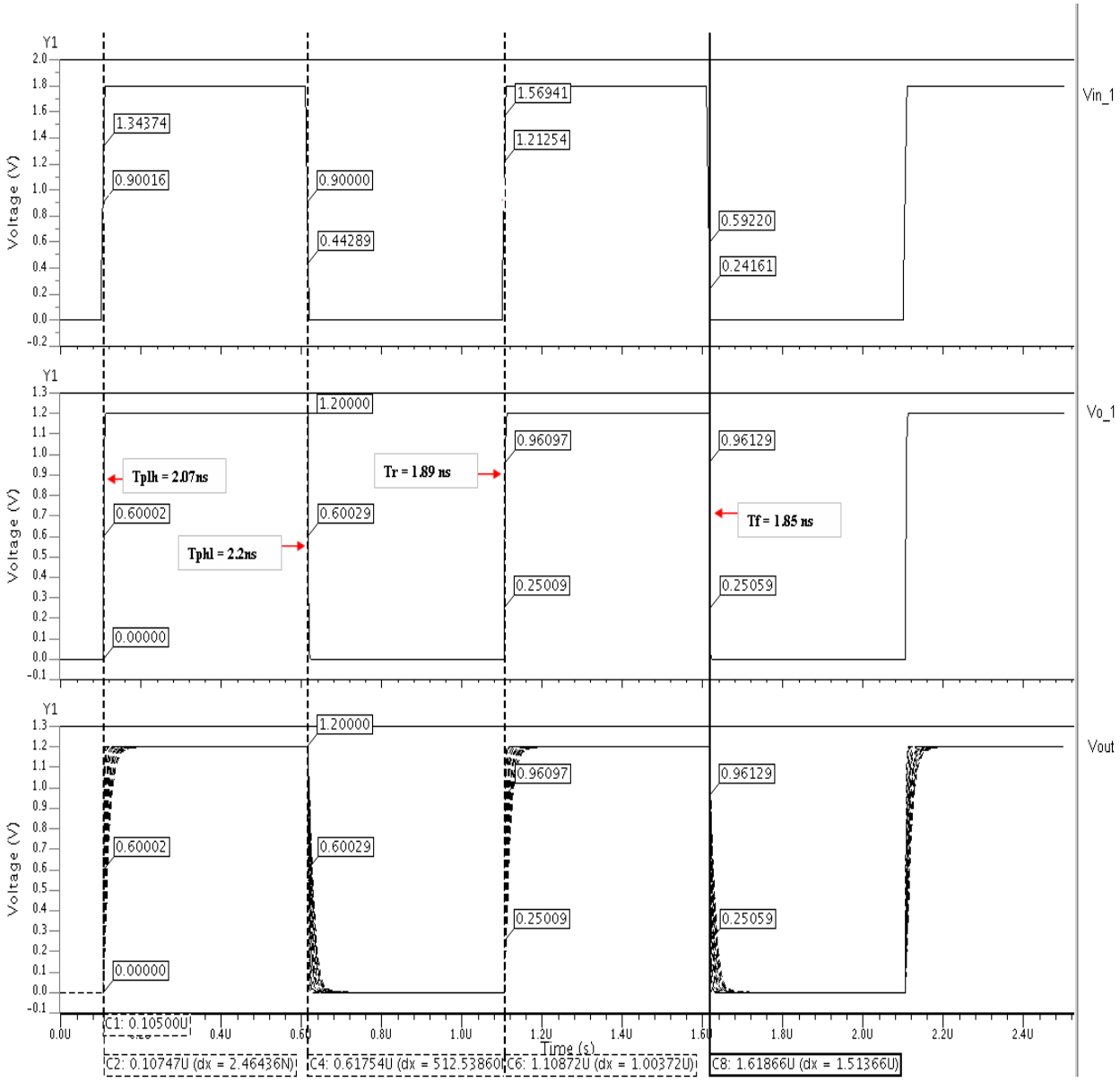

Fig 3.17 : Transient Analysis of Input buffer at C_L = 0.2pf

Dynamic characteristic for input buffer at various Temperatures is as below:

Process : Normal

Voltage : 0.0 – 1.8 v

Temp : -40 ^oC, 25 ^oC, 125 ^oC

Slope : 0.02

Cap : 0.2pf

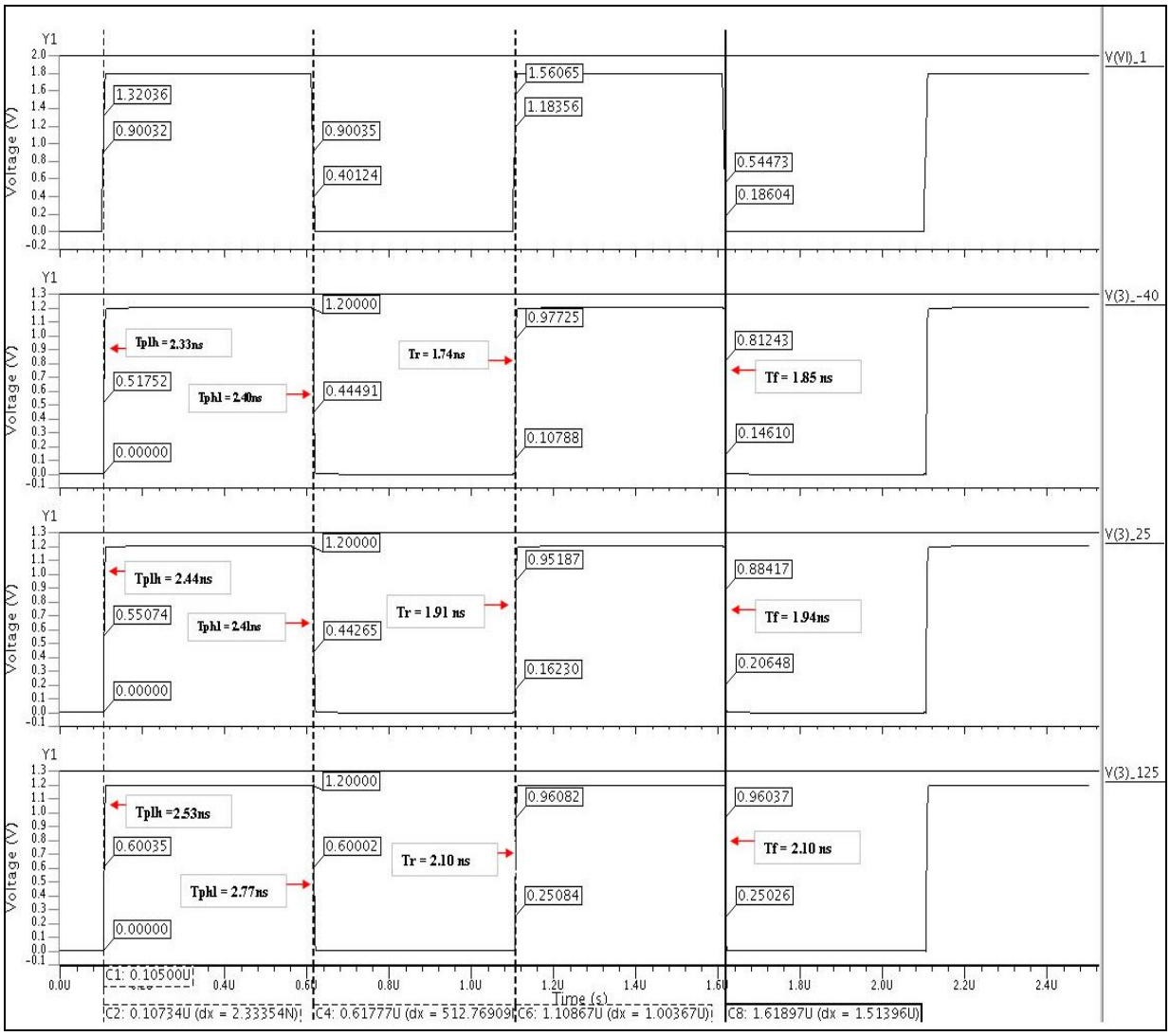

Fig 3.18 : Dynamic characteristics at various Temperature

3.5 Design of Output Buffer and Simulation Results:

Output buffer contain various component like TestPin Block, Level shifter, Predriver, Buffer etc. The architecture of output buffer given here contains Multiplexer, Level Shifter followed by Buffer. This can be described as Driver section

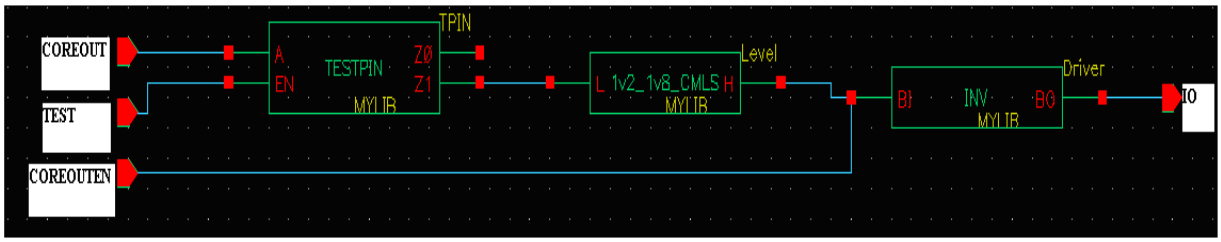

Fig 3.19 : Symbolic View of Output Buffer

3.5.1 TEST PIN Block:

Input of this block is come from CORE part. This block contain enable Pin as TEST. Incase when TEST pin is Low, the signal will not be processed any more because circuit is in TEST Mode. When TEST is HIGH at that time, Buffer come into Role as now circuit is in Normal Mode. In this architecture this block will Provide " Z0" as output when TEST is LOW. For case when TEST is HIGH, signal from COREOUT pin will be passed to Level Shifter.

3.5.2 Level-Shifter :

We have already discussed about importance and working of Level Shifter in Previous section. In output buffer design we have to design High dc level Shifter, which manage voltage level of the signal compatible to IO level. In this case the External and CORE Supply voltage will be applied to different node compare to previous design

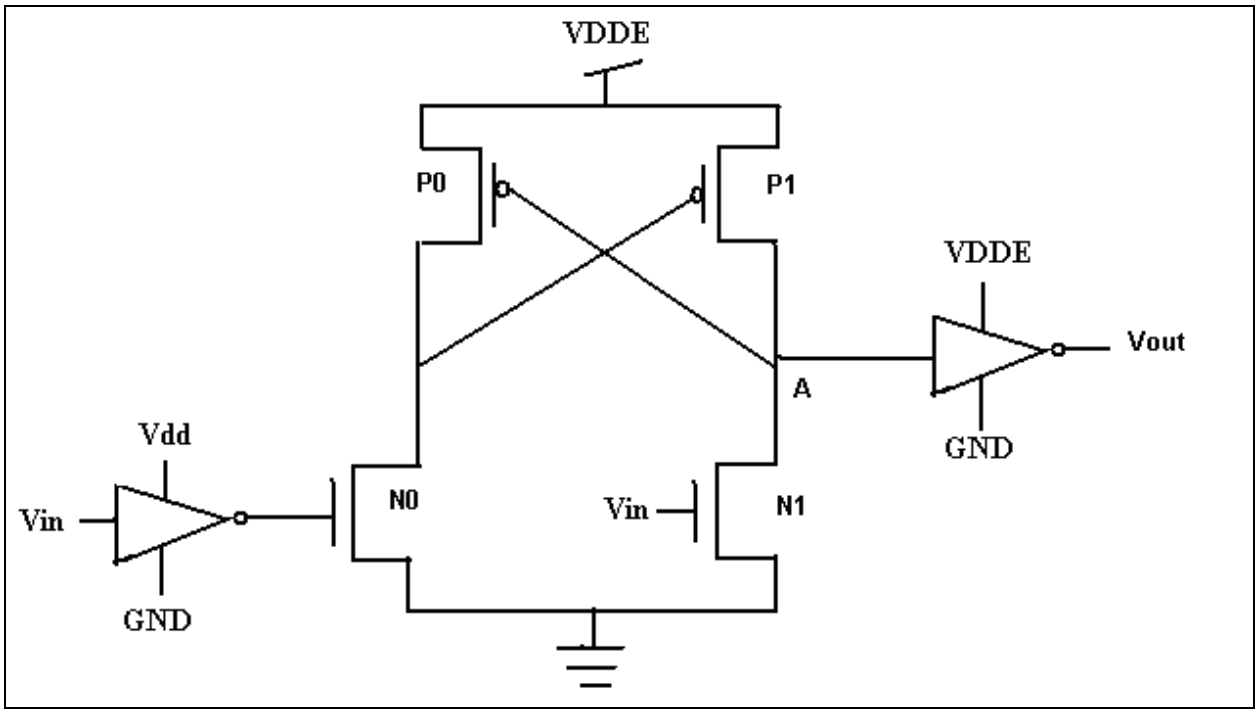

Fig 3.20 Level Shifter [Low –to- High]

Functioning:

Above circuit will operate as in case for High –to –Low, Level shifter .

Design and Simulation results:

For design this Level shifter same criteria will be follow. the only thing we need to keep in difference is that the Process parameter of MOS as well as Supply voltage value.

Simulation Result :

Fig show output of Level Shifter in Both case of TEST signal. First row of fig show input and third row shows output when TEST is Low and HIGH respectively.

When TEST pin is Low at that time level shifter can not provide Full swing output. In other case the level of the output has been extended upto full swing. i.e. VDDE to GND.

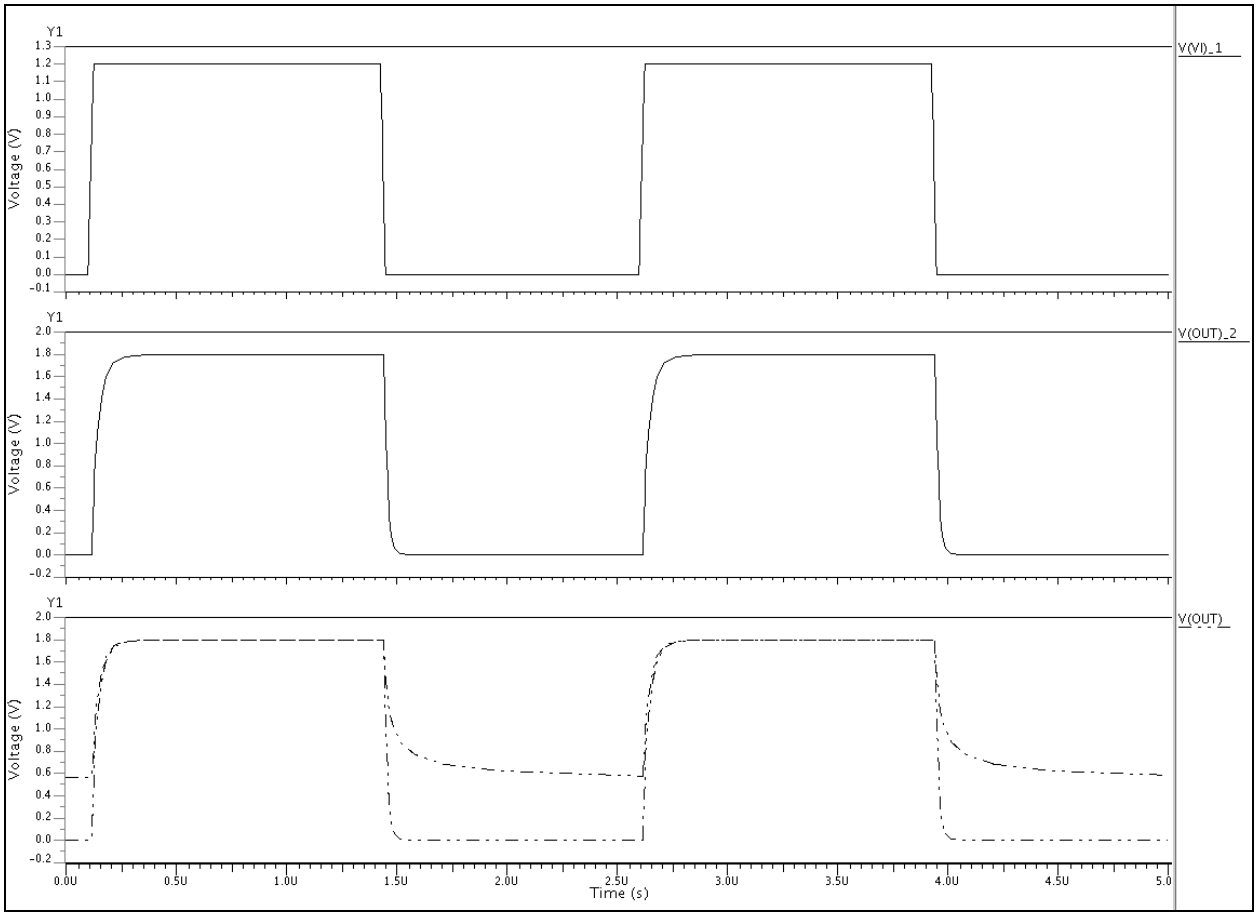

Fig 3.21 : Simulation result of Level Shifter

3.5.3 Output Drivers:

CMOS output pad Buffers are used to drive large capacitive loads which arise from long global interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads. The drive capability of such a buffer should be such as to achieve the requisite rise and fall times into a given capacitive load. Normally the drive capability of I/O buffers as high as 24mA and as low as 0.8mA is available. Conventionally a XmA buffer would mean to source or sink XmA while fulfilling the worst case CMOS dc levels at the output of the sourcing/sinking transistor. Once signal has been converted to VDDE level, now output Drivers decide Driving capability of buffer. In this architecture COREOUTEN plays key role as we have seen in Function table of buffer.

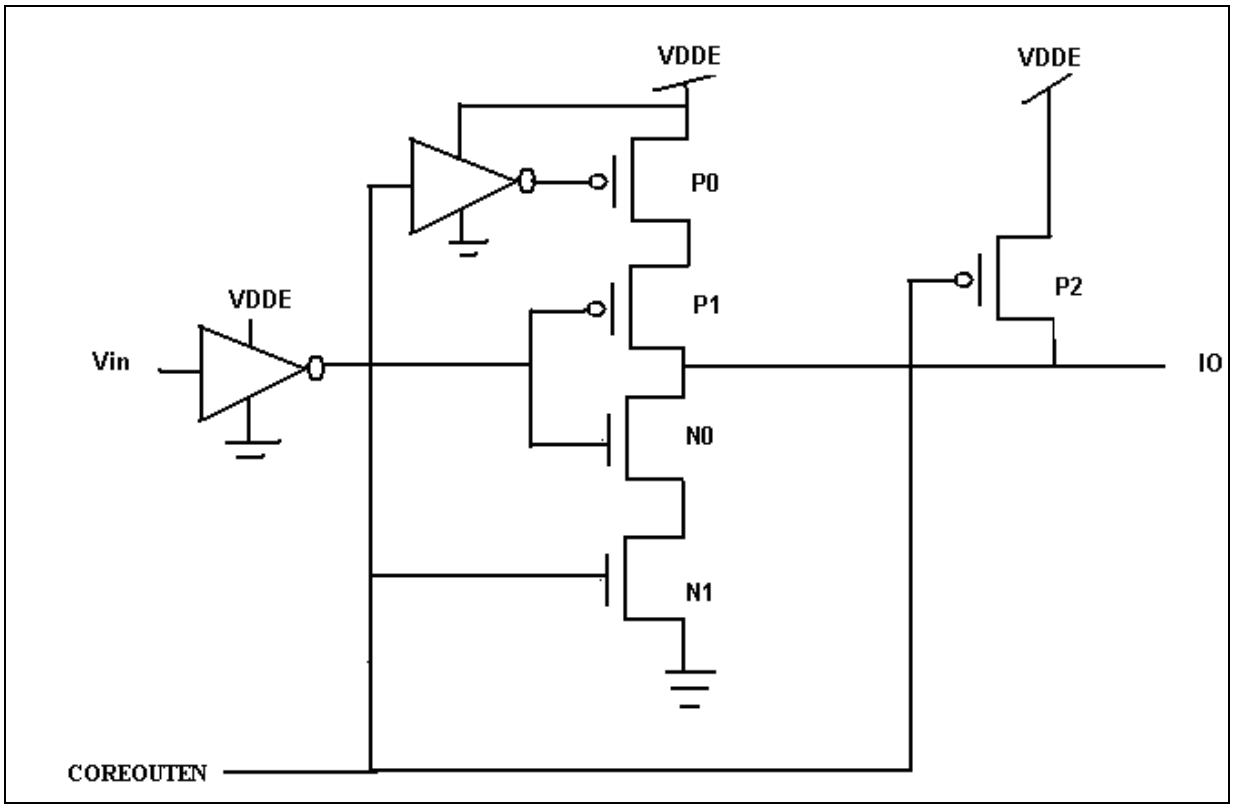

Fig 3.22 : Output Driver

Fig shows design of output driver. Output signal will be controlled by COREOUTEN pin. Two stage inverter has been used here as buffer. Sizing of the final stage inverter is important to decide current capability .

Functioning:

- As COREOUTEN is HIGH

Both P0 and N1 is ON, while P2 is OFF. As result signal will pass to the IO pin.

- As COREOUTEN is LOW

  P0 and N1 is OFF, while P2 is ON. This will pull up the signal to VDDE level ,in place of let the IO pin float.

Design and simulation results

- Consider figure where P0 and P1 transistor is ON ,sourcing current under worst case CMOS dc output levels. The PMOS would be in it's linear region of operation and the current

  $I_{DS} = \beta[(V_{gs} - V_{thp})Vds - Vds^2/2]$

  $\Rightarrow \beta = I_{DS} / [(V_{gs} - V_{thp})Vds - Vds^2/2]$

  We have

  $\beta = \mu_p \varepsilon / t_{ox} . (W/L)_p$

  I_{DS} = 2 mA

  Cox = 87.9 E-7 F/cm^2

- This will give aspect Ratio for PMOS as
  (W/L)p = 38.68

- We take this ratio as

(W/L)p = 40

- Similarly when NMOS is in Linear region we have
  $I_{DS} = \beta[(V_{gs} - V_{thn})Vds - Vds^2/2]$
- This will give aspect Ratio for NMOS as
  (W/L)p = 21.43
- We take this ratio as

(W/L)n = 21

Simulation results:

Fig shows Output signal when COREOUTEN is Low and High respectively. In case when COREOUTEN is low IO signal will be pull up to VDDE Level. When signal is at HIGH level normal signal from CORE is passed to IO PAD. second row of output shows Voltage in both case. The next row shows the current level provided by output drivers.

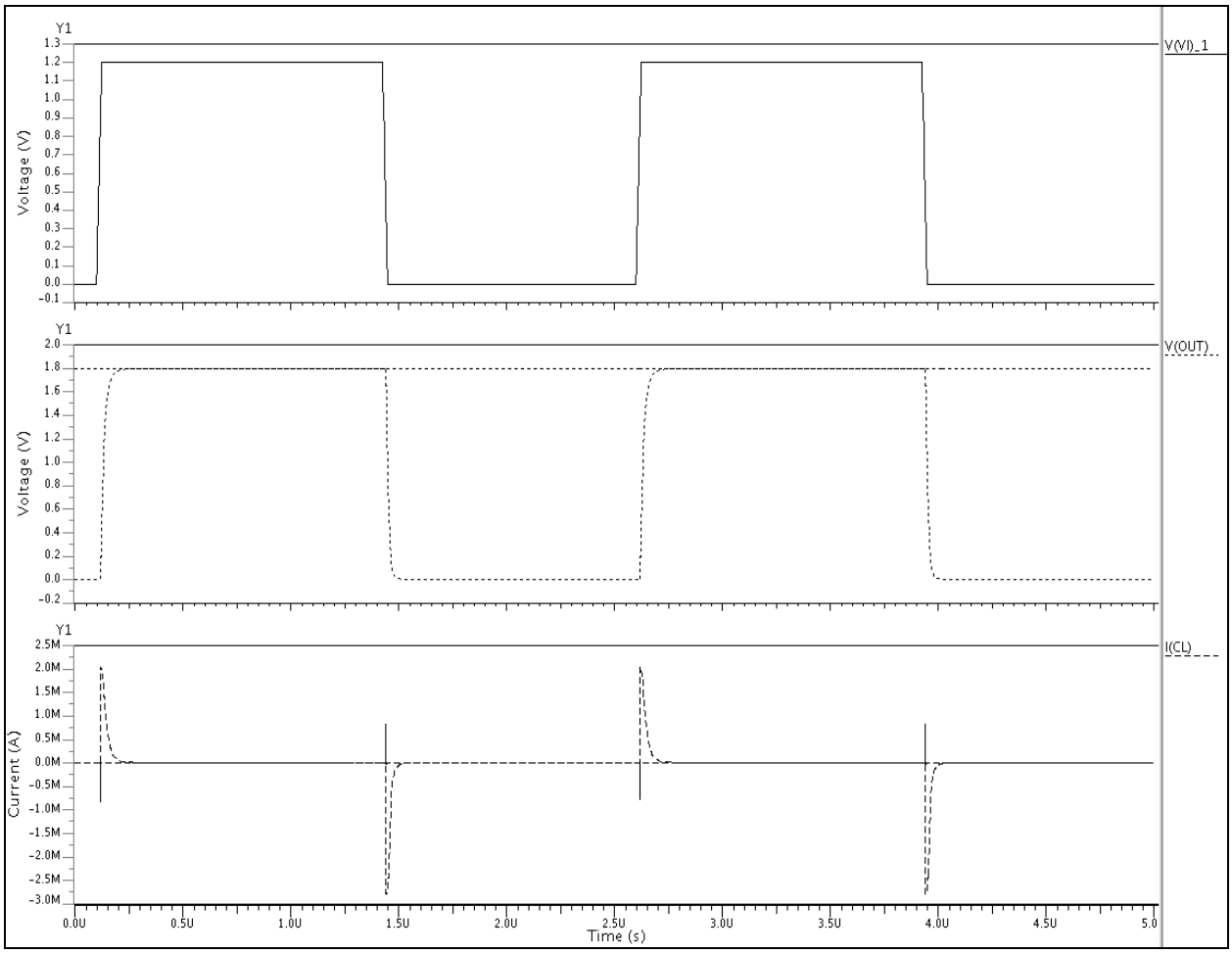

Fig 3.23 : Simulation results of output Drivers

3.5.4 Simulation result of OUTPUT Buffer :

Fig shows Transient characteristics for Driver section. This result has been obtained at Follow condition :

Process	:	Normal
Voltage	:	Vdd – 1.2 , VDDE – 1.8
Temp	:	27 ^{O}C
Slope	:	0.01
Cap	:	10 pf
Result:		
t_{plh}	:	10.43ns
t_{phl}	:	7.52ns
t_r	:	7.61ns
t_f	:	6.08ns

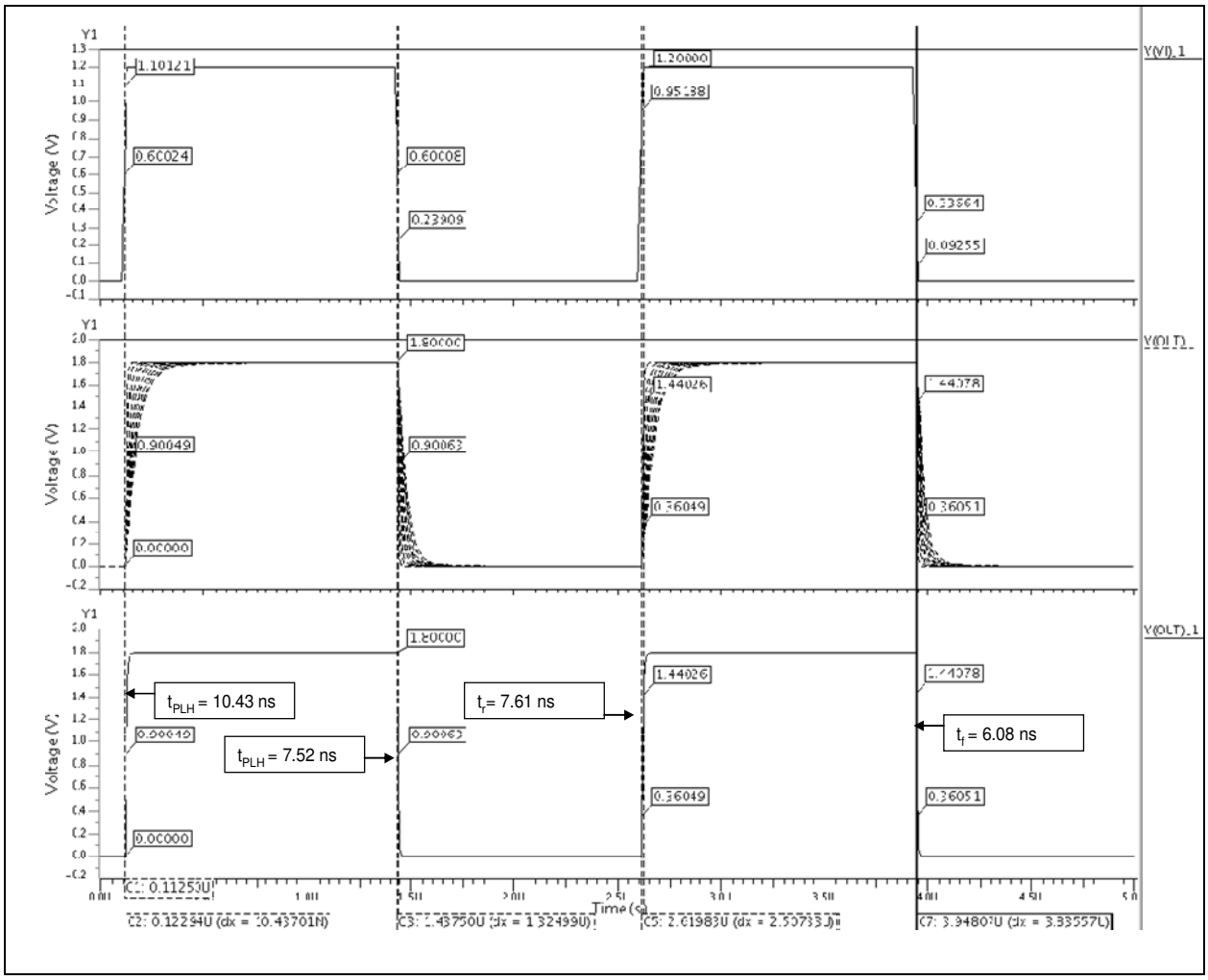

Fig 3.24 : Dynamic characteristics of Driver

Fig below shows effect of Temperature variation over Delay and Current Capability of Output Buffer:

Applied conditions are as Below:

Process : Normal

Voltage : 1.2,1.8

Temp : -40,25,125

Slope : 0.01

Cap : 10.0pf

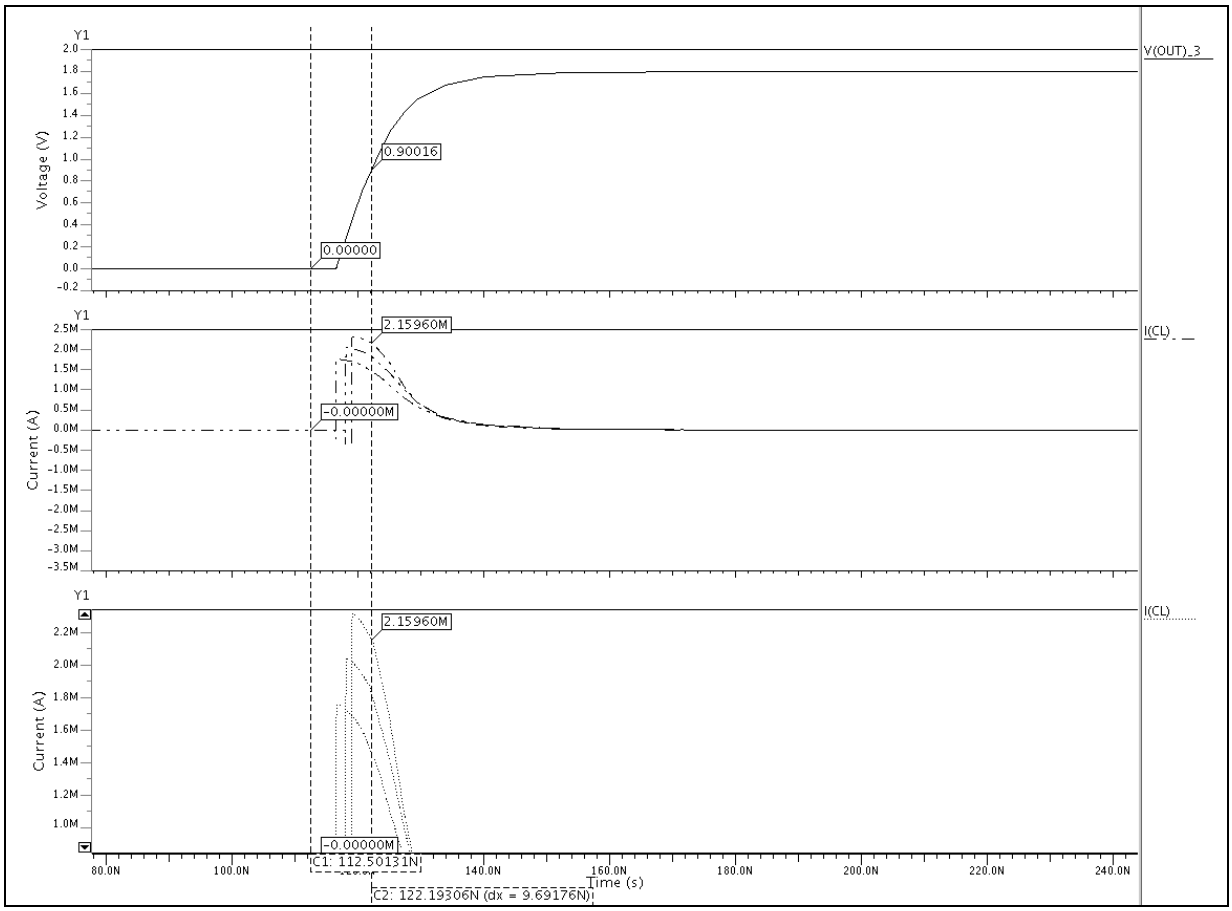

Fig 3.25 : Current capability with respect to change in temperature

Temp (^{0}C)	**t_{PLH}(ns)**	**t_{PHL}(ns)**	**t_r(ns)**	**t_f(ns)**	**I_{out}(mA)**
-40	9.69	7.50	6.71	5.42	2.30
25	10.52	7.62	7.83	5.92	2.00
125	10.83	7.83	8.89	6.88	1.85

3.6 Current at various Temperature

Ch. 4 Characterization Results

In Previous chapter we have discussed about various design and simulation . In this chapter we will analyze Effect of various Process parameter, Temperature on chip performance. Simulations only inform us how a particular circuit behaves, not how to change the circuit to make it better. Development of proper functioning circuit include analysis at various condition and change design according to result obtained.

4.1 Input Buffer Analysis

Fig shows measurement arrangement for Input. Cz is considered as Capacitance on output of input buffer .

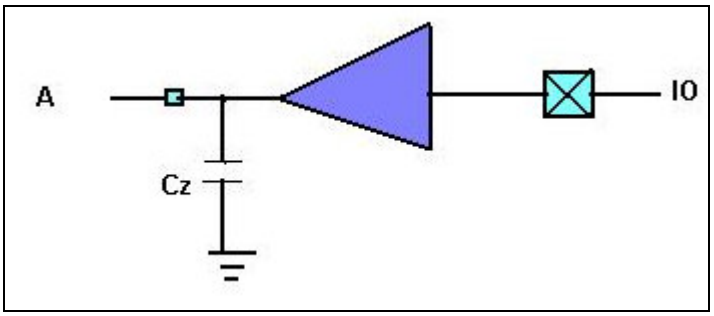

Fig 4.1 : Input Test Setup

Following results details response of design at various Process , Voltage , Temperature , slope and Capacitance (PVTSC). Following terminologies are used for Table given below :

Process : Indicates Worst, best and ,Normal condition

V : Supply voltage

Temp : Temperature in ^{0}C

Slope : slope of input signal

Cap : Load at output pin in pf

All timing parameters are in ns and power is in pw Unit

Propagation Delay Margin **:** 50%-50%

Rise and Fall time Margin **:** 20%-80%

Table 4.1 shows results at various Capacitive Load. It also shows simulation results at various Process parameters. With increase in load there will be increase in delay .

Process	**V**	**Temp**	**Slope**	**Cap**	**t_{plh}**	**t_{phl}**	**t_r**	**t_f**	**Power**
Slow	1.8	27	0.01	0.1	3.15	3.01	2.11	2.08	10
				0.5	5.40	5.36	3.3	3.5	10.2
typ	1.8	27	0.01	0.1	2.60	2.46	1.64	1.60	1.5
				0.5	4.45	4.40	3.2	3.1	1.5
fast	1.8	27	0.01	0.1	2.18	2.01	1.28	1.23	4.9
				0.5	3.6	3.4	2.50	2.45	4.9

4.1 Capacitance and Process Variation

Table 4.2 shows results at various Temperatures. Here different Slope and Cap value has been applied and Temperature has been varied over wide range. With increase in Temp, delay will increase due to change in mobility.

Process	**V**	**Temp**	**Slope**	**Cap**	**t_{plh}**	**t_{phl}**	**t_r**	**t_f**	**Power**
slow	1.9	-40	0.03	0.2	5.11	5.08	3.97	3.86	14.3
		27	0.03	0.2	5.38	5.36	4.22	4.14	19.7
		130	0.03	0.2	5.53	5.48	4.51	4.54	185.6
typ	1.8	-40	0.03	0.2	4.07	4.01	3.08	2.99	11.27
		27	0.03	0.2	4.37	4.30	3.28	3.19	17.31
		130	0.03	0.2	4.53	4.45	3.53	3.48	64.16
fast	1.7	-40	0.03	0.2	3.20	3.17	2.41	2.31	15.58
		27	0.03	0.2	3.53	3.35	2.54	2.47	49.41
		130	0.03	0.2	3.74	3.68	2.74	2.68	252

4.2 Temperature and Process Variation

4.2 Output Buffer Analysis

Fig shoes arrangement for Output Test setup. Cb is capacitance in pf for single bus. It can be vary from 10 pf to 100pf.

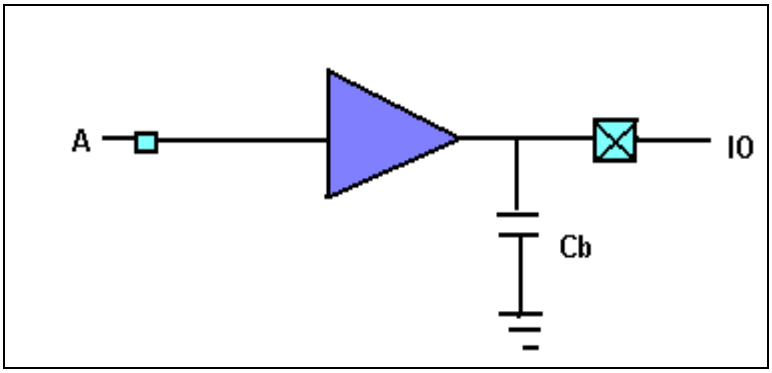

Fig 4.2 : Output Test setup

Table 4.3 shows results at various Capacitive Load. It also shows simulation results at various Process parameters. With increase in load there will be change in delay , rise and fall time will increase. Terminologies used here are same as for the case of Input buffer.

Process	**V**	**Temp**	**Slope**	**Cap**	**t_{plh}**	**t_{phl}**	**t_r**	**t_f**	**Power**
Slow	1.2	27	0.01	10	12.23	9.42	8.70	5.90	9.1
				30	23.19	17.11	26.64	17.14	12.3
typ	1.2	27	0.01	10	10.49	7.55	7.80	5.51	10.7
				30	19.40	14.0	23.4	14.55	19.6
fast	1.2	27	0.01	10	8.5	5.9	7.0	4.4	48.0
				30	16.6	11.8	20.49	12.5	57.3

4.3 Process and Load variation

able 4.4 shows results at various Temperatures. Here different Slope and Cap value has been applied and Temperature has been varied over wide range. With increase in Temp, signal rise and fall slower, as mobility of carriers will effected and delay will increase.

Process	**V**	**Temp**	**Slope**	**Cap**	**t_{plh}**	**t_{phl}**	**t_r**	**t_f**	**Power**
slow	1.2	-40	0.02	20	17.13	12.67	15.34	9.50	9.0
		27	0.02	20	17.54	13.24	17.37	11.12	11
		130	0.02	20	18.02	13.82	21.0	13.5	91.0
typ	1.2	-40	0.02	20	14.77	10.73	13.25	8.92	11.0
		27	0.02	20	14.94	10.90	15.40	9.55	18.0
		130	0.02	20	15.03	11.50	18.34	11.73	60.3
fast	1.2	-40	0.02	20	12.35	8.65	11.7	7.16	17.0
		27	0.02	20	12.44	9.01	13.18	8.57	55.2
		130	0.02	20	12.58	9.79	15.73	10.47	273.0

4.4 Temperature and Process variation

Conclusion

To avoid Noise effect on input Switching, Schmitt trigger is used at Input Buffer. Width of NMOS and PMOS is crucial factor to decide different threshold point for Device. Level shifter is followed by Schmitt trigger to obtain signal level compatible to input core part. With Worst parameter device provide more propagation delay, rise time and fall time, while with typical parameter switching characteristics match with specification.

Driving capability of buffer will increase with increase in Width of Last stage inverter or decrease in length of those MOS. With increase in Temperature Propagation delay will increase and rise time, fall time will increase .Increase in Slope at input side or increase in Load at output pin will result in more delay. With increase in Temperature Current capability will be lower.

Future Work:

This Design consists Input and Output buffer. Work can be carried out further on the following issues:

- With addition of Block defined here for Input buffer, ESD Protection, COREOFF detection block, Input Filter of desired frequency can be designed.
- Mechanism required for Slew Rate control can be provided at output Buffer. ASRC (Active Slew Rate Controller) is best option for this
- To Design Open Drain Part Of Driver.
- Driving capability of Output buffer can be increased to 4 or 8 mA
- Buffer can be designed for Mix-mode [Fast + HS]

Appendix A: Spice File for Input Buffer

==========

```
********************************************************************************
* Library Name:  MYLIB
* Top Cell Name: 1v8_SLB_1
* View Name:     schematic
********************************************************************************
*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.GLOBAL gnd!
+       vdd!
+       vddl

*.PIN gnd!
*+    vdd!

.SUBCKT 1v8_SLB_1 A B_out EN L_out S_Out
*.PININFO A:I EN:I  B_out:O L_out:O S_Out:O
XMIEN net0116 EN gnd! gnd! w=0.135 l=0.07

XMNMOSL L_out net042 gnd! gnd! w=0.135 l=0.07
XMM10 net0116 EN vddl vddl w=0.27 l=0.07

XMPMOSL L_out net042 vddl vddl  w=0.27 l=0.07
XMM7 net080 net042 vddl vddl w=0.27 l=0.07
XMM9 net042 net080 vddl vddl  w=0.27 l=0.07
XML2PMOS net072 S_Out vdd! vdd! w=0.8 l=0.3
XMM5 gnd! net30 net18 vdd! w=0.6 l=0.4
XMM4 net18 A vdd! vdd! w=2.0 l=0.4
XMM3 net30 A net18 vdd! w=2 l=0.4
XMPMOS S_Out net30 vdd! vdd! w=1.5 l=0.4
XML2NMOS net072 S_Out gnd! gnd! w=0.4 l=0.3
XMM8 net042 S_Out gnd! gnd! w=1.0 l=0.3
XMM6 net080 net072 gnd! gnd! w=1.0 l=0.3
XMM2 vdd! net30 net34 gnd! w=0.4 l=0.4
```

XMM1 net30 A net34 gnd! w=1.5 l=0.4
XMM0 net34 A gnd! gnd! w=2 l=0.4
XMNMOS S_Out net30 gnd! Gnd w=0.4 l=0.4
XMPI1 net074 L_out vddl vddl w=3.15 l=0.07
XMNI1 net074 L_out gnd! gnd! w=1 l=0.07
XMPI2 B_out net074 net0121 vddl w=3.15 l=0.07
XMPI3 net0121 net0116 vddl vddl w=3.15 l=0.07
XMNI2 B_out net074 net0105 gnd! w=1 l=0.07
XMNI3 net0105 EN gnd! gnd! w=1 l=0.07

.ENDS

.CIR File

==========

* Input Buffer :

.OPTION SIMUDIV=4 BE XA=3.400000e-07 NOASCII MTHREAD
Vvdd vdd! 0 1.8
Vgnd gnd! 0 0
Vvddl vddl 0 1.2

.INCLUDE $Process_parameter_path
.INCLUDE $netlist_path

.PARAM k = 0.1p
.STEP PARAM k 0.1 0.5 0.1

X1 Vi 3 En 2 1 1v8_SLB_1

Vin Vi 0 pulse (0.0 1.8 0.1u 0.01us 0.01us 0.5us 1.0us)
Ven En 0 1.2
Cl Out 0 k
.temp -40 25 125

.OP
.Tran 0.1ns 5us

.PROBE V I

Appendix A: Spice File for output Buffer

==========

```
********************************************************************************
* Library Name:  MYLIB
* Top Cell Name: 1v2_1v8_TL2
* View Name:     schematic
********************************************************************************

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.GLOBAL gnd!
+       vdd!
+       vddh

*.PIN gnd!
*+    vdd!

.SUBCKT 1v2_1v8_TL2 A EN OE OUT Z0 Z1
*.PININFO A:I EN:I OE:I OUT:O Z0:O Z1:O
XMIP1 net0126 OE vddh vddh w=6.0 l=0.28
XMP2 net076 net062 vddh vddh w=0.4 l=0.2
XMP3 net062 net076 vddh vddh w=0.4 l=0.2
XMP4 net0102 net062 vddh vddh w=6.0 l=0.28
XMSP OUT OE vddh vddh w=18.0 l=0.28

XMN2 net076 net0112 gnd! gnd! w=8.0 l=0.28
XMN3 net062 Z1 gnd! gnd! w=8.0 l=0.28
XMN4 net0102 net062 gnd! gnd! w=4.0 l=0.28
XMIN1 net0126 OE gnd! gnd! w=4.0 l=0.28

XMP0 A net91 Z1 vdd! w=0.135 l=0.1
XMP1 A EN Z0 vdd! w=0.135 l=0.1
XMLP net0112 Z1 vdd! vdd! w=0.54 l=0.1
XMPI net91 EN vdd! vdd! w=0.54 l=0.1
XMN1 A net91 Z0 gnd! w=0.135 l=0.1
XMNI net91 EN gnd! gnd! w=0.27 l=0.1
XMN0 A EN Z1 gnd! w=0.135 l=0.1
```

```
XMLN net0112 Z1 gnd! gnd! w=0.27 l=0.1


XMBP0 OUT net0106 net086 vddh w=18.0 l=0.28
XMBN0 OUT net0106 net0110 gnd! w=12.0 l=0.28

XMENP net086 net0126 vddh vddh w=18.0 l=0.28
XMENN net0110 OE gnd! gnd! w=12.0 l=0.28

XMIP0 net0106 net0102 vddh vddh w=18.0 l=0.28
XMIN0 net0106 net0102 gnd! gnd! w=12.0 l=0.28

.ENDS
```

.CIR File

```
================================================================
* Output Buffer :

.OPTION SIMUDIV=4 BE XA=3.400000e-07 NOASCII MTHREAD
Vvdd     vdd!   0 1.2
Vgnd     gnd!   0 0
Vvddh    vddh   0 1.8

.INCLUDE $Process_parameter_path
.INCLUDE $netlist_path

.PARAM n = 0.0v
.STEP PARAM n 0.0 1.8 1.8
.PARAM k = 10.0p
.STEP PARAM k 10.0p 100.0p 10.0p

X1 Vi En Oe Out Z0 Z1 1v2_1v8_TL2

Vin Vi 0 pulse (0.0 1.2 0.1u 0.025us 0.025us 1.3us 2.5us)
Ven En 0 1.2
Voe Oe 0 n
Cl Out 0 k
.temp -40 25 125

.OP
.Tran 0.1ns 5us



.PROBE V I
```

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