Analysis of Signatures for Observation IP and updating RTL for non-zero Signatures

Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

In Electronics & Communication Engineering

(VLSI Design)

By

Sneh Gandhi

18MECV05

Electronics & Communication Engineering Department

Institute of Technology

Nirma University

Ahmedabad - 382 481

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Internal Guide:

Dr. Usha Mehta

PG Coordinator - VLSI Design,

Institute of Technology,

Nirma University

External Guide:

Rakesh Kandula

Silicon Architecture Engineer,

Intel India Pvt Ltd.

Bangalore

Electronics & Communication Engineering Department

Institute of Technology

Nirma University

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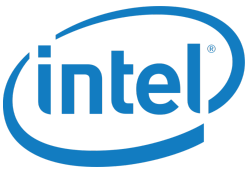
Company Certificate



This is to certify that the major project entitled **Analysis of Signatures for Observation IP and updating RTL for non-zero Signatures** submitted by **Sneh Gandhi (18MECV05)**, towards the partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design, Electronics & Communication Engineering, Institute of Technology, Nirma University, Ahmedabad, is the record of work carried out by her under my supervision and guidance. The work submitted in our opinion has reached a level required for being accepted for the examination.

Date: Place: Bangalore

Mr. Rakesh Kandula
Silicon Architecture Engineer,
Intel India Pvt Ltd
Bangalore

University Certificate

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Date: **Place: Ahmedabad**

Dr. Usha Mehta
Internal Guide and PG Coordinator - VLSI Design

Dr. Dhaval Pujara
HOD, EC Department

Dr. Alka Mahajan
Director, ITNU

Statement of Originality

I, **Sneh Gandhi**, Roll No. **18MECV05**, give undertaking that the Major Project entitled **Analysis of Signatures for Observation IP and updating RTL for non-zero Signatures** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electronics and Communication Engineering (VLSI Design)** of Institute of Technology, Nirma University, Ahmedabad, contains no material that has been awarded for any degree or diploma in any university or school in any territory to the best of my knowledge. It is the original work carried out by me and I give assurance that no attempt of plagiarism has been made.It contains no material that is previously published or written, except where reference has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

Signature of Student,	Endorsed by
Date:	Dr. Usha Mehta
Place:	(Signature of Guide)

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I would also thank the Institution, all faculty members of Electronics and Communication Engineering Department, Nirma University, Ahmedabad for their special attention and suggestions towards the project work.

- Sneh Gandhi

18MECV05

Abstract

MISRs and Compressors are used for Signature analysis in built-in self-test (BIST) Mechanism of digital VLSI circuits.MISR's and Compressor are probably the most commonly used data compaction tools.Signature Analysis is done to check aliasing errors in design.Theory on errors due to aliasing and its proven criteria for the register design, however, are still missing.

This thesis explains the dependency of aliasing on MISR and Compressor used in Observation IP in SOC.Observation IP is designed to determine the presence or absence of faults in SOC at various protocol buses e.g.AMBA.It is also used in IFST,PCI and in address ring of cache.As this IP is used in various parts of SOC it is very important to minimize aliasing due to configuration else we will end up in series of failures.

The task of analysing output Signatures for aliasing based on the length and feedback network of MISR and Compressor configuration is explained in this thesis. It is observed that there are void signatures generated at the output due to non-zero input vectors.The output is not expected to be void,as we could not identify whether the MISR is resseted or input is not applied.The analysis of signatures is done using python.The various libraries of python used for aliasing study are pandas,csv,os,random etc.

Using this analysis MISR's RTL is modified resulting in minimal aliasing of Observation IP. Compressor's RTL is also modified in such a way that no void signature can be obtained at the output.

List of Abbreviations

SoC	System on Chip.
RTL	Register Transfer Logic.
HDL	Hardware Description Language
MISR	Multiple Input Signature Register
IP	Intellectual Property
LFSR	Linear Feedback Shift Register
DFT	Design For Test
DFD	Design For Debug
DUT	Device Under Test
HVM	High Volume Manufacturing
LVx	Laser Voltage Probing
LTM	Laser Timing Tool
IFST	Infield System Testing
PCI	Peripheral Component Interconnect
MUT	Module Under Test
ATE	Automatic Test Equipment
SISR	Single Input Signature Register

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Chapter 1

Introduction

Signature Analysis is done using BIST Mechanism to check whether the circuit is fault-free or faulty.If the output signatures matches with golden signatures then the circuit is tested to be fault-free else it is faulty circuit.But if the defective DUT generates same signatures as the golden,this will result in aliasing errors which leads to loss in fault coverage of the system.Techniques for analysis of aliasing errors for multiple input linear feedback shift registers have been discussed in [1].No exact expression for aliasing probability for MISR's is available that admits arbitrary length test response. In the following, we present the aliasing error due to Compaction Units(MISR and Compressor) and proved that it will reduce as the degree of polynomial increases .We also present aliasing of Compaction Unit depends on its configuration, length and feedback network and not only test sequence.This Chapter explains about Introduction to BIST Mechanism, Objective and Requirement of thesis.

1.1 Introduction to BIST Mechanism

MISRs are perhaps the most widely used method for data compaction in BIST mechanism of digital circuit [2]-[3]. Fig.1 Mentions architecture typical of the BIST. The data obtained at the circuit outputs under test (MUT) from the application of a series of test vectors is stored synchronously in the Compaction Unit. At the end of the test process, to assess the validity of the MUT, the state of the Compaction Unit (the MUT signature) is tested against the intended signature. The major disadvantage of all techniques is that a defective MUT can generate the same output as that of simulated one, resulting in an aliasing error[4] the result of which is coverage loss of the design. The frequency

of these errors usually depends on the entire sequence of outputs of the defective MUT, and therefore its accurate analysis is only possible through exhaustive long simulations.In addition to its impracticality, this method of analysis is unable to provide: i) analytical methods for a early estimation of the aliasing error frequency (and, thus, estimation of the aliasing coverage loss ii) Criteria for explaining the dependence of aliasing errors on the Compaction Unit design; and iii) details on the effect of non-simulated faults on the Compaction Unit aliasing output. Nevertheless, as far as MISRs are concerned, this analysis was successfully extended only to: a) the particular case of LFSR , with the creation of an model of aliasing and analysis of time effects between errors[5]; and b) MISR based on non-primitive and primitive polynomials. In this latter case it has been shown that the resulting aliasing probability is similar to that of any other polynomial of the same degree.[6]

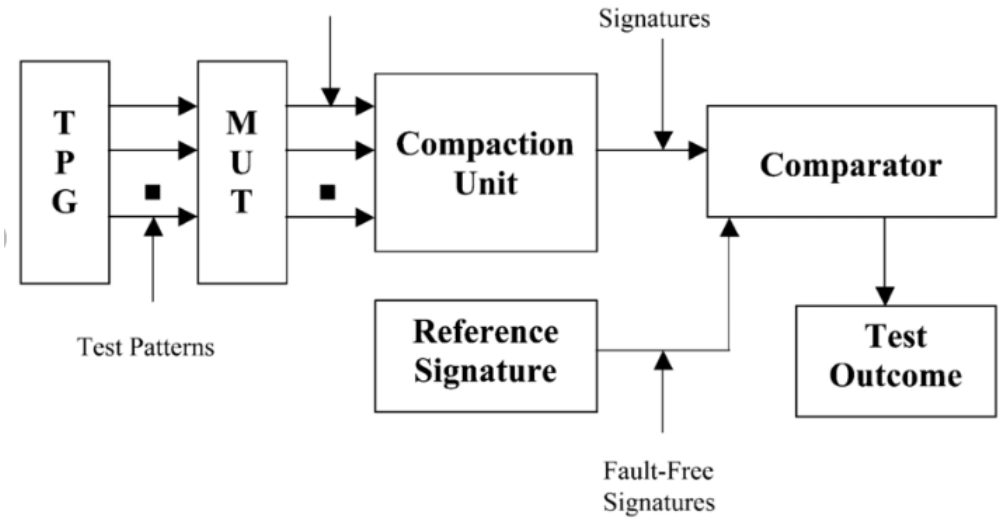

Figure 1.1: General BIST Architecture

1.2 Objective

Objectives for the project are as follows:

- To design modules of Observation IP using system Verilog.
- To design Compressor and MISR using python.
- To Simulate both the designs from System Verilog and from python and to compare the results.

- To study aliasing of MISR for different Primitive as well as Non-Primitive Polynomials of 16 and 32 bits for different compression ratios.
- To Update hardware of Compressor or MISR for non-zero Signature.
- To decide which Compression ratio results in better efficiency.

1.3 Requirements

The development and implementation of this project requires the following:

- Basics of System Verilog.
- Basics of Components of Observation IP e.g. LFSR/MISR, Compressor.
- Python Script to work with csv and Pandas libraries.
- Tools Flow Methodology

Chapter 2

Literature Survey

This Chapter explains about testing process with ATE, Response Compaction Techniques, Introduction to Signature Analysis and Fundamentals of Signature Registers.

2.1 Testing Process with ATE

Test patterns are applied at pin input in traditional scan test methodology, and scan out pin is used to gather the response of design. The response is loaded to the ATE, in synchronization with the test patterns, when the device is under test. This output response is tested bit by bit against expected response of ATE that has 0s and 1s. With the growing functionalities of the digital systems, the input patterns of data and output response were the key difficulties in testing process,when the DUT is being tested.The output response, consisting of 0s and 1s, is tested bit by bit against the expected response of ATE.

The methods discussed here are equally applicable to combinational and sequential circuits. Some of the commonly used words have to be explained before beginning discussion on response analysis techniques.

- Compaction – In this method the reduction in the number of bits takes place at output during testing with some information loss[7]. The ratio of compacted bit stream to the original one is very high. Once the data is compacted using compaction, there is no way to retrieve the original data so data compaction is non-invertible process.

- Compression – In this method the reduction in the number of bits takes place at output during testing without information loss[7]. The ratio of compressed bit

stream to the original one is very high. Once the data is compressed, we can retrieve the original data from compressed version.So data compression is invertible process.

- Aliasing - When the Signature of faulty circuity matches with the fault free circuit due to compaction,resulting in passing test for faulty circuit due to which fault may propagate in the design.This is known as Aliasing[8]

2.2 Techniques For Output Compaction

The input patterns are applied to DUT's pins, and their generated output is compacted to avoid their one by one comparison against the simulated response .The number of test pins and test data should be controlled according to compaction technique.Ultimately compaction compacts the data to one bit. Some techniques for data compaction are discussed here.

2.2.1 Syndrome Testing

This compaction technique is simplest among all compaction techniques .In this technique the number of 1s and 0s are counted in output response[9].The maximum range for count is from 0 to maximum bit number of bit stream. For general usage, the single one-count of response bit stream is less sure.If the counting of 1s does not meet the required value ,then the answer produced to the output is faulty.

2.2.2 Transition Count Testing

This technique of response compaction differs from previous techniques in the way 1s and 0s are counted. Unlike previous techniques here the transitions from 1s to 0s and 0s to 1s are counted[8].In addition, transfer count checking depends on the order in which the data bits appear.

2.2.3 Parity Check Compression

This compression technique[10] uses the information stored in the compression form and to observe the output to detect faults in the circuit being tested.This scheme detects all single-bit errors in the response and all odd number of multiple-bit errors.All errors consisting of even number of bits are masked.

2.2.4 Cyclic Redundancy Check

The Code of Cyclic Redundancy (CRC) is a general form of cyclic code. Which are used extensively[11] for purposes of error detection. A CRC encoder adds p-parity bits to an input binary string in such a way that the resulting code words fit polynomial multiples of a polynomial g(x) degree p generator.

2.3 Signature Analysis

Signature Analysis is used for testing and diagnosis of complex digital circuits[2].It uses LFSR or MISR, with one additional input from a selected point in DUT at its first stage. Upon clock implementation, LFSR or MISR continues on the basis of the logic based on configurations from its internal states and its feedback network.

2.3.1 Fundamentals of Signature Registers

LFSR is used for anaysis of signatures (also known as the signature register), which progresses data from left to right with its stored logic values and has feedback along with an external input [8] to form a serial input to the first stage. Before repeating the sequence, LFSR will count through all possible 2^n 1 states. This is known as the sequence with maximum length. The signature register used uptill now has only one input, which is

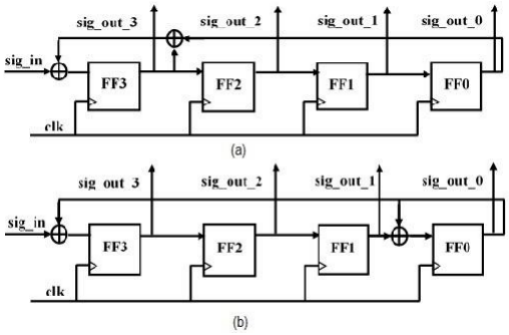

Figure 2.1: LFSR with characteristic polynomial x4 + x1 + 1 using (a) external feedback (b) internal feedback

external, known as the SISR. Multiple input configurations is also possible with multiple inputs.This is known as MISR .MISR has parallel inputs and parallel outputs.MISR calculates the signature for the bit stream produced from the number of check points or scan chains as opposed to SISR, which calculates the signature for only one scan chain.More about MISR is discussed in chapter 3.

Chapter 3

Signature Analysis of Observation IP

S0C integrates several IPs with different functionalities i.e Video IP, Audio IP, Security IP, Testing IP etc. There are different types of testing IPs from different IP providers,Observation IP is one type of testing IP used to test the faulty chips in the design. Following chapter explains about Introduction to Observation IP,Components of Observation IP,Introduction to Signature Analysis,Libraries of python used for Signature Analysis of Observation IP,Signature Analysis of Observation IP using Python.

3.1 Introduction to Observation IP

This IP is designed to determine the presence or absence of faults in SOC at various protocol buses e.g.AMBA.It is also used in IFST and PCI to determine faults.It is also used in address ring of cache.If address goes wrong we will end up in series of failures.Hence it is very important that the Observation IP that contains compressor and a MISR should be robust for aliasing.

3.1.1 Components of Observation IP

As shown in Figure2.1 the Observation IP consists of following modules a) Compressor b) MISR c)Data Accumulation Unit d) Debugging blocks.

- Compressor-To compress the incoming traffic.
- MISR-To produce order dependent output signatures.
- Data Accumulation Unit-To produce order independent output signatures.
- Debugging blocks-Useful for debugging.

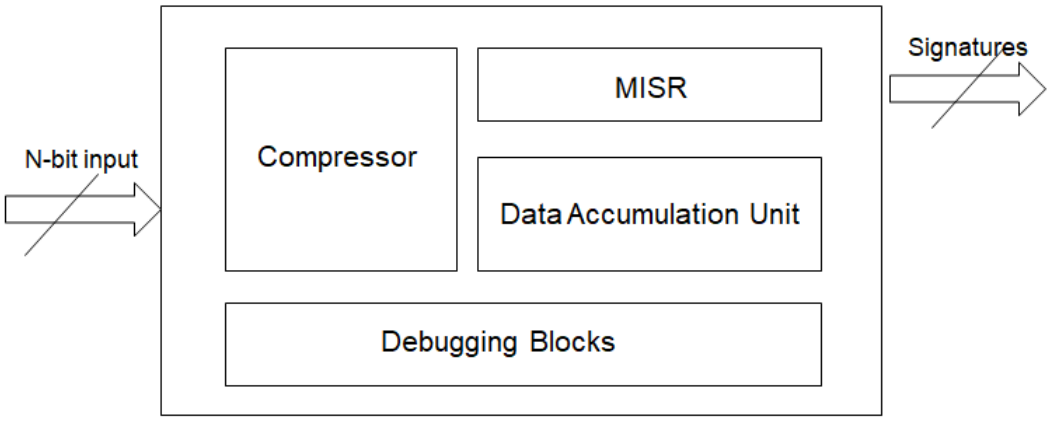

Figure 3.1: Block diagram of Observation IP

Compressor

Compressor is a block that compresses the incoming traffic. Based on the data input and the valid the compression takes place. In this IP the input to Compressor is n-bits where n is user entered bits. This bits are Compressed to 16-bits or 32-bits and it depends on user. The data at the input of Compressor is represented in two ways i.e Data which is divisible by 16 and 32 and the data which is not divisible by 16 or 32.

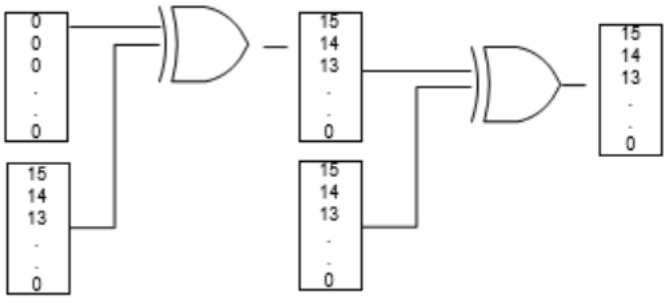

Figure 3.2: Compressor Architecture

- Data divisible by 16/32: Consider 32-bits of data at the input of Compressor. This data is divided into 16 or 32 bits chunks. This 32 or 16 bits chunks will be xored and the final result will be of 16 or 32 bits which will be input to the MISR.

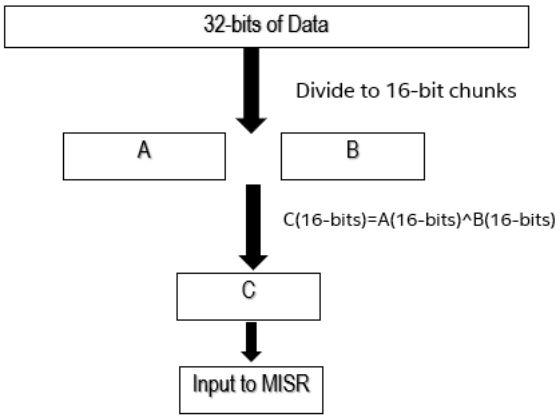

Figure 3.3: Compression of data divisible by 16 or 32

- Data not divisible by 16/32:Consider 66-bits of data at the input of Compressor. This data is divided into 16 or 32 bits chunks and based on input zeros are prefixed in the beginning for e.g. in this case 30 zeros will be prefixed. This 32 or 16 bits chunks will be xored and the final result will be of 16 or 32-bit.

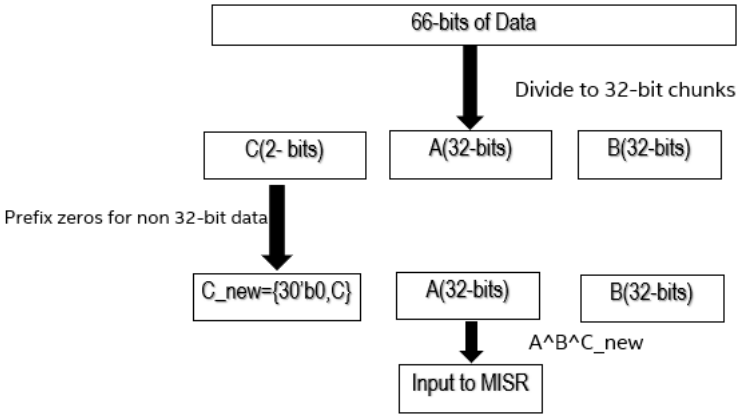

Figure 3.4: Compression of data not divisible by 16 or 32

MISR

MISR stands for Multiple Input Signature Register.The MISR[12] is the primary technique used in signature analysis. The outputs of the circuit under test (CUT) are connected to the inputs of the MISR while the test patterns are applied to the CUT. The final contents of the MISR are compared with golden to determine whether the CUT is faulty or not. MISR has parallel inputs and parallel outputs. LFSR can be configured as MISR based on the enable signal provided,such that when the enable signal is 1 the hardware acts as a LFSR and when it is 0 the hardware acts as a MISR.The Compressed input is provided at the input of MISR and based on the polynomial the MISR gives different Signatures.The Polynomials are of two types 1) Primitive 2) Non-Primitive.[13] Primitive Polynomials: The Polynomials producing highest length sequence are known as Primitive Polynomials.e.g.length=2^n-1. The Polynomials having length less than 2^n-1 are Non-Primitive Polynomials.

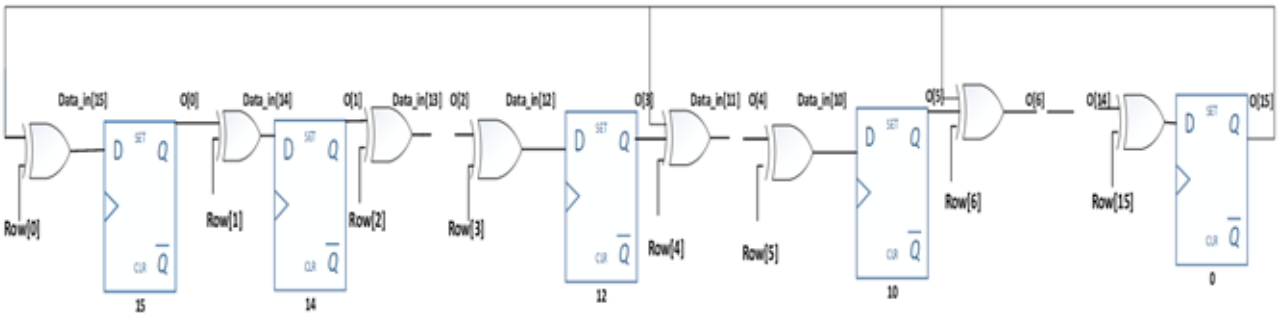

Figure 3.5: 16-bit MISR

In the figure above the input is given at the input of xor gate.The Polynomial shown here is $x^{16}+x^{12}+x^{10}+1$ for 16-bits and it is $x^{32}+x^{25}+x^{15}+x^7+1$ for 32-bit. In addition user can manually enter the polynomial of MISR.

Data Accumulation Unit

This is one of the component of Observation IP.The compressed data from the output of compressor is input to this unit. The main difference between Data Accumulation Unit and MISR is Signature Collection.Misr gives Signature at the output which is order dependent.The order in which data is coming decides the Signature. For example three input vectors appearing in order “a,b,c” vs “b,a,c” at the input of the block, results in

different block outputs.[14] Working of Data Accumulation Unit : f(n+1) (data for cycle n+1) = f(n) (data in cycle n) + f(n-1) (data till cycle n-1).

3.2 Introduction to Signature Analysis

Hewlett-Pickard[2] introduces this Signature Analysis approach as the technique for both research and diagnosis of digital systems. It uses an MISR or LFSR and calculates the signature for the bit stream , with one additional input from a selected point in DUT at its first stage. Upon clock implementation, LFSR or MISR continues on the basis of the logic based on external input and the feedback from its internal states.The remainder can be used as the signature for the specific input in the signature register. The length of signature produced at the end of this test depends on register length.

3.2.1 Signature Analysis using Python

This analysis deals with studying aliasing data in python based on the length and feedback of MISR and the configuration of Compressor.

Input Generation

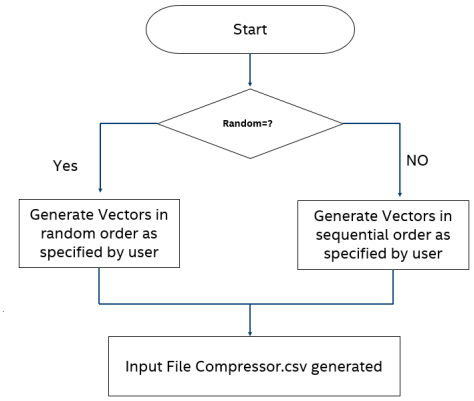

Figure 3.6: Generation of inputs

- From Figure3.1 Initially set of n-bit random vectors are generated where n is the input width of Compressor. The vectors generated will be random or in sequence If the user gives yes than random number upto specified limits will be generated else it will be generated in sequence. This random or sequential vectors are stored in COMPRESSOR.csv file.

Output Generation

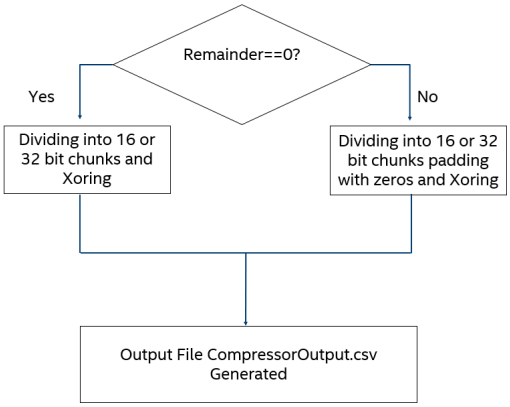

Figure 3.7: Generation of outputs

- From Figure3.2 After Compressor input vectors generation the code will check for remainder if the remainder is 0 then bits will be divided to 16 or 32 bit chunks and it will be xored.
- If the remainder is not equal to 0 then zeros will be padded according to configuration and the chunks will be xored. This random vectors are input to Compressor and are compressed to 16-bit or 32-bit based on user.This Compressed vectors are stored in compressorOutput.csv file.

MISR Output Generation

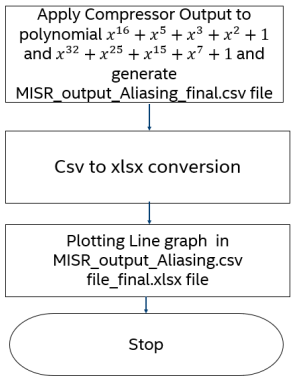

Figure 3.8: Generation of MISR Output

– From Figure3.3 This Compressed vectors are given as an input to MISR and based on the polynomial the final Signature is obtained at the output.Here the user has the flexibility to enter the polynomial manually and the check aliasing of that polynomial.

– Also if no polynomial is entered the default polynomial is executed for 16-bit and 32-bit.For 16-bit MISR the default polynomial is $x^{16}+x^5+x^3+x^2+1$ and for 32-bit the default polynomial is $x^{32}+x^{25}+x^{15}+x^7+1$.

– Finally the line graph is obtained containing information about Signatures and its aliasing.

Combined Input Output Generation

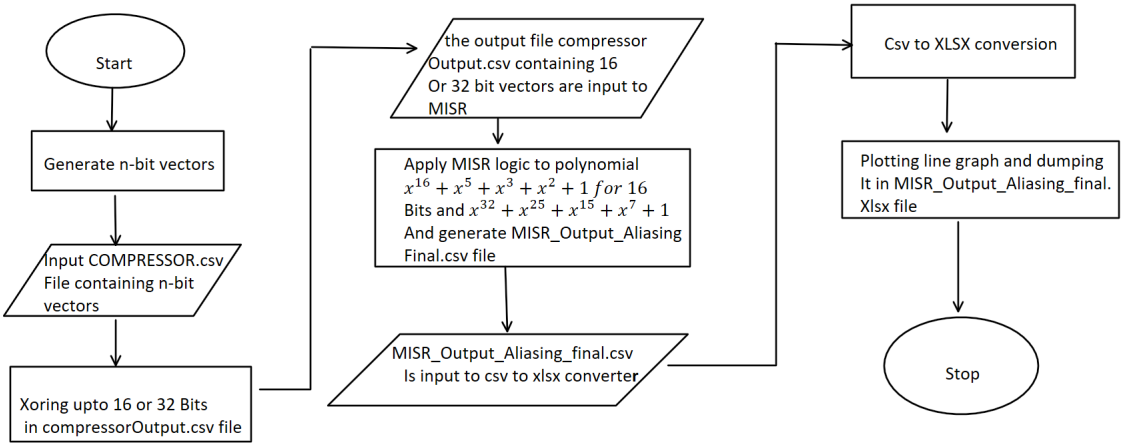

Figure 3.9: Combined Input Output Generation

3.2.2 Libraries of python used for Signature Analysis

The Python contains following libraries that can be used for various purpose in Signature Analysis:

- Pandas: It is an open-source, BSD-licensed Python library providing high-performance, easy-to-use data structures and data analysis tools for the Python programming language.It is used for reading and writing files from excel.

- Matplotlib: It is a comprehensive library for creating static, animated, and interactive visualizations in Python.It is used to plot graphs in Excel.

- Csv: This format is the most common import and export format for spreadsheets and databases.It is used for reading and writing files from excel.
- Os: It provides functions for interacting with the operating system. OS, comes under Python's standard utility modules.Used to delete unwanted files.
- Random: It is used for generating random vectors.
- Collection: This module implements specialized container datatypes providing alternatives to Python's general purpose built-in containers, dict , list , set , and tuple .

3.3 Updated Architecture of MISR and Compressor

By observing the results from python the design of Compressor and MISR is updated such that the aliasing will be minimum and also void signature generation could be stopped.

3.3.1 Updated MISR Architecture

- By observing the results of aliasing of 16 bit and 32 bit MISR,it was found that the aliasing in case of 32 bit MISR is very less so the architecture of observation IP was updated to 32-bit MISR.
- The polynomial used for 32 bit MISR is $x^{32}+x^{25}+x^{15}+x^{7}+1$.

3.3.2 Updated Compressor Architecture

Compressor is a block that compresses the incoming traffic.Based on the data input and the valid the compression takes place. bits[14].The data at the input of Compressor is represented in two ways i.e Data which is divisible by 16 and 32 and the data which is not divisible by 16 or 32.This type of architecture results in void signatures for non-zero input data. To overcome this void signatures the compressor architecture is updated such that it will not result in void signatures for non-zero input data.

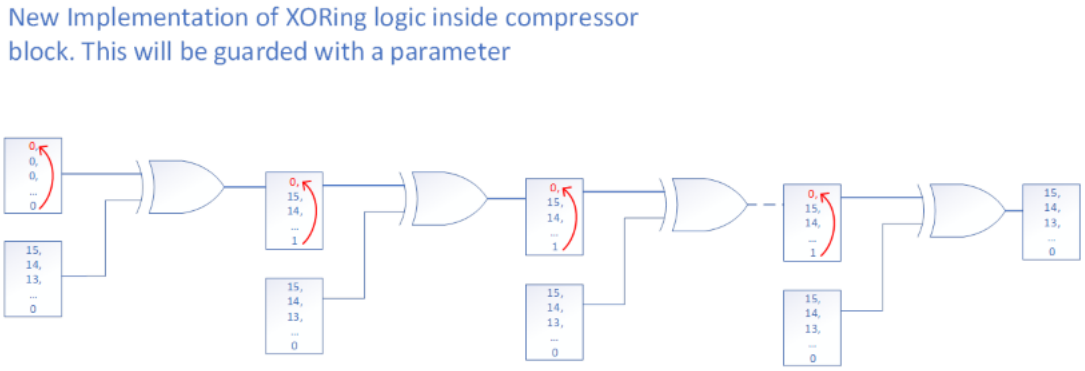

Figure 3.10: Updated Compressor design

Chapter 4

Results

This chapter explains the dependency of aliasing on the compression ratios and MISR length. Here we can conclude on the best possible configuration of MISR and Compressor using aliasing data of 32 bit and 16 bit MISR for different compression ratios.

4.1 Observations

We cannot observe aliasing data of input vectors greater than 2^{19} because excel provides limited rows. So here the data in randomly generated and also can be sequencially generated in the range specified by the user.

4.1.1 Comparison of aliasing data for 16 bit and 32 bit MISR with random input stream

Table4.1 explains the dependency of aliasing on compression ratios and length of MISR and random generation of input patterns. For e.g. for a given 2x compression ratio the aliasing of signatures for 16 bit MISR is 5 and for 32 bit MISR it is 1. So there are set of signatures that are repeated 5 times for $x^{16}+x^5+x^3+x^2+1$ polynomial and it is unique for 32 bit MISR of polynomial $x^{32}+x^{25}+x^{15}+x^7+1$.

Compression Ratios	**Aliasing of signatures for 32-bit MISR**	**Aliasing of signatures for 16-bit MISR**
2x	1	5
4x	1	5
16x	1	4
32x	1	5
64x	1	4

Table 4.1: Aliasing for larger Compression Ratios in random for $x^{16}+x^5+x^3+x^2+1$ and $x^{32}+x^{25}+x^{15}+x^7+1$

4.1.2 Comparison of aliasing data for 16 bit and 32 bit MISR with input stream in order

Table4.2 explains the dependency of aliasing on compression ratios and length of MISR and sequential input pattern generation. For e.g. for a given 2x compression ratio the aliasing of signatures for 16 bit MISR is 8 and for 32 bit MISR it is 2. So there are set of signatures that are repeated 8 times for 16 bit MISR of polynomial $x^{16}+x^5+x^3+x^2+1$ and it is repeated 2 times for 32 bit MISR of polynomial $x^{32}+x^{25}+x^{15}+x^7+1$ polynomial.

Compression Ratios	**Aliasing of Signatures for 32-bit MISR**	**Aliasing of Signatures For 16-bit MISR**
2x	2	8
4x	2	8
16x	2	8
32x	2	8
64x	2	8

Table 4.2: Aliasing for larger Compression Ratios in sequence for $x^{16}+x^5+x^3+x^2+1$ and $x^{32}+x^{25}+x^{15}+x^7+1$

Chapter 5

Conclusion and Future Work

Output Signatures of Observation IP has been studied for Aliasing based on the MISR length and feedback network and configuration of Compressors of different compression ratios. Based on this study concluded that the best possible configuration of MISR, which gives less aliasing is 32 bits. Also found input patterns that result in void signatures at the output of MISR e.g.66660006666 and updated the design of compressor resulting in no void signature generation at the output of MISR.

Future Work is to enhance the script such that it is applicable to all configurations of MISR and Compressor and to check the aliasing data of MISR's and Compressor present in all IPs before handling IP to SOC for integration.

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