Post Silicon Validation of DC-DC Boost Converter Analog IP

A Thesis

Submitted in Partial Fulfillment of the Requirements for the Degree of

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ELECTRONICS & COMMUNICATION ENGINEERING
(VLSI DESIGN)

By

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Certificate

This is to certify that the Internship Report entitled **"Post Silicon Validation of DC-DC Boost Converter Analog IP"** submitted by **Mr.Mayurkumar Patel (18MECV10)** towards the partial fulfilment of the requirements for the award of degree in Master of Technology in the field of Electronics & Communication Engineering (VLSI Design) of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this internship work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.
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- Mayur Patel (18MECV10)

Abstract

The thesis work is on post-silicon validation of Boost convertor Analog IP during the internship period. DC-DC booster is analog IP which is used for DC voltage scaling with reference to input voltage. Voltage scaling is dependent on the duty cycle of the switching of MOSFET. Control signal of Analog IP comes from digital control block. For validation, digital part of Booster IP is prototyped inside the FPGA and analog IP is mounted on Validation board.

Validation Test cases for IP are derived from Test specification of IP, and then test cases are categorised into characterization test, functional test, validation test, robustness check etc. All these tests are performed with help of expensive lab equipments such as Mixed signal osciloscope, Function generator, Power supply, Source meter, thermostream under controlled environment. The results of test cases compared with test specification and the results out of specs were reported back to designer for improvement in Second tapeout.

To bulid up pre-silicon validation platform, FPGA Prototype of digital RTL implemented with model of analog IP. FPGA prototying helps in pre silicon phase for validation bring up, software developement and FPGA verification. FPGA based Validation can provide a demonstration for downstream customers, providing confidence the system is functioning as specified.

Contents

List of Figures

List of Abbreviations

I2C	Inter-Integrated Circuit
I2S	Inter-IC-Sound
FPGA	Field Programmable Gate Array
UART	Universal Asynchronous Receiver/Transmitter
TDM	Time Division Multiplexing

Chapter 1

Introduction

1.1 General

This document provides an overview of key parameters of Booster IP that will be driving Class-D amplifier against Charge pump used to drive Class-D amplifier and also about the validation test which are performed. Booster is DC-DC step up coverter Analog IP.Booster IP is fabricated on individual chip before integrating into Class-D audio amplifier IC. It is used to provide higher voltage than VDD supply at gate to drive high end MOSFET of Class-D amplifier as shown in Figure 1.1. Multi channel Class-D power amplifiers with digital inputs and full diagnostics intended for car entertainment systems[1].

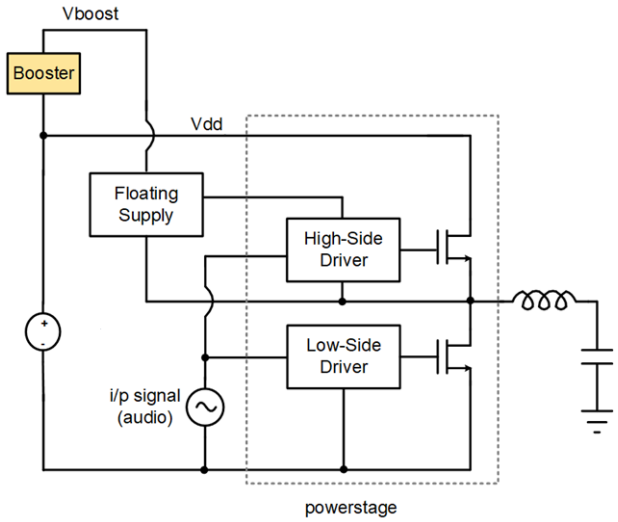

Figure 1.1: Class-D Amplifier with booster

1.2 Brief Design

The booster is used to supply the driver of the high side power transistor of the NMOST-NMOST Class-D output stage[2]. Process used is BCD Power.When switch is on inductor will store enrgy and when switch is off Output capacitor would get charged. Switch on and off time is controlled by the controll loop which monitors output voltage and set the on and off time of switch.N type MOSFET is used as switch and P type MOSFET is used as diode[3].

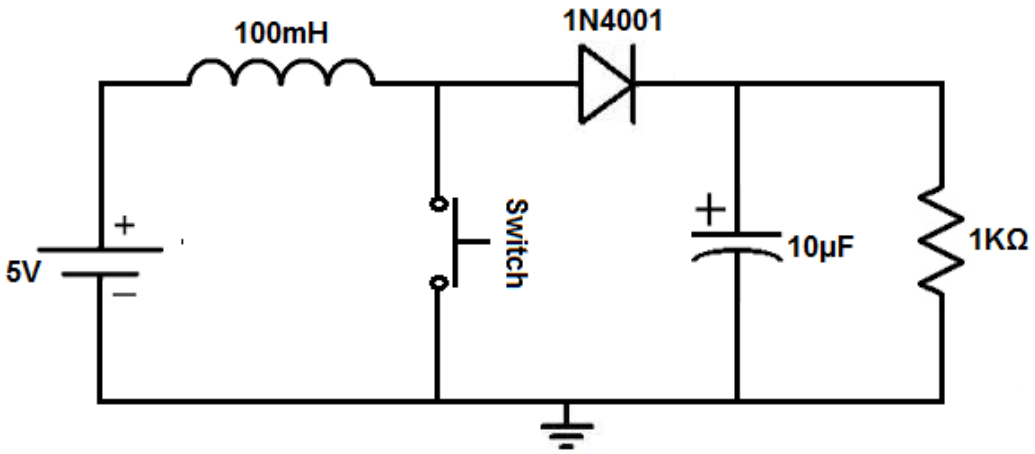

Figure 1.2: DC-to-DC-boost-converter-circuit

1.3 Booster Validation

Validation is done post tape out of the IP. However, the validation strategy is started simultaneously with the design of IP at pre tape out stages. In validation strategy, the first thing is to create test specification from the functional specification of IP. After test specification are created, test cases are generated. From test cases, the test procedure is decided and list of instrument which are required to carry out the test.

Booster Analog IP is validated for three sample across typical and extreme condition.Validation was carried out on pilot plot.In Validation, functional, robustness and characterisation test was performed. The Class-D amplifier IC have many analog and mix signal blocks as mentioned below.

- Powerstage
- Digital Audio Module

- PWM Carrier Generator
- Internal Supply Reference

Also it has many digital block in design as below.

- Digital Controlloop
- Protection (temperature, supply, current)
- Manager (including 8051 micro controller)
- DfT strategy

To do validation, manager which sits inside the IC needs to be emulated in FPGA to provide control for validation test cases. The micro-controller is used for flexibility of the design of the Manager function compared to dedicated hardware state machines. Problems in the manager can be fixed using a software (ROM code) update instead of a full mask change. Only non-timing critical tasks will be done by the μC like settings, control and diagnostics readout. Functions that need a fast response like protection handling, will be handled by dedicated hardware (the glue logic). The 8051 μC is chosen because of low cost (license free) and relative simple design which is good enough for the Manager function of non-timing critical tasks. To do validation, manager which sits inside the IC needs to be emulated in FPGA to provide control for validation test cases.

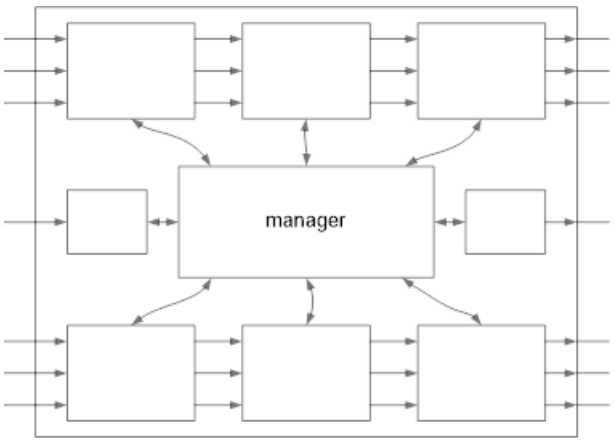

Figure 1.3: Manager connected to different blocks of IC

1.4 Validation Board

To validate booster IP, few handshaking/status signals to/from the digital (manager) are needed. Therefore booster digital RTL is created which is ported into Kintex 7 FPGA. FPGA is connected to validation board via FMC connector.

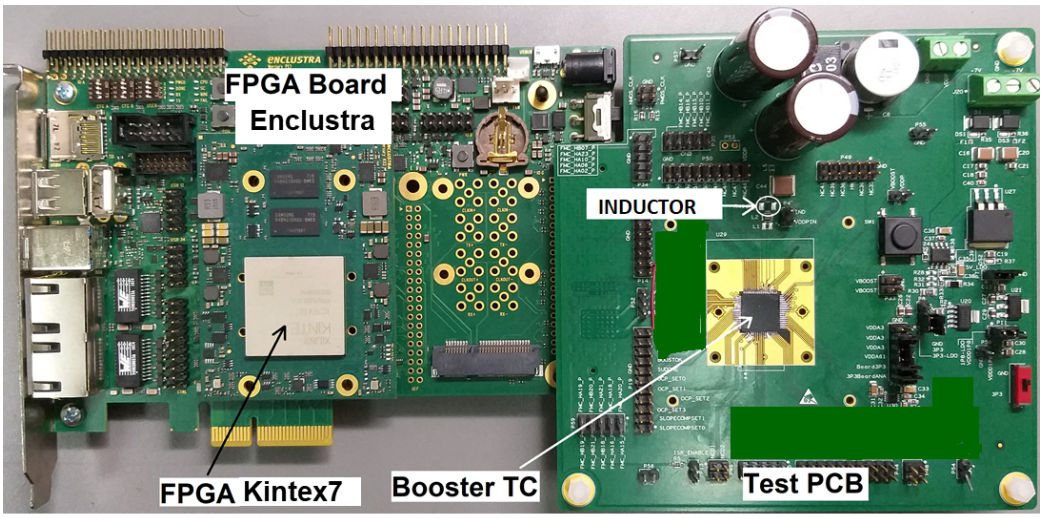

Figure 1.4: Validation board and FPGA

Chapter 2

Literature Survey

This chapter gives details about the topics which are referred validation activities. For Validation of Booster analog IP, digital control RTL part is implemented inside FPGA. What is RTL design is explained in the section 2.1. Section 2.2 explain about the technology on which Audio amplifier IC is fabricated. Later section explain about Communication protocol used in IC. Class D audio amplifire IC communicates through I2C protocol. All the blocks are controlled by by I2C and input to IC is in the form of I2S and TDM. All the IC validation task are automated by the NI testand software. Which is explained in last section.

2.1 RTL Design

Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL. While these languages are capable of defining systems at other levels of abstraction, it is generally the RTL semantics of these languages, and indeed a subset of these languages defined as the synthesizable subset. This means the language constructs that can be reliably fed into a logic synthesis tool which in turn creates the gate-level abstraction of the design that is used for all downstream implementation operations.RTL is based on synchronous logic and contains three primary pieces namely, registers which hold state information, combinatorial logic which defines the nest state inputs and clocks that control when the state changes.

2.2 SOI Technology

A Silicon On Isolator (SOI) process is very suitable for switching devices like Class-D amplifiers due to possibility to avoid latch-up with oxide isolation and the low parasitic capacitances.Class D amplifier is designed based on SOI technology. The amplifier has been realized in A-BCD [**?**] which is an SOI based BCD (Bipolar, CMOS, DMOS) singlepoly, double metal technology. A cross-section of a 60V DMOS transistor in A-BCD is shown in figure 2.1.

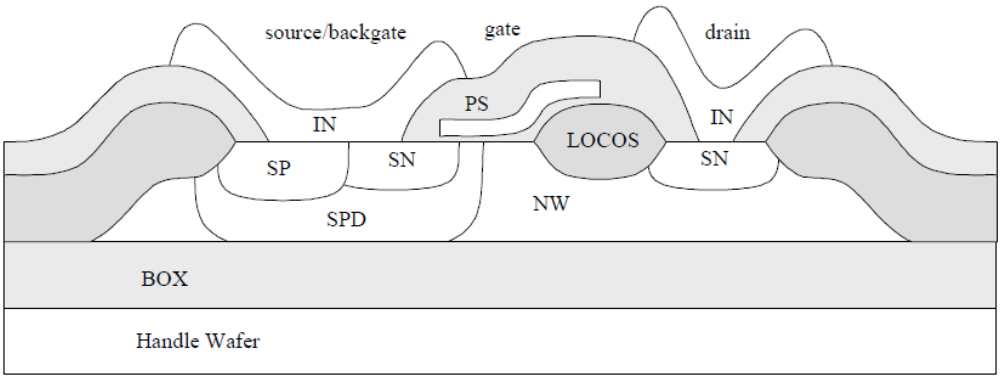

Figure 2.1: Cross-section of HV-DMOS in A-BCD

The dielectric isolation between the integrated components makes designs in A-BCD inherently free from latch-up phenomena. Consequently, the backgate diodes of the DMOS power transistors in the switching power stage can be exploited as freewheel diodes without the need for external schottky diodes. In conventional bulk technologies external diodes are often necessary to prevent injection of minority carriers into the substrate which can lead to latch-up. A particular advantageous feature of A-BCD is the remarkably small reverse recovery charge associated with the backgate diodes of the DMOS transistors. The reverse recovery charge is almost an order of magnitude smaller than that of a comparable DMOS transistor in bulk technology. The small reverse recovery charge makes A-BCD especially suited for switching applications since reverse recovery is one of the major sources of EMI.

2.3 Communication and Audio signal protocol

2.3.1 I2C

I2C is a serial protocol for two-wire interface to connect low-speed devices like microcontrollers, EEPROMs, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems[4]. In Class D amplifier IC, we have micro-controller which is acting as master and other Module such as digital audio module, controlloop, pwm carrier generator etc. are working as slave. Mirco-controller sends commands to this IPs via I2C. Also for Debug purpose we can send I2C commands from outside of the IP via PCs.

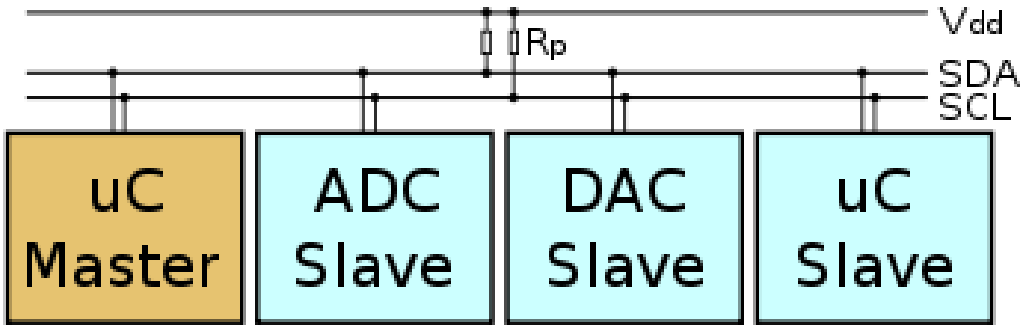

Figure 2.2: I2C-bus

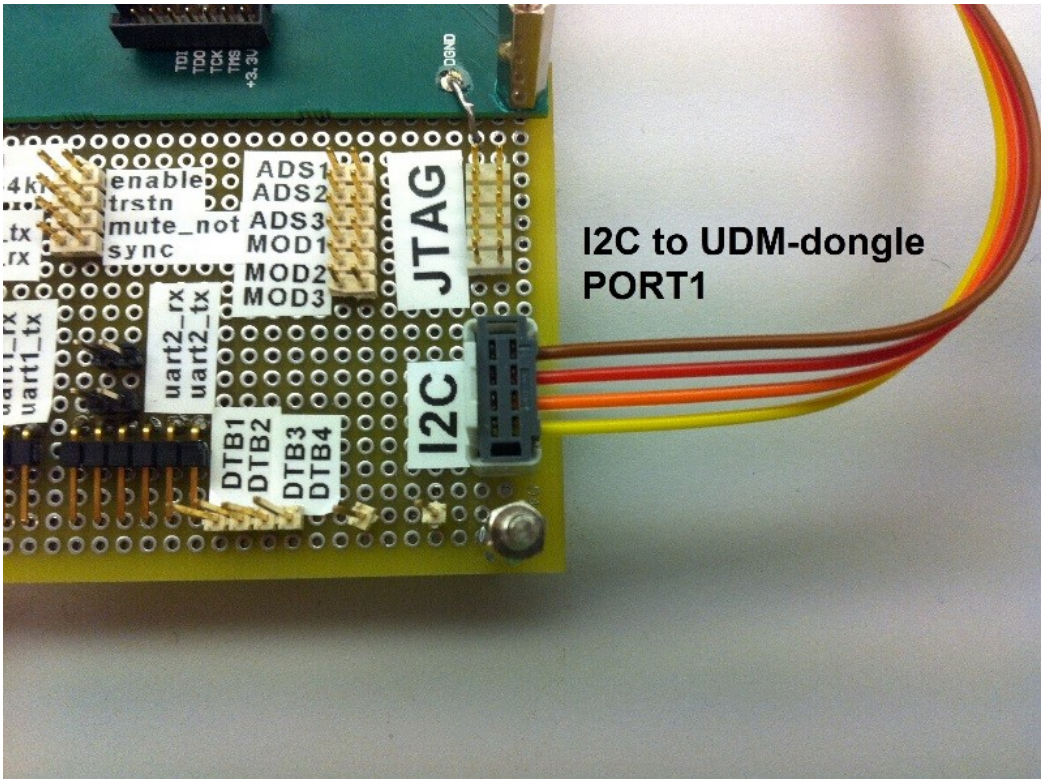

Figure 2.3: I2C-bus on validation board

In I2C wired AND configuration is used as shown in figure 2.4. Both SDA and SCLK are connected to VDDP via pull-up registor. In case of multiple master wants to access same slave module than the master wants to write 1 will be masked by the master who wants to write 0. Whichever data is masked that master will release control of the SCLK and will go into the WAIT state till the SCLK will be released by another master.

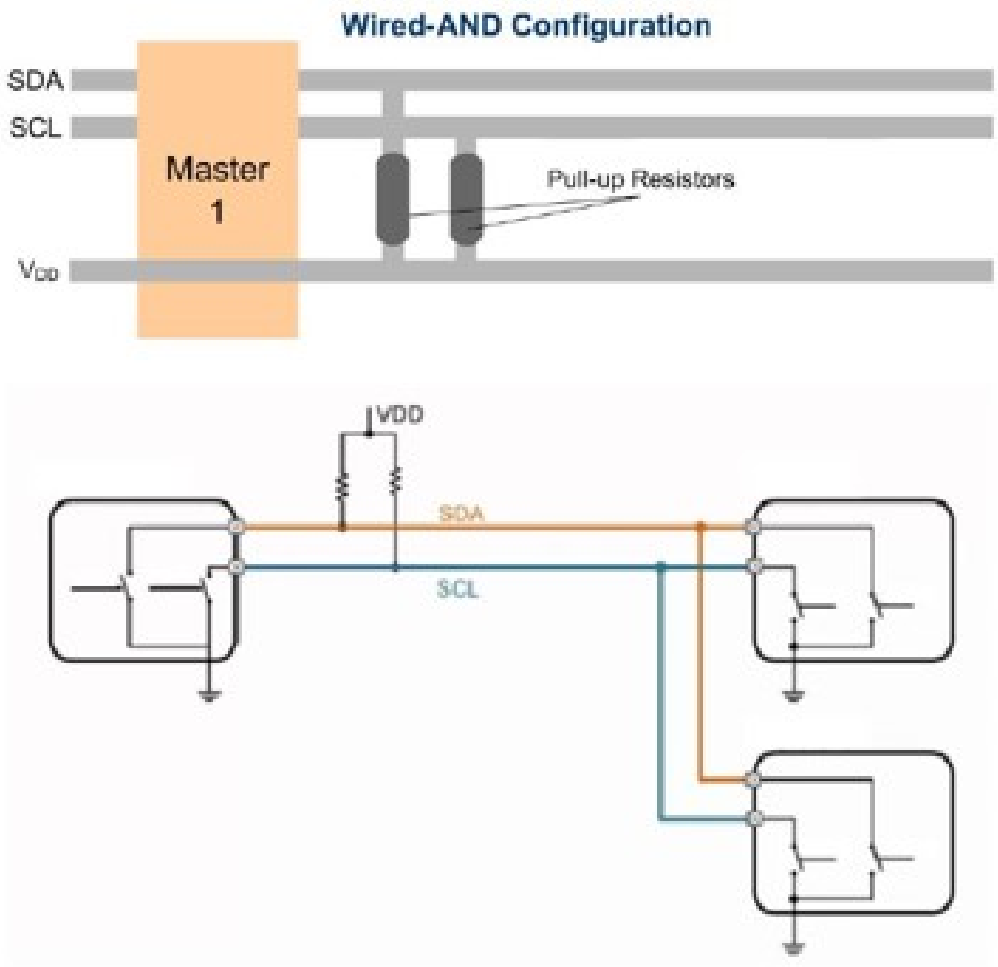

Figure 2.4: Wired-AND configuration is used in I2C

2.3.2 I2S

I2S is Inter IC Sound.It is used to communicate PCM audio data between integrated circuits. Class D audio amplifier takes I2S and TDM audio format as input. It supports two channel for I2S. One channel can be used for right channel and other channel can be used as left channel. It used to connect digital audio devices It handles audio data separately from clock signals. An I2S bus design consists of three serial bus lines: a line with two time-division multiplexing (TDM) data channels[SD], a word select line[WS] and a clock line[SCK]. The word select line indicates the channel being transmitted:

- For WS = 0 -> channel 1 (left)
- For WS = 1 -> channel 2 (right)

Data is transmitted two's complement, MSB first.I2S Bus uses standard TTL logic levels. Typical clock [SCK] frequency is 2.5MHz, maximum clock speed is 3.125MHz. The WS line is sent one clock before the data is sent. The Master drives SCK, and WS. Either the Transmitter, Receiver, or Controller may be the Master

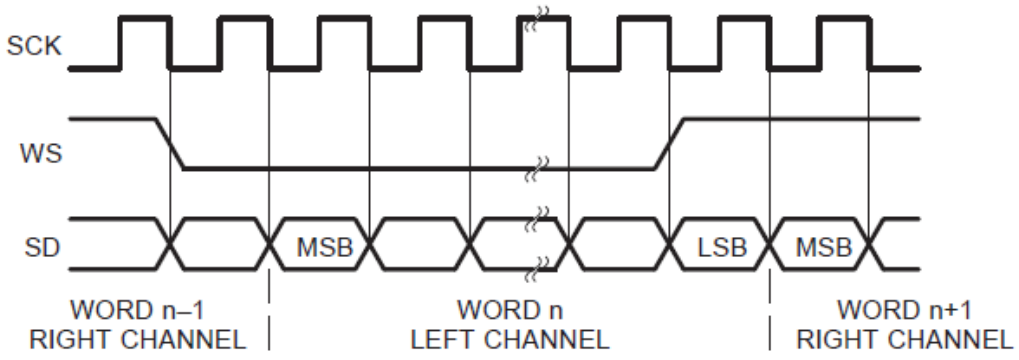

Figure 2.5: I2S audio format

2.3.3 TDM

TDM is time division multiplexed audio communication protocol. For TDM there is no standard protocol, but we can use as per our convenience. TDM frame can have upto 16 slot. We can transmit up to 8 channel with right and left channel in all 16 slot. TDM is similar protocol as I2S. Difference is that I2S can have only two slot per frame where as in TDM can have 16 slot. We can use each slot for transmitting different information. TDM also have data line SD, word select line WS, and clock SCK. WS select line is for synchronisation of TDM frame. When frame start is indicated by either high to low or low to high transition. Also we can use WS line for indicating bit width of one slot of TDM frame. Here incase of Audio amplifier IC, TDM is used for transmitting 4 channels and also for transmitting voltage and current information.

2.3.4 NI TestStand

NI TestStand is the test sequencer software for Automation from National Instrument. TestStand is ready-to-run test management software that is designed to help quickly develop automated test and validation systems. With TestStand, we can develop, execute, and deploy test system software. We can extend the functionality of our system by developing test sequences in TestStand that integrate code modules written in any programming language. TestStand provides extensible plug-ins

for reporting, database logging, and connectivity to other enterprise systems. We can deploy test systems to production with easy-to-use operator interfaces.

Chapter 3

Validation

This chapter explain about Validation activities carried out for Audio amplifier IC. Work is carried out in four phases. The following sections provide detailed work summary. For validation, automation framework was developed to perform the test. Automation is required to get reliable and repeatable results. First section explain about the Design and Automation framework. The next section explain about the test cases executed and the procedure. FPGA platform bringup section explain about validation platform development and the FPGA prototyping. Last section discribe about the RTL design for TDM receiver module and Implementation of it in FPGA.

3.1 Design and Automation framework

As a validation engineer, it is important to understand IP design, use cases, specification, and the scenarios for which it is designed. Previous generation of Audio amplifire IC by NXP is TDF853.6 To get started with the validation knowledge of previous project is important. Therefore, validation was started with the learning of TDF8536. All the validation document go-through happened in the start of project. Then the decision was made on how much reuse is possible for Validation framework, test cases and Instrument would required for Audio amplifier. For automation of different instruments (Source meter, oscilloscope, multi-meter) and different probes Labview programming was used. All these instruments are used to do measurement of current, voltages, intermediate signals, and the derating of different electrical component. Derating of component is degradation of performance with the temperature variation. Logging of result was also done through LabVIEW.

The measurement are very sensitive so it is important to choose right kind of probe. There are different kinds of current probe, active probe and passive probe. Therefore, learned basics of LABVIEW tools. This tools is used to make graphic user interface which control all the lab instrument. We can create different virtual environment and can control or program all the instrument. Automation is very important because taking all the reading manually is very cumbersome process and there might be a chances that while handing the instrument we disturb the configuration of bench. This can cause failure of device or reading taken might not be right.

3.2 Test cases performed

As a part of booster validation characterization test, learned efficiency test setup, startup current setup and Load transient setup and also collected data for 100 device across different condition as mentioned in test plan.

Knowledge transformation session for RTL design was arranged to port Booster IP in FPGA. The learning of the workshop are

- Pin changes and debug port assignments in code for validation purpose
- Bit stream generation for different voltage levels
- Reset button change as required for the automation
- Labview reset assigned for automation purpose
- Bit file generation for different vddp and ocpset value. ocpset values define the threshold for overcurrent protection
- Generating bit file for making some input digital pins zeros and ones as suggested by analog design engineer for particular test
- Finding the spare fmc pins and their respective fpga pins

In functional test, over current protection test, over voltage, under voltage, Boost high signal, etc. test were performed. In Over current protection test, manually applied different threshold values and checked the current and the output of comparator. In characterisation test leakage current test for 20 devices with resistor on board and without on board resistor at room temperature was performed. To perform test specific bitfile was required. Following bitfiles were generated

- Generated of bitstream file which will cut off chip enable signal on pressing user button 0. This bitstream file was used to perform off voltage in shutdown mode test.
- Generated bitstream file for VDDP voltages as mentioned in test plan with different value to perform over current protection test.
- Generated bitstream file for VDDP voltages 5.5, 14.4 and 45 V with ocpset value 1110.
- Performed load transient test with Murata inductor on board for VDDP 5.5 V and frequency 2.7 MHz, 3 MHz and 3.6 MHz.

3.3 FPGA platform bringup

In this period learned about FPGA emulation. For emulation we have used OpalKelly XEM6010 FPGA and Breakout board 6110 for connection to other modules. OpalKelly provides more controllability and observability by FrontPanel Software on PC. We can have as many virtual inputs and virtual outputs as we wants. USB microcontroller communicate between FrontPanel and FPGA via endpoint. We can give inputs from software and can observe output on software via UART. Front Panel can be designed by XML.

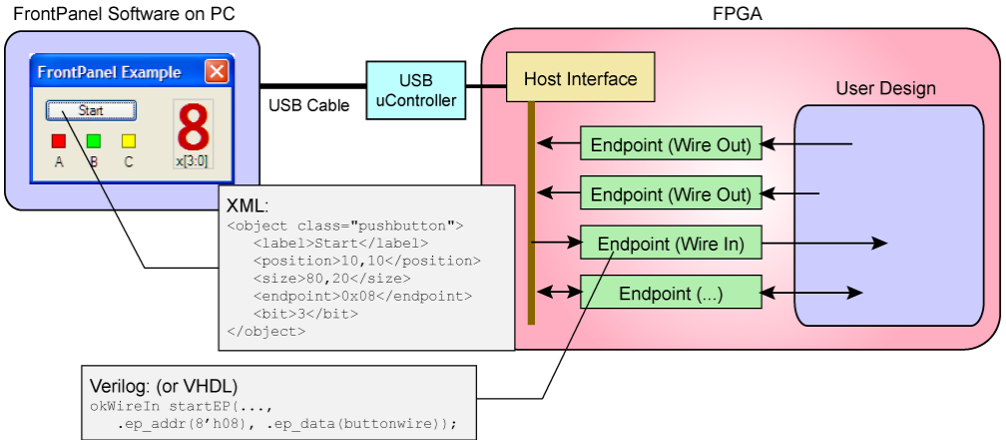

Figure 3.1: OpalKelly FPGA board interface

For development of the class-D amplifier ROM-code, a real-time and real-life environment is needed. In the first silicon-spin , there was a similar amount of RAM available as ROM (16 kB). Since the second spin however the ROM-size has

been increased drastically, to 48 kB, while the RAM-size has been decreased to 6 kB. This means that ROM-code development can no longer be done via the on-chip RAM. Therefore an FPGA-implementation of the Class-D amplifier manager has been created. This fpga-manager is identical to the class-D amplifier manager and is used to run the amplifier software. On the Class-D amplifier IC itself, a dedicated program will run which modifies the its manager to basically a UART handler that interfaces between the ESFR-registers/interrupts on the Class-D amplifier IC itself and the fpga via the onboard UART.

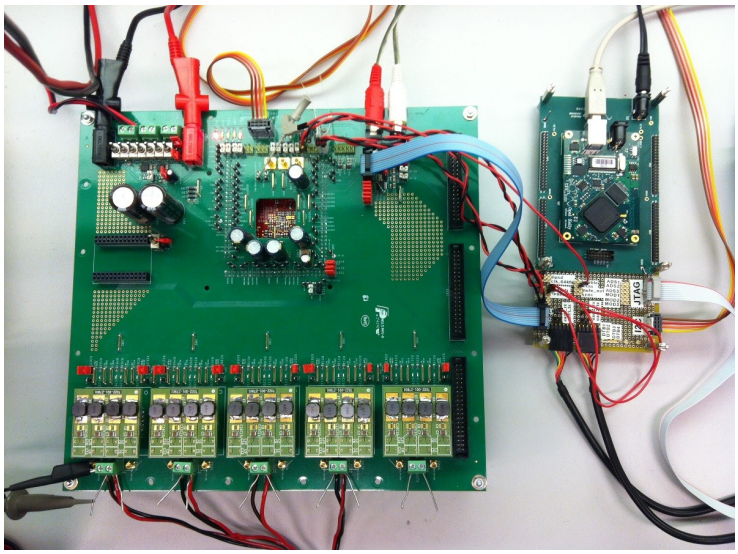

Figure 3.2: FPGA and validation board of class-D amplifier

3.4 Implementation of Digital block inside FPGA

This section describe the implementation of the micro-controller inside the fpga, as well as the UART and some additional circuits (TDM-generator, output pins).

3.4.1 Clock Distribution

In the fpga a clock multiplier (DCM) is used to create the necessary clocks for the manager and UART. The input of this clock multiplier is clk64kfs that comes from the Class-D amplifier board, via digital test bus. The DCM inside the fpga will use this clock to generate a clk1024kfs and clk512kfs. With this setup, it is ensured that the UART baud-rate on both ends (fpga and class-D amplifier IC) is always matched, ensuring stable UART transmission. Finally, a clock-gate has been implemented that will disable the clock to the manager when a UART-transmission

is ongoing, see UART chapter as well. Currently the manager inside the fpga is running @ 1024kfs by default. However there are some (setup-) timing issues. Probably, this will not influence performance of the board. However, if needed the clock frequency on the board can be halved by next command during initializing of the fpga (in tcl).

3.4.2 Manager

The class-D amplifier manager has been ported to the FPGA with only minor changes to ensure proper operation in the chosen setup. The most important difference is the use of RAM's instead of ROM's in the fpga-manager. This obviously allows loading custom software (ROM-code) into the design, which was the main goal of this development. Besides the ability to load new software, the fpga memories behaves identical to the BAP3 memories, including address mapping.

3.4.3 UART

The UART connection between class-D amplifier and fpga is the key attribute of this design. Via this connection, most ESFR-register read- and write actions are performed (initiated by fpga) as well as signaling of interrupts (initiated by Class-D amplifier).

3.5 TDM Receiver design

TDM receiver is digital module. It consists of Digital audion interface module, block memory for storing data, Interface module which include pipe in fifo, pipe out fifo and Control for fifo, and CGU clock generation unit as shown in 3.3. TDM receiver decodes the serial TDM or I2S audio input stream and store into the memory, which can be accessed by the TCL environment for retrieving useful information .TDM frame are also used for sending the voltage and current information sensed by the current sense IP. This document describes the features of the TDM receiver and gives a description of the implementation.

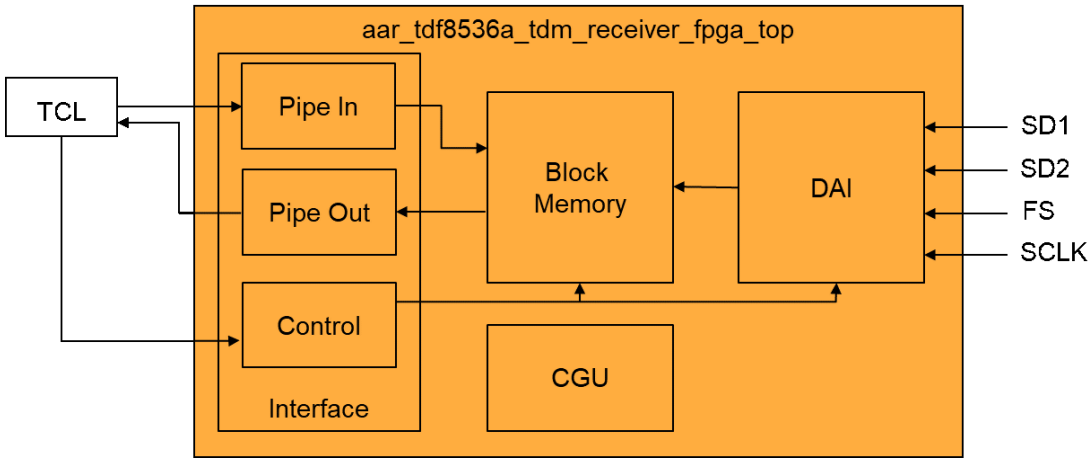

Figure 3.3: Top Module of TDM

3.5.1 Digital Audio Interface

The DAI that consists of a frame-decoder and a crossbar-mixer. On the left hand side is the TDM / I2S interface consisting of the pins sclk, sdx and fs. On the right hand side is the interface with the interpolator and the framesync and status outputs. The framesync output is derived from the external frame-sync fs. The internal frame-sync is always a positive (0-1-0) pulse, whereby the width of the pulse is exactly one clkm clock period 3.4. The status output is a record of signals. At the top, the config and channel-mapping signals allow setting the audio data format (TDM / I2S), number of bits per slot, number of slots per frame, etc., and the mapping of data from a frame slot to one or more channels. Furthermore, the control signals enable and start allow controlling the mode of operation of the DAI. When enable is asserted the DAI module becomes operational, and when enable is de-asserted the DAI module is in sleep-mode; in this mode the state of the DAI does not change due to the activation of clock gating of all registers.

When signal start is being de-asserted the DAI (a) keeps the framesync output low, and (b) synchronizes the internal frame-sync to the external frame-sync (fs pin) such that the delay between them is C+M+NOCHANNELS clock-cycles (on average), where C and M are naturals representing a number of clkm clock cycles that can be set via signals in the config record. Remark that actual delay is a little larger because of some synchronization flip-flops both in the sclk and clkm clock domains.

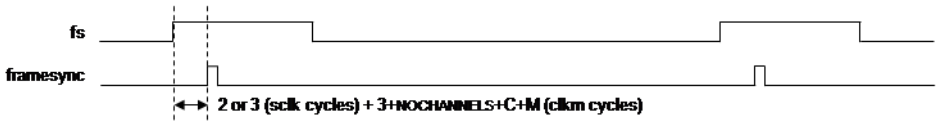

Figure 3.4: Relationship between the internal and external frame-sync.

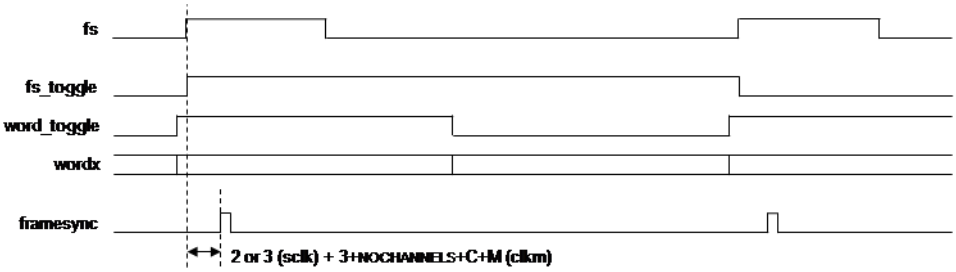

Figure 3.5: Relationship between the inputs, outputs and intermediate signals of the DAI.

The interface with the interpolator consists of an address- and a data bus. The address bus allows selecting samples of a certain channel via the data (output) bus, whereby the value of address determines the selected channel. The path from address to data is combinatorial. The sample buffer is updated at every internal framesync pulse.

The outputs of the DAI (crossbar mixer) are synchronous to the internal clock clkm which runs between 90 and 100 MHz. Clock clkm is derived from the sclk clock by means of a PLL, external to the DAI, whereby clkm cycles 4x, 8x, 16x, 32x, or 64x times faster than sclk depending on the actual data format.

Crossbar Mixture

The functions of the crossbar mixer are:

1. Synchronization of the control and data inputs that are transmitted by the frame-decoder to the clkm clock domain.
2. Mapping of the data words which are transmitted by the frame-decoder to the appropriate channel(s) based on the setting of the 2 dimensional signal-array channelmapping[x].

3. Framesync generation, status generation and error-detection Remark that the crossbar mixer is being clocked with the internal clkm clock which runs 4 to 64 times faster than the sclk clock, depending on the data input format.

3.5.2 Memory Instance

Block Memory is generated by the IP Core Generator from ISE [5]. The top level consists of a memory and supporting logic to access that memory. Memory read/write operation is done through the pipe in FIFO and pipe out FIFO. Asynchronous FIFO are used here as read and write clock domains are different. Block memory read and write operation are in sync with clock clk_1024kfs. The width of mem_addresss is 16 bits and the width of dina and douta is 32 bits. Memory can be accessed by two ways manually and automatically. Selecting "manual" or "automatic" access is provided by muxing the signals connecting to the memory access.

Manual memory access is done by connecting okWireIn and okWireOut data to the memory. Signal mem_write_man is used to enable the manual access and so selecting the mem_(.*)_man signals. Signals mem_write_man and also mem_write_enable come from okWireIn instance ep00 by means of ep00wire (its output). Also the other mem_(.*)_man signals are connected to okWireIn and okWireOut instances.

Automatic memory access is done by pipe and fifo. Instead of the above manual access (by okWireIn and okWireOut), the memory should be accessible by the okPipeIn and okPipeOut. This method should be much more efficient for large amount of data[6].

To synchronize data between the pipe and the memory, a fifo-buffer needs to be inserted. Documentation on the fifos generated by ISE (version 9.3 as in cadenv'ed version of ise, xilinx). For Automatic memory access, write to the memory, an instance of okPipeIn is used. The 16 bits width data from the pipe, mem_write_data_pipe, is feed through the fifo. To generate in Fifo through IP Core Generator [5] below settings are used:

Read Mode: Standard FIFO
Data Port Parameters
Write Width: 16
Read Width: 32

Write Depth: 65536
Read Depth: 32768

Note that the okPipeIn and okPipeOut have 16 bit data width, and so connecting to the 32 bit memory is not trivial. Also in this case the write clock, ti_clk, from the okHost interface, is about 48MHz and the read-clock, clk_1024kfs, is about (50MHz) the same speed. However, at the input data is coming in with 2 bytes at the time, and at the output data is read 4 bytes per clock cycle. That implies that filling the fifo would go faster than emptying. For the first version, it is decided to initiate the reading manually, thus from a okWireIn, by means of signal mem_write_fifo_read. First check ep00wire availability.Then implementing reading from the fifo, thus when posedge on mem_write_fifo_read_start.

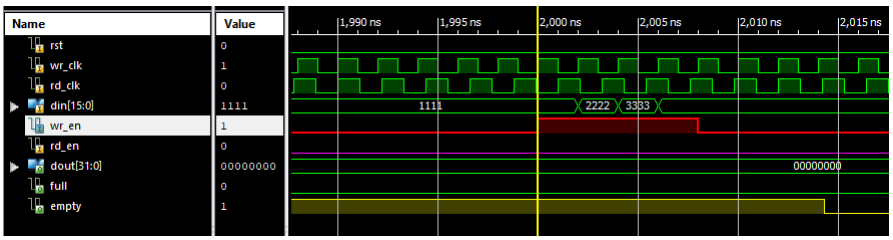

Figure 3.6: Simulation capture for writing to FIFO.

Simulation capture for reading from FIFO 3.7. Whenever rd_en = 1, posedge of rd_clk are asserted when fifo empty = 0, then 32 bit dout data will come out at the next posedge of rd_clk. This simulation information for read/write is used for address counter for automatic memory read and write operation.

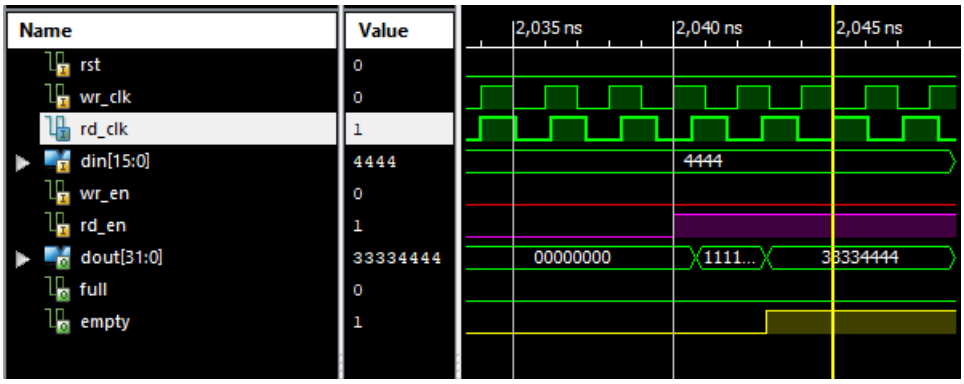

Figure 3.7: Simulation capture for reading from FIFO.

Chapter 4

Conclusion

For the booster IP validation, 100 samples was tested inside the Laboratory. Each sample was tested across different voltages, different temperature and across different frequencies. Validation activities carried out from the very initial phase of Validation strategy to the execution of strategy. Pre tape out activities such as automation framework developement, validation board development, FPGA prototyping, Instrument requirement listing, test procedure developement are performed. Learnings from this validation are RTL design, FPGA prototyping, LabVIEW programming and Validation of analog IP.

Validation Test case derivation from Test specification of IP, and then test cases categorisation into characterization test, functional test, validation test, robustness check etc are also leanings of Post silicon Validation. All these tests are performed with help of expensive lab equipments such as Mixed signal osciloscope, Function generator, Power supply, Source meter, thermostream under controlled environment. The results of test cases compared with test specification and the results out of specs were reported back to designer for improvement in Second tapeout.

To bulid up pre-silicon validation platform, FPGA Prototype of digital RTL implemented with model of analog IP. FPGA prototying helps in pre silicon phase for validation bring up, software developement and FPGA verification. FPGA based Validation can provide a demonstration for downstream customers, providing confidence the system system is functioning as specified. A FPGA prototype is used to develop both hardware and software iteratively. If accurate software models are not available, prototyping may be the only option. FPGA-based prototype can provide a functioning hardware platform long before silicon is available. This enables early software development tasks such as OS integration and application testing. Only a hardware prototype will run fast enough for practical software development.

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